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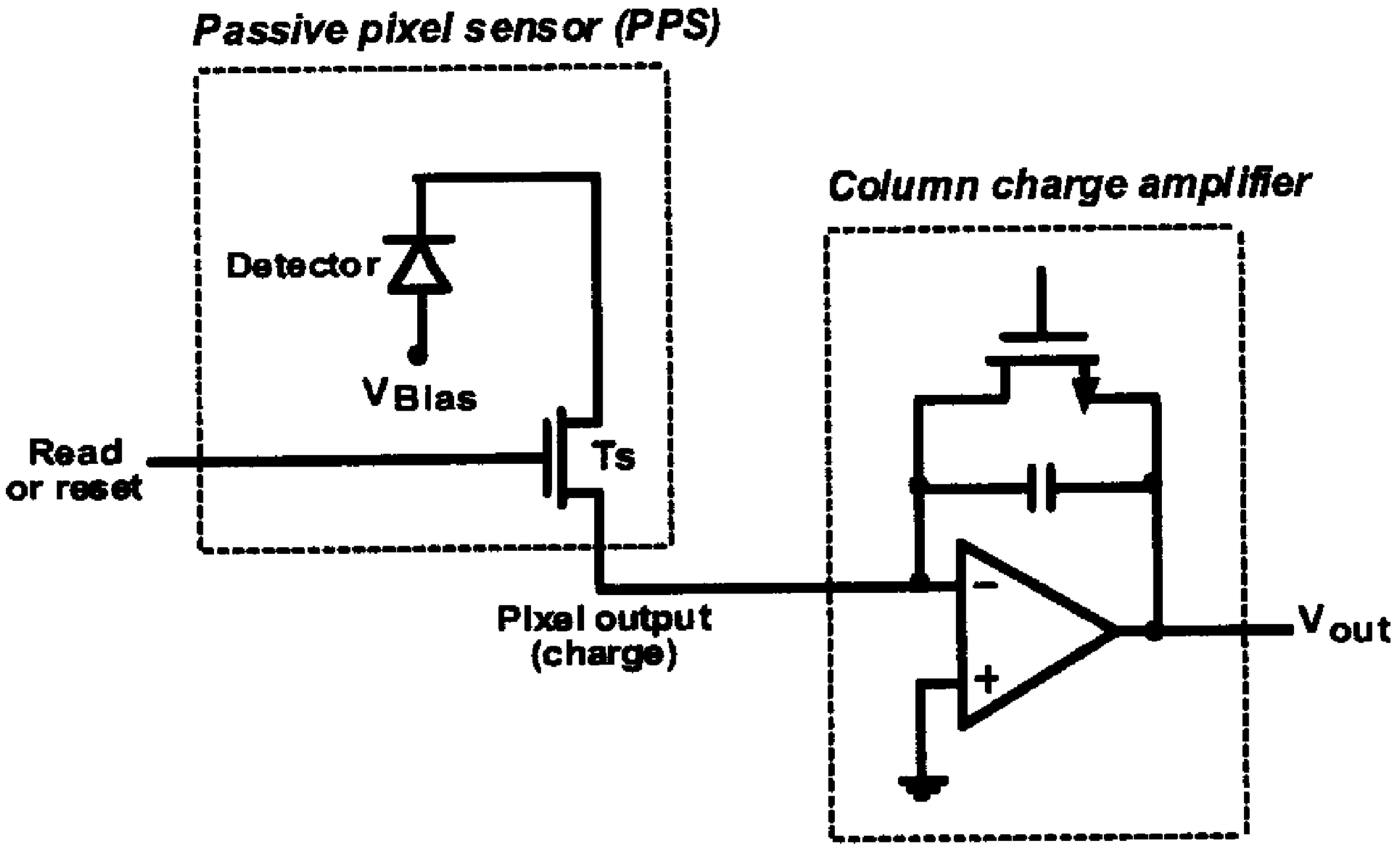
(54) Titre : ARCHITECTURES D'IMAGERIE A CAPTEURS ACTIFS DE PIXELS, TOTALEMENT INTEGREES
(54) Title: FULLY INTEGRATED ACTIVE PIXEL SENSOR IMAGING ARCHITECTURES



(57) Abrégé/Abstract:
The present invention discloses fully integrated active pixel sensor (APS) architectures where the detectors and imaging pixel sensor circuitries are fabricated using the same materials, and on the same substrate. APS architectures with photoconductor detectors and with multi-functional TFTs that perform both switching and light detection functions are disclosed.

ABSTRACT

The present invention discloses fully integrated active pixel sensor (APS) architectures where the detectors and imaging pixel sensor circuitries are fabricated using the same materials, and on the same substrate. APS architectures with photoconductor detectors and with multi-functional TFTs that perform both switching and light detection functions are disclosed.

FULLY INTEGRATED ACTIVE PIXEL SENSOR IMAGING ARCHITECTURES

FIELD OF THE INVENTION

The present invention pertains to the field of digital imaging and active pixel sensor arrays, and in particular, to integrated detector-pixel imaging sensor apparatus employing photoconductors and/or phototransistors as imaging detectors which are fully integrated into the active pixel sensor array.

BACKGROUND

The term digital imaging refers to the function of a system capable of producing a digital electronic image from optical image information. Such a system is usually consisted of a matrix of pixelated optical detectors each associated with their own electronic circuits (which together are called pixels), connected to peripheral circuits (biasing, addressing, readout and digitizer circuitries).

One of the commonly used architectures for large area imaging is the passive pixel sensor (PPS) shown in figure 1.a. Here, a detector, for example, an amorphous selenium (a-Se) based photoconductor, a Cesium Iodide (CsI) phosphor coupled to an amorphous silicon (a-Si:H) p-i-n photodiode, or even a crystalline p-n junction, is integrated with a readout circuit comprising a transistor switch such as an a-Si:H thin-film transistor (TFT). Signal charge is accumulated on the pixel sensor during an integration cycle and is transferred to an external charge amplifier via the transistor switch, T_S, during a readout/reset cycle. The transferred charge is converted to an equivalent voltage in the charge amplifier and is then further processed (sampling and/or digitization) towards reconstruction of a digital image. It is noted that the pixel capacitance mentioned above is the p-i-n photodiode capacitance or an integrated storage capacitor for the a-Se photoconductor arrangement, or the p-n junction capacitance. Other additional analog signal processing sequences are also possible, for example, double sampling mechanisms are typically used to correct for the effect of non-uniformities within the circuitry. These non-uniformities may comprise process non-uniformities in the form of offsets, and, in the case of a-Si:H

technology, non-uniformities in pixel circuit performance due to transistor instability. For example, International Publication Nos. WO9634416 and WO9705659 further disclose flat-panel detectors for radiation imaging using PPS architecture.

While the PPS has the advantage of being compact and therefore suitable for high-resolution imaging, reading a small output signal of the PPS for low input optical signal results in a noisy voltage at the output of the charge integrator, due to the fact that charge integrators potentially add a considerable amount of noise to the input signal. This lowers the signal-to-noise ratio (SNR) at low signal levels, and thus, degrades the pixel dynamic range.

One approach for improved SNR is disclosed in International Publication No. WO02067337 indicating that the SNR can be increased by employing in-situ, or pixel, amplification via an a-Si:H current-mediated active pixel sensor (C-APS) as depicted in figure 1.b. Reported gain, linearity and noise performance show an improvement and indicate that the a-Si:H C-APS, coupled with an established x-ray detection technology such as a-Se or CsI/p-i-n photodiodes, can meet the stringent requirements for low noise digital x-ray imaging for applications such as fluoroscopy, which no more than 1000 electrons of noise are allowed. In C-APS architecture, T2 is used to reset the voltage of the detector, and an on-pixel transconductance amplifier (T1) converts the detector voltage to an equivalent output current, which is then integrated in the column charge amplifier. The advantage of C-APS to PPS is the high gain; since the pixel capacitor is not discharged, a constant output current is provided as long as the row select transistor, T3, is on. Double sampling is necessary in C-APS to remove effects of non-uniformities among pixels.

Another approach disclosed in International Publication No. WO02067337 reports a near-unity gain pixel amplifier, namely, an a-Si:H voltage-mediated active pixel sensor (V-APS). A V-APS architecture is illustrated in figure 1c. The pixel configuration is exactly similar to that of C-APS architecture, however, in V-APS, the pixel output is the detector voltage which is buffered out by the pixel amplifier. The advantage of V-APS over PPS and C-APS is that the charge amplifier is replaced by a simple voltage buffer. This helps less complicated design and less expensive implementation of peripheral circuits. Like the C-APS, double sampling mechanisms can be applied to the V-APS to correct for the effect of non-uniformities within the circuitry.

The difference between C-APS and V-APS is in pixel output signal, i.e., current versus voltage, the pixel circuit of both architectures (figures 1.b and 1.c) is exactly the same, and is the basic structure of active pixel architecture, consisting of three field effect transistors. Many other variations of the basic architectures have been reported to improve functionality of the circuit. For example international publication No. WO2000019706 disclose methods of high speed resetting of the pixel, or as another example, international publication WO2006042407 introduces multimode architectures for high dynamic range, and low noise imaging applications as illustrated in figure 2.a; a four-transistor approach. Other non classical architectures such as two-transistor multimode architectures have also been reported [1, 2] as shown in figure 2.b, where addressing each row is performed by providing a separate bias voltage for the entire row. Although such architectures provide smaller pixel size for higher imaging resolution, but they require more complex peripheral circuits, and non standard driving methods. Different photo-sensors have been claimed to be used in PPS architectures such as a-Si pin diodes, a-Se photoconductors, MIS diodes and source-gated phototransistors (WO/2003/073507). In many cases, the TFT backplane is fabricated first, and then the photodetectors are integrated.

This background information is provided for the purpose of making known information believed by the applicant to be of possible relevance to the present invention. No admission is necessarily intended, nor should be construed, that any of the preceding information constitutes prior art against the present invention.

SUMMARY OF THE INVENTION

An object of the present invention is to provide a fully integrated active pixel imaging apparatus. In accordance with an aspect of the present invention, there is provided an active imaging apparatus comprising: a differential detector for generating a first signal in response to photons incident thereupon; and an active circuitry coupled to said detector for receiving said first signal and for generating a second signal, that the amplitude of the said second signal represents the said first signal.

In accordance with another aspect of the invention, there is provided a three-transistor fully integrated active pixel architecture for low-cost active imaging without a dedicated detector, in

which, one of the switching transistors performs functions of switching as well as photodetection.

In accordance with another aspect of the invention, there is provided a three-transistor fully integrated active pixel architecture for low-cost active imaging without a dedicated detector, in which, one of the switching transistors performs functions of switching action as well as photodetection, and a switched amplifying transistor is employed to integrate functions of a switching and a driving transistor.

BRIEF DESCRIPTION OF THE FIGURES

Figure 1.a. Pixel architecture of a passive pixel sensor PPS array according to the prior art.

Figure 1.b. Pixel architecture of a current-mediated active pixel sensor C-APS array according to the prior art.

Figure 1.c. Pixel architecture of a voltage-mediated active pixel sensor V-APS array according to the prior art.

Figure 2.a. Pixel architecture of a 4-transistor multimode pixel sensor according to the prior art.

Figure 2.b. Pixel architecture of a 2-transistor multimode pixel sensor according to the prior art.

Figure 3.a. Illustration of a schematic diagram (top view and symbol) of a photoconductor.

Figure 3.b. Pixel architecture of a fully integrated APS architecture integrated with photoconductors; exposure to light increases the output signal.

Figure 3.c. Pixel architecture of a fully integrated APS architecture integrated with photoconductors; exposure to light decreases the output signal.

Figure 3.d. Array configuration of a fully integrated APS architecture integrated with photoconductors connected to column output amplifiers.

Figure 4.a. Example of charge (or current) integrator as the output amplifier connected to sampling circuits and digitizer.

Figure 4.b. Example of a transimpedance amplifier as the output amplifier connected to sampling circuits and digitizer.

Figure 4.c. Example of a voltage amplifier as the output amplifier connected to sampling circuits and digitizer.

Figure 5.a. Illustration of a schematic diagram (top view and symbol) of a photoconductor integrated with a reset TFT; the gate can be either beneath or atop the active layer.

Figure 5.b. Pixel architecture of a fully integrated APS architecture integrated with photoconductors and reset TFTs; exposure to light increases the output signal.

Figure 5.c. Pixel architecture of a fully integrated APS architecture integrated with photoconductors and reset TFTs; exposure to light decreases the output signal.

Figure 6.a. Illustration of an exposed channel TFT (top view and symbol); the gate can be either beneath or atop the active layer. In case of a top-gate TFT configuration, if the channel is illuminated from above, transparent conductor is used for the gate to allow incident photons reach the active channel.

Figure 6.b. Pixel architecture of a fully integrated APS architecture with multifunctional TFTs; the reset TFT also serves as the photodetector.

Figure 6.c. Pixel architecture of a fully integrated APS architecture with multifunctional TFTs; the row-select TFT also serves as the photodetector, the AMP is a switched amplifying TFT.

DETAILED DESCRIPTION OF THE INVENTION

Definitions

The term "detector" is used to define a device that converts photons of radiation in any region of the electromagnetic spectrum to electrical charge directly or indirectly.

The term "transistor" is used to define a field effect semi-conducting device for switching, amplifying or transconducting purposes. Such transistor could be a thin film transistor (TFT) or of other similar devices.

The term "pixel" is used to define an imaging element consisting of one or more detectors coupled to a readout circuit.

The term "readout circuit" is used to define an electronic circuit consisting of one or more transistors that connects the detector to the peripheral circuits.

The term "peripheral circuit" is used to define electronic circuits connected to a pixel (or array of pixels) fully integrated or external, necessary to operate the imager for generating digital image information.

The term "architecture" is used to define the configuration of the detector and its readout circuit in a pixel.

The term "fully integrated" is used to define a pixel architecture where the pixel photodetector and the pixel readout circuit are fabricated using the same semiconductor materials.

The term "multi-functional TFT" is used to define a TFT that behave either as a transistor switch, a transistor amplifier or as a photodetector.

Unless defined otherwise, all technical and scientific terms used herein have the same meaning as commonly understood by one of ordinary skill in the art to which this invention belongs.

The present invention provides fully integrated active pixel digital imaging architectures comprising detectors coupled to readout circuitry, wherein the readout circuitry generates amplified signal when compared to the passive architecture PPS. Each detector generates photo-carriers in response to photons incident upon the detector and produces current or charge, which results in a voltage change across the detector or the associated capacitor with the detector. This voltage change produces the input signal to the readout circuitry, which then outputs a voltage or current signal representative of the detector signal.

Portions of the readout circuitry that are common for a column, row, or group of pixels may be multiplexed between these pixels in an array. Thus it would be readily understood by a worker skilled in the art, that in the various embodiments of the present invention, common column, row or group readout circuitry may be multiplexed between pixels, and that this may require additional circuitry, for example switching circuits or multiplexing circuits. In addition, multiplexers may also be used to reduce the readout circuit complexity by decreasing the total number of digital counters, for example, required for a column, row, or group of pixels. Furthermore, common column or row readout circuitry may also be implemented such that the common readout circuitry is individual to each pixel. It would also be understood that the pixels of various embodiments may be implemented in arrays of any size, or dimension. Furthermore, where portions of readout circuitry have been identified as being shared by one or more columns of pixels, it should be understood that the circuitry may equivalently be shared by one or more rows of pixels or one or more other groups of pixels.

Embodiments of the present invention can be operated with various switching and timing sequences. For example, where a double sampling technique is used, the transistor switching and timing may vary from a sequence in which no double sampling technique is used. In various embodiments of the present invention described herein, related transistor switching and timing cycles and sequences are provided as examples, and numerous other cycles and sequences are possible as would be obvious to a worker skilled in the art.

As would be readily understood by a worker skilled in the art, the present invention may be applied to any digital imaging application. For example, the present invention may be applied to medical imaging, x-ray inspection systems such as in the inspection of aircraft wings, security

systems such as screening of luggage at airports, non-destructive material tests, radiography or optical imaging, as well as other forms of digital imaging applications as would be readily understood.

Photoconductor-TFT integrated APS

Fully integrated APS architectures coupled with photoconductor (PC) photodetectors (Fig. 1.a) are shown in Fig. 3.b and 3.c. Each pixel comprises two detectors -one is light-shielded- connected to an active pixel sensor circuitry. The two PCs are used as a photo-to-voltage converter: under light illumination, the photocurrent generated in the exposed PC produces a large voltage change by flowing through the shielded PC. While the for high illumination intensities the generated voltage change is nonlinear with respect to the light intensity, for very small changes (for very low incident light intensity) the small signal analysis results in the total APS current gain of:

$$APS_{C-Gain} = \frac{\Delta I_{out}}{I_{ph}} = \pm \frac{G_{m\ APS} \cdot R_{Dark\ PC}}{4}$$

Where $G_{m\,APS}$ is the transconductance gain of the standard APS pixel, and $R_{Dark\,PC}$ and I_{ph} are the dark resistance and the photo-generated current (not including the dark current) of the photoconductor respectively. The current gain can be really high regarding the fact that the dark resistance of the PC is very high. This architecture is suitable for real-time imaging as it provides a fee-running pixel. One possible array configuration of the photoconductor integrated APS pixels architecture is depicted in figure 3.d, where *READ* addressing lines are shared among all pixels in the same row and output lines are shared among all pixels in the same column. It should be noted that other configurations are also possible when addressing lines are shared column wise, and outputs of all pixels in the same row are connected to each other.

Output amplifiers

Depending on the type of amplifier connected to the array, it is possible to readout the signal from active pixel sensors in terms of current or voltage; namely, C-APS and V-APS respectively. When charge (or current) integrators (fig. 4.a) or transimpedance amplifiers (fig. 4.b) are used, the output lines are held at a constant voltage (e.g., zero volts) where the output current flows into the column readout circuits and a corresponding voltage (the output voltage) is generated for further processing such as sampling, subtraction and digitization. For V-APS, voltage buffers/

amplifiers are used (fig. 4.c) where the AMP TFTs buffer the sensor voltage on the output lines connected to the output column voltage buffers/amplifiers.

To improve the imaging speed of photoconductor-TFT integrated active pixel sensors, resetting TFTs can be provided along with the photoconductors to reset the gate of the AMP TFT to a preset voltage as fast as practical (Fig. 5.a). Two possible architectures of such pixels are illustrated in Figs. 5.b and 5.c. In the absence of light, the voltage at the gate of AMP, V_S, is always half that of the V_{DD}, which is considered the reset voltage. To bring back the V_S to the initial reset voltage after the pixel is read, V_{DD} is applied to V_{GS}, and $V_{DD}/2$ to V_{GR}. This ensures the quick resetting of V_S to $V_{DD}/2$ because of the symmetrical resistances connected from V_S to V_{DD} and to the ground (same voltage drop across gate-source of resetting TFTs results same ON state resistance for resetting TFTs). An array configuration of such pixel architectures is depicted in Fig. 5.d, with addressing lines (*Read*, V_{GS} and V_{GR}) are common for pixels in the same row and output lines shared between pixels in the same column. The array is read out either as C-APS or V-APS depending on the output amplifiers connected (Fig. 4.a, 4.b and 4.c).

Fully integrated APS with multi-functional TFTs

Characteristics of thin film transistors change when the channel is exposed to light. Under illumination, a switch TFT in the OFF region shows increased leakage current. A multi-functional TFT is illustrated in Fig. 6.a where the channel is exposed to light. The transistor functions both as usual TFT depending on voltage levels applied to its three terminals, as well as a sensitive photodetector when the TFT is in OFF state and its channel is exposed to light. Fig. 6.b shows the standard three-transistor APS architecture with row-select (RS), and amplifying (AMP) TFTs light shielded and reset (RST) transistor exposed. In this architecture RST performs both as the reset transistor to preset the voltage eat the gate of AMP, and as a photodetector because it is not light shielded. To reset the pixel, V_{SR} is set to high voltage (e.g. 15V) and the RST switch TFT is turned on. During integration, the V_{SR} is set to a lower voltage (e.g. 0V) when any incident photon on the exposed channel of RST increases the leakage and decreases the preset voltage at the gate of AMP. The pixel is later read in active mode by turning on the RS switch TFT and reading out either the pixel current using a C-APS column readout (Fig. 4.a or 4.b), or the pixel voltage by employing a V-APS readout circuitry (Fig. 4.c). It is also possible to preset the voltage of AMP gate to a lower voltage (e.g. 5V) and applying a higher voltage (e.g.

15V) to V_{SR} during integration, to increase the preset voltage as the result of photo integration. Operation cycles and different biasing conditions of the transistors are listed in Fig. 6.c. In this architecture, the area of RST TFT is designed to be large to maximize the fill factor, however, AMP and RS TFTa should also be large to have high pixel gain. One possible array configuration of this pixel architecture is depicted in Fig. 6.d where output different amplifiers are used depending if C-APS or V-APS output desired.

It is possible to implement a fourth transistor in this three-transistor design and avoid switching V_{SR}. In this case, the design converts to the pixel architecture disclosed in Fig. 5.a (or 5.b), with the gate of SENS or REF transistors fully cover the channel. Figures 5.a and 5.b are the geral form of four-transistor APS architectures where either SENS or REF TFTs (or both) act as multifunctional TFTs.

Figure 7.a shows an other possible architecture of fully integrated APS with multi-functional TFTs, which has larger a fill factor compared to the pixel architecture of Fig. 6.b because the large RS TFT connected to the source of AMP has been removed, but a smaller RST TFT has been added. Also this architecture benefits from a higher pixel transconductance gain as the result of removing the degenerate resistor (ON state resistance of RS TFT) from the source of AMP. The gate of AMP TFT is preset to zero (or below threshold) voltage by grounding V_{SR} and switching both RS and RST TFTs on. During integration, RS is switched off, while a high voltage (e.g. 15V) is applied to V_{SR}, when photons incident on the RS TFT channel increases the leakage current and result in voltage change at the gate of AMP. Because of zero (or below threshold) preset voltage the AMP TFT is OFF during integration. To read the pixel, the RST is turned OFF and RS is switched on, the capacitive coupling of RS gate voltage on the floating gate of AMP increase its voltage (while preserving the integrated signal charge) and turns on the AMP TFT when the pixel output signal is read either in terms of current or voltage. Refer to Fig. 7.b. for a detailed list of biasing conditions and driving signals for operating the pixel. One possible array configuration of this architecture is depicted in Fig. 7.c, where different column output amplifiers are used depending if current mediated (C-APS) or voltage mediated (V-APS) output desired (see Fig. 4.a, 4.b and 4.c).

One version of a two-transistor fully integrated APS architecture is disclosed in Fig. 8.a which is similar to pixel architecture of Fig. 6.b without the RS TFT. In this circuit, pixel readout is performed by changing the voltage of the source (or drain) of the AMP TFT [2]. For example the pixel is reset to a high positive voltage (e.g. V_{DD} or less) and both drain and source of AMP are kept at the same high voltage level. During integration, the low voltage of VSR, results discharging of the pixel preset voltage at the gate of AMP in case there is any light exposure. For readout, the voltage at the source of AMP is reduced (e.g. to zero volts) and the current is drained from the output where it is integrated or converted to a corresponding voltage by the output circuitry. One possible method of driving such pixel architecture is shown in Fig. 8.b and an array configuration is depicted in Fig. 8.c. This array is read in C-APS mode.

Another method of implementing a fully integrated two-TFT APS is disclosed in Figure 9.a (similar to the idea disclosed for hybrid, not fully integrated, 2-T APS in [1]), where the RST and AMP TFTs share one terminal to reduce the need for an extra addressing line as in Fig. 8.a. The operation of the pixel is similar to the pixel architecture of Fig. 8.a where the readout is performed by applying a proper voltage to the source (or drain) of AMP TFT. One example of required driving signals to operate the pixel (and imager array) is shown in Fig. 9.b where possible signal waveforms can be extracted from. The pixel is reset to a moderate voltage level, and during integration, the preset voltage is increased as the result of light absorption by the SENS TFT (output voltage is at a higher voltage level that the preset voltage), while appropriate voltages at the READ and OUTPUT (both high) keep the AMP TFT in OFF state. The readout is performed by providing a positive gate-source voltage (higher than the threshold voltage) for AMP TFT similar to the pixel architecture of Fig. 8.a. One example of driving signals for pixel architecture of Fig. 9.a is disclosed in Fig. 9.b, and an array configuration is depicted in Fig. 9.c. This imager is read in C-APS mode.

REFERENCES

[1]: F. Taghibakhsh, K.S. Karim, "High dynamic range 2-TFT amplified pixel sensor architecture for digital mammography tomosynthesis" IET Circuits Devices & Systems, vol. 1, no. 1, pp. 87-92, (2007).

[2]: F. Taghibakhsh, K.S. Karim, "Amplified Pixel Sensor Architectures for Low Dose Computed Tomography using Silicon Thin Film Technology", Proceedings of SPIE, vol. 6510, (2007).

WE CLAIM:

1. An imaging apparatus comprising:
   a) Two photoconductor detectors for generating a first signal in response to photons incident upon one of them; and
   b) a two-transistor active readout circuitry fully integrated with said detectors for receiving said first signal and for generating a second signal representative of said first signal.

2. An imaging apparatus comprising:
   a) Two photoconductor detectors for generating a first signal in response to photons incident upon one of them; and
   b) a four-transistor active readout circuitry fully integrated with said detectors for receiving said first signal and for generating a second signal representative of said first signal.

3. An imaging apparatus comprising:
   a) a multi-functional transistor that act both as a switch and as a detector for generating a first signal in response to photons incident thereupon, and;
   b) an active pixel sensor readout circuitry connected to the said multi-functional transistor for receiving said first signal and for generating a second signal representative of said first signal.

4. An imaging apparatus comprising:
   a) a multi-functional transistor that acts both as a switch and as a detector for generating a first signal in response to photons incident thereupon, and;
   b) an active pixel sensor readout circuitry comprising of a multi-functional transistor that acts both as a switch and an amplifier for receiving said first signal and for generating a second signal representative of said first signal.

5. An imaging array of active pixels comprising a two dimensional array according to claims 1 or 2 or 3 or 4, in a way that addressing and biasing lines such as *Read* and *Reset* and V_{SR} are shared between pixels in the same row (or column), and output lines are shared between pixels in the same column (or row).

6. A high energy radiation imaging device comprising:
   a) A phosphorescence or scintillator layer generating a first optical signal upon absorbing high energy radiation
   b) An imaging array according to claim 5 receiving the said first optical signal and generating a second electrical signal representing the first optical signal, and hence, the high energy radiation.

7. Use of the imaging array according to claim 5 for imaging applications in the optical wavelength range such as in digital cameras and photocopiers.

8. Use of the imaging array according to claim 5 for imaging applications in the short and ultraviolet wavelength range for biomedical imaging applications including devices and arrays for DNA and protein sequencing, detection, mapping, and separation.

9. Use of short wavelength light emitting phosphorescent or scintillator materials, for high energy radiation detectors, according to claim 6 to increase the detection efficiency of the claimed imager in claim 6.

10. Use of the imaging array according to claim 6 for x-ray imaging applications such as chest radiography, cardiac imaging, mammography, fluoroscopy, protein crystallography, gamma ray imaging, or non-destructive inspection applications.

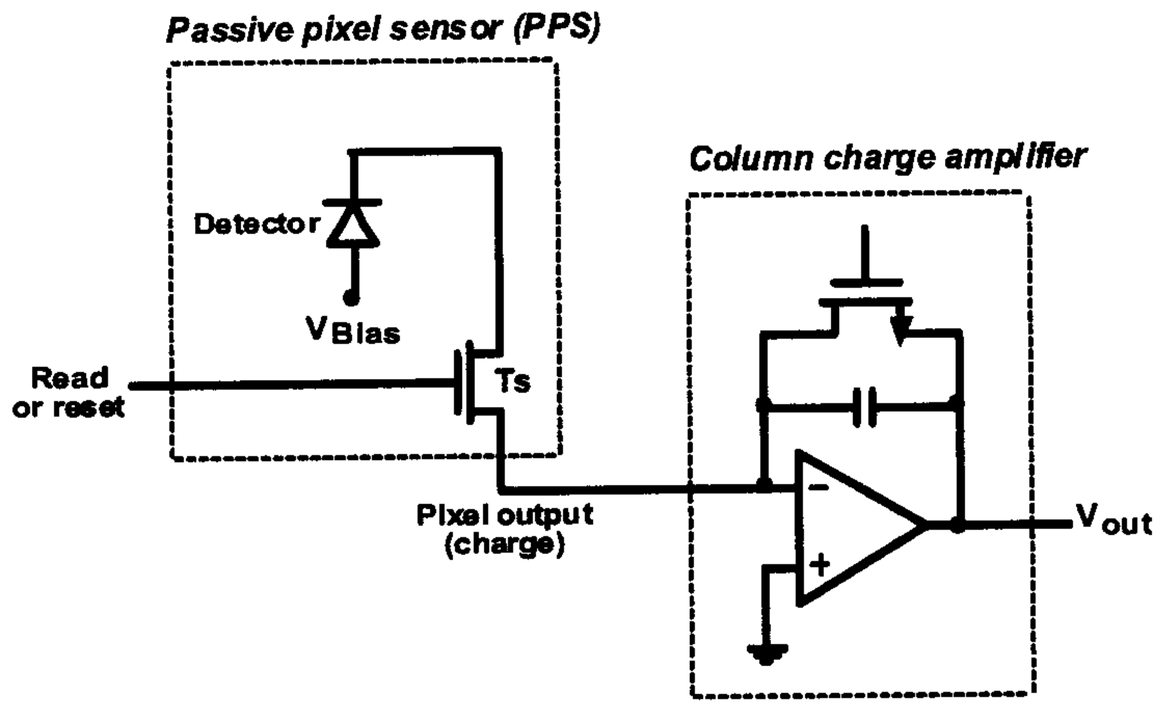


Figure 1.a

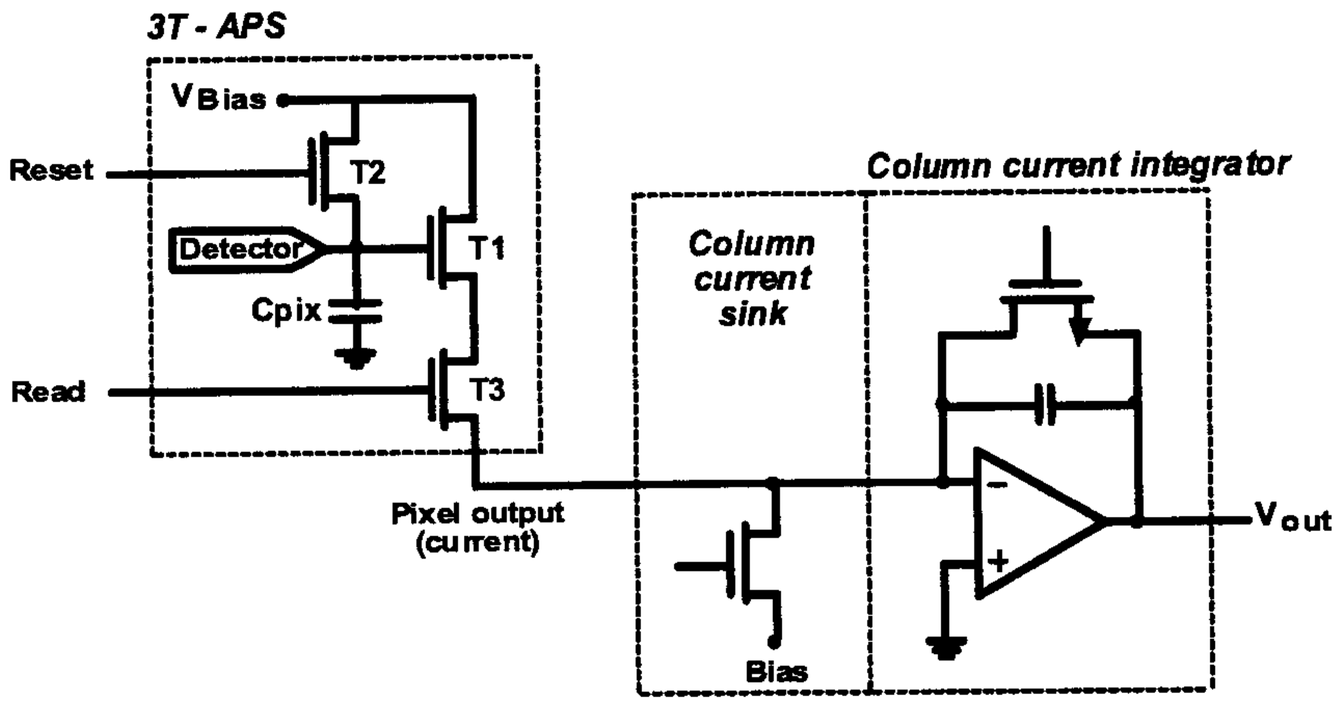


Figure 1.b

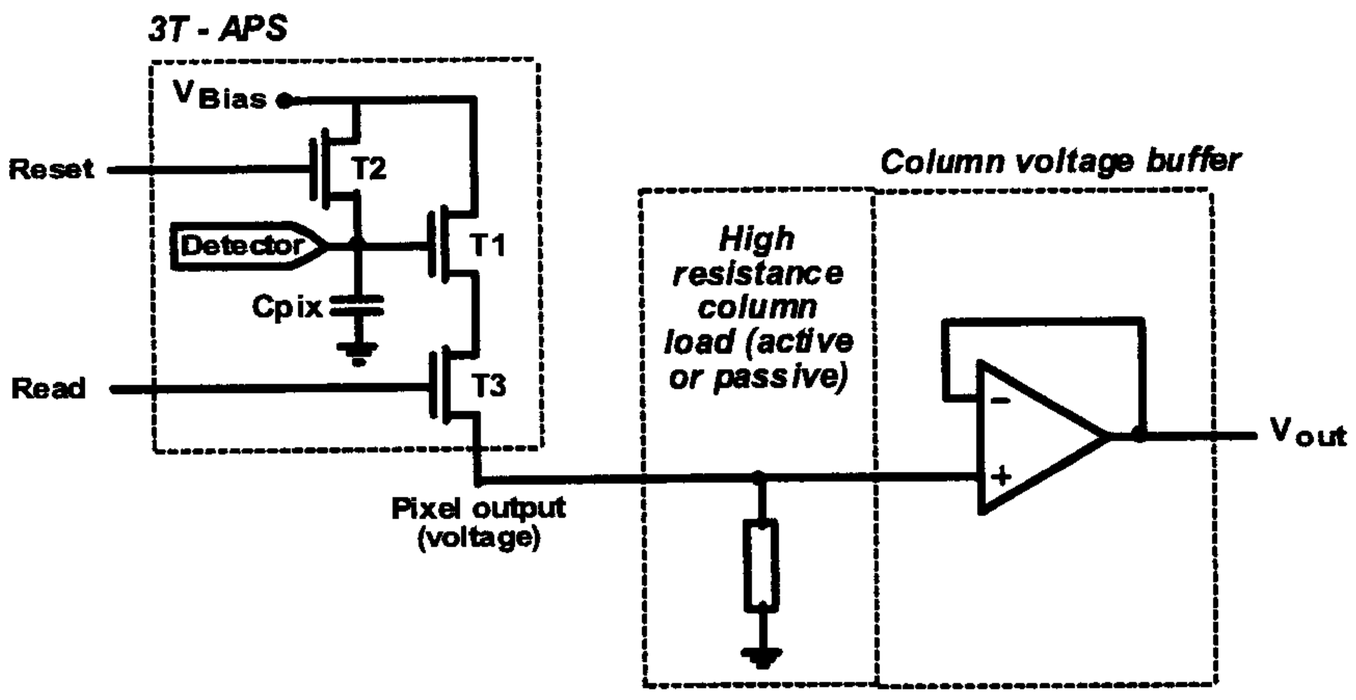


Figure 1.c

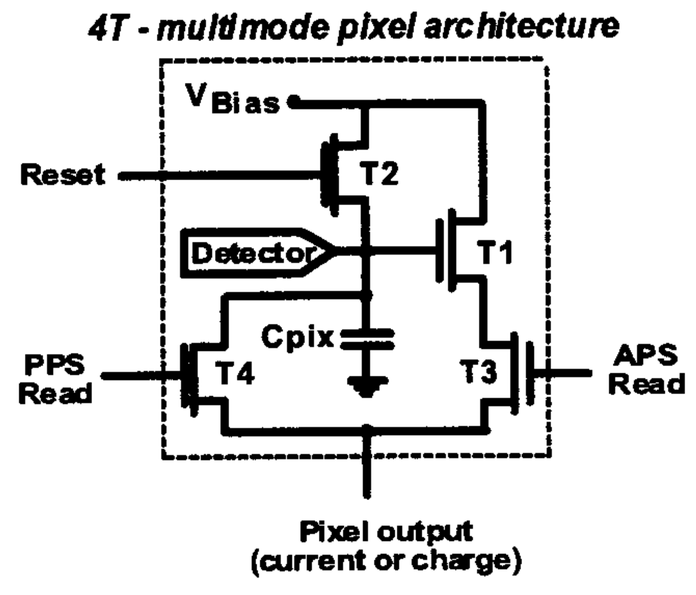


Figure 2.a

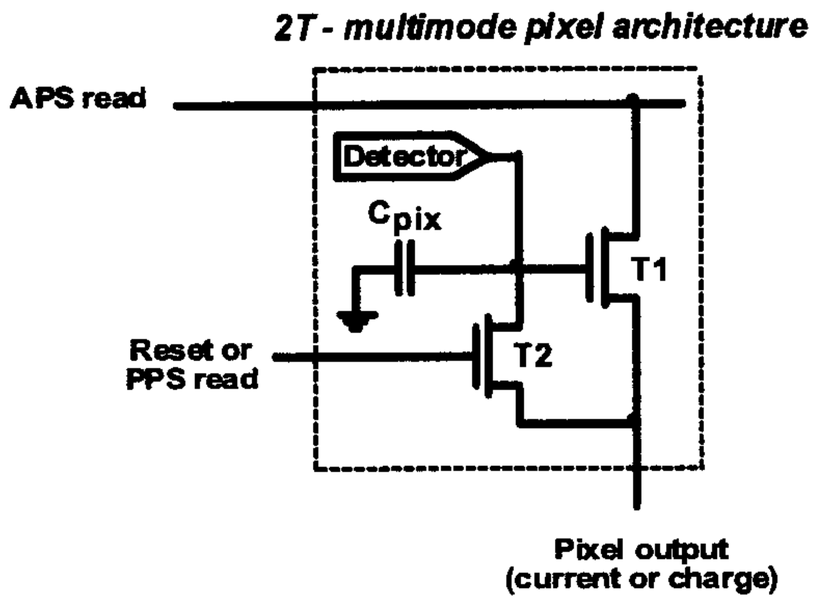


Figure 2.b

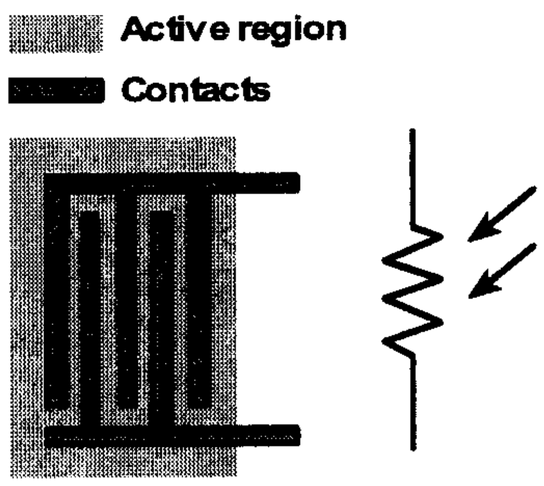


Figure 3.a.

Figure 3.b.

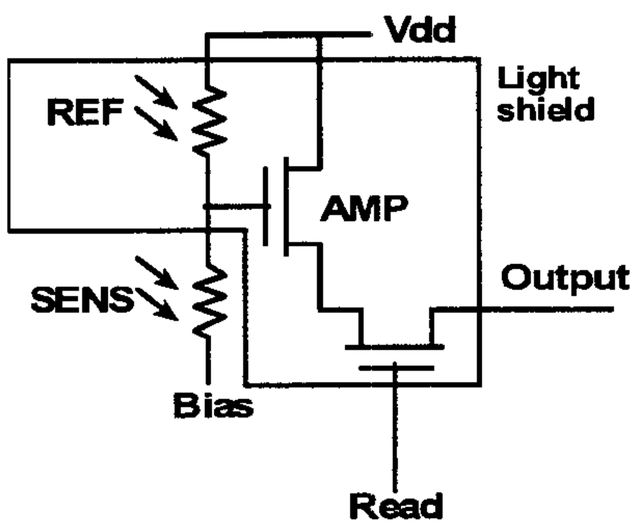


Figure 3.c.

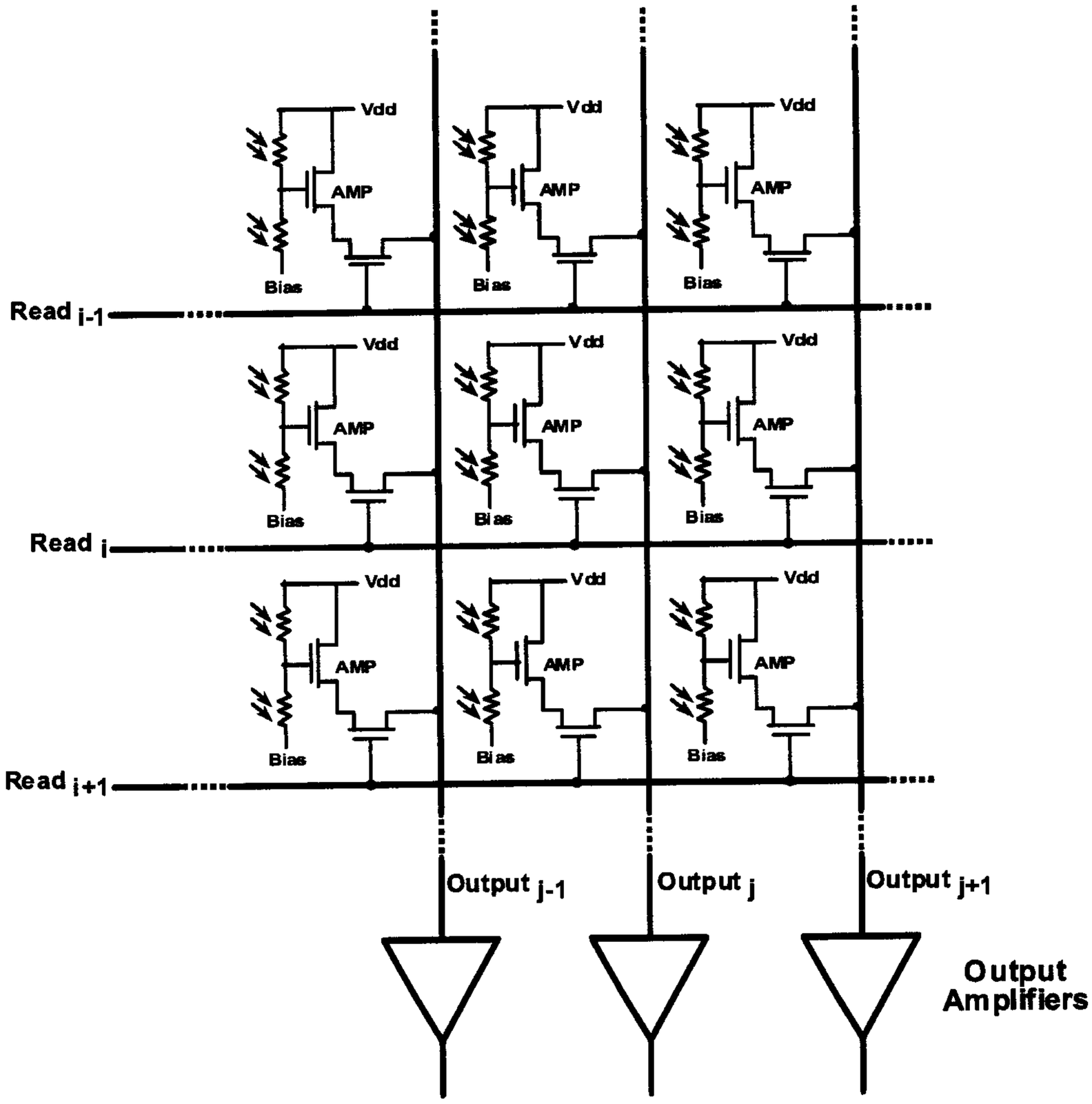

Vdd
AMP
Bias
Read j-1
Read j
Read j+1
Output j-1
Output j
Output j+1
Output Amplifiers

Figure 3.d

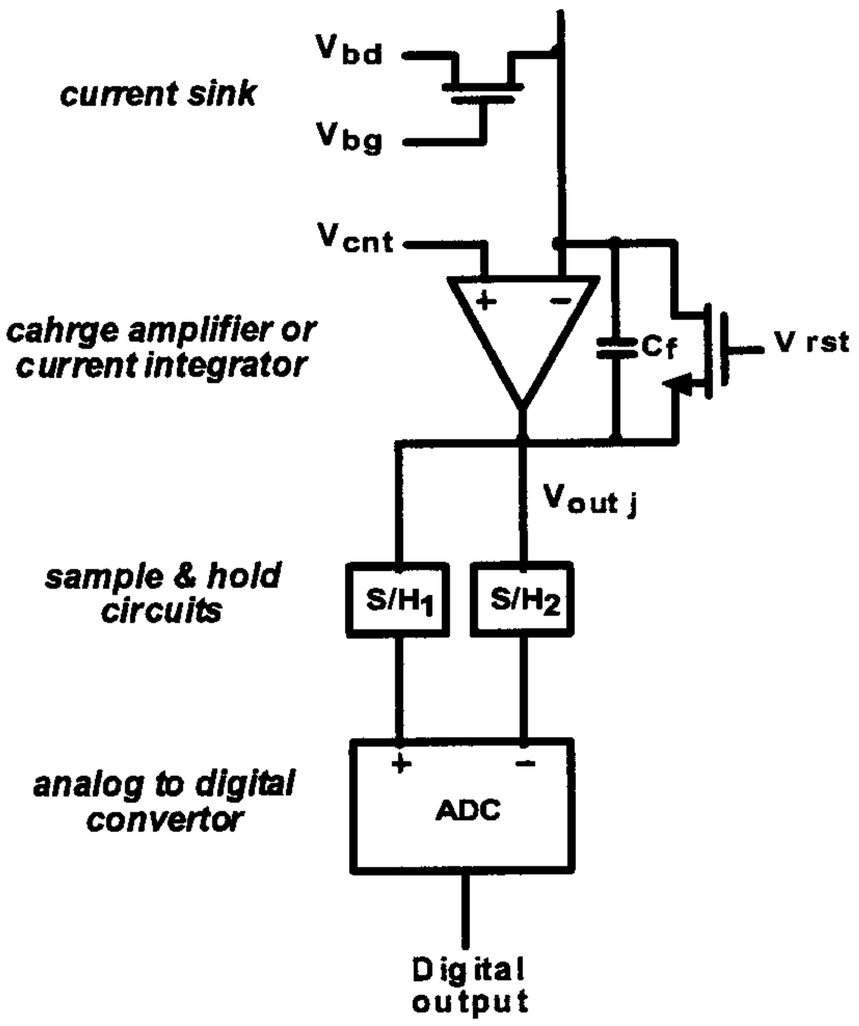


Figure 4.a

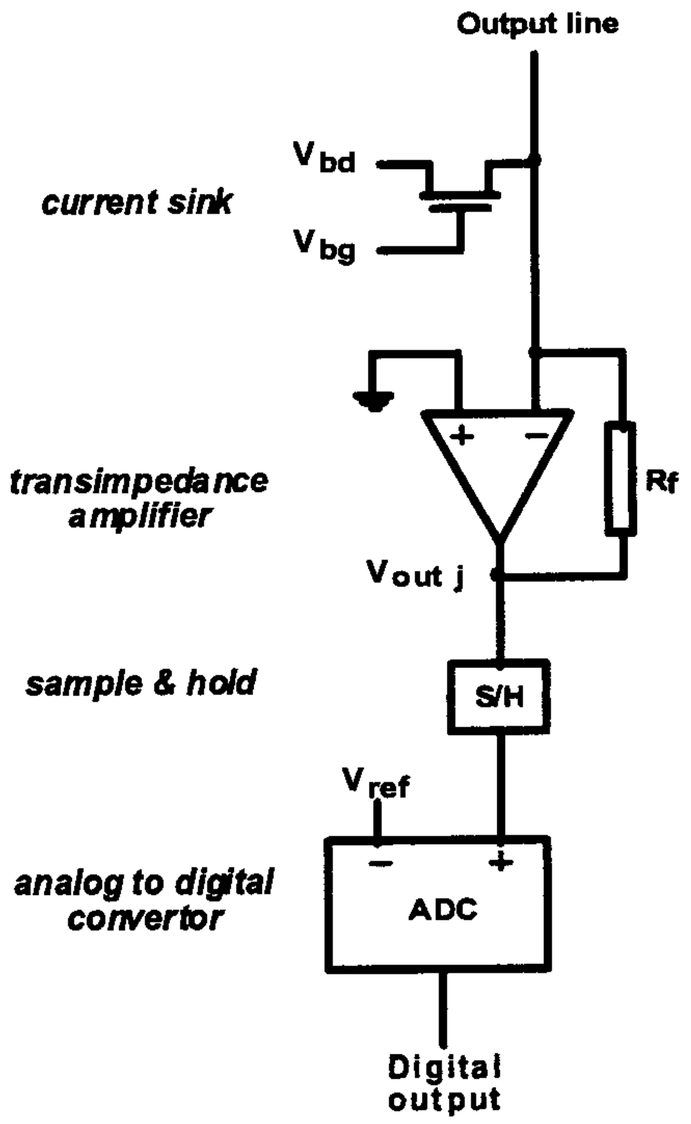


Figure 4.b

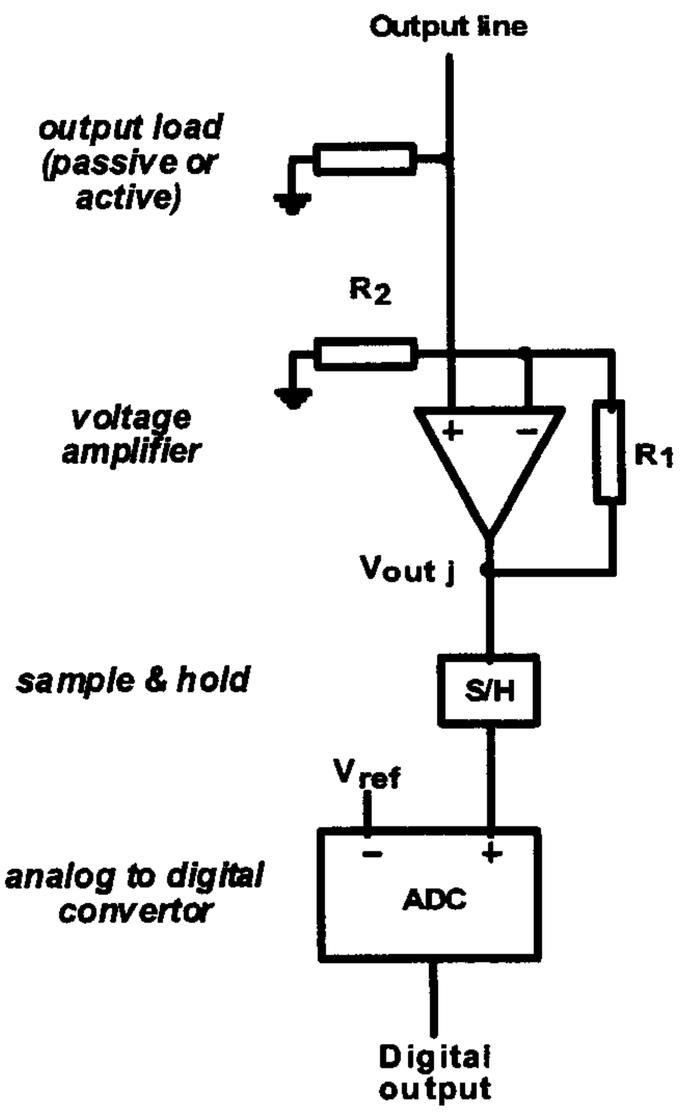


Figure 4.c

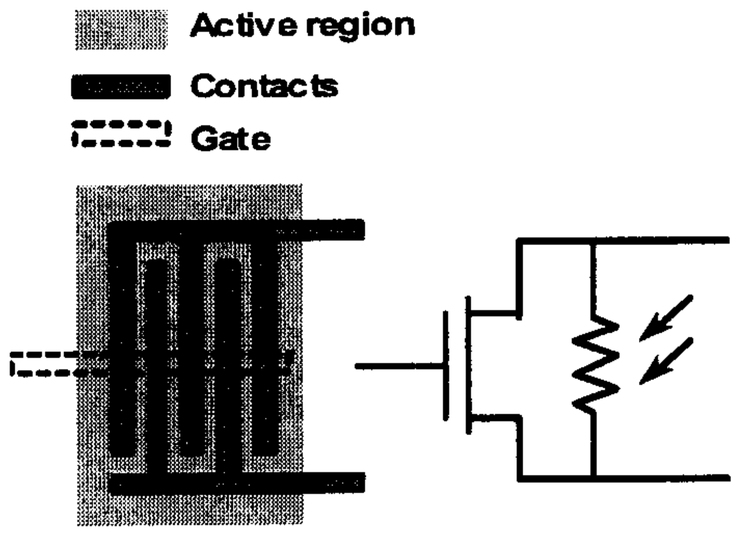


Figure 5.a

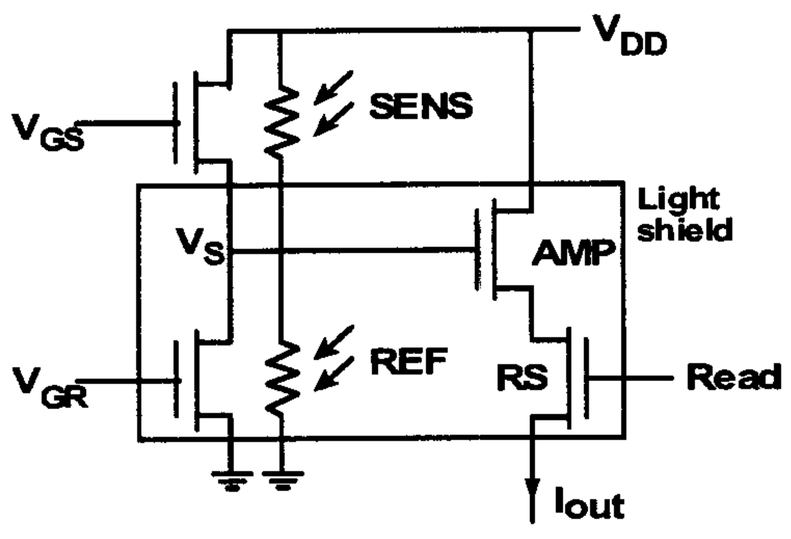


Figure 5.b

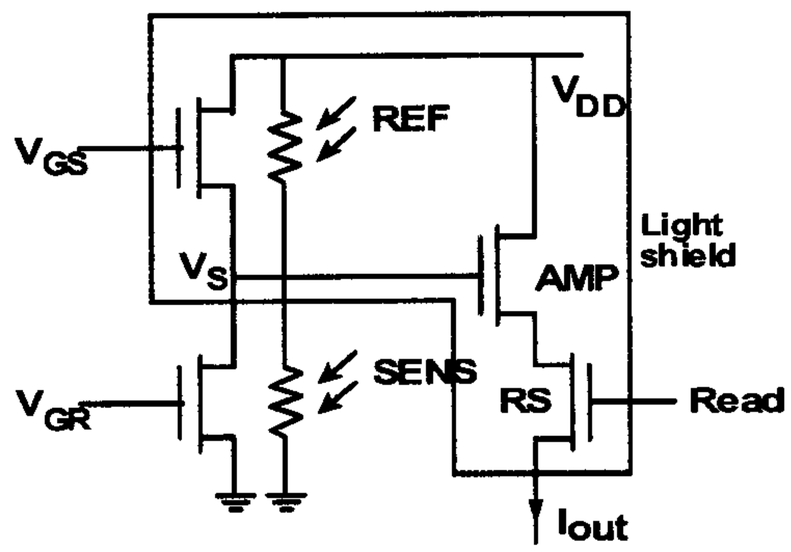


Figure 5.c

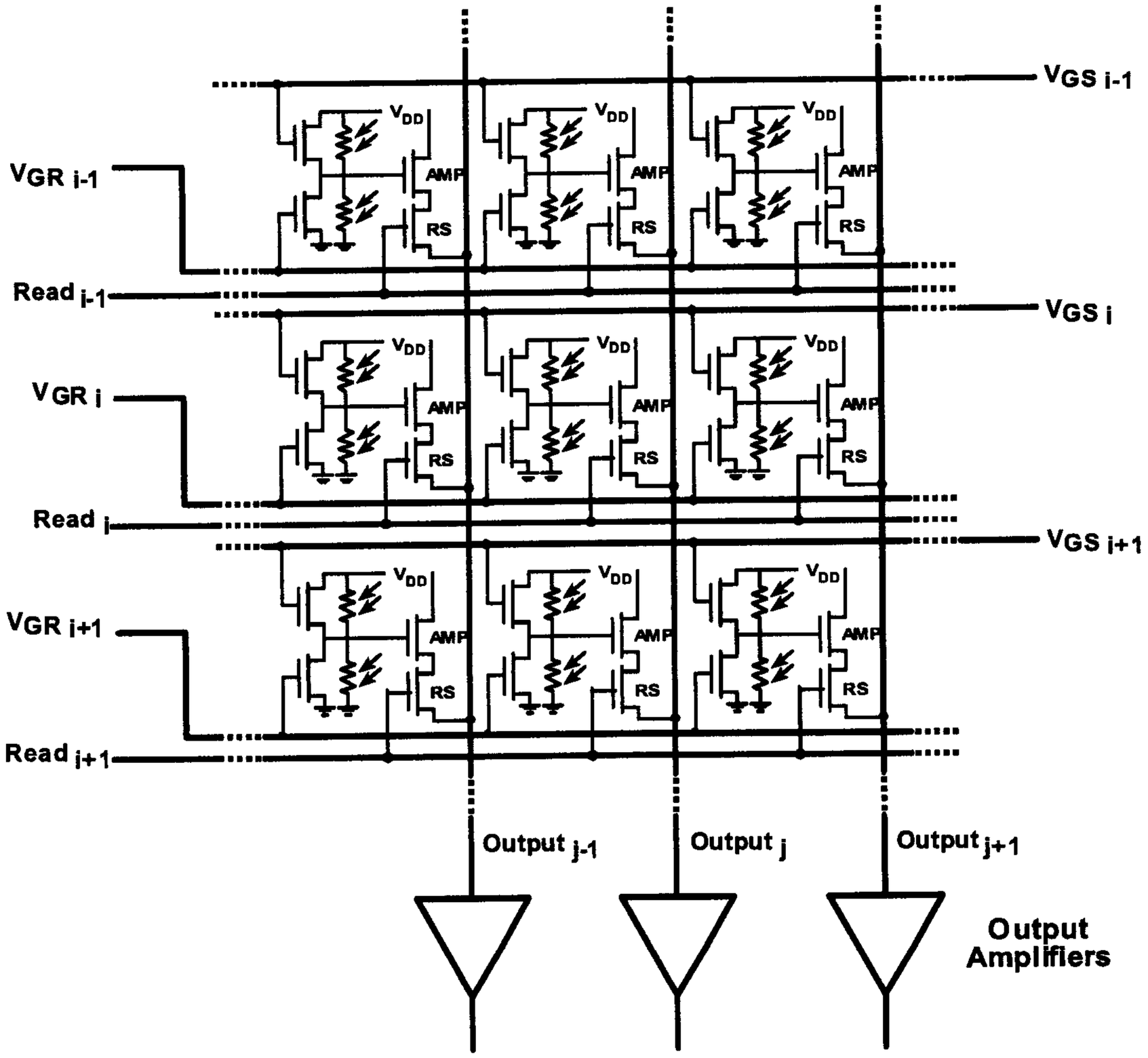

VGS i-1
VGR i-1
VDD
AMP
RS
Read i-1
VGS i
VGR i
Read i
VGS i+1
VGR i+1
Read i+1
Output j-1
Output j
Output j+1
Output Amplifiers

Figure 5.d

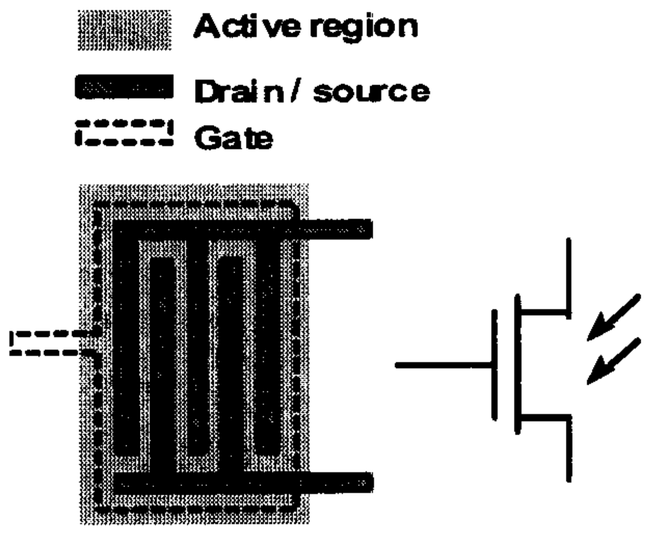


Figure 6.a

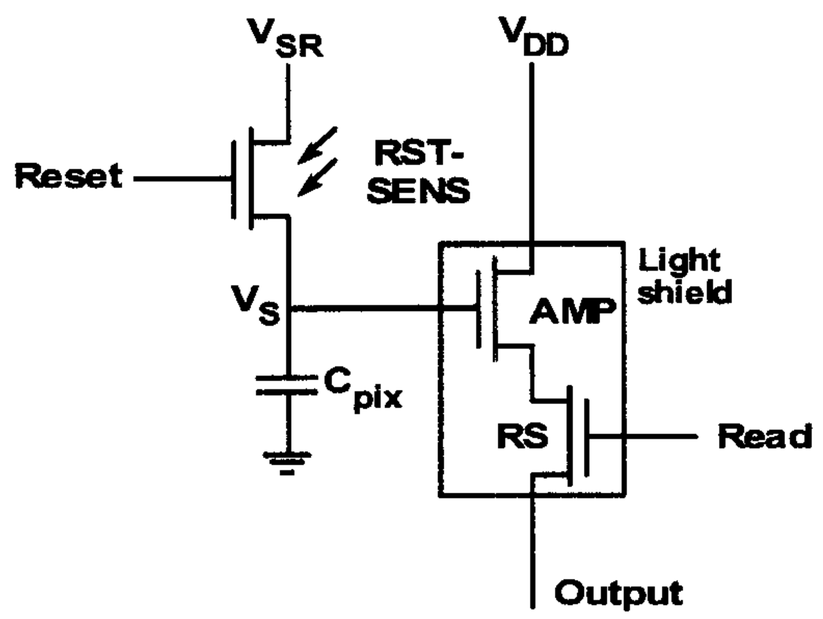


Figure 6.b

	Resetting	Integration	Redaout
Reset	High (10V...20V)	Low (0V…-5V)	Low (0V…-5V)
Read	Low (0V…-5V)	Low (0V…-5V)	High (10V…20V)
V_{RS}	High (10V…20V)	Low (0V…-5V)	Low (0V…-5V)
Output	-	-	Signal
RST-RS	ON-OFF	OFF-OFF	OFF-ON

Figure 6.c

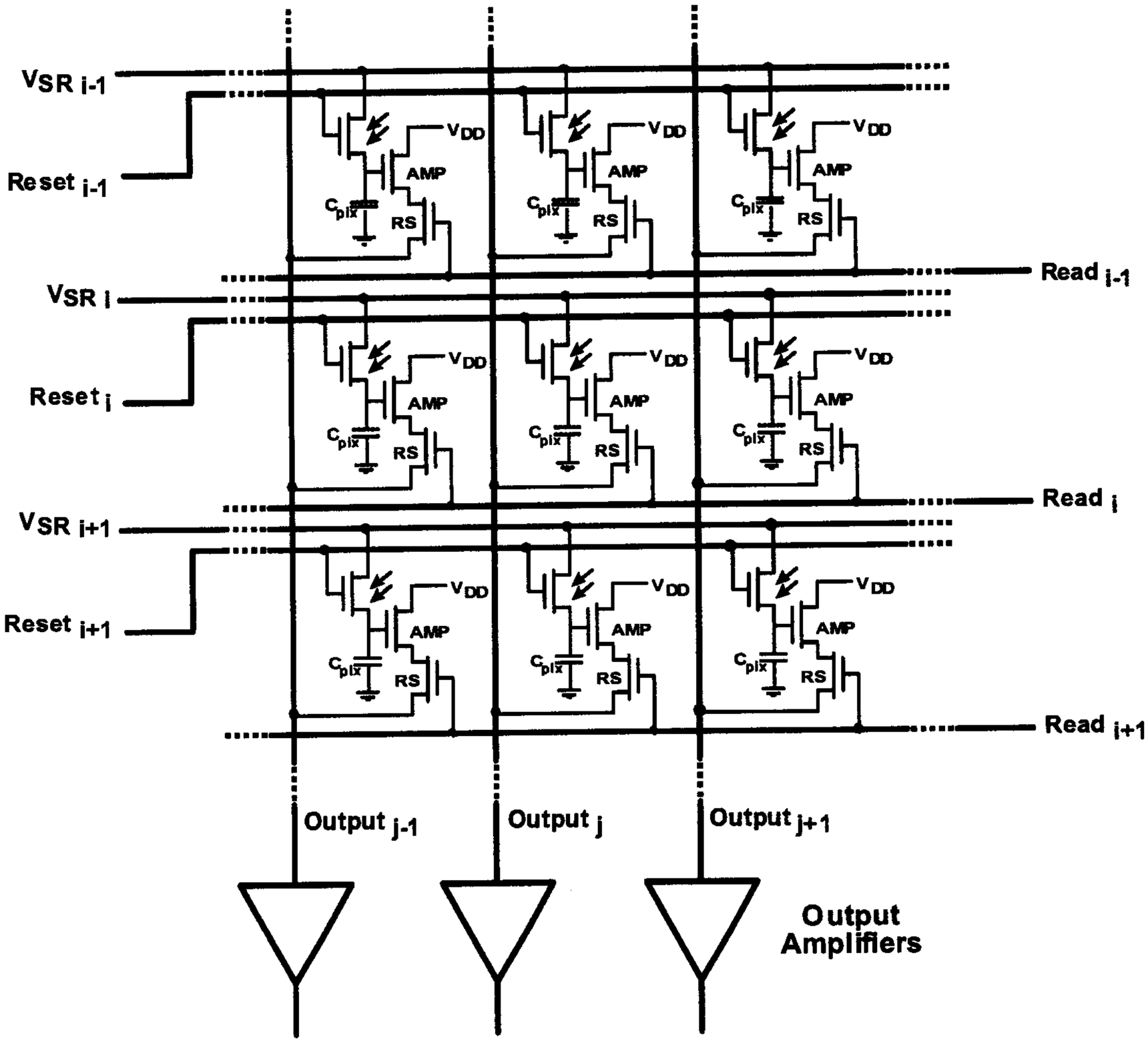

VSR i-1
Reset i-1
VSR i
Reset i
VSR i+1
Reset i+1
VDD
AMP
Cpix
RS
Read i-1
Read i
Read i+1
Output j-1
Output j
Output j+1
Output Amplifiers

Figure 6.d

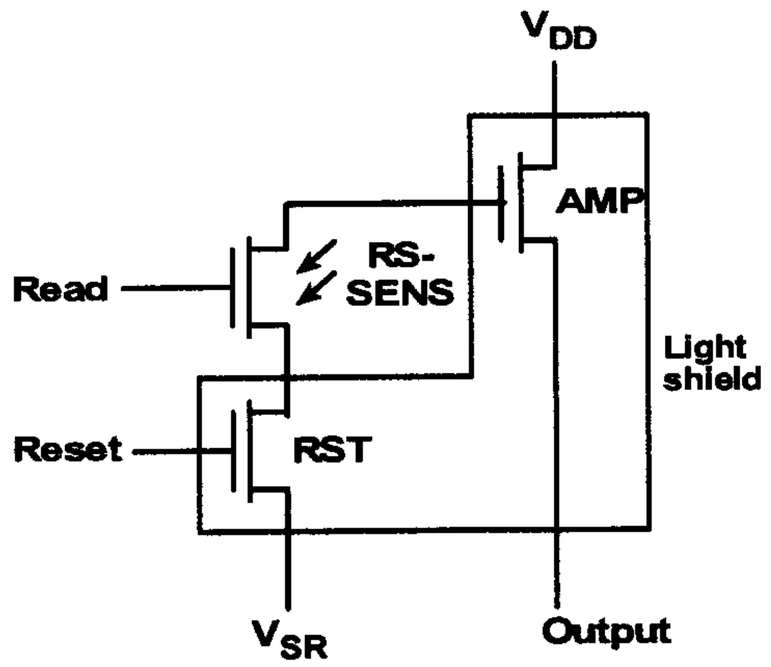


Figure 7.a

	Resetting	Integration	Redaout
Reset	High (10V...20V)	High (10V...20V)	Low (0V…-5V)
Read	High (10V...20V)	Low (0V…-5V)	High (10V…20V)
V_{RS}	Low (0V…-5V)	High (10V...20V)	-
Output	-	-	Signal
RST-AMP-RS	ON-OFF-ON	ON-OFF-OFF	OFF-ON-ON

Figure 7.b

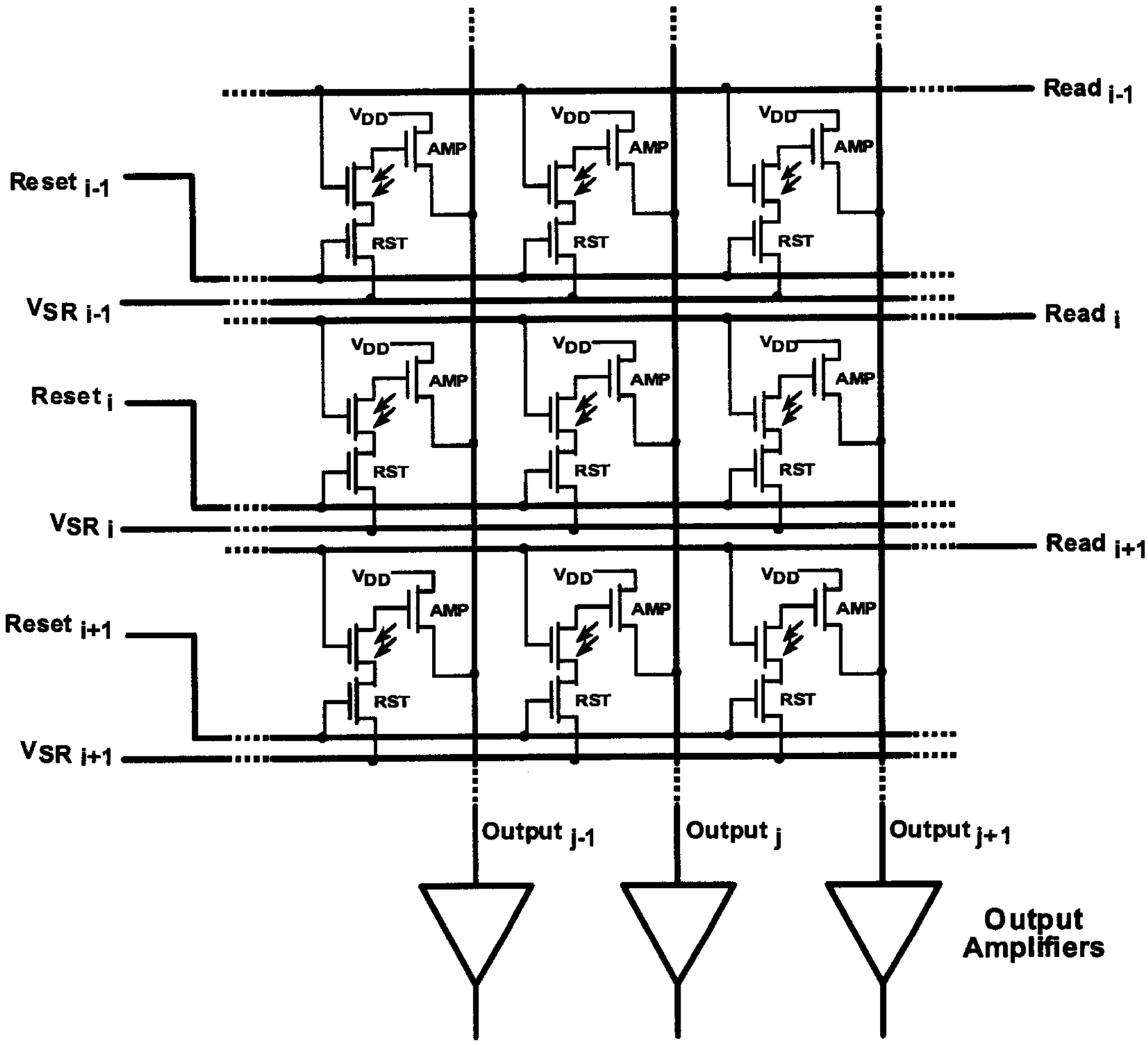

Read i-1
Reset i-1
VSR i-1
Read i
Reset i
VSR i
Read i+1
Reset i+1
VSR i+1
VDD
AMP
RST
Output j-1
Output j
Output j+1
Output Amplifiers

Figure 7.c

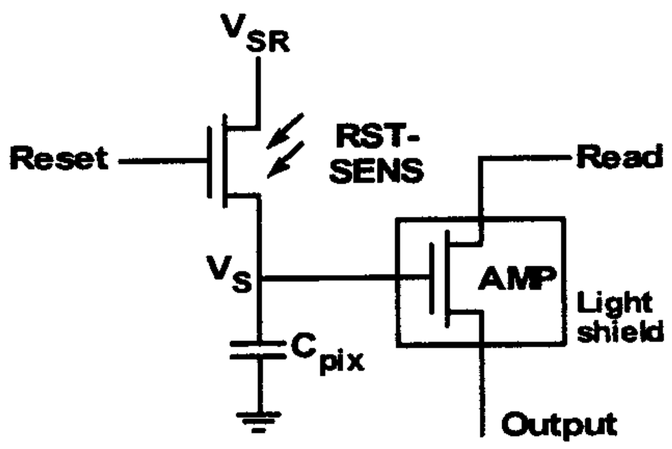


Figure 8.a

	Resetting	Integration	Readout
Reset	High (10V...20V)	Low (0V…-5V)	Low (0V…-5V)
Read	High (10V...20V)	High (10V...20V)	Low (0V…-5V)
V_{RS}	High (10V...20V)	Low (0V…-5V)	Low (0V…-5V)
Output	High (10V...20V)	High (10V...20V)	Signal (High)
RST-AMP	ON-OFF	OFF-OFF	OFF-ON

Figure 8.b

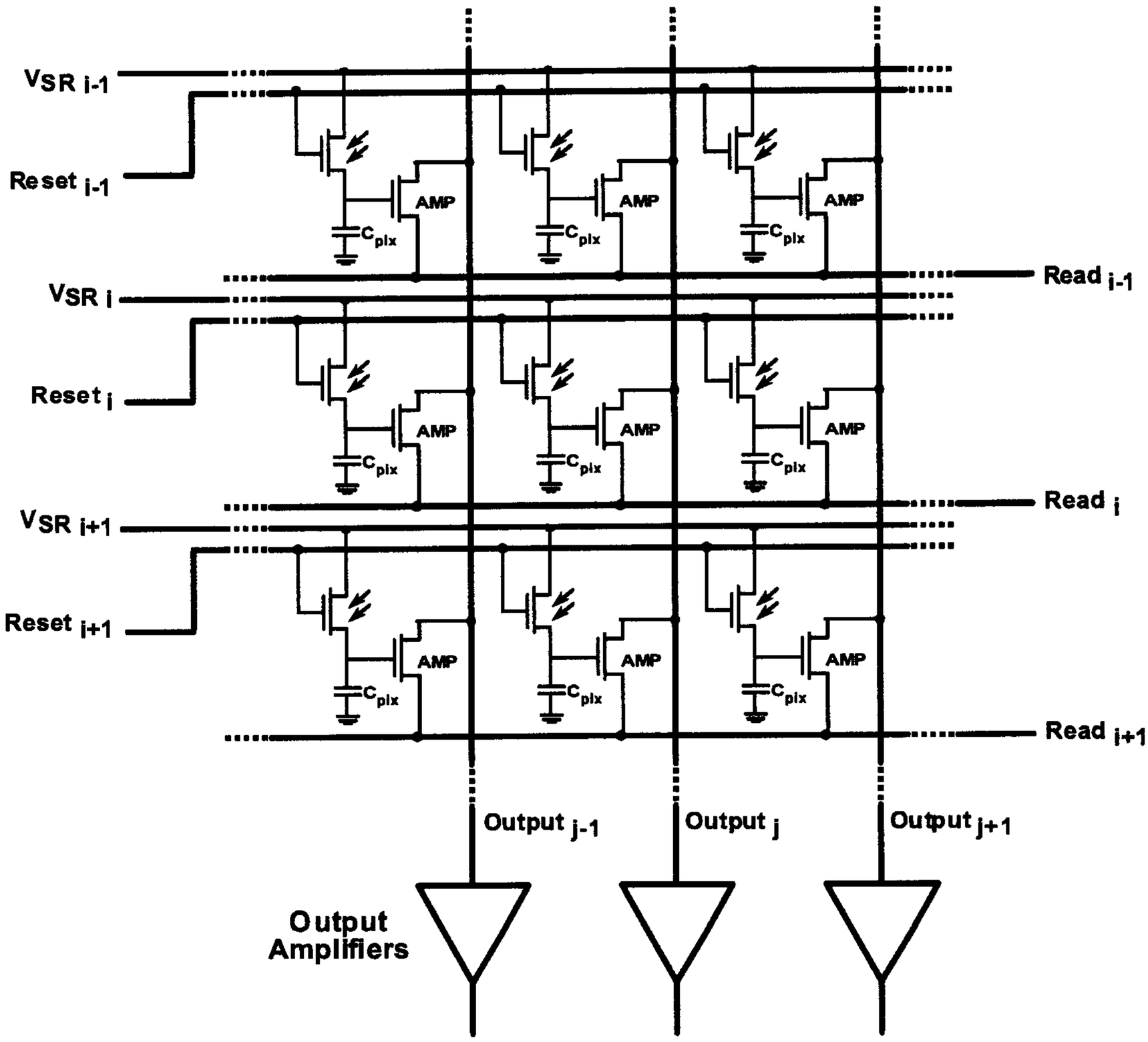

VSR i-1
Reset i-1
VSR i
Reset i
VSR i+1
Reset i+1
AMP
Cpix
Read i-1
Read i
Read i+1
Output j-1
Output j
Output j+1
Output Amplifiers

Figure 8.c

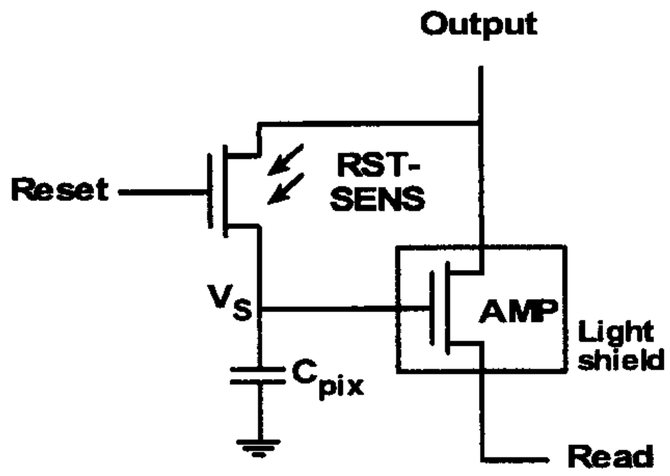


Figure 9.a

	Resetting	Integration	Readout
Reset	High (10V...20V)	Low (0V...-5V)	Low (0V…-5V)
Read	High (10V...20V)	High (10V...20V)	Low (0V…-5V)
Output	Moderate (5V...10V)	High (10V...20V)	Signal (High)
RST-AMP	ON-OFF	OFF-OFF	OFF-ON

Figure 9.b

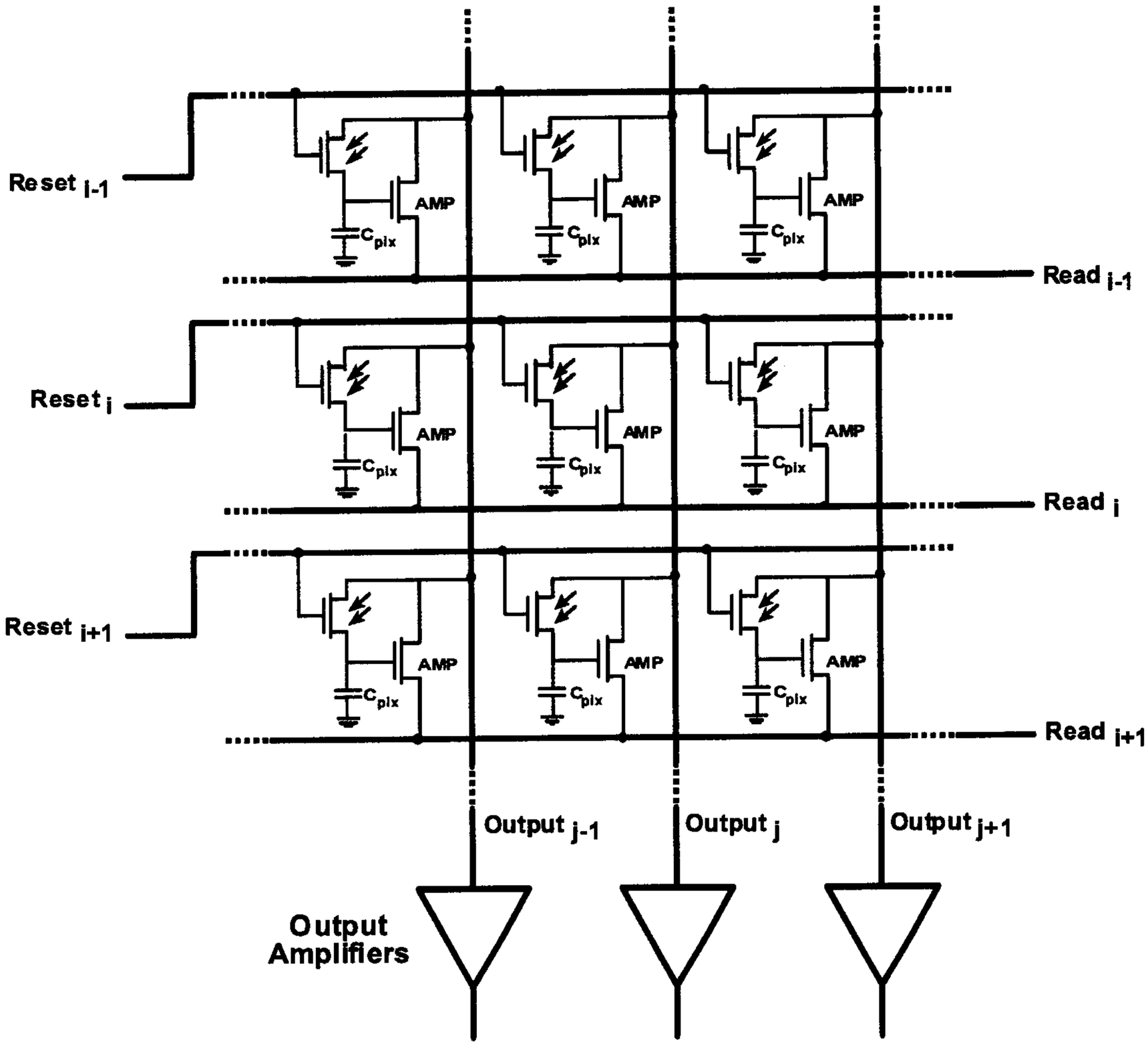
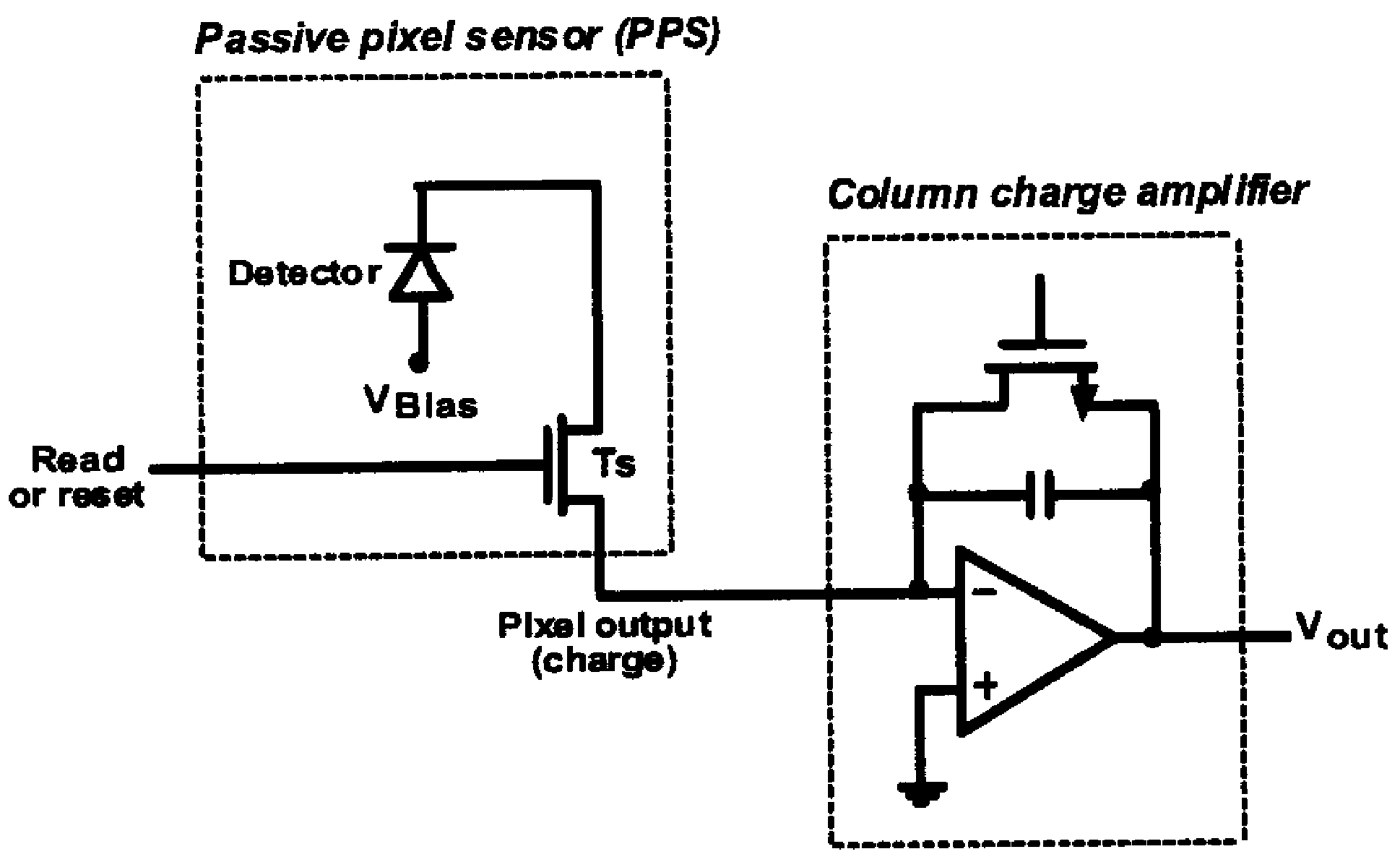

Reset i-1
Reset i
Reset i+1
AMP
C_{pix}
Read i-1
Read i
Read i+1
Output j-1
Output j
Output j+1
Output Amplifiers

Figure 9.c


Passive pixel sensor (PPS)
Detector
VBias
Read
or reset
Ts
Pixel output
(charge)
Column charge amplifier
Vout