

---

**(12) PATENT ABRIDGMENT (11) Document No. AU-B-44488/89**  
**(19) AUSTRALIAN PATENT OFFICE (10) Acceptance No. 623192**

---

(54) Title  
**COMMUNICATION SYSTEM USING A COMMON MEMORY**

International Patent Classification(s)  
(51)<sup>4</sup> **G06F 013/00 G06F 015/16**

(21) Application No. : **44488/89**

(22) Application Date : **08.11.89**

(30) Priority Data

(31) Number (32) Date (33) Country  
**63-282805 09.11.88 JP JAPAN**

(43) Publication Date : **17.05.90**

(44) Publication Date of Accepted Application : **07.05.92**

(71) Applicant(s)  
**FUJITSU LIMITED**

(72) Inventor(s)  
**TOSHIHIDE OKABE**

(74) Attorney or Agent  
**SPRUSON & FERGUSON , GPO Box 3898, SYDNEY NSW 2001**

(56) Prior Art Documents  
**AU 614502 81567/87 G06F 13/00 15/16**  
**EP 133568**

(57) Claim

1. A communication system in which a common memory is used for storing data transmitted by a plurality of units, said system comprising:  
means for writing data transmitted from a first one of said units into a predetermined area of said common memory,

means for producing an interruption signal for interrupting a second one of said respective units based on the data stored in said common memory, said means for producing an interruption signal comprising a decoder for decoding a write command and address data transmitted from the first unit to provide an interruption signal corresponding to the first unit, and

means for reading the data from said predetermined area of said common memory which corresponds to said first unit, following an interruption process of said second unit in which said second unit receives said interruption signal produced by said interruption signal producing means, whereby

a communication between first and second units can be conducted.

2. The communication system according to claim 1, wherein said decoder comprises an address decoder for decoding an address of the data to be written in said common memory and a gate for receiving the write command from the first unit to form said interruption signal based on said address data.

FORM 10

COMMONWEALTH OF AUSTRALIA

PATENTS ACT 1952

COMPLETE SPECIFICATION

623192

(ORIGINAL)

FOR OFFICE USE:

Class      Int Class

Complete Specification Lodged:  
Accepted:  
Published:

Priority:

Related Art:

Name and Address  
of Applicant:

Fujitsu Limited  
1015, Kamikodanaka, Nakahara-ku  
Kawasaki-shi  
Kanagawa 211  
JAPAN

Address for Service: Spruson & Ferguson, Patent Attorneys  
Level 33 St Martins Tower, 31 Market Street  
Sydney, New South Wales, 2000, Australia

Complete Specification for the invention entitled:

Communication System Using a Common Memory

The following statement is a full description of this invention, including the best method of performing it known to me/us

A B S T R A C T

A plurality of processors and a particular processor use a common memory. A processor for  
5 requesting a communication with the particular processor writes a data in a predetermined address of the common memory which corresponds to the processor. Upon writing the data into the common memory, an interruption signal is produced to interrupt the  
10 particular processor. The particular processor processes the interruption signal and determines which processor requests the communication with the particular processor and reads a data from the address area in the common memory which corresponds  
15 to the processor, thereby enabling a communication between the processors to be conducted.

20

25

Communication System using a Common Memory

Background of the Invention

The present invention relates to a system for communicating between data processing systems and  
5 between units constituting a data processing system.

With the recent expansion in the variety of data processes, communication is carried out between data processing systems or between units constituting a data processing system.

10 Communication between units (apparatuses within the same system) or between adjacent systems, can be conducted through a memory commonly owned by those units.

In prior art systems a data reading is carried  
15 out using a polling method. With this method, communication speed between units depends on the polling period, which limits the effectiveness of the communication by the common memory cannot. Therefore, a more effective communication method  
20 using a common memory is necessary. Figure 1 shows a prior art communication system using a common memory.

According to the prior art common memory technology, a writable and readable memory is co-owned by a plurality of units (for example, unit A  
25 and unit B) and a special meaning (for example, a

command area or data area) is given to the predetermined address of the common memory 2.

When unit A1 intends to send something to unit B1, predetermined data such as commands are written  
5 in a predetermined address of the common memory in unit A1.

Unit B1 enables the data to be read out periodically from the previously defined address by using a wellknown polling method and recognizes the  
10 above communication data transmitted from unit A1.

According to the communication system of the above prior art method, it is necessary for unit B1 to periodically perform a polling to common memory  
2. The communication speed depends on the polling  
15 period of unit B1 and therefore cannot reach the desired level.

#### Summary of the Invention

An object of the present invention is to provide a communication system in which the communication  
20 speed in a common memory is not limited by the polling period of the common memory when, in a communication between data process systems or between units constituting a data process system, polling is conducted by the unit on the receiving side.

25 ~~A feature of the present invention is to provide~~  
<sup>Accordingly</sup>  
k



a communication system in which a common memory is used for storing data transmitted by a plurality of units, said system comprising:

means for writing data transmitted from a first one of said units into a predetermined area of said common memory,

5 means for producing an interruption signal for interrupting a second one of said respective units based on the data stored in said common memory, said means for producing an interruption signal comprising a decoder for decoding a write command and address data transmitted from the first unit to provide an interruption signal corresponding to the  
10 first unit, and

means for reading the data from said predetermined area of said common memory which corresponds to said first unit, following an interruption process of said second unit in which said second unit receives said interruption signal produced by said interruption signal  
15 producing means, whereby

a communication between first and second units can be conducted.  
Brief Description of the Drawing

Figure 1 shows a view for explaining the communication system according to the prior art,

20 Figure 2 shows the principle of the communication system according to the present invention,

Figure 3 shows a block diagram of an embodiment of the present invention,

Figure 4 shows a block diagram of the present embodiment in which  
25 MAC is shown more in detail,



LMM/627E

Figure 5 shows a flowchart of an interruption routine conducted in a service processor, and

Figure 6 is a block diagram of another embodiment of the present invention.

5 Detailed Description of the Preferred Embodiment

As shown in Figure 2, in a data processing system equipped with a plurality of units (A, B) 1 and common memory 2, an interruption signal 4 is transmitted from a unit (A) 1 to a unit (B) 1 in accordance with a writing 3 to a predetermined address of the common memory 2, the predetermined address in the common memory corresponding to unit (A). Unit (B) 1 receives an interruption signal 4 produced by unit 22. It performs an interruption process and reads the data in a predetermined area of the common memory 2, the predetermined area corresponding to the interruption signal, thereby performing a communication between units.

The present invention provides a communication system between data processing systems and between units constituting a data process system. When an event to be notified to a predetermined unit (for example unit (B)) happens and a writing 3 corresponding to the event is conducted in the predetermined address of the common memory from the

unit (A) and the address of the common memory is decoded by an address decoder 22, it produces an interruption signal 4 to a predetermined unit (B). The predetermined unit (B) receiving the interruption  
5 signal 4 reads the predetermined address corresponding to the kind of interruption signal 4 to recognize the content of the event. A predetermined event can be notified quickly from one unit (A) to another (B) and thus, the unit receiving  
10 the notification does not need to apply a polling process to the common memory 2. Therefore, the structure of a common control program of a unit (A, B) is simplified, thereby increasing the processing capability of respective units (A, B).

15 Figure 3 shows a block diagram of an embodiment of the present invention. A unit 22 decodes the address in which the data is written as shown by a writing 3 in the common memory 2 from respective units (communication units A, B, C...) 1 and produces  
20 an interruption signal 4 to the predetermined unit (D) 1. This unit 22 is important in realizing the present invention. The same reference numbers show the same items throughout all the drawings.

A communication system using a common memory  
25 according to the present invention will be explained

by referring to Figures 3 more in detail.

The present embodiment does not relate to two-way communication but to one-way communication in which the data is transmitted from units (A, B, and C) to notify a certain event to unit (D). By expanding this system, a communication from a particular unit to a discretionary unit can be realized.

When an event occurs in units (A, B, and C) it is notified to unit(D)1. Then respective units (A, B, and C) write the item code, for example, on the address representing an area 21 corresponding to respective units on common memory 2.

Then three kinds of interruption signal 4 corresponding to units (A, B, and C) for performing a writing 3 are produced by address decoder circuit 22a and transmitted to unit (D) 1 through logical product circuit 22b.

Unit (D) 1 reads the content of areas 21 of the common memory 2 (namely, the areas corresponding to units (A), (B) and (C)) which are previously determined in accordance with three kinds of interruption signals 4, thereby quickly recognizing the above notification event.

As described above, the present invention

provides a system for communicating between data processing systems and between units forming a data processing system. It writes, as shown by a writing 3, a code of an event in an address corresponding to the units (A, B, and C) on the common memory 2 when the event occurring in respective units (A, B, and C) is notified to the other unit (D). Then it produces an interruption signal 4 for the other unit by decoding the writing address in common memory 2, and notifies the other unit (D) of the occurrence of the event by using different interruption signals 4.

As described above, the present communication system performs a communication between data processing systems and units constituting a data processing system. A unit produces an interruption signal 4 to a predetermined unit (D) by using a writing 3 into a predetermined address of the common memory, the address corresponding to respective units (A, B and C). The interruption signal 4 produced by unit 22 is received through the interruption process for unit (D) 1 to read predetermined area data of the common memory in accordance with the interruption signal 4, thereby performing a communication between units. A predetermined event can be notified from one unit to another at high speed and the unit

receiving the notification does not need to perform a polling process to the common memory 2. This simplifies the structure of the control program in respective units (A, B, C, D...) 1 and includes a  
5 processing capability of respective units.

A detailed circuit of a memory access controller (MAC) 30 of a communication system using the common memory in accordance with the present invention is shown in Figure 4.

10 Processors (1), (2), (3)...(8) 31 are connected to common memory 32, through system information bus (SIBUS) 33 which is used as a common bus. Another processor corresponds to unit D of Figure 3 and comprises a service processor (SVP) 34. The  
15 embodiment shown in Figure 4 comprises 8 processors (1)...(8) 31 and SVP 34 which communicates with them, thereby providing a communication control system using a common memory 32, in which N vs. 1 communication is conducted. MAC 30 further comprises  
20 system information bus input registers (SIBIR (0), (1) and (2)) 35 and multiplexer (MPX), first command register (CMD) 36, first address register (ADR) 37 and first write data register (WDR) 38, decoder 39 and memory control logic circuit (MEM  
25 CNTL) 40, first read data register (RDR) 41, second

read data register (RDR) 42, interruption register  
(INTR) 43, second command register (CMD) 44, second  
address register (ADR) 45, second write data register  
(WDR) 46 and system information bus output register  
5 (SIBOR) 47. The outputs of respective information  
bus input registers (SIBIR (0), (1) and (2)) 35 are  
connected to multiplexer (MPX). The output of the  
multiplexer (MPX) is connected to first command  
register (CMD) 36, first address register (ADR) 37  
10 and first write data register (WDR) 38. The output  
of first command register (CMD) 36 and first address  
register (ADR) 37 are connected to decoder 39 and the  
output of first write data register 38 is connected  
to common memory 32. The output of first address  
15 register 37 is also connected to a gate (G) to  
provide the address signal for common memory 32. The  
data read from common memory 32 is set in first read  
data register (RDR) 41 and the output of first read  
data register 41 is provided to second read data  
20 register (RDR) 42. An interruption signal obtained  
by decoding the output from first command register  
(CMD) 36 and first address register (ADR) 37 by  
decoder 39 is set in interruption register (INTR) 43.  
System information buffer in register (SIBIR(0), (1)  
25 and (2)) 35 is formed to have three kinds of

information set therein so that the differences in  
time between 4-bit-command, 18-bit-address and 16-  
bit-writing data is absorbed. Multiplexer (MPX)  
selects the above three kinds of information. The  
5 selected information is set in respective registers  
36, 37 and 38 after they are divided into 4-bit-  
command, 18-bit-address and 16-bit write data.  
Decoder 39 decodes the outputs of first command  
register 36 and first address register 37 as recited  
10 above.

First command register (CMD) 36 receives a write  
command and first address register 37 receives a  
particular address, thereby forming an 8-bit  
interruption signal. The 8-bit interruption signal  
15 corresponds to the request for the interruption  
received from processors (1)...(8) 31 and the thus-  
obtained interruption signal is set in interruption  
register (INTR) 43. When a write command is received  
by first command register (CMD) 36, memory controller  
20 (MEM CNTL) 40 performs a write control of common  
memory 32 by obtaining write data from first write  
register (WDR) 38 and stores the 16-bit write data  
in an address designated by first address register  
(ADR) 37. The storing areas correspond to respective  
25 processors (1)...(8) and the write data is stored in

an area corresponding to the processor which requests an interruption operation. The interruption signal from the decoder 39 is set in interruption register 43 and is provided to service processor 34 as an interruption request signal. Service processor (SVP) 34 receives the interruption signal and determines which of bits 0 to 7 in interruption register 43 is 1 and enables an interruption process routine so that the communication areas of the common memory 32 corresponding to processors 1 to 8 are read. Therefore, service processor (SVP) 34 performs a read and write operation for common memory 32. Therefore, the 4-bit read command outputted from service processor (SVP) 34 is stored in the second command register (CMD) 44. This 4-bit command (CMD) is provided to memory controller (MEM CNTL) 40 through first command (CMD) register 36 to perform a read operation of common memory 32. When the data is read from the communication area of common memory 32, the reading address is provided by service processor (SVP) 34 as 18 bit address data through second address register (ADR) 45. The read out content is provided to service processor (SVP) 34 through first and second read registers (RDR) 41 and 42. When the data is written to common memory 32 from service

processor (SVP) 34, the write command is set in second command register (CMD) 44 and the write data is set in second write register (WDR) 46, thereby controlling memory controller (MEM CNTL) 40 to perform a write operation for common memory 32 by writing the write data into common memory 32.

Figure 5 shows a flowchart of an interruption process routine applied to common memory 32 and is conducted by the service processor (SVP) 34. When an 8-bit interruption signal is provided in interruption register (INTR) 43, service processor (SVP) 34 enters an interruption process routine for common memory 32 and an interruption handler starts to operate (ST1). At first, the process reads 8-bit interruption signal from interruption register (INTR) 43 (ST2) and specifies (ST3) the processor number among the processors (1) to (8) depending on which of bits 0 to 7 is 1. When the processor (1) sends an interruption request to common memory 32, it stores the data in the area corresponding to the processor (1) in the common memory and the service processor (SVP) 34 executes a read operation for the communication area in common memory 32 (ST4), the communication area corresponding to the processor (1). Therefore, the service processor (SVP) 34 sets a read command and

read address in the second command register (CMD) and the second address register (ADR) 45, respectively, to read common memory 32 and the content of common memory 32 is read out to service processor (SVP) 34.

5 In step ST5, the process analyzes the command which is provided as a part of data obtained from the communication area of common memory 32, thereby transmitting the data as a message transmission to a task of the service processor (SVP) 34 in accordance with the command (ST6). As shown in Figure 5, the service processor (SVP) 34 has a plurality of kinds of tasks corresponding to respective processes, and the data is transmitted to the respective tasks based on the result of the analysis of the command in accordance with data transmitted by the corresponding processor. Therefore, generally speaking, N vs. 1 communication is possible between processors (1) to (8) and service processor (SVP) 34.

Figure 6 shows a detailed diagram of the communication system using the common memory in a case of N vs. N processors. The same reference numbers as shown in Figure 4 represent the same items. The embodiment shown in Figure 6 differs from the embodiment shown in Figure 4, which represents the N vs. 1 communication case, as follows. Within memory

access controller (MAC) 30, the output of decoder 39, namely, the interruption request signal of 8 bits is set in an interruption register (INTR) 43. In the previous embodiment shown in Figure 4, the content of  
5 interruption register (INTR) 43 is sent to the service processor (SVP) 34, which is different from processors (1) to (8). However, in the embodiment shown in Figure 6 the service processor (SVP) 34 is not used and the interruption signal is again  
10 transmitted to processors (1) to (8).

The interruption register (INTR) 43 contains 8 bits and respective bits correspond to processors (1) to (8). Respective processors are not requested by the interruption request signal issued by the  
15 processors themselves. Therefore, each of respective processors (1) to (8) masks a bit of the interruption signal, the bit corresponding to each of respective processors (1) to (8). Namely, the processor which issues the interruption request is different from  
20 the processor which receives the interruption signal. Thus, it becomes possible to perform a communication with other processors by using the interruption process signal.

Data are transmitted from processor (1), through  
25 system information bus (SIBUS) 33 and system

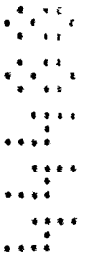
information buffer input register (SIBIRO to 2) 35 in  
memory access controller (MAC) 30. Memory access  
controller (MAC) 30 sets these data in 4-bit command  
register (CMD) 36, 18-bit address register (ADR) 37  
5 and 16-bit write register (WDR) 38, respectively.  
Decoder 39 decodes the 4-bit write command in command  
register (CMD) 36 to confirm that the data are for  
writing and uses the write command and an address  
provided by address register (ADR) 37 to provide an  
10 8-bit interruption signal, thereby setting it in  
interruption register (INTR) 431. In order to  
perform an interruption to processor (3), for  
example, the content of interruption register (INTR)  
431 is provided such that the third bit is 1 and  
15 other bits are 0. Therefore, the signal read out  
from interruption register (INTR) 431 is sent to  
processors (1) to (8), but as the bit corresponding  
to processor (3) is "1", an interruption request is  
provided only to processor (3). Then, processor (3)  
20 performs an interruption process routine, and  
therefore, processor (3) provide a read command to  
common memory 32 through system information buffer  
input register (SIBIR) 35. Thus, an address is  
provided for access to a communication area of  
25 common memory 32. This area corresponds to the

processor (1) as command register (CMD) 44 provides a  
READ command. Memory controller (MEM CNTL) 40 is  
controlled to perform a read operation and the read  
address is provided through read address register  
5 (ADR) 37. Then, data is read out from a  
communication area on read memory 32 corresponding to  
processor (1). The data are provided to system  
information bus (SIBUS) 33 through read data register  
(RDR) 41 and system information buffer output  
10 register (SIBOR) 46. The system information bus  
(SIBUS) 33 shown at the bottom of the drawing is the  
same as that shown in the top of the drawing.  
Therefore, the data is read out from common memory 32  
to the processor (3). The data read out from common  
15 memory 32 are provided by processor (1), thereby  
enabling a communication from processor (1) to  
processor (3).

As stated above, according to the present  
invention, the data from respective processor units  
20 are written into a predetermined address of the  
common memory and an interruption signal for  
interrupting a predetermined processor is generated.  
This interruption signal is received by a different  
processor unit, thereby enabling the data on the  
25 predetermined area of the common memory to be read

out in accordance with the interruption process and enabling a communication between units.

5



10

15



20



25

The claims defining the invention are as follows:

1. A communication system in which a common memory is used for storing data transmitted by a plurality of units, said system comprising:  
means for writing data transmitted from a first one of said units  
5 into a predetermined area of said common memory,

means for producing an interruption signal for interrupting a second one of said respective units based on the data stored in said common memory, said means for producing an interruption signal comprising a decoder for decoding a write command and address data transmitted from  
10 the first unit to provide an interruption signal corresponding to the first unit, and

means for reading the data from said predetermined area of said common memory which corresponds to said first unit, following an interruption process of said second unit in which said second unit  
15 receives said interruption signal produced by said interruption signal producing means, whereby

a communication between first and second units can be conducted.

2. The communication system according to claim 1, wherein said decoder comprises an address decoder for decoding an address  
20 of the data to be written in said common memory and a gate for receiving the write command from the first unit to form said interruption signal based on said address data.

3. The communication system according to claim 1, wherein said common memory has a plurality of areas corresponding to  
25 respective units which request data transmission.

4. The communication system according to claim 1, wherein said second unit for receiving said interruption signal accesses said common memory based on the content of a predetermined address in accordance with the kind of said interruption signal and reads the  
30 content from the area of the common memory, the area corresponding to the first unit.

5. The communication system according to claim 4, wherein said second unit for receiving the interruption signal reads the content of an interruption register and determines the area of the common  
35 memory which corresponds to the first unit to read the data from the common memory, decodes a command included in the read data and transmits the data to a task corresponding to said command in said second unit.



6. The communication system according to claim 1, wherein said second unit for receiving the interruption signal and for performing the interruption processes comprises a service processor.

7. The communication system according to claim 1, wherein  
5 said plurality of units comprises N first processors and a second processor,

said data writing means comprises a first command register for storing a command from said first processor, a first address register for storing an address of data to be written in said common memory and a  
10 write data register for storing said data, said first command register, first address register and write data register being connected to said N first processors,

said interruption signal producing means comprises a decoder for decoding the outputs of said first command register and first address  
15 register, to produce said interruption signal and an interruption register for storing said interruption signal, and

said data reading means comprises a second command register for storing a command from said second processor, and a second address register for storing an address from which data is read from the common  
20 memory, said second command register and second address register being connected to said common memory through said first command register and first address register, said data reading means further comprising a read data register connected to the common memory for storing the data read out from said common memory; wherein said second command register, second  
25 address register, read data register and interruption register are connected to said second processor, whereby said N first processors communicate with said second processors.

8. The communication system according to claim 1, wherein  
30 said plurality of units comprises N processors, one of said N processors communicating with another of said N processors, and requesting a communication, wherein said one of said N processors writes data in a predetermined address of the common memory and produces an interruption signal to interrupt said another processor, which receives the interruption signal and reads the data from the communication area of  
35 the common memory which corresponds to said one processor based on the interruption signal and then masks a bit corresponding to one unit itself in the interruption signal, whereby said one of said N processors communicates with said another of said N processors.



627E

9. The communication system according to claim 1, wherein  
said data writing means comprises a command register for storing a  
command from said one processor, address register for storing an address  
of data to be written in said common memory by said one processor and  
5 write data register for storing said data,

said interruption signal processing means comprises a decoder for  
decoding the outputs of said command register and address register to  
produce said interruption signal, and an interruption register for  
storing said interruption signal, and

10 said data reading means comprises a read data register for storing  
said data read from said common memory in accordance with a read command  
stored in said command register and a read address stored in said address  
register and corresponding to one processor.

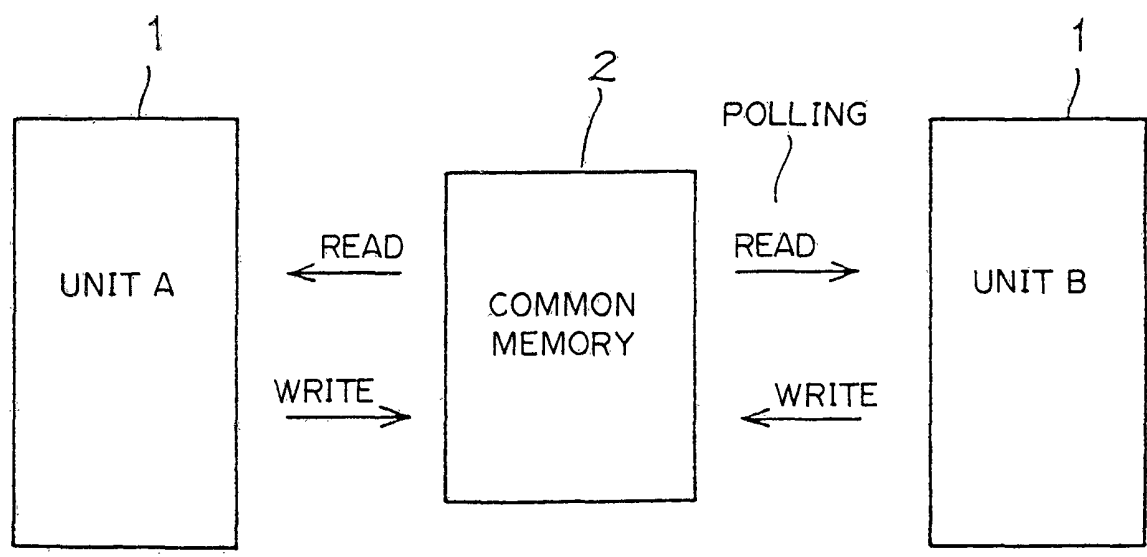
15 10. A communication system substantially as hereinbefore described  
with reference to Figures 2 to 6 of the drawings.

DATED this FOURTEENTH day of FEBRUARY 1992  
Fujitsu Limited

Patent Attorneys for the Applicant  
SPRUSON & FERGUSON



0100 4400



PRIOR ART

Fig. 1

8170 4/10/64

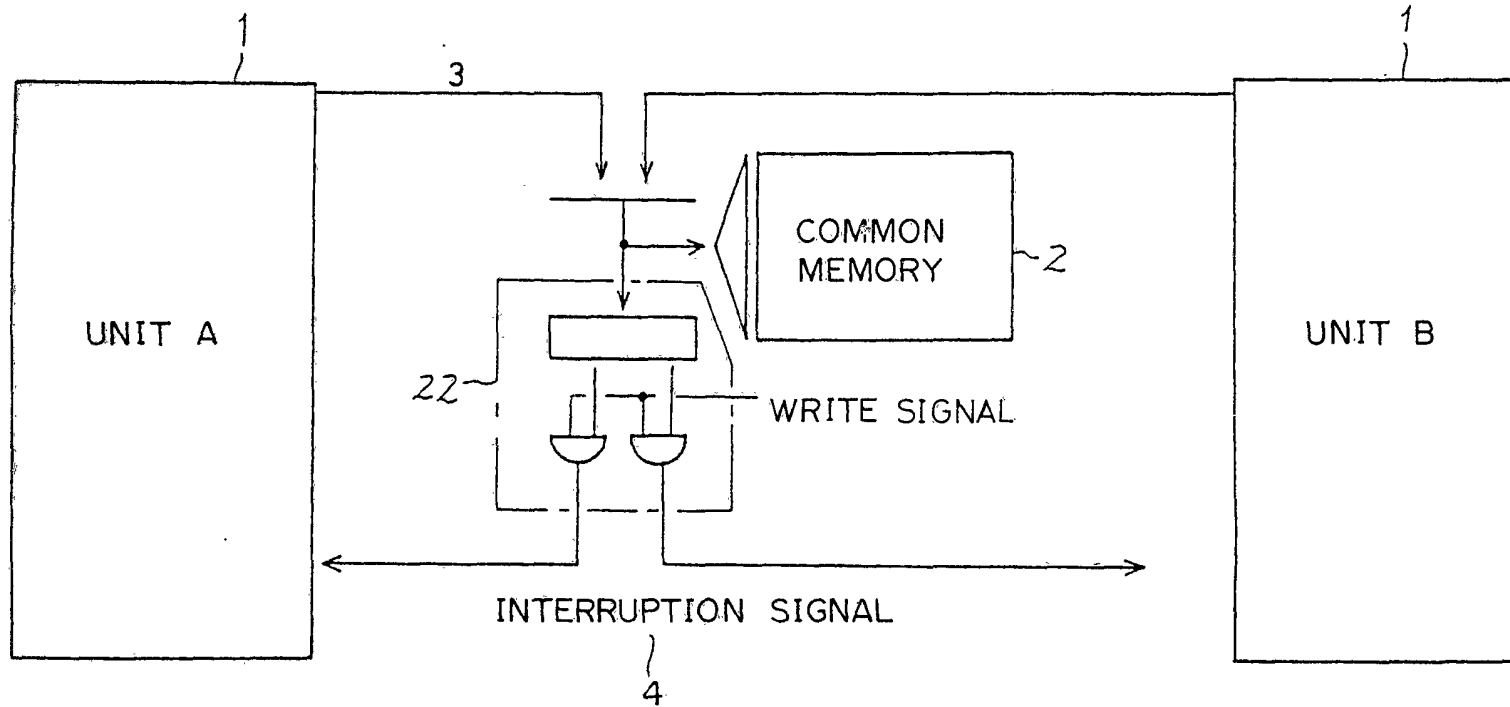


Fig. 2

0100 4400

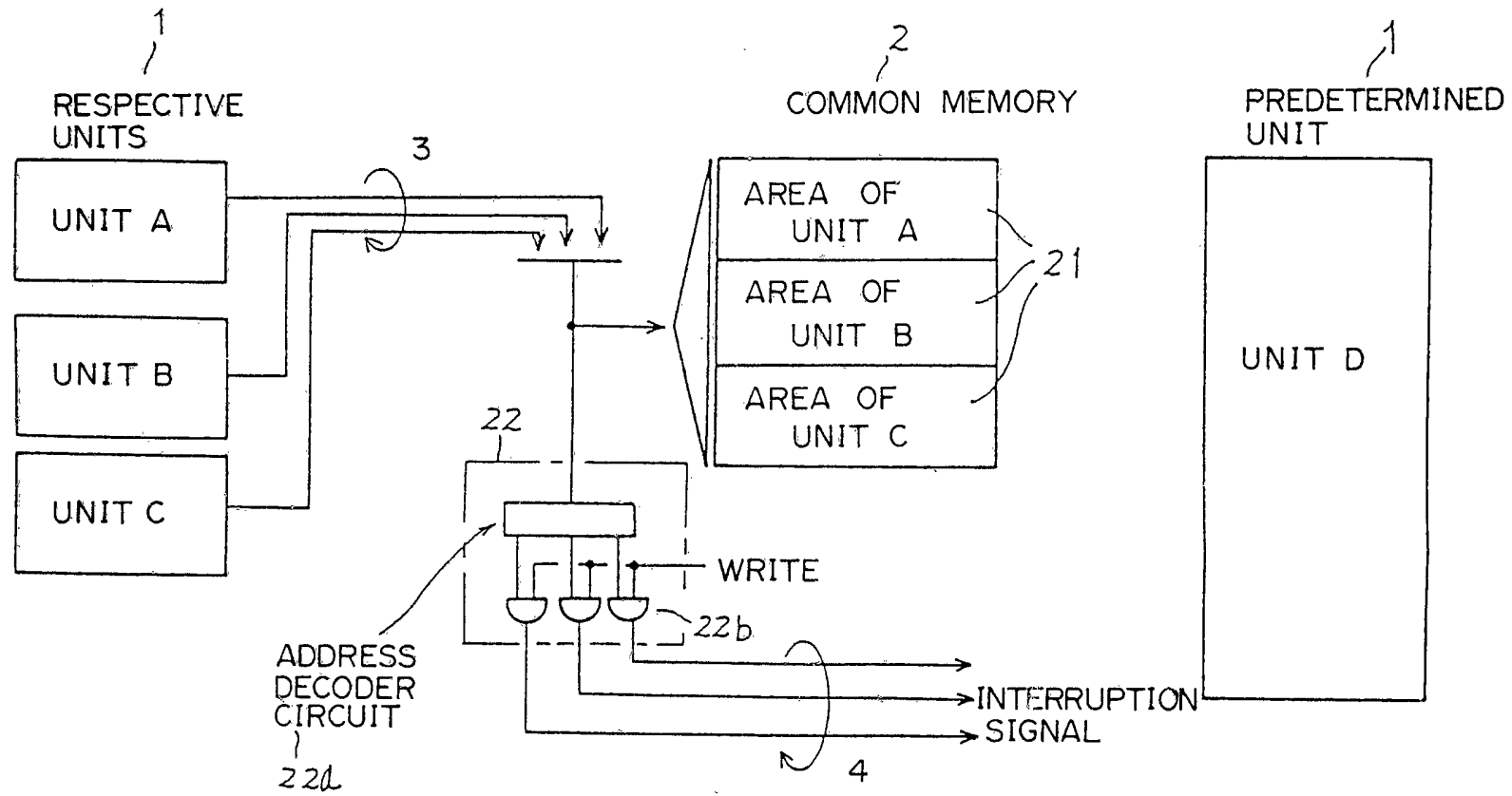


Fig. 3



44488/89

INTERRUPTION  
OF COMMON MEMORY

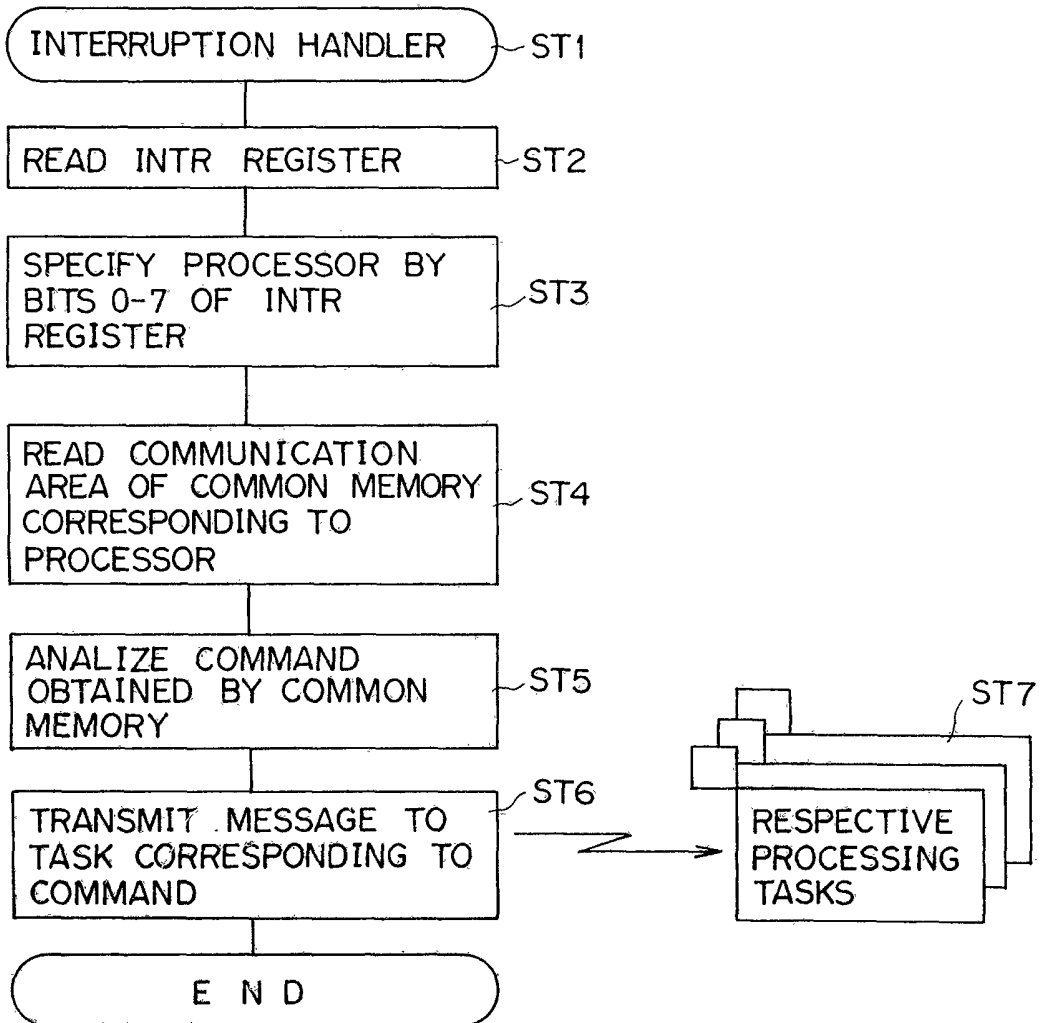


Fig. 5

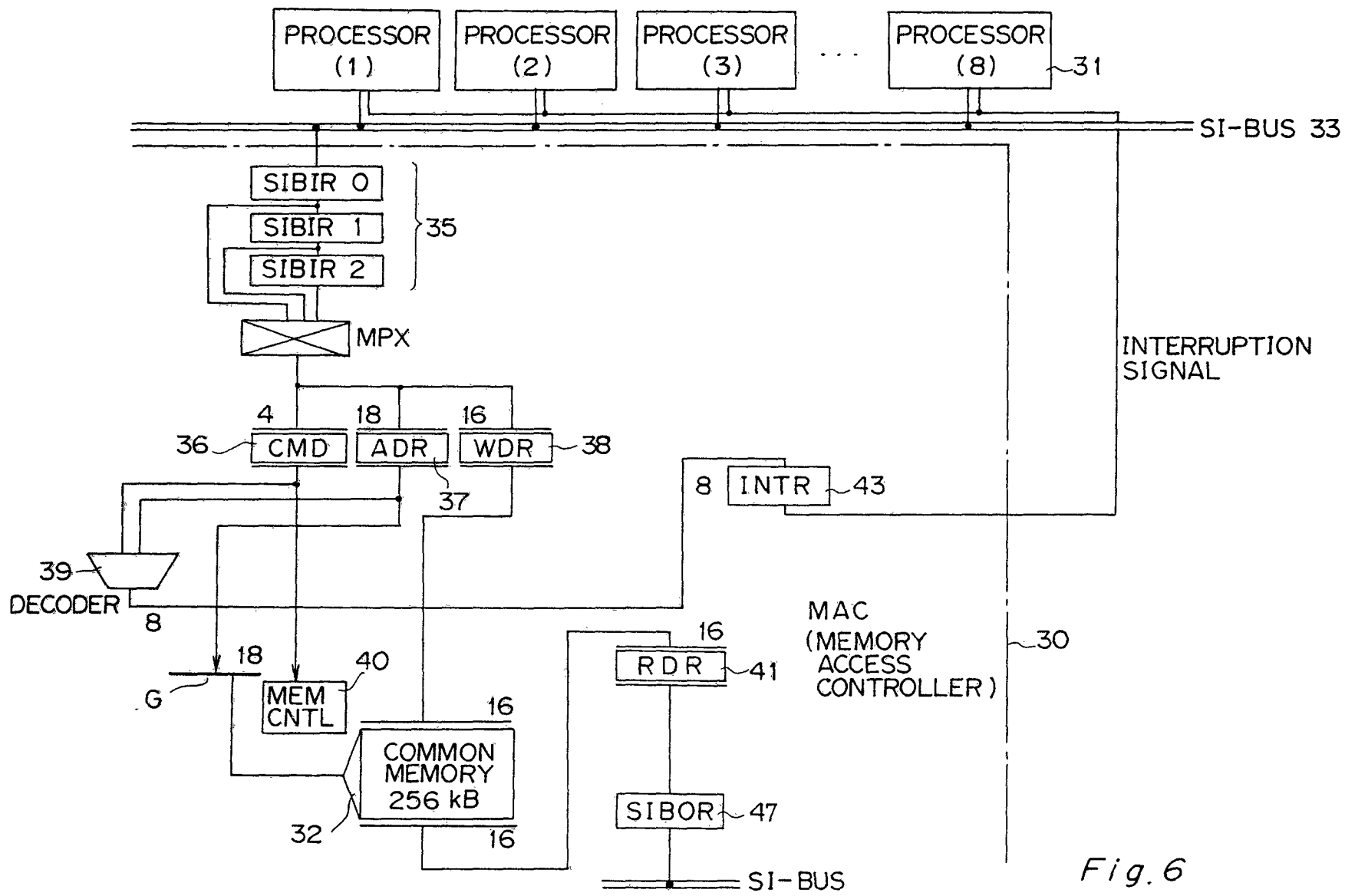


Fig. 6