US 20110049712A1

(19) **United States**

(12) **Patent Application Publication**

(10) **Pub. No.: US 2011/0049712 A1**

(43) **Pub. Date: Mar. 3, 2011**

Goida

(54) **WAFER LEVEL STACKED DIE PACKAGING**

(75) Inventor: **Thomas M. Goida**, Windham, NH (US)

(73) Assignee: **ANALOG DEVICES, INC.**, Norwood, MA (US)

(21) Appl. No.: **12/896,186**

(22) Filed: **Oct. 1, 2010**

Related U.S. Application Data

(62) Division of application No. 11/874,083, filed on Oct. 17, 2007, now Pat. No. 7,829,379.

Publication Classification

(51) **Int. Cl.**

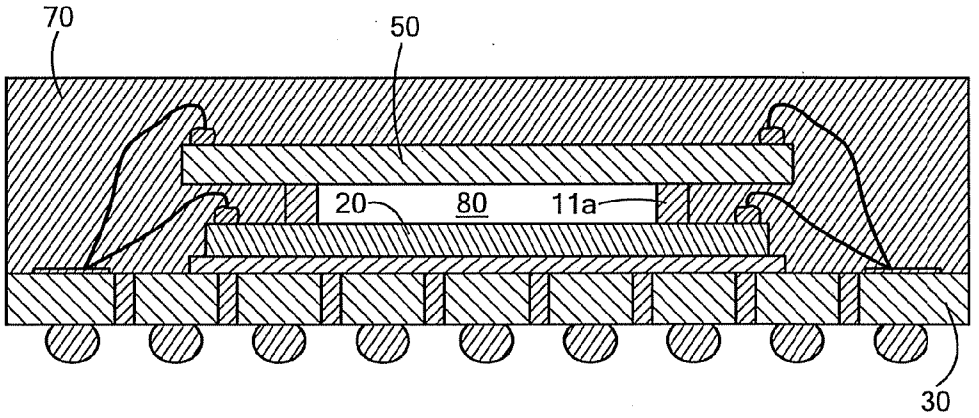
H01L 23/49 (2006.01)

H01L 23/498 (2006.01)

(52) **U.S. Cl.** **257/738**; 257/777; 257/E23.069

(57) **ABSTRACT**

A stacked die package in which an adhesive pad separates a bottom die from a top die. The pad may be in the form of a wall of adhesive about a central hollow area. The bottom die is attached to a base with a low temperature curing adhesive or a snap cure adhesive.



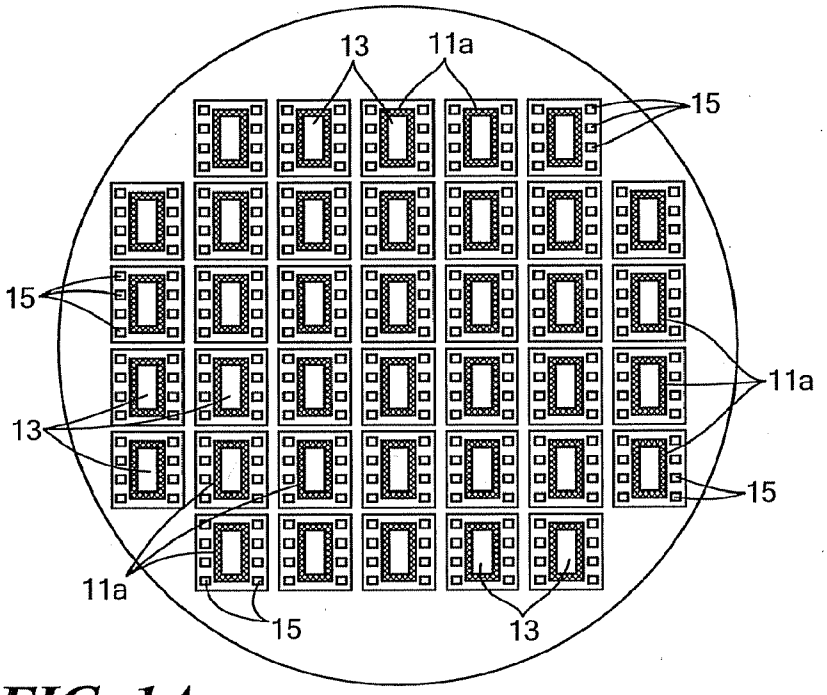


FIG. 1A

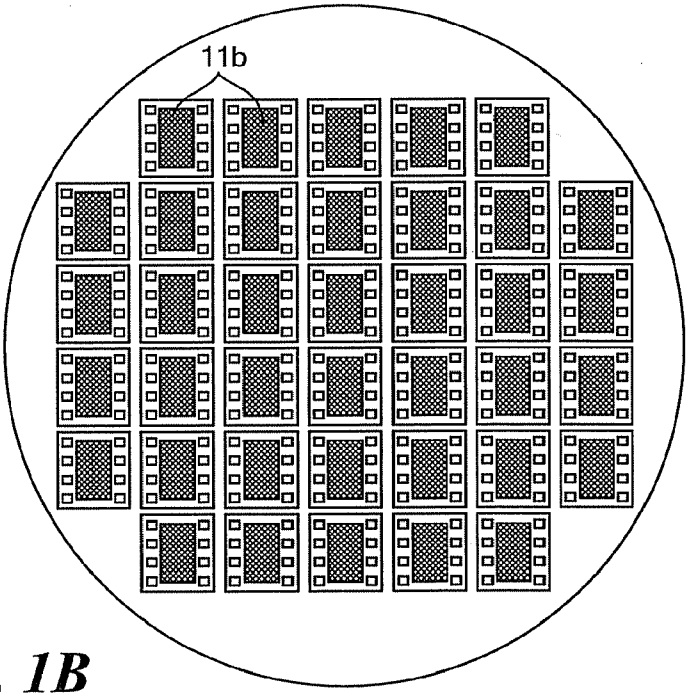


FIG. 1B

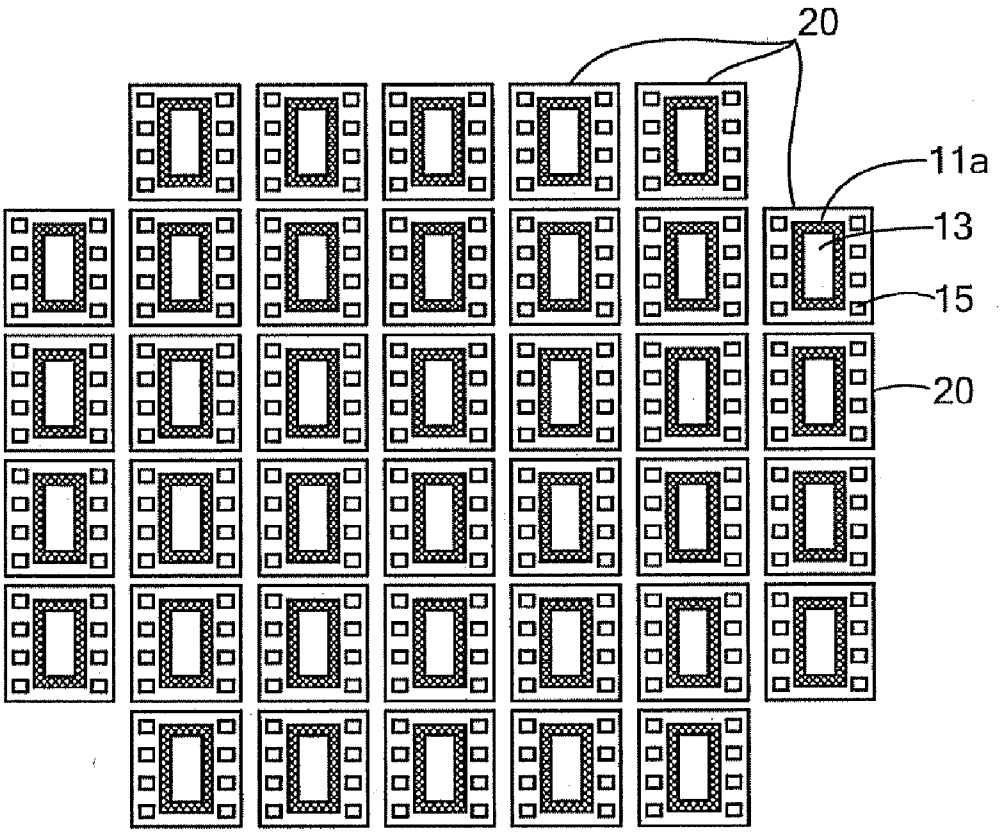


FIG. 2

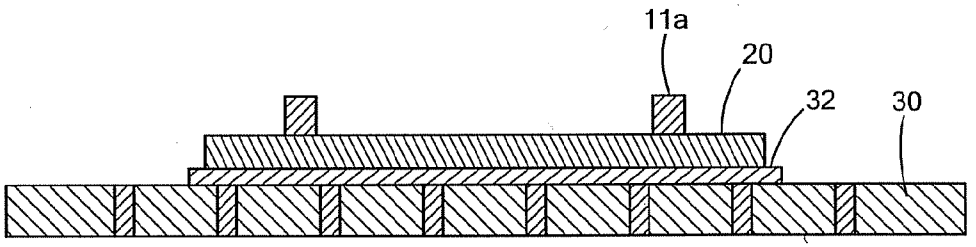


FIG. 3

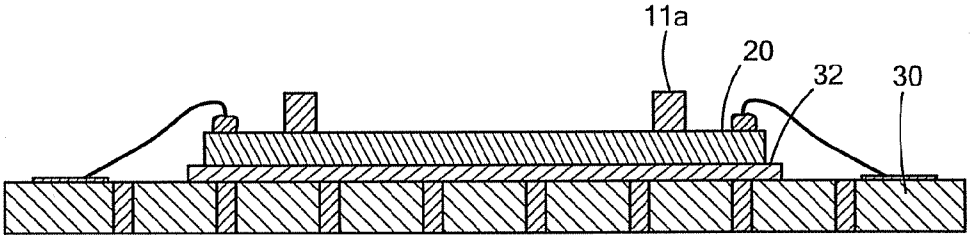


FIG. 4

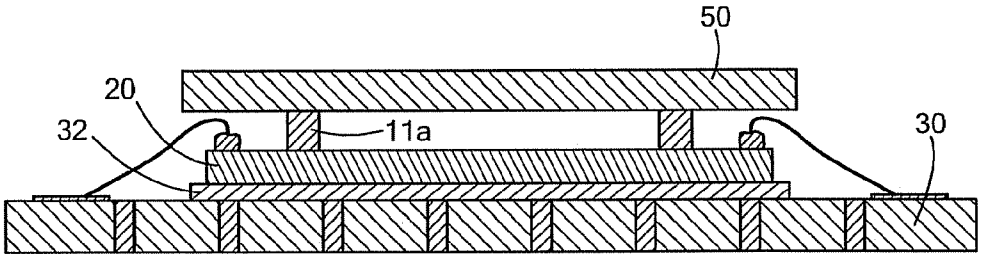


FIG. 5

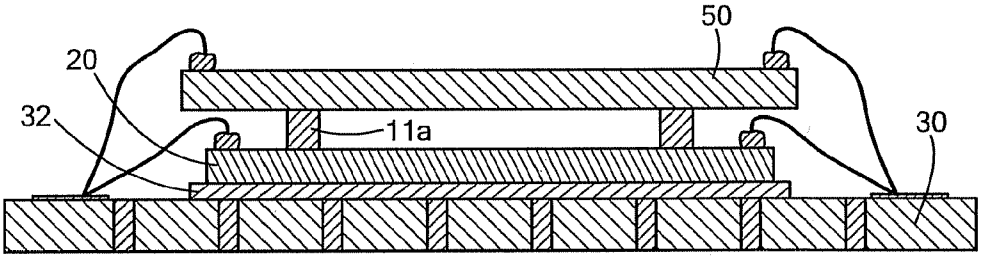


FIG. 6

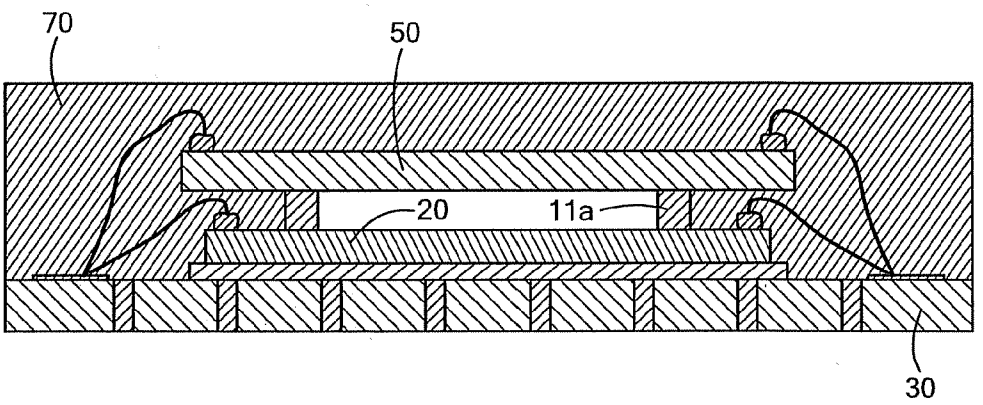


FIG. 7

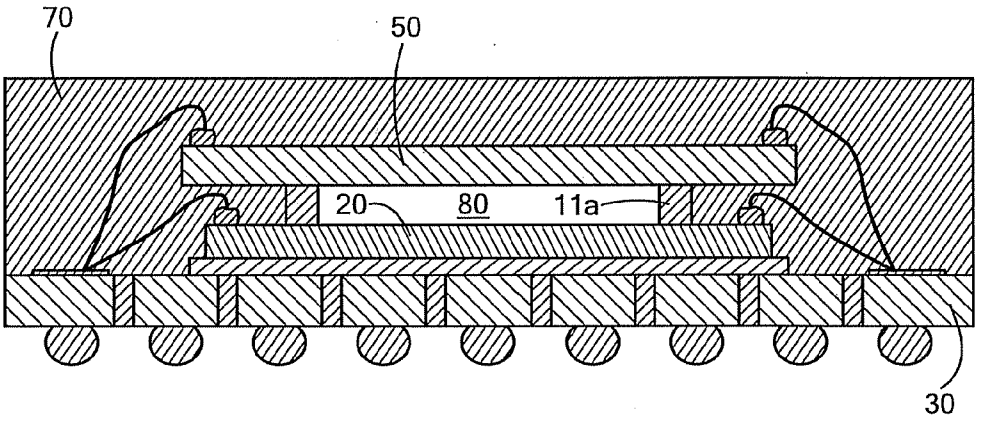


FIG. 8

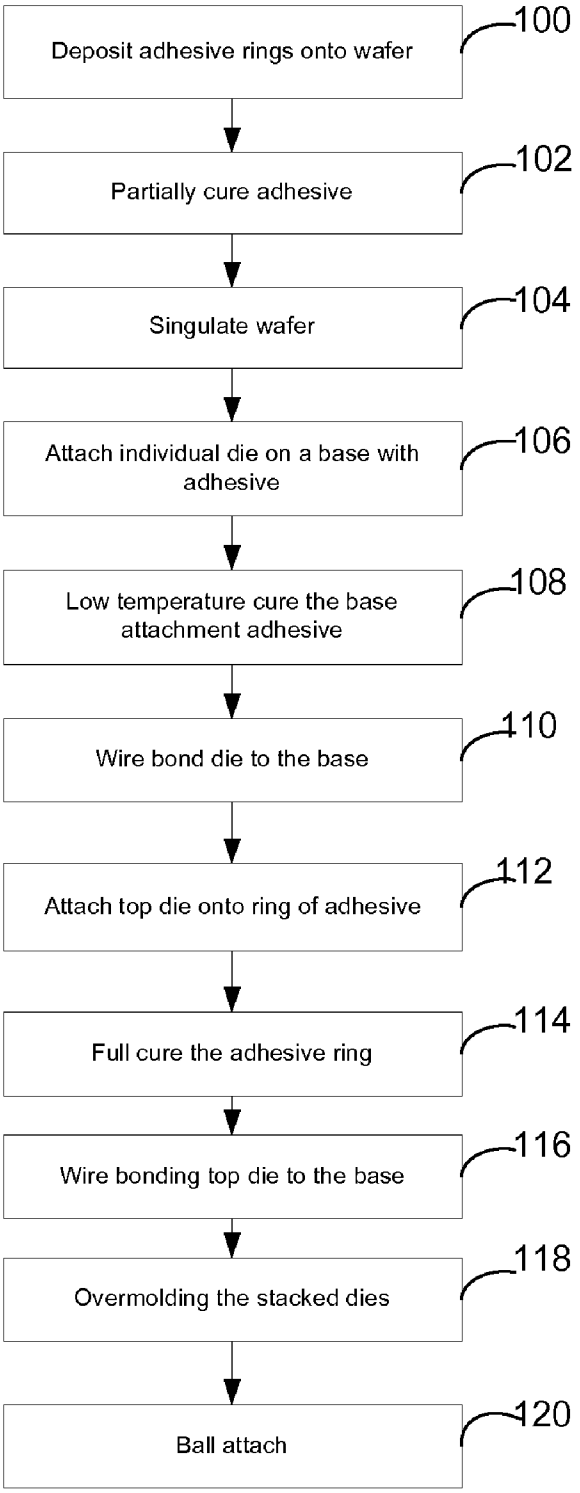

Deposit adhesive rings onto wafer
100
Partially cure adhesive
102
Singulate wafer
104
Attach individual die on a base with adhesive
106
Low temperature cure the base attachment adhesive
108
Wire bond die to the base
110
Attach top die onto ring of adhesive
112
Full cure the adhesive ring
114
Wire bonding top die to the base
116
Overmolding the stacked dies
118
Ball attach
120

FIG. 9

WAFER LEVEL STACKED DIE PACKAGING

[0001] The present application is a divisional application of U.S. patent application Ser. No. 11/874,083, filed Oct. 17, 2007, now issued as U.S. Pat. No. _____, the full disclosure of which is hereby incorporated by reference herein.

BACKGROUND OF THE INVENTION

[0002] The present invention relates to stacked microelectronic devices and methods of manufacturing the same.

[0003] Stacked die packaging typically comes in any of three forms: pyramid configuration, inverted pyramid configuration and same size die configuration. In a pyramid configuration the top die is smaller than the bottom die. The opposite is true in the inverted pyramid configuration. Alternatively, the dies can be the same size. In all stacked die configurations, an adhesive is typically applied to attach the top and bottom die together. In the case of the inverted pyramid with a larger die on top, the inclusion of a spacer is often required which introduces two separate and additional die attach steps in package assembly processes. Spacers are made from several different types of materials that include silicon and polymer based pre-defined tapes. Electrical connections are provided by bonding electrodes on the dies to wires for connection to the base.

SUMMARY OF THE INVENTION

[0004] In accordance with embodiments of the invention, a stacked die package includes at least two microelectronic semiconductor dies, one affixed on top of the other. An adhesive wall atop the bottom die outlines an air gap between a bottom and top die. In one embodiment, the adhesive wall is in the shape of a rectangle and forms a perimeter about a hollow area centrally disposed above the die. In other embodiments, the adhesive wall may be C-shaped, V-shaped, H-shaped or X-shaped to name a few configurations. The top die is affixed on the adhesive wall to create the stacked dies. In a specific embodiment, the adhesive wall provides a thickness between the dies in a ratio of at least 1:1 with the width of the wall. The stacked dies are mounted on a base. Wire bonds connect atop surface of each of the dies to the base. The stacked die package can be encased within a non-conductive material molded over the first and second semiconductor dies. The package may further include conductive balls attached to a bottom surface of the base for facilitating electrical connections.

[0005] In accordance with a method of manufacturing, a pattern of adhesive pads is deposited on the active surface of a semiconductor wafer. Among the possible adhesive patterns are an array of rings of adhesive or an array of geometrically shaped solid blocks of adhesive. The wafer is thereafter singulated to separate it into individual first semiconductor dies, each die having an adhesive pad thereon. A rear surface of each first semiconductor die can be attached to a base. Wire bonding may be performed between the first semiconductor die and its respective base. A second semiconductor die is attached atop the adhesive pad onto the first semiconductor die to form a stacked die package. Wire bonding may be further performed to electrically attach the second semiconductor die to the base. Overmolding the first and second semiconductor die stacks with non-conductive materials encases the individual packages. In a preferred embodiment, the wafer may be backgrinded before the deposit of a pattern of adhesive. The method may further include partially curing the adhesive before singulating the wafer.

[0006] Stress on the die surface of the underlying die typically imparted by the adhesive layer is reduced by using only an adhesive wall leaving an adhesive free air gap region. Application of the adhesive to the active surface of the semiconductor wafer provides for an efficient manufacturing process. Other objects and advantages of the invention will become apparent during the following description of the presently preferred embodiments of the invention taken in conjunction with the drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

[0007] The foregoing features of the invention will be more readily understood by reference to the following detailed description, taken with reference to the accompanying drawings, in which:

[0008] FIGS. **1**A and **1**B are plan views of an intermediate semiconductor product in accordance with embodiments of the invention.

[0009] FIG. **2** is a schematic plan view of the product of FIG. **1**A after singulation into individual dies.

[0010] FIG. **3** is a schematic side elevational view of a single die after attachment to a base.

[0011] FIG. **4** is a schematic side elevational view of the die of FIG. **3** after wire bonding.

[0012] FIG. **5** is a schematic side elevational view of the die of FIG. **4** after attachment of the top die.

[0013] FIG. **6** is a schematic elevational view of the stacked dies of FIG. **5** after wire bonding of the top die.

[0014] FIG. **7** is a schematic side elevational view of the stacked dies of FIG. **6** after overmolding.

[0015] FIG. **8** is a schematic side elevational view of the stacked dies of FIG. **7** after ball attachment.

[0016] FIG. **9** is a flowchart diagram of an embodiment of the invention of a method for making stacked dies.

DETAILED DESCRIPTION OF SPECIFIC EMBODIMENTS

[0017] In order to make a stacked die package in a mass production method, a starting material may be a semiconductor wafer as is well known in the art. The typical semiconductor wafer is made from silicon. An array of microelectronic circuits is formed on the semiconductor wafer. Typically, the array of circuits is formed in rows and columns of individual microelectronic circuits. The semiconductor wafer includes an active surface onto which wire connections can be made and a rear surface for mounting. When thickness is an issue, a backgrinding process may be performed on the wafer bearing the circuits to make it and, thus, the resulting dies thinner.

[0018] In accordance with an aspect of the present invention as seen in FIG. **9**, adhesive pads **11***a*, **11***b* are deposited **100** onto the active surface of the semiconductor wafer wherein each adhesive pad **11***a*, **11***b* is aligned with one of the individual microelectronic circuits. The adhesive pad **11***a*, **11***b* is an amount of adhesive having a thickness such that it will advantageously act as a spacer between a bottom die and top die of a package.

[0019] The adhesive pads may be applied to the wafer in any of a number of methods. Such methods include screen printing or photolithography. The adhesive material may be selected from any of a number of adhesives suitable for use in

making microelectronic components. Such adhesives may include, for example, polyimide or BCB (benzocyclobutene). The thickness of the adhesive to be used as a spacer depends upon the geometrical features of the silicon die for a given packaging application. For a stacked die in which the smaller die is placed on top, a smaller thickness spacer is acceptable, for example, in the range of 5 to 20 microns. In an embodiment in which a larger die is placed on top of the smaller die to form a stacked package the thickness of the adhesive may be, for example, between 50 and 75 microns. Such a thick adhesive pad may be more suitable for application through a screen printing method. The method and products of the present invention may be used with any thickness adhesive pad that can be used to produce a useable device.

[0020] In accordance with one embodiment as shown in FIG. **1**A, the adhesive pads **11***a*, are rings of adhesive. The adhesive forms a wall that leaves a hollow area **13** centrally disposed above each die as shown in FIG. **1**A. This hollowed out central portion **13** leaves an air gap that will thus not stress the bottom die in a manner normally associated with the adhesive. Spacers based on organic material can induce thermomechanical shear stress on the top side of the bottom silicon die in a stacked die package. The magnitude of this shear stress will depend on the material properties, geometry of the spacer and interface adhesion area. This shear stress has potential to cause delamination and/or cracking in die passivation and/or inner layer structures inside the silicon die. The adhesive rings reduce the adhesion area and are thus designed to reduce these shear stresses. The adhesive acts as a wall that forms the perimeter about the hollow central portion. In the embodiment of FIG. **1**A, the ring of adhesive is in the shape of a rectangle. It is contemplated that in specific embodiments, a minimal aspect ratio for thickness (height) of the wall to width of the wall should be 1 to 1. The actual aspect ratio of the adhesive wall will depend upon the geometrical features of the bottom die and type of application. Such walls may be used to create pads in shapes other than a ring that still create an air gap and derive similar advantages of reduced stress. Such shapes are innumerable including C-shaped, H-shaped, V shaped or X-shaped among others.

[0021] In accordance with an alternative embodiment such as that shown in FIG. **1**B, the adhesive pads **11***b* are geometrically shaped as solid blocks of adhesive. The shape shown in FIG. **1**B is that of a rectangular block of adhesive. Certainly, an oval or other shapes may be used as well.

[0022] In accordance with a preferred embodiment, each adhesive pad is oriented over a microelectronic circuit but within boundaries set by bond pads **15** for use along the periphery of a die. Thus, the bond pads **15** for the microelectronic circuit are exposed and accessible outside the periphery of the adhesive pad. Once the adhesive pads have been deposited, an intermediate semiconductor product has been completed for further use in the manufacturing of stacked die packaging.

[0023] The method of manufacture continues with the step of partially curing **102** the adhesive to bring it to its B-stage. B-stage is an intermediate stage in a thermosetting resin reaction in which the plastic remains in a soft state. The intermediate semiconductor product is then ready for singulation. The singulation process **104** typically involves sawing the wafer into individual dies **20** as shown in FIG. **2**. Each die **20** includes a microelectronic circuit and the adhesive pad **11***a*, **11***b* that had been deposited thereon.

[0024] The individual dies may then be picked and placed onto a base **30**. A suitable pickup nozzle is used to accommodate the circuit with adhesive pad thereon. A snap cure or low temperature curing adhesive **32** on the base **30** attaches **106** the bottom of the die **20** to the base. The base **30** may be a substrate or lead frame or other suitable base for supporting a stacked die package. The snap cure or low temperature curing adhesive **32** may then be cured without fully curing the adhesive pad **11***a*, **11***b* on the die **20**. The curing may take place at a lower temperature than will cure the adhesive pad or the curing can take place in a short time span such that the adhesive pad does not cure. Standard die attach materials, such as ABLESTIK 84-1, are cured at temperatures well below full cure for adhesives such as polyimide or BCB. For example, a die attach material might be cured at temperatures between 125° C. and 150° C. for approximately one hour. The BCB or polyimide used for the adhesive pad may, on the other hand, cure at over 300° C. for more than 30 minutes to an hour.

[0025] After attaching the bottom die to the base, the adhesive attaching the die to the base is cured without curing the adhesive pad **108**. Thus, the adhesive pad may remain in its B-stage during this low temperature or quick curing. At this point, wire bonding **110** can be performed to connect bond pads on the bottom die to the base, as shown in FIG. **4**.

[0026] A top die **50** is then ready for attachment **112** above the bottom die **20**. The top die **50** is placed on the adhesive pad **11***a*, **11***b* as shown in FIG. **5**. Full curing **114** of the B-stage adhesive pad is then performed to securely attach the bottom and top dies of the stacked die package. Wire bonding **116** may then be completed from the top die **50** to the base **30** as shown in FIG. **6**. Overmolding **118** encases the stacked die package in a nonconductive material as shown in FIG. **7**. Overmolding may be performed, for example, using a standard transfer molding process. Depending on the type of package and base that has been used, at this point ball attachment to the bottom of the base may be performed in order to provide conductive points for accessing the microelectronics as shown in FIG. **8**.

[0027] In accordance with embodiments of the invention, an air gap **80** remains disposed between the bottom die and the top die when a wall of adhesive was used to form the adhesive pad. In particular, when a ring of adhesive **11***a* is formed the air gap **80** is centrally disposed. This relieves that central area of stress associated with an adhesive connection.

[0028] Of course, it should be understood that various changes and modifications to the preferred embodiments described above will be apparent to those skilled in the art. For example, a stacked die package in accordance with the invention can be made with a smaller or larger top die with respect to the bottom die. Moreover, the base of the package may be a semiconductor substrate or a lead frame depending upon the desired package. Furthermore, additional layers of dies may be included so that multiple dies are stacked using the described methods. These and other changes can be made without departing from the spirit and scope of the invention and without diminishing its attendant advantages. It is therefore intended that such changes and modifications be covered by the following claims.

What is claimed is:

1. A stacked die package comprising:

a first microelectronic semiconductor die;

an adhesive pad atop the die;

a second microelectronic semiconductor die affixed atop the adhesive pad; and

a base on which the first microelectronic semiconductor die is attached by an adhesive that cures at a lower temperature than the adhesive in the adhesive pad.

2. The stacked die package of claim **1**, further comprising wire bonds connected between a top surface of the first microelectronic semiconductor die and the base.

3. The stacked die package of claim **2**, further comprising wire bonds connected between a top surface of the second microelectronic semiconductor die and the base.

4. The stacked die package of claim **3**, further comprising nonconductive material molded over the first and second semiconductor dies.

5. The stacked die package of claim **4**, further comprising conductive balls attached to a bottom surface of the base.

6. The stacked die package of claim **1**, wherein the adhesive pad forms a perimeter about a hollow area centrally disposed above the die.

7. The stacked die package of claim **6**, wherein the adhesive pad is in the shape of a rectangular wall.

8. The stacked die package of claim **6**, wherein the adhesive pad has a width on the die and a thickness from the die to a top of the pad, wherein a ratio of the thickness to the width is at least 1:1 and the second microelectronic semiconductor die is separated from the first microelectronic semiconductor die by the wall thickness.

9. The stacked die package of claim **1**, wherein the adhesive attaching the first microelectronic semiconductor die to the base comprises a low temperature curing adhesive, which cures at temperatures between 125° C. and 150° C.

10. A stacked die package comprising:

a first microelectronic semiconductor die;

an adhesive pad atop the die;

a second microelectronic semiconductor die affixed atop the adhesive pad; and

a base on which the first microelectronic semiconductor die is attached by a snap cure adhesive, which cures more quickly than the adhesive in the adhesive pad.

11. The stacked die package of claim **10**, further comprising wire bonds connected between a top surface of the first microelectronic semiconductor die and the base.

12. The stacked die package of claim **11**, further comprising wire bonds connected between a top surface of the second microelectronic semiconductor die and the base.

13. The stacked die package of claim **12**, further comprising nonconductive material molded over the first and second semiconductor dies.

14. The stacked die package of claim **13**, further comprising conductive balls attached to a bottom surface of the base.

15. The stacked die package of claim **10**, wherein the adhesive pad forms a perimeter about a hollow area centrally disposed above the die.

16. The stacked die package of claim **15**, wherein the adhesive pad is in the shape of a rectangular wall.

17. The stacked die package of claim **15**, wherein the adhesive pad has a width on the die and a thickness from the die to a top of the wall, wherein a ratio of the thickness to the width is at least 1:1 and the second microelectronic semiconductor die is separated from the first microelectronic semiconductor die by the wall thickness.

* * * * *