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USB TYPE-C SIGNAL INTERFACE CIRCUIT

RELATED APPLICATIONS

[0001] This application is an International Application of U.S. Patent Application Number 16/000,730, filed on June 5, 2018, which claims the benefit of priority to U.S. Provisional Application No. 62/656,274, filed on April 11, 2018, which are herein incorporated by reference in their entirety.

TECHNICAL FIELD

[0002] The disclosure relates to the field of electronic circuits, in particular to a USB type-C signal interface circuit.

BACKGROUND

[0003] Electronic circuits may include individual electronic components, such as resistors, transistors, capacitors, inductors, and diodes, among others, connected by conductive wires or traces through which electric current can flow. Electronic circuits may be constructed using discrete components, or more commonly integrated in an integrated circuit where the components and interconnections are formed on a common substrate, such as silicon.

BRIEF DESCRIPTION OF THE DRAWINGS

[0004] The disclosure is illustrated by way of example, and not of limitation, in the figures of the accompanying drawings.

[0005] **FIG. 1** is a block diagram of a USB type-C (USB-C) connector according an embodiment.

[0006] **FIG. 2** is a circuit diagram of a single port Thunderbolt® (TBT) notebook power source/sink circuit, according to an embodiment.

[0007] **FIG. 3** is a circuit diagram of sub-portions of a USB-C controller according to an embodiment.

[0008] **FIG. 4** is a circuit diagram illustrating a system having a USB-C controller according to another embodiment.

[0009] FIG. 5A is a circuit diagram of a system having a USB-C controller according to yet a further embodiment.

[0010] FIG. 5B is a circuit diagram of an IEC electrostatic discharge (ESD) protection circuit of the USB-C controller of FIG. 5A according an embodiment.

[0011] FIG. 5C and FIG. 5D are circuit diagrams of additional ESD protection circuitry on the system side of the USB-C controller of FIG. 5A according to an embodiment.

[0012] FIG. 6 is an eye diagram, verified on silicon, illustrating results from high-speed data multiplexing of the disclosed USB-C controllers according to an embodiment.

[0013] FIG. 7 is a circuit diagram illustrating a system having a USB-C controller according to an alternative according to an embodiment.

[0014] FIG. 8 is a flow chart for a method of designing a USB-C controller to form a high-speed, type-C interface circuit according to one embodiment.

DETAILED DESCRIPTION

[0015] A USB type-C receptacle, with capabilities of up-side down connection and accessible to external physical connectors, may access interface circuitry for reverse detection, multiplexers for flip correction, and IEC electrostatic discharge (ESD) protection. The data lines (DP/DM, also denoted as D+/D-) may employ additional sensing for battery charging and USB2.0 high-speed signaling. There is presently no one-die solution (e.g., a single integrated circuit chip) for these capabilities. Accordingly, a hardware manufacture that incorporates USB technology may need to use external components for one or another capability, which may degrade the high-speed signaling and increase costs, for example.

[0016] In various embodiments, a device may include a USB-C controller instantiated as a first integrated circuit (e.g., implemented as an instance on a single integrated circuit) that includes a first set of terminals to be coupled to host controllers and a second set of terminals to be coupled to sets of D+/D- terminals of a type-C receptacle. A D+/D- multiplexer may selectively couple the first set of terminals to the second set of terminals. An electrostatic discharge (ESD)

protection circuit may be coupled between the D+/D- multiplexer and the second set of terminals. A charger detector circuit may be coupled between a positive data system terminal and a negative data system terminal of the first set of terminals, the charger detector circuit to detect whether the second set of terminals is coupled to a USB charger through the type-C receptacle. When terminals are referred to herein, reference is understood to be made to integrated circuit terminals, metal lines, pins, and other input/output connectors, depending on implementation.

[0017] FIG. 1 is a block diagram of a USB type-C (USB-C) connector 100 according an embodiment. Many of the terminals on the USB-C connector 100 are replicated on the top and on the bottom so that the USB-C connector may fit into a USB-C receptacle right side up or up-side down and still function. Those familiar with the USB-C standard will recognize these terminals, and with particular reference to the present disclosure, the positive data terminals (D+) and the negative data terminals (D-), highlighted with a box 101, which may be coupled to a USB 2.0 data bus. Additional terminals include ground terminals (GND), VBUS terminals, sideband use terminals (SBU1, SBU2), channel configuration terminals (CC1, CC2), and USB 3.1 transceiver/receiver terminals (TX/RX). The CC terminals may enable cable attach detection, cable orientation detection, role detection, and current-mode detection, e.g., standard mode or alternate mode.

[0018] The unused CC terminal may become the VCONN terminal, which may supply power to USB-C controller chips in active cables or adaptors. The VBUS terminal may be used for the cable bus power and GND terminal for the cable ground. The SBU terminals may be for communicating with other-than-USB protocols in alternate mode, such as with the DisplayPort (DP) protocol, high-definition multimedia interface (HDMI) protocol, the Thunderbolt® (TBT) protocol, the mobile high-definition link (MHL) protocol, and the Peripheral Component Interconnect Express (PCIe) protocol, and the like.

[0019] With additional reference to FIG. 1, the position of each D+ terminal and each D- terminal may be flipped between the top and the bottom of the USB-C receptacle. This is due to the USB Type-C specification definition a Type-C port, which may be associated with a Type-C plug or a Type-C receptacle. For ease of

use, the Type-C plug and the Type-C receptacle are designed as a reversible pair that operates regardless of the plug-to-receptacle orientation. Accordingly, a USB-C controller may include multiplexing between top and bottom duplicate terminals depending on the orientation of the USB-C connector placed therein. Further, a configuration channel (CC) signal may be transmitted through either of the CC1 or the CC2 terminals, which may follow CC protocol for flip correction, so as to signal the multiplexers which set of terminals to select as will be discussed in detail.

[0020] **FIG. 2** is a circuit diagram of a single port Thunderbolt® (TBT) notebook power source/sink circuit 200, according to an embodiment, for system context of where the disclosed type-C signal interface circuit may be employed. The type-C signal interface circuit may also be employed in other USB type-C devices and systems. In embodiments, the circuit 200 may include a type-C receptacle 201, a USB-C controller 202, a power subsystem 212, a TBT controller 222, an embedded controller 232, a USB host controller 242, and a proprietary host controller 252. In embodiments, the disclosed type-C signal interface circuit may be employed as a part of or integrated within the USB-C controller 202. The power subsystem 212 may provide a five volt (5V) provider path 213, to generate VBUS_OUT for use by other USB-C circuitry, and a power consumer path 214 to power the power subsystem 212.

[0021] In various embodiments, the type-C receptacle 100 may contain terminals that correspond to the terminals of the type-C connector 100 of **FIG. 1**, e.g., VBUS, SBU1, SBU2, D+/D- (top), D+/D- (bottom), CC2, CC1, and GND. These terminals may be coupled to corresponding terminals on the USB-C controller 202, respectively, the VBUS_C_CTRL, SBU2, SBU1, DPLUS_TOP, DMINUS_TOP, DPLUS_BOT, DMINUS_BOT, CC2, and CC1 terminals. The USB-C controller 202 may be configured for alternate mode operation, which enables other communication protocols, which was just discussed.

[0022] As illustrated, the USB-C controller 202 may include a number of additional connections and circuitry, not all that are relevant here, and may be manufactured as a single integrated circuit. Note the additional negative auxiliary

terminal (AUX_N), positive auxiliary terminal (AUX_P), TBT transmit control signal terminal (LSTX), and TBT receive control signal terminal (LSRX) on the USB-C controller 202 may be coupled to corresponding terminals on the TBT controller 222. The AUX_N, AUX_P terminals may provide auxiliary signals for DisplayPort signaling and the LSTX, LSRX terminals may provide TBT link management using Universal Asynchronous Receiver-Transmitter (UART)-based technology, for example. Furthermore, a positive data system terminal (e.g., DPLUS_SYS) and a negative data system terminal (e.g., DMINUS_SYS) of the USB-C controller 202 may be coupled to system data lines that are routed to the USB host controller 242. A data transmitter terminal (e.g., UART_TX) and a data receiver terminal (e.g., UART_RX) may be coupled to the proprietary host controller 252. The proprietary host controller 252 may be a proprietary controller such as a test and debug controller of a host computing system in which the circuit 200 is located, e.g., the notebook or other computing system that hosts the USB-C controller 202.

[0023] In various embodiments, the embedded controller 232 may be coupled to the USB-C controller 202 through, for example, an inter-integrated circuit connection (I2C), e.g., a synchronous, multi-master, multi-slave, packet switched, single-ended, or a serial computer bus. The USB-C controller 202 may include an I2C address that is determined by the SWD_CLK terminal.

[0024] The USB-C controller 202 may communicate with the power subsystem 212 over I2C, which manages the power provided to the upstream type-C ports. The USB-C controller 202 may also update the TBT controller 222 over I2C based on the alternate mode negotiation to sink Thunderbolt® or USB or DisplayPort protocol data. The USB-C controller 202 may control the transfer of USB 2.0 D+/D- lines from the top and bottom of the type-C receptacle 201 to the D+/D- lines of the TBT controller 222. The USB-C controller 202 may also handle the routing of SBU1 and SBU2 lines from the type-C receptacle 201 to the TBT controller 222 for the link management. In embodiments, the USB-C controller 202 may offer on-chip ESD protection on D+/D- and SBU lines as well as on-chip

VBUS Short protection on SBU and CC lines. Some of these capabilities will be discussed in more detail below.

[0025] FIG. 3 is a circuit diagram of sub-portions of a USB-C controller 302, associated with a single port, according to an embodiment. In one embodiment, the USB-C controller 302 is the USB-C controller 202 of Figure 2. The USB-C controller 302 may include a configuration channel (CC) interface circuit 310, a USB-C sideband signal interface circuit 330, and a USB-C D+/D- interface circuit 360.

[0026] In various embodiments, the CC interface circuit 310 may include a gate drive and 10V charge pump 311 and a pair of transistor switches 312 to enable VCONN functionality on CC1/CC2 depending on the connector direction. Either of CC1 or CC2 may be used for CC protocol and the other one may be connected to V5V using 312 switches to give power to the cable. The CC interface circuit 310 may further include reference circuitry 314 to compare and detect certain types of signals received through the CC1 and CC2 terminals, and to generate outgoing control signals over the CC1 and CC2 terminals.

[0027] In some embodiments, the USB-C sideband signal interface circuit 330 may include a four-by-two multiplexer 332 with resistance isolation on the inputs and having switches driven using a 5V charge pump 328. The four-by-two multiplexer 332 may selectively couple a first pair of terminals (e.g., AUX1, AUX2 terminals) to a pair of SBU terminals (e.g., SBU1, SBU2), and selectively couple a second pair of terminals (e.g., LSTX, LSRX terminals) to the pair of SBU terminals (e.g., SBU1, SBU2). The general purpose input/output (GPIO) boxes may be adapted to receive communication links of protocols other than USB. In one embodiment, the switches of the four-by-two multiplexer 332 are metal-oxide-semiconductor field-effect transistors (MOSFETs), e.g., specifically low-voltage n-type field effect transistors (LVNFETs). In one embodiment, the charge pump 328 may drive the gates of the LVNFETs such that the LVNFETs each operate in a linear region and exhibit less than a seven-ohm resistance.

[0028] In some embodiments, a USB-C D+/D- interface circuit 360 may include a four-by-four multiplexer 362 that includes switches that are also driven by a 5V

charge pump 358. The four-by-four multiplexer 362 may selectively couple the positive data system terminal (DP_SYS) to one of the first and second positive data terminals (DP_TOP, DP_BOT), the data transmitter terminal (UART_Tx) to one of the first and second positive data terminals (DP_TOP, DP_BOT), the negative data system terminal (DM_SYS) to one of the first and second negative data terminals (DM_TOP, DM_BOT), and the data receiver terminal (UART_Rx) to one of the first and second negative data terminals (DM_TOP, DM_BOT).

[0029] In one embodiment, the switches of the four-by-four multiplexer 362 are MOSFETs, e.g., specifically n-type field effect transistors (NFETs). The 5V pump 528 may be a low-ripple charge pump (e.g., low-ripple 5V charge pump) coupled to gates of the MOSFETs of the four-by-four multiplexer 362. The low-ripple charge pump may drive the MOSFETs to operate in a linear region and such that each MOSFET exhibits less than seven-ohm resistance.

[0030] In embodiments, the high-speed operation of the disclosed USB-C controllers may meet USB2.0 high-speed data rates with signaling rates of 480 Mbps, USB2.0 full-speed data rates with signaling rates of 12 Mbps, may provide UART signaling, and provide access to a battery charger for USB devices.

[0031] **FIG. 4** is a circuit diagram illustrating a system 400 having a USB-C controller 402 according to another embodiment. In one embodiment, the USB-C controller 402 is the USB-C controller 202 of **FIG. 2** or the USB-C controller 302 of **FIG. 3**. The system 400 may further include a host microcontroller unit (MCU) 403 and the type-C receptacle 201 (**FIG. 2**). The type-C receptacle 201 may include sets of D+/D- terminals, e.g., D+_UP and D+_DOWN (the top and bottom positive signal terminals) and D-_UP and D-_DOWN (the top and bottom negative signal terminals). The host MCU 403 may include a pair of host controllers, such as the USB host controller 242 and the proprietary host controller 252, with corresponding controller terminals. The USB host controller 242 may include a positive controller terminal (DP_USB) and a negative controller terminal (DM_USB). The proprietary host controller 252 may include a transmission controller terminal (UART_TX) and a reception controller terminal (UART_RX).

[0032] In various embodiments, the USB-C controller 402 includes a first set of terminals coupled to the sets of host controller terminals of the host MCU 403 and a second set of terminals coupled to sets of D+/D- terminals of the type-C receptacle 201. For example, the first set of terminals may include positive data system terminal (DP_SYS) and a negative system terminal (DM_SYS) coupled to the DP_USB and DM_USB terminals, respectively, of the host MCU 403. Furthermore, the first set of terminals may include a data transmitter terminal (UART_TX) and a data receiver terminal (UART_RX) coupled to the corresponding UART_TX and UART_RX terminals of the host MCU 403. In embodiments, the second set of terminals includes a first positive data terminal (DP_TOP) coupled to the D+_UP terminal, a second positive data terminal (DP_BOT) coupled to the D+_DOWN terminal, a first negative data terminal (DM_TOP) coupled to the D-_UP terminal, and a second negative data terminal (DM_BOT) coupled to the D-_DOWN terminal of the type-C receptacle 201.

[0033] In the various embodiments, the USB-C controller 402 includes a D+/D- multiplexer 406, which may be made up of a first set of four n-type field effect transistors (NFETs) 406A and a second set of four NFETs 406B. The D+/D- multiplexer 406 may selectively couple the first set of terminals to the second set of terminals in a way that enables flip correction between top and bottom terminals of the USB-C connector 100. The NFETs of the D+/D- multiplexer 406 may be controlled through the CC signal using CC protocol.

[0034] More specifically, the multiplexer 406 may selectively couple the positive data system terminal (DP_SYS) to one of the first and second positive data terminals, the data transmitter terminal (UART_TX) to one of the first and second positive data terminals, the negative data system terminal (DM_SYS) to one of the first and second negative data terminals, and selectively couple the data receiver terminal (UART_RX) to one of the first and second negative data terminals.

[0035] In one embodiment, the positive data system terminal (DP_SYS) and the negative data system terminal (DM_SYS) are associated with a first USB host port connection of a single USB port. In this embodiment, the data transmitter terminal (UART_TX) is a second positive data system terminal and the data receiver

terminal (UART_RX) is a second negative data system terminal. These second positive and negative data system terminals may be associated with a second USB host port connection of the single USB port.

[0036] In this way, the D+/D- multiplexer 406 may enable the use of both top and bottom D+/D- terminals of the USB connector together at the same time. For example, the multiplexing may provide the ability for a small USB-C host device, which has sufficient room for only one (or perhaps two) USB-C ports, to connect two different USB devices to the USB-C host devices via a single USB port. In one embodiment, a special split USB cable may be employed that connects into the single USB port of the USB-C host device and into USB ports of the two different USB devices.

[0037] Furthermore, the use of both the top and bottom D+/D- terminals of the USB connector may facilitate the enhancement of the quality of the high-speed data signal through the USB-C controllers and the connectors. This may be performed through sending a diagnostics signal through the unused D+/D- terminals, e.g., a command from a USB device to boost the USB signal for better detection of the USB device. Other diagnostic signals may also be sent. The advantage of sending a diagnostic signal in this way may be that the diagnostic signal need not be sent through the entire USB-C controller (and its other signaling circuitry) to assert an action or improve detection or performance. Protocols that may operate over the unused D+/D- terminals include RS232 as well as other interconnect protocols. Furthermore, the availability of both the top and bottom D+/D- terminals of the USB connector for data transmission may be applied to double the data rate of any existing protocol. Since the D+/D- multiplexer may have four lane outputs possible at any time, the output rate may be doubled by sending the high-speed data across both the top and bottom data lines for the same communication link.

[0038] The USB-C controller 402 may further include a charger detector circuit 410 selectively coupled between a positive data system terminal and a negative data system terminal of the first set of terminals. The charger detector circuit 410 may detect whether a device coupled to the second set of terminals, through the type-C receptacle 201, includes a USB charger and thus contains a battery to be

charged rather than connected for high-speed data transfer. The charger detector circuit 410 may include a first switch 412 coupled to the positive data system terminal (DP_SYS) and a second switch 414 coupled to the negative data system terminal (DM_SYS) to facilitate the selective coupling just referenced. In one embodiment, the first switch 412 and the second switch 414 are controllable by first logic (e.g., firmware, state machine, or other logic) to disconnect the charger detector circuit 410 during high-speed data transfer of the USB-C controller, which reduces the battery charging capacitive load on the D+/D- lines and maintains better signal integrity.

[0039] In various embodiments, after connection by the USB device and the charger detector circuit 410 detects whether to perform charging or high-speed data transfer, the charger detector circuit 410 may open the first and second switches 412, 414 to disconnect the charger detector circuit 410. Alternatively, the charger detector circuit 410 may be disconnected after a set time window or upon a predetermined signal from the first logic.

[0040] The USB-C controller 402 may further include an IEC electrostatic discharge (ESD) protection circuit 420 coupled between the D+/D- multiplexer 406 and the second set of terminals, e.g., the DP_TOP, DP_BOT, DM_TOP, and DM_BOT terminals. The IEC ESD protection circuit 420 may provide ± 8 KV of contact discharge protection and ± 15 KV of air gap discharge protection based on IEC61000-4-2 level 4C protection. The IEC ESD protection circuit 420 may be separated into a first IEC ESD protection circuit 420A coupled to the first set of four NFETs 406A and a second IEC ESD protection circuit 420B coupled to the second set of four NFETs 406B. The IEC ESC protection circuit 420 may protect against electrostatic discharge and provide better signal integrity for high-speed signals, and avoid extra routing at board level, which would otherwise be required if located on a second integrated circuit chip from the chip on which the multiplexer is disposed.

[0041] The present design of the disclosed USB-C controllers may have added challenges due to the added circuitry. For example, high-speed switches (the NFETs) of the D+/D- multiplexers should be of low resistance to meet the high-

speed eye diagram. The resistance may be minimized by increasing the switch size, but with increased switch size may also result in increased switch capacitance on high-speed data lines. Increased capacitances may cause the high-speed eye diagram to fail. Accordingly, a balance in the switch size is sought to reduce DP/DM self-capacitances and mutual-capacitances. Reducing switch size may help meet the high-speed eye diagram and cross-talk performances and by reducing the capacitance created by sources and drains of the NFETs.

[0042] Further, to reduce resistance and capacitance simultaneously, the MOSFET's (NFETs) of the switches of the D+/D- multiplexers may be operated in a linear region by using the 5V charge pump to meet less than seven ohm resistance of each NFET. Using the charge pump for high-speed transmission may cause a high swing at the charge pump output and thus corrupt the high-speed data. High swing at the charge pump may be resolved by using a low-ripple charge pump.

[0043] In embodiments, a high-speed data line is to have as minimum loading as possible for purposes of speed. Integrating a USB high-speed data line with additional circuitry may include risks as the USB high-speed data line may already be loaded with the high-speed driver load and a battery charger load. Any increase in the loading may impact the performance of the high-speed eye diagram.

[0044] Furthermore, adding IEC ESD clamps to the high-speed data lines may present a large capacitance on the data lines that may further affect the high-speed eye diagram performance. As illustrated in **FIG. 4**, each data lane may be connected to an on switch and an off switch while in operation. The first and second switches 412, 414 may add the load of two off switches to an already loaded line. Additionally, the signaling range of a high-speed signal is about plus or minus 400mV. A UART is a single-ended mode of signaling with a swing of 3.3V. Any coupling from one end of the off switch to the other may corrupt the high-speed data.

[0045] To reduce the ESD clamp loading, series diodes (discussed with reference to **FIG. 5B**) may be employed to isolate the clamp in normal operating conditions and reduce the capacitance without impacting the ESD performance. The loading of the charger detector circuit 410 may be minimized by using

firmware-controlled switches (for the first switch 412 and the second switch 414) for the path between high-speed data lines and the battery charger on a USB device or adaptor. These logic-controlled switches may be kept off during high-speed data traffic. To improve signal integrity from the coupling due to power supplies and off switches, decoupling of sources and drains of NFET switches may be achieved using maximum metal spacing (e.g., two times the metal spacing) and grounded metal shields between the sources and drains of the NFET switches. Further, source/drain coupling to gate may be reduced by isolating gates using resistances. To do so, an inverter may be used to drive each NFET, and a resistance (such as a 2K-ohm resistance) may be added to the inverter's pull-up path, e.g., between the drain and output going to the NFET's gate. No resistance may be added to the inverter's pull-down path to ensure that the NFET switches, when disabled, are pulled down strongly. The resistance added to the pull-up path is to avoid coupling of one gate to another gate.

[0046] **FIG. 5A** is a circuit diagram of a system 500 having a USB-C controller 502 according to yet a further embodiment. The system 500 is similar to the system 400 of **FIG. 4**, as indicated by the same or similar circuit elements. The USB-C controller 502 may also be similar to the USB-C controller 402 of **FIG. 4**. In one embodiment, the USB-C controller 502 includes the D+/D- multiplexer 406, an IEC ESD protection circuit 520 coupled to the connector side of the D+/D- multiplexer 406, and additional ESD protection circuitry 526 coupled to the system side of the D+/D- multiplexer 406. The additional ESD protection circuitry 526 may include first, second, third, and fourth system ESD protection circuitry 526A, 526B, 526C, and 526D, respectively. The IEC ESD protection circuit 520 may provide 8 KV of protection and be separated into a first IEC ESD protection circuit 520A coupled to the first set of four NFETs 406A and a second IEC ESD protection circuit 520B coupled to the second set of four NFETs 406B, for example. The IEC ESD protection circuit 520 and the additional ESD protection circuitry 526 may provide ESD clamp isolation using the illustrated diodes (**FIGS. 5B, 5C, and 5D**) to reduce capacitances.

[0047] **FIG. 5B** is a circuit diagram of the ESD protection circuit 520 of the USB-C controller 502 of **FIG. 5A** according an embodiment. In this embodiment, the ESD protection circuit 520 includes a five volt, IEC ESD RC snapback clamp 534 coupled between a local power supply and ground. The ESD protection circuit 520 may further include at least one Human Body (HBM) diode coupled between the local power supply and each of the first positive data terminal (DM_TOP), the first negative data terminal (DM_TOP), the second positive data terminal (DP_DOWN), and the second negative data terminal (DM_DOWN). The ESD protection circuit 520 may further include at least one HBM diode coupled between the ground and each of the first positive data terminal, the first negative data terminal, the second positive data terminal, and the second negative data terminal.

[0048] In a related embodiment, the ESD protection circuit 520 may further include a first set, a second set, a third set, and a fourth set of HBM diodes coupled between the local power supply and the first positive data terminal, the first negative data terminal, the second positive data terminal, and the second negative data terminal, respectively. In one example, each set of diodes is a set of three diodes although another number of diodes is envisioned. The ESD protection circuit 520 may further include a fifth set, a sixth set, a seventh set, and an eighth set of HBM diodes coupled between the ground and the first positive data terminal (DP_TOP), the first negative data terminal (DM_TOP), the second positive data terminal (DP_DOWN), and the second negative data terminal (DM_DOWN), respectively. In one example, each set of diodes is a set of three diodes. The ESD protection circuit 520 may further include a resistor 536 and a supply diode 538 between the IEC ESD RC snapback clamp 534 and VDD, to bias VDD_R local supply to a known voltage of VDD minus diode drop.

[0049] **FIG. 5C** and **FIG. 5D** are circuit diagrams of additional ESD protection circuitry on the system side of the USB-C controller of **FIG. 5A** according to an embodiment. In various embodiments, the additional ESD protection circuitry includes additional system ESD protection circuitry for each of the first set of terminals coupled to the host controllers, e.g., for each of the positive data system

terminal (DP_SYS), the negative data system terminal (DM_SYS), the data transmitter terminal (UART_TX), and the data receiver terminal (UART_RX).

[0050] More specifically, with reference to **FIG. 5C**, first system ESD protection circuitry 526A may include a first human body model (HBM) snapback clamp 534A coupled to a ground and a first pair of diodes 542A connected in series and coupled between the first HBM snapback clamp 534A and the positive data system terminal (DP_SYS). Further, second system ESD protection circuitry 526C may include a second HBM snapback clamp 534C coupled to the ground and a second pair of diodes 542C connected in series and coupled between the second HBM snapback clamp 534C and the negative data system terminal (DM_SYS).

[0051] With additional reference to **FIG. 5D**, third system ESD protection circuitry 526B may include a third HBM snapback clamp 534B coupled to the ground and a first pair of diodes 542B connected in series and coupled between the third HBM snapback clamp 534B and the data transmitter terminal (UART_TX). Further, fourth system ESD protection circuitry 526D may include a fourth HBM snapback clamp 534D coupled to the ground and a second pair of diodes 542D connected in series and coupled between the fourth HBM snapback clamp 534D and the data receiver terminal (UART_RX). In embodiments, the pairs of diodes employed in the system ESD protection circuitry may be standard diodes or HBM diodes depending on level of ESD protection desired. These additional pairs of diodes 542A, 542B, 542C, and 542D may reduce capacitive load of the HBM snapback clamps 534A, 534B, 534C, and 534D, respectively.

[0052] **FIG. 6** is an eye diagram, verified on silicon, illustrating results from high-speed data multiplexing of the disclosed USB-C controllers according to an embodiment. Note the large eye opening in the eye diagram is indicative of good high-speed performance of the multiplexing that includes the IEC ESD protection circuitry.

[0053] **FIG. 7** is a circuit diagram illustrating a system 700 having a USB-C controller 702 according to an alternative according to an embodiment. The USB-C controller 702 may be similar to the USB-C controllers 402 and 502, but contain a D+/D- multiplexer 706 made up of p-type MOSFETs, e.g., PFETs. The D+/D-

multiplexer 706 may include a first set of four PFETs 706A and a second four PFETs 706B. The USB-C controller 702 may further include a negative charge pump 709 to drive gates of the PFETs of the D+/D- multiplexer 706.

[0054] FIG. 8 is a flow chart for a method 800 of designing a USB-C controller to form a high-speed, type-C interface circuit according to one embodiment. The method 800 may be performed by processing logic that comprises hardware (e.g., circuitry, dedicated logic, programmable logic, microcode, etc.). In some embodiments, the method 800 is performed wholly or in part by one of the USB-C controllers discussed herein.

[0055] In various embodiments, the method 800 may begin by operating a USB-C controller instantiated as a first integrated circuit, wherein the USB-C controller includes a D+/D- multiplexer, a charger detector circuit, and an electrostatic discharge (ESD) protection circuit (810). The operating the USB-C controller may be performed as illustrated in any of blocks 820, 830, and/or 840. For example, the method 800 may continue with selectively coupling, by the D+/D- multiplexer, a first set of terminals to a second set of terminals, wherein the first set of terminals are coupled to host controllers and the second set of terminals are coupled to sets of D+/D- terminals of a type-C receptacle (820). The coupling by the D+/D- multiplexer may be performed in response to, or after, connection orientation is determined based on CC signal(s) on the CC channel of the USB-C controller.

[0056] With additional reference to FIG. 8, the method 800 may continue with detecting, by the charger detector circuit, whether the second set of terminals are coupled to a USB charger through the type-C receptacle, wherein the charger detector circuit is coupled between a positive data system terminal and a negative data system terminal of the first set of terminals (830). The detecting by the charger detector circuit may be performed in response to, or after, determining that a second or peripheral device is connected or attached to the type-C receptacle.

[0057] With additional reference to FIG. 8, the method 800 may continue with providing ESD protection by the ESD protection circuit, wherein the ESD protection circuit is coupled between the D+/D- multiplexer and the second set of terminals (840). The ESD protection by the ESD protection circuit may be provided

whenever the second or peripheral device is coupled to the second set of terminals through the Type-C receptacle.

[0058] In the above description, numerous details are set forth. It will be apparent, however, to one of ordinary skill in the art having the benefit of this disclosure, that embodiments of the present disclosure may be practiced without these specific details. In some instances, well-known structures and devices are shown in block diagram form, rather than in detail, in order to avoid obscuring the description.

[0059] Some portions of the detailed description are presented in terms of algorithms and symbolic representations of operations on data bits within a computer memory. These algorithmic descriptions and representations are the means used by those skilled in the data processing arts to most effectively convey the substance of their work to others skilled in the art. An algorithm is here and generally, conceived to be a self-consistent sequence of steps leading to a desired result. The steps are those requiring physical manipulations of physical quantities. Usually, though not necessarily, these quantities take the form of electrical or magnetic signals capable of being stored, transferred, combined, compared and otherwise manipulated. It has proven convenient at times, principally for reasons of common usage, to refer to these signals as bits, values, elements, symbols, characters, terms, numbers or the like.

[0060] It should be borne in mind, however, that all of these and similar terms are to be associated with the appropriate physical quantities and are merely convenient labels applied to these quantities. Unless specifically stated otherwise as apparent from the above discussion, it is appreciated that throughout the description, discussions utilizing terms such as “receiving,” “adjusting,” or the like, refer to the actions and processes of a computing system, or similar electronic computing device, that manipulates and transforms data represented as physical (e.g., electronic) quantities within the computing system's registers and memories into other data similarly represented as physical quantities within the computing system memories or registers or other such information storage, transmission or display devices.

[0061] The words “example” or “exemplary” are used herein to mean serving as an example, instance or illustration. Any aspect or design described herein as “example” or “exemplary” is not necessarily to be construed as preferred or advantageous over other aspects or designs. Rather, use of the words “example” or “exemplary” is intended to present concepts in a concrete fashion. As used in this application, the term “or” is intended to mean an inclusive “or” rather than an exclusive “or.” That is, unless specified otherwise, or clear from context, “X includes A or B” is intended to mean any of the natural inclusive permutations. That is, if X includes A; X includes B; or X includes both A and B, then “X includes A or B” is satisfied under any of the foregoing instances. In addition, the articles “a” and “an” as used in this application and the appended claims should generally be construed to mean “one or more” unless specified otherwise or clear from context to be directed to a singular form. Moreover, use of the term “an embodiment” or “one embodiment” or “an embodiment” or “one embodiment” throughout is not intended to mean the same embodiment or embodiment unless described as such.

[0062] Embodiments described herein may also relate to an apparatus for performing the operations herein. This apparatus may be specially constructed for the required purposes, or it may comprise a general-purpose computer selectively activated or reconfigured by a computer program stored in the computer. Such a computer program may be stored in a non-transitory computer-readable storage medium, such as, but not limited to, any type of disk including floppy disks, optical disks, CD-ROMs and magnetic-optical disks, read-only memories (ROMs), random access memories (RAMs), EPROMs, EEPROMs, magnetic or optical cards, flash memory, or any type of media suitable for storing electronic instructions. The term “computer-readable storage medium” should be taken to include a single medium or multiple media (e.g., a centralized or distributed database and/or associated caches and servers) that store one or more sets of instructions. The term “computer-readable medium” shall also be taken to include any medium that is capable of storing, encoding or carrying a set of instructions for execution by the machine and that causes the machine to perform any one or more of the methodologies of the

present embodiments. The term “computer-readable storage medium” shall accordingly be taken to include, but not be limited to, solid-state memories, optical media, magnetic media, any medium that is capable of storing a set of instructions for execution by the machine and that causes the machine to perform any one or more of the methodologies of the present embodiments.

[0063] The algorithms and displays presented herein are not inherently related to any particular computer or other apparatus. Various general-purpose systems may be used with programs in accordance with the teachings herein, or it may prove convenient to construct a more specialized apparatus to perform the required method steps. The required structure for a variety of these systems will appear from the description below. In addition, the present embodiments are not described with reference to any particular programming language. It will be appreciated that a variety of programming languages may be used to implement the teachings of the embodiments as described herein.

[0064] The above description sets forth numerous specific details such as examples of specific systems, components, methods and so forth, in order to provide a good understanding of several embodiments of the present disclosure. It will be apparent to one skilled in the art, however, that at least some embodiments of the present disclosure may be practiced without these specific details. In other instances, well-known components or methods are not described in detail or are presented in simple block diagram format in order to avoid unnecessarily obscuring the present disclosure. Thus, the specific details set forth above are merely exemplary. Particular embodiments may vary from these exemplary details and still be contemplated to be within the scope of the present disclosure.

[0065] It is to be understood that the above description is intended to be illustrative and not restrictive. Many other embodiments will be apparent to those of skill in the art upon reading and understanding the above description. The scope of the disclosure should, therefore, be determined with reference to the appended claims, along with the full scope of equivalents to which such claims are entitled.

[0066] In the above description, for purposes of explanation, numerous specific details are set forth in order to provide a thorough understanding of the present

disclosure. It will be evident, however, to one skilled in the art that the present disclosure may be practiced without these specific details. In other instances, well-known circuits, structures, and techniques are not shown in detail, but rather in a block diagram in order to avoid unnecessarily obscuring an understanding of this description.

Reference in the description to “one embodiment” or “an embodiment” means that a particular feature, structure, or characteristic described in connection with the embodiment is included in at least one embodiment of the disclosure. The phrase “in one embodiment” located in various places in this description does not necessarily refer to the same embodiment.

CLAIMS

What is claimed is:

1. A device comprising a USB-C controller instantiated as a first integrated circuit, the USB-C controller comprising:

a first set of terminals to be coupled to host controllers;

a second set of terminals to be coupled to sets of D+/D- terminal of a type-C receptacle;

a D+/D- multiplexer to selectively couple the first set of terminals to the second set of terminals;

an electrostatic discharge (ESD) protection circuit coupled between the D+/D- multiplexer and the second set of terminals; and

a charger detector circuit coupled between a positive data system terminal and a negative data system terminal of the first set of terminals, the charger detector circuit to detect whether the second set of terminals is coupled to a USB charger through the type-C receptacle.

2. The device of claim 1, wherein the first set of terminals comprises the positive data system terminal and the negative data system terminal coupled to a USB host controller and a data transmitter terminal and data receiver terminal coupled to a proprietary host controller, the second set of terminals comprises first and second positive data terminals coupled to corresponding D+ terminals of the type-C receptacle and first and second negative data terminals coupled to corresponding D- terminals of the type-C receptacle, and wherein the D+/D- multiplexer is to be coupled:

the positive data system terminal to one of the first and second positive data terminals;

the data transmitter terminal to one of the first and second positive data terminals;

the negative data system terminal to one of the first and second negative data terminals; and

the data receiver terminal to one of the first and second negative data terminals.

3. The device of claim 1, wherein the first set of terminals comprises a set of Universal Asynchronous Receiver-Transmitter (UART) terminals.
4. The device of claim 1, wherein the first set of terminals is associated with a first connection of a single USB port, and wherein the second set of terminals is associated with a second connection of the single USB port.
5. The device of claim 1, wherein the charger detector circuit is further coupled between a data transmitter terminal and a data receiver terminal of the first set of terminals, the charger detector circuit further to detect whether a second positive data terminal and a second negative data terminal of the second set of terminals are coupled to a second USB charger through the type-C receptacle.
6. The device of claim 1, wherein the ESD protection circuit comprises:
 - an IEC ESD RC snapback clamp coupled between a local power supply and a ground;
 - at least one HBM diode coupled between the local power supply and each of the second set of terminals; and
 - at least one HBM diode coupled between the ground and each of the second set of terminals.
7. The device of claim 1, wherein the USB-C controller further comprises system ESD protection circuitry comprising:
 - a first human body model (HBM) snapback clamp coupled to a ground;
 - a first pair of diodes connected in series and coupled between the first HBM snapback clamp and a positive data system terminal of the first set of terminals;
 - a second HBM snapback clamp coupled to the ground; and
 - a second pair of diodes connected in series and coupled between the second HBM snapback clamp and a negative data system terminal of the first set of terminals.

8. The device of claim 1, wherein the D+/D- multiplexer is controlled to provide flip correction based on a configuration channel (CC) signal.
9. The device of claim 1, wherein the charger detector circuit includes a first switch coupled to the positive data system terminal and a second switch coupled to the negative data system terminal, the first switch and the second switch controllable by first logic to disconnect the charger detector circuit during high-speed data transfer of the USB-C controller.
10. The device of claim 1, wherein the USB-C controller further comprises a charge pump coupled to gates of metal-oxide-semiconductor field-effect transistors (MOSFETs) of the D+/D- multiplexer, wherein the charge pump is to drive the MOSFETs to operate such that each MOSFET exhibits less than seven-ohm resistance.
11. A system comprising:
a USB host controller and a proprietary host controller;
a USB type-C receptacle; and
a USB-C controller coupled to the USB type-C receptacle, to the USB host controller, and to the proprietary host controller, the USB-C controller comprising:
a first set of first terminals coupled to the USB host controller;
a second set of terminals coupled to the proprietary host controller;
a third set of terminals to be coupled to sets of D+/D- terminals of the USB type-C receptacle;
a D+/D- multiplexer to selectively couple the first and second sets of terminals to the third set of terminals;
an electrostatic discharge (ESD) protection circuit coupled between the D+/D- multiplexer and the third set of terminals; and
a charger detector circuit coupled between a positive data system terminal and a negative data system terminal of the first set of terminals, the charger detector circuit to detect whether the third set of terminals is coupled to a USB charger through the type-C receptacle.

12. The system of claim 11, wherein the first set of terminals comprises the positive data system terminal and the negative data system terminal, the second set of terminals comprises a data transmitter terminal and data receiver terminal, the third set of terminals comprises first and second positive data terminals coupled to corresponding D+ terminals of the type-C receptacle and first and second negative data terminals coupled to corresponding D- terminals of the type-C receptacle, and wherein the D+/D- multiplexer is to couple:

- the positive data system terminal to one of the first and second positive data terminals;

- the data transmitter terminal to one of the first and second positive data terminals;

- the negative data system terminal to one of the first and second negative data terminals; and

- the data receiver terminal to one of the first and second negative data terminals.

13. The system of claim 11, wherein the first set of terminals comprises a set of Universal Asynchronous Receiver-Transmitter (UART) terminals.

14. The system of claim 11, wherein the first set of terminals is associated with a first connection of a single USB port, and wherein the second set of terminals is associated with a second connection of the single USB port.

15. The system of claim 11, wherein the ESD protection circuit comprises:

- an IEC ESD RC snapback clamp coupled between a local power supply and a ground;

- at least one HBM diode coupled between the local power supply and each of the second set of terminals; and

- at least one HBM diode coupled between the ground and each of the second set of terminals.

16. The system of claim 11, wherein the USB-C controller further comprises system ESD protection circuitry comprising:
- a first human body model (HBM) snapback clamp coupled to a ground;
 - a first pair of diodes connected in series and coupled between the first HBM snapback clamp and a positive data system terminal of the first set of terminals;
 - a second HBM snapback clamp coupled to the ground; and
 - a second pair of diodes connected in series and coupled between the second HBM snapback clamp and a negative data system terminal of the first set of terminals.
17. The system of claim 11, wherein the D+/D- multiplexer is controlled to provide flip correction based on a configuration channel (CC) signal.
18. The system of claim 11, wherein the charger detector circuit includes a first switch coupled to the positive data system terminal and a second switch coupled to the negative data system terminal, the first switch and the second switch controllable by first logic to disconnect the charger detector circuit during high-speed data transfer of the USB-C controller.
19. The system of claim 11, wherein the USB-C controller further comprises a charge pump coupled to gates of metal-oxide-semiconductor field-effect transistors (MOSFETs) of the D+/D- multiplexer, wherein the charge pump is to drive the MOSFETs to operate such that each MOSFET exhibits less than seven-ohm resistance.
20. A method comprising:
- operating a USB-C controller instantiated as a first integrated circuit, wherein the USB-C controller comprises a D+/D- multiplexer, a charger detector circuit, and an electrostatic discharge (ESD) protection circuit, and wherein operating the USB-C controller comprises:
 - selectively coupling, by the D+/D- multiplexer, a first set of terminals to a second set of terminals, wherein the first set of terminals are coupled to host

controllers and the second set of terminals are coupled to sets of D+/D- terminals of a type-C receptacle;

detecting, by the charger detector circuit, whether the second set of terminals are coupled to a USB charger through the type-C receptacle, wherein the charger detector circuit is coupled between a positive data system terminal and a negative data system terminal of the first set of terminals; and

providing ESD protection by the ESD protection circuit, wherein the ESD protection circuit is coupled between the D+/D- multiplexer and the second set of terminals.

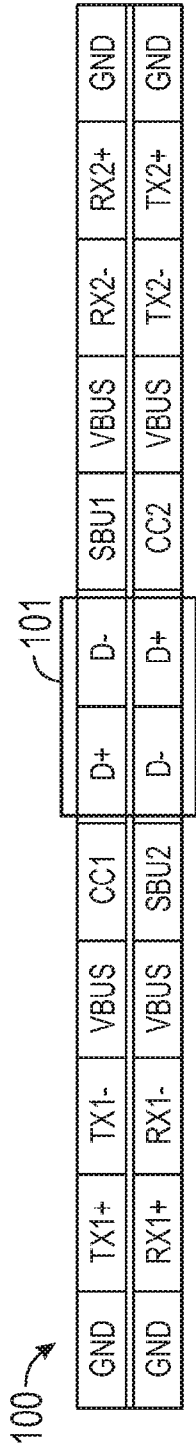
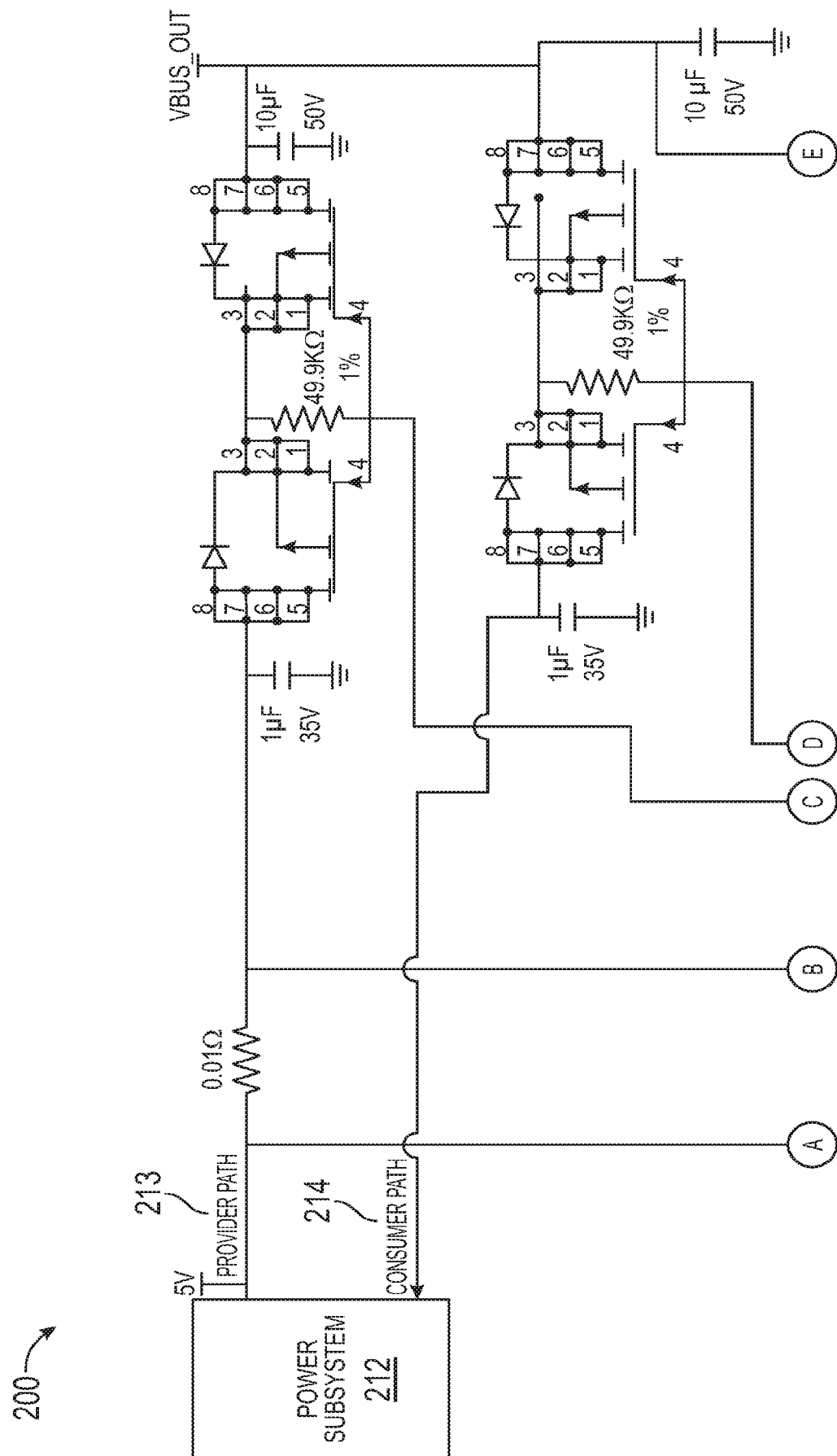
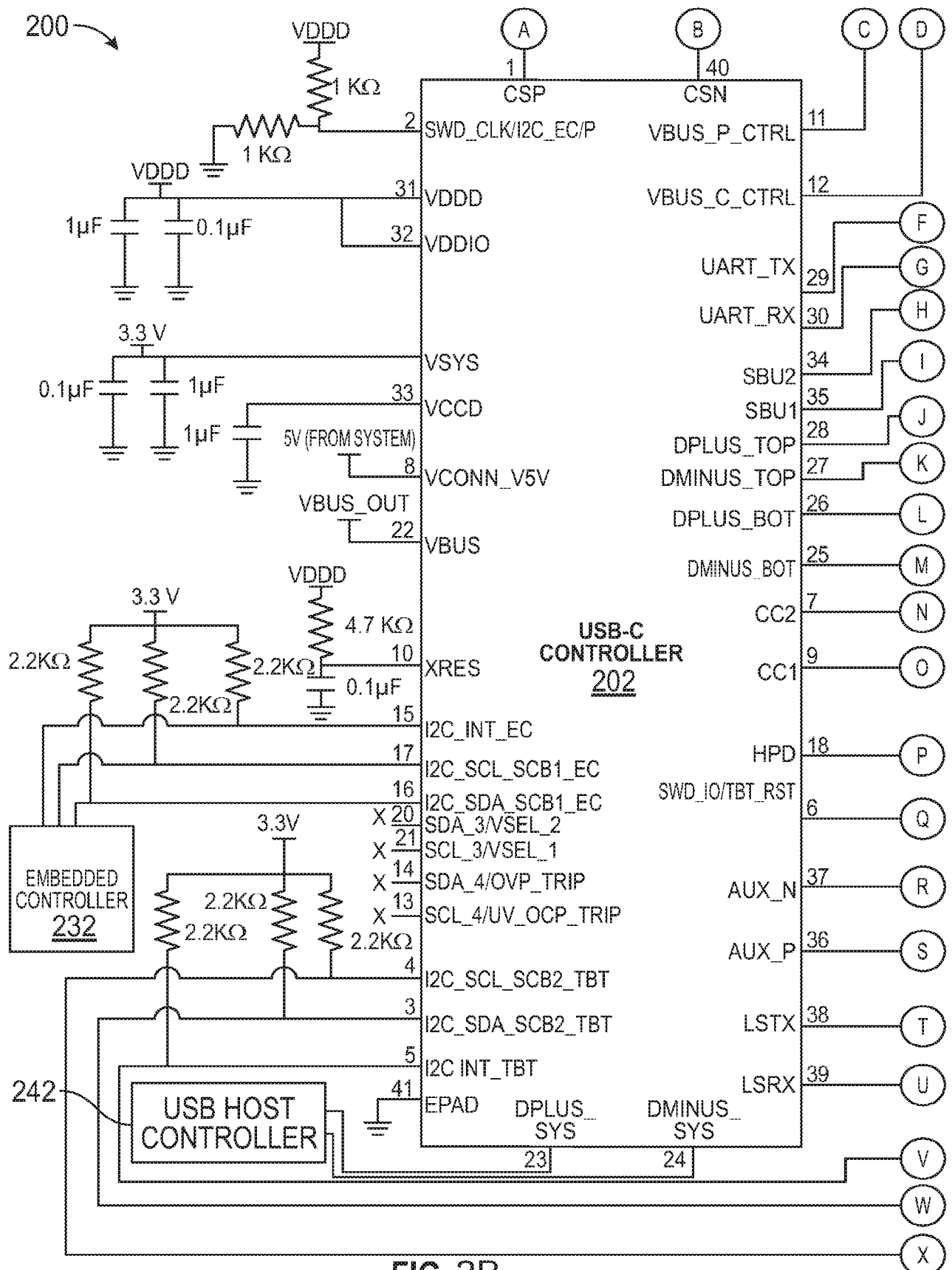


FIG. 1



24
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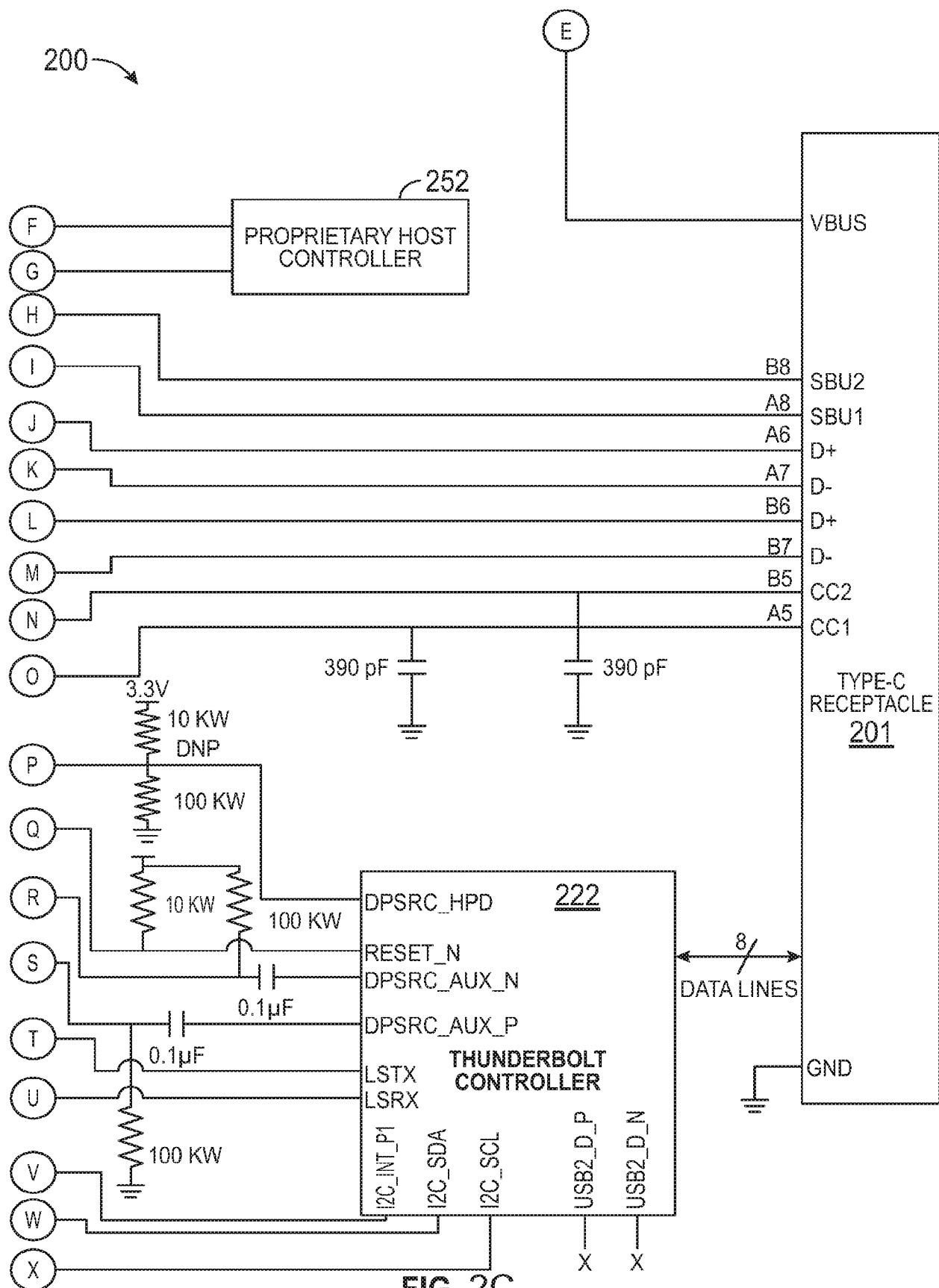


FIG. 2C
(Continued)

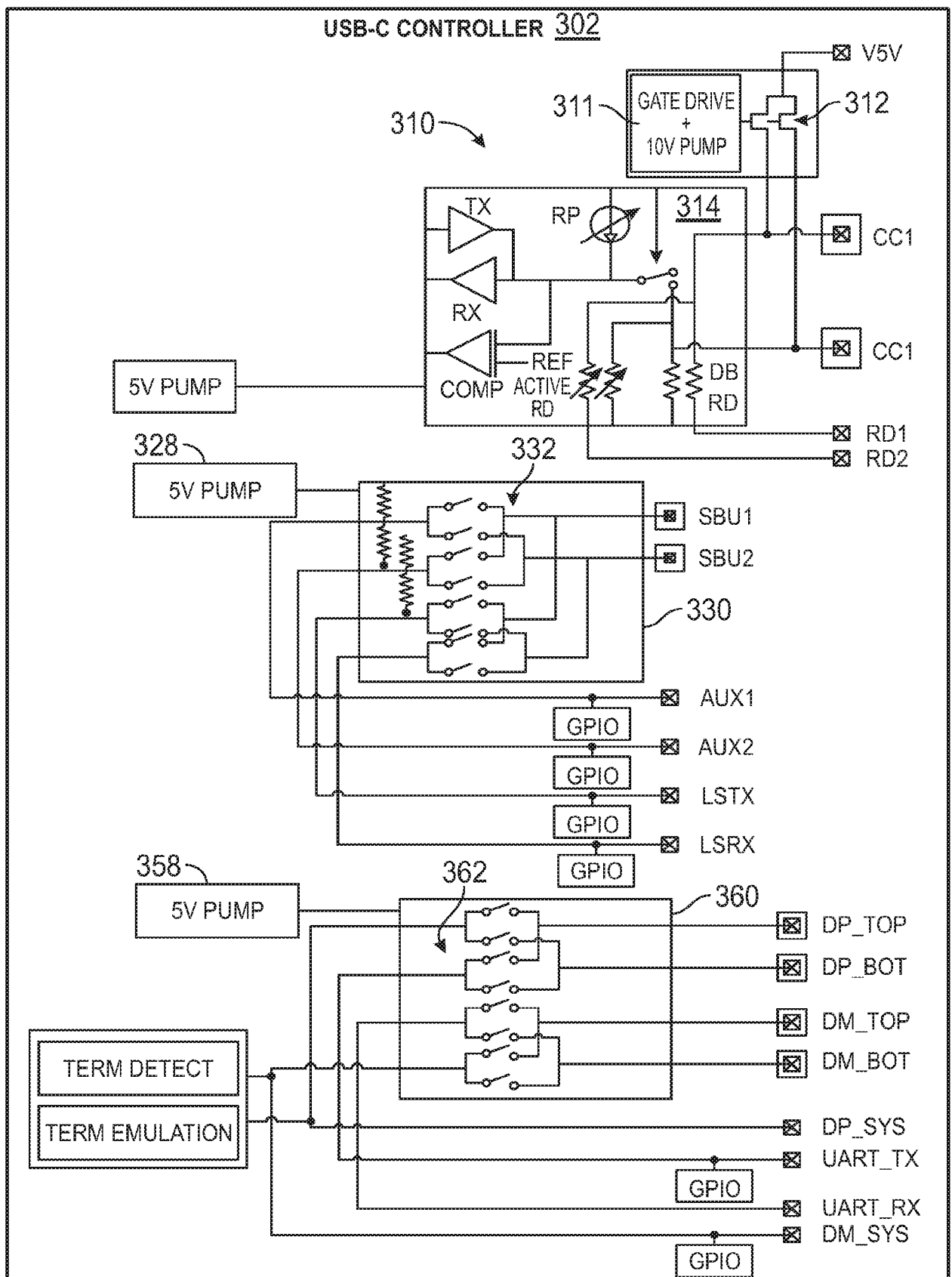


FIG. 3

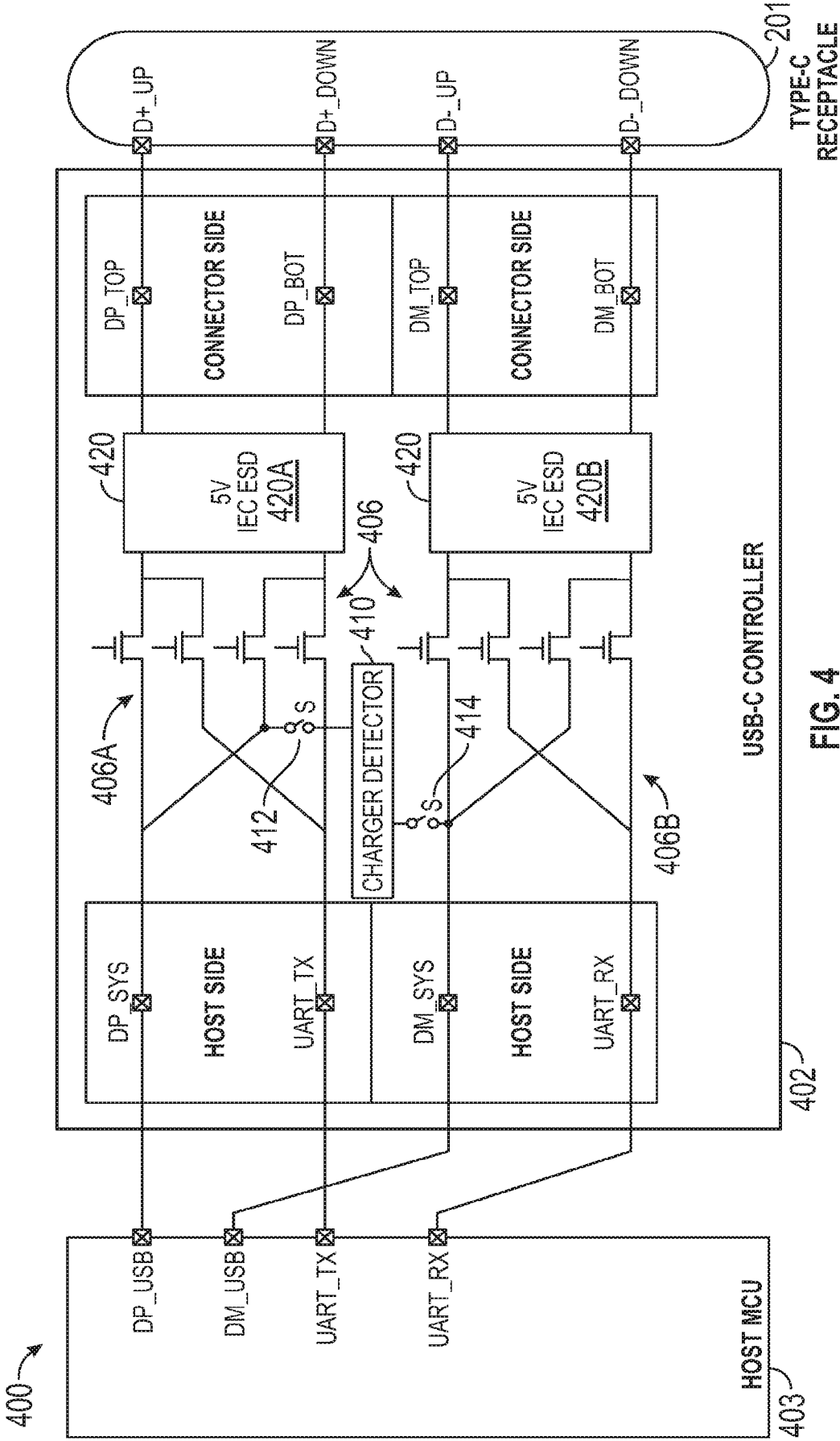


FIG. 4

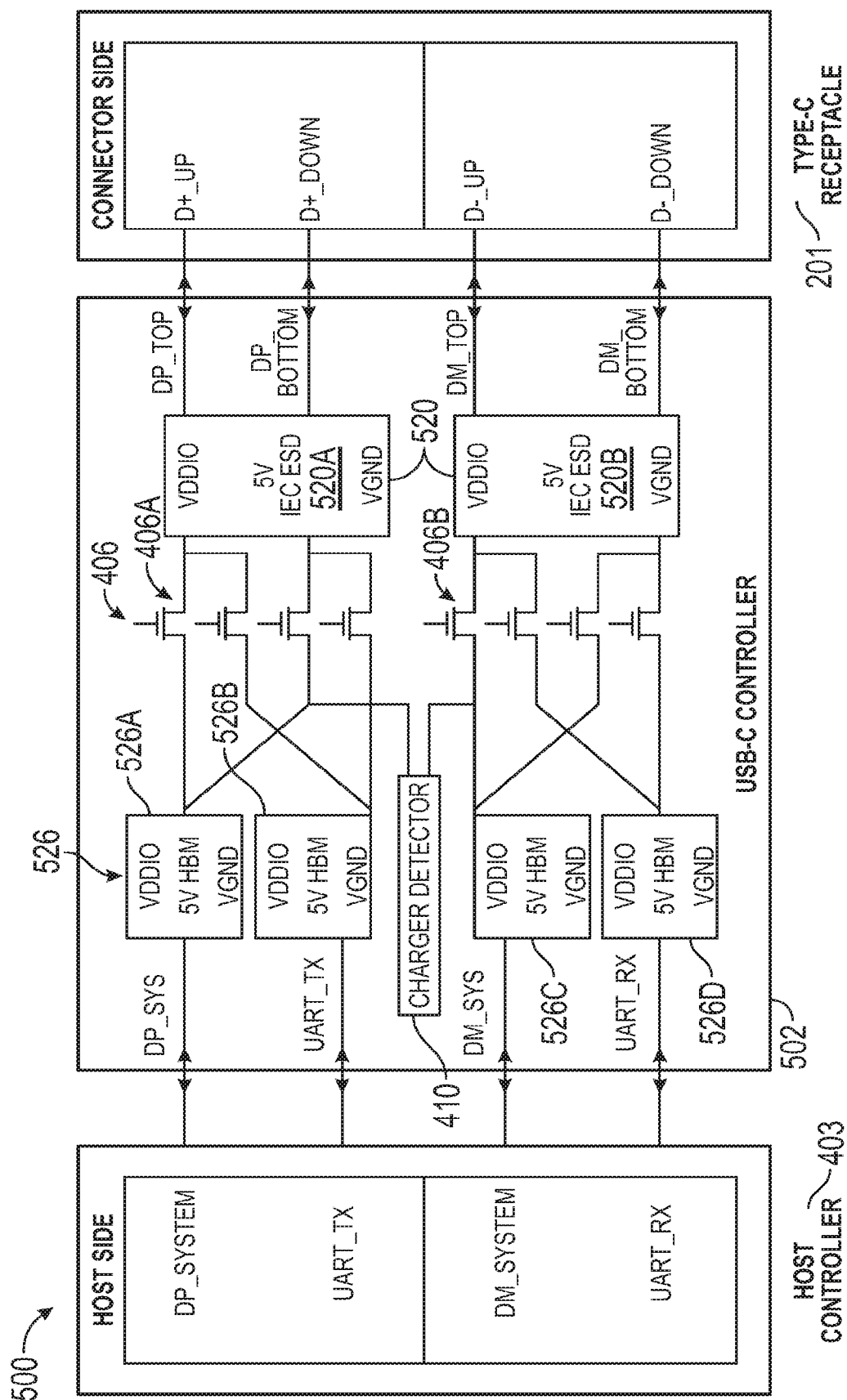


FIG. 5A

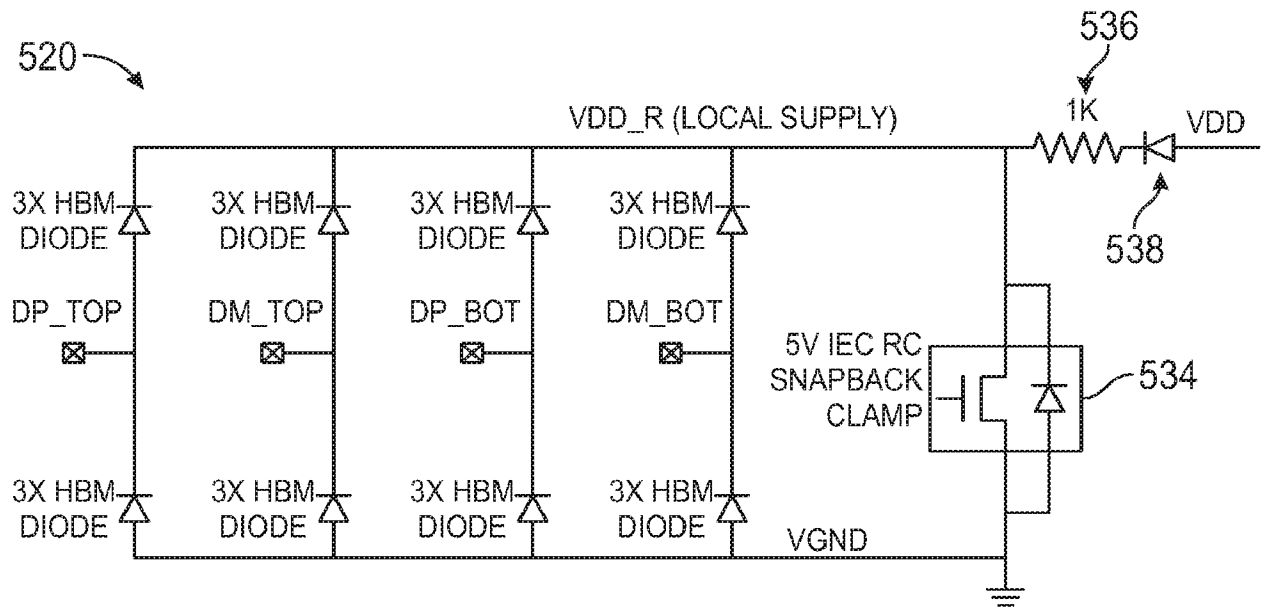


FIG. 5B

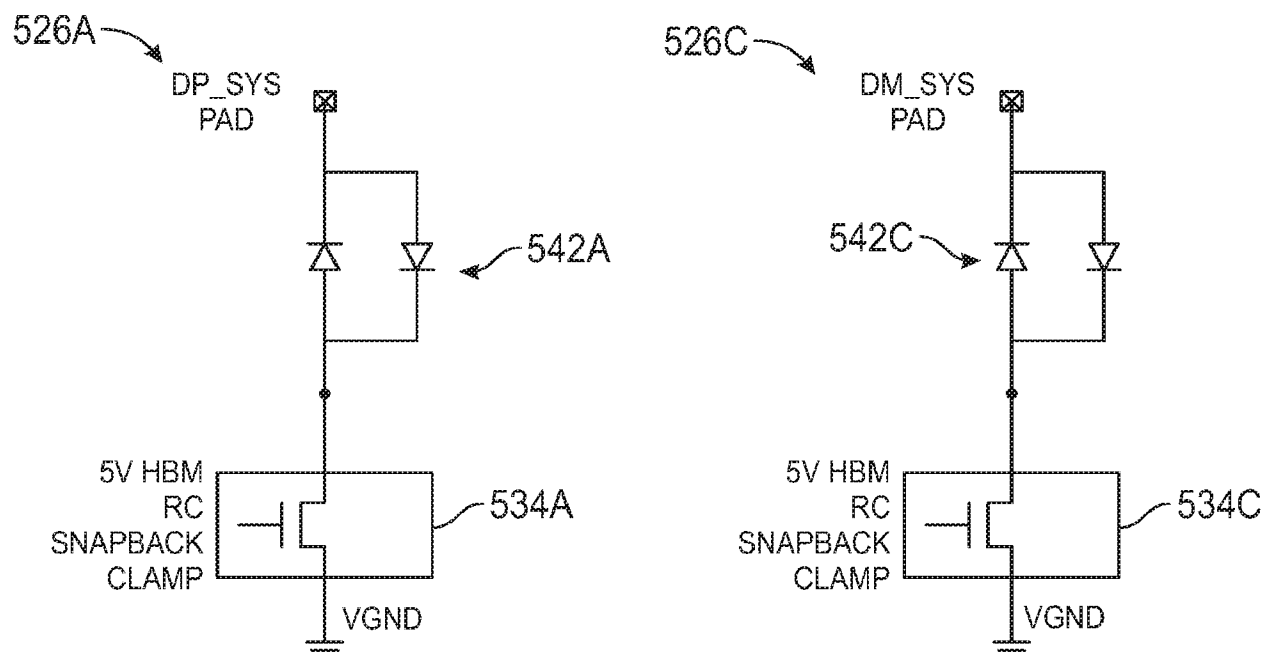


FIG. 5C

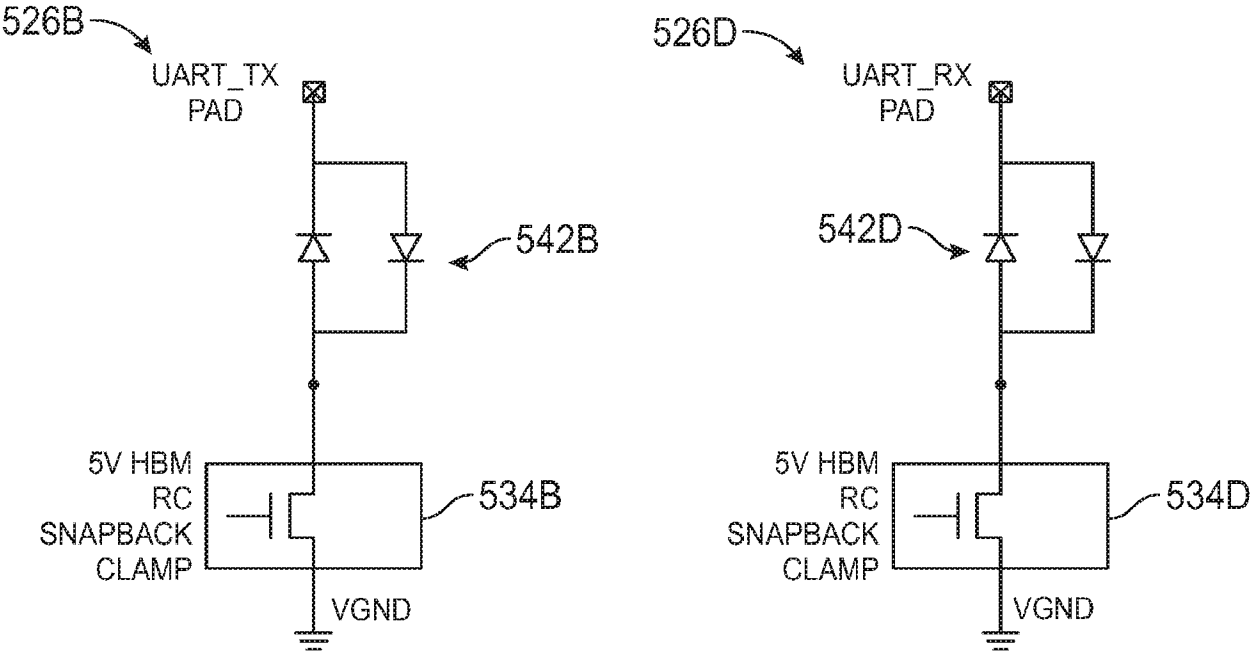


FIG. 5D

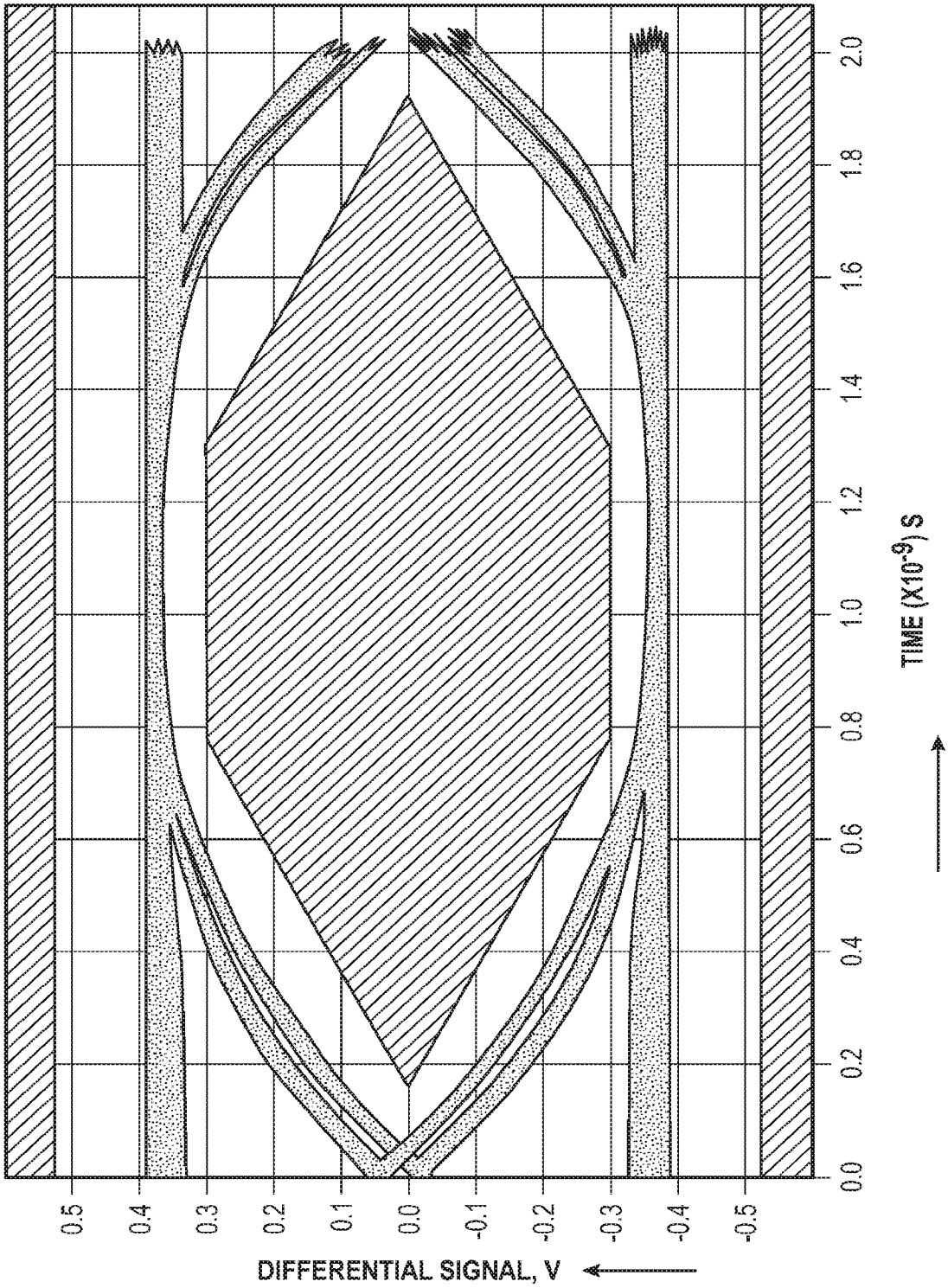


FIG. 6

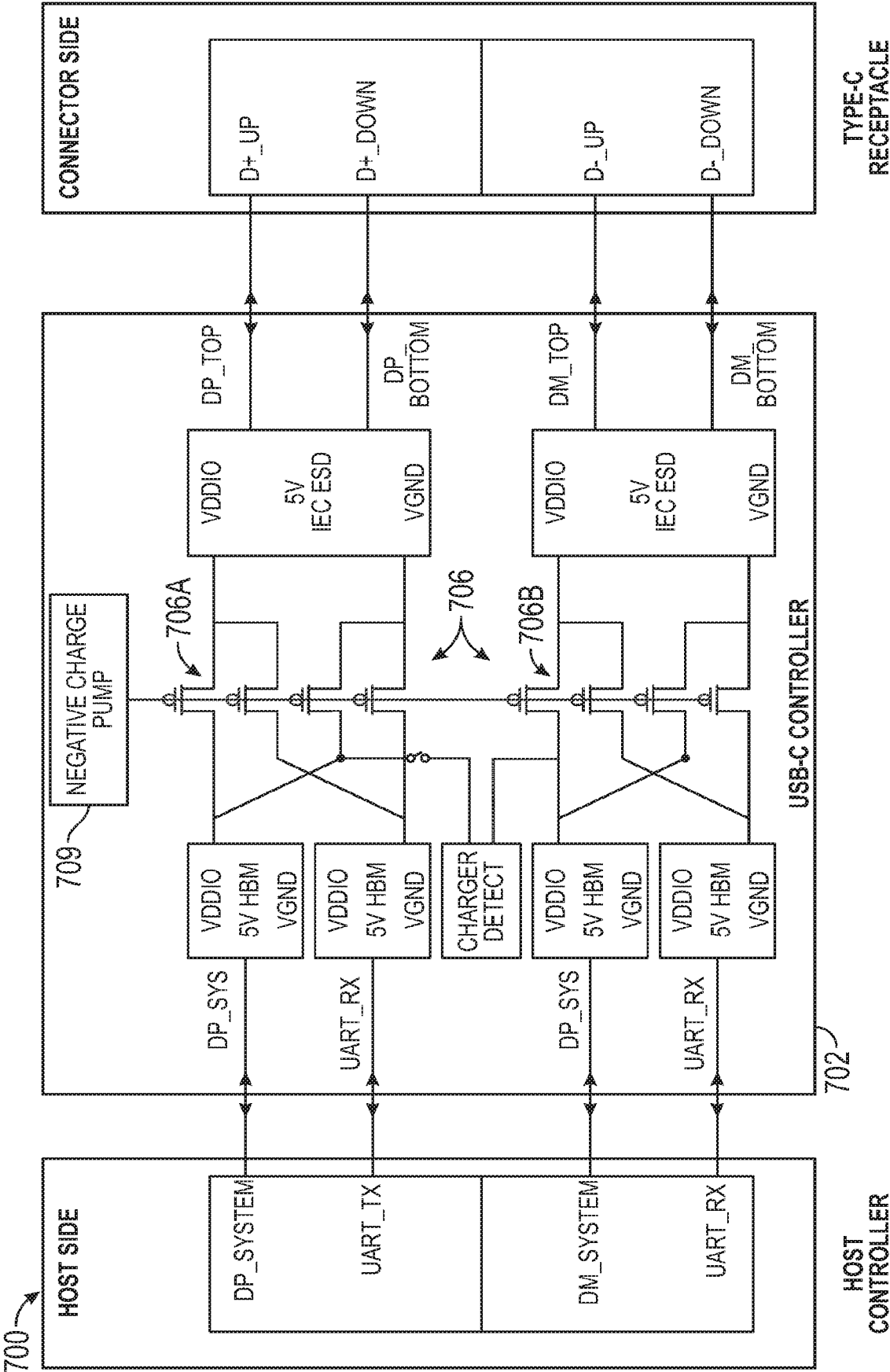
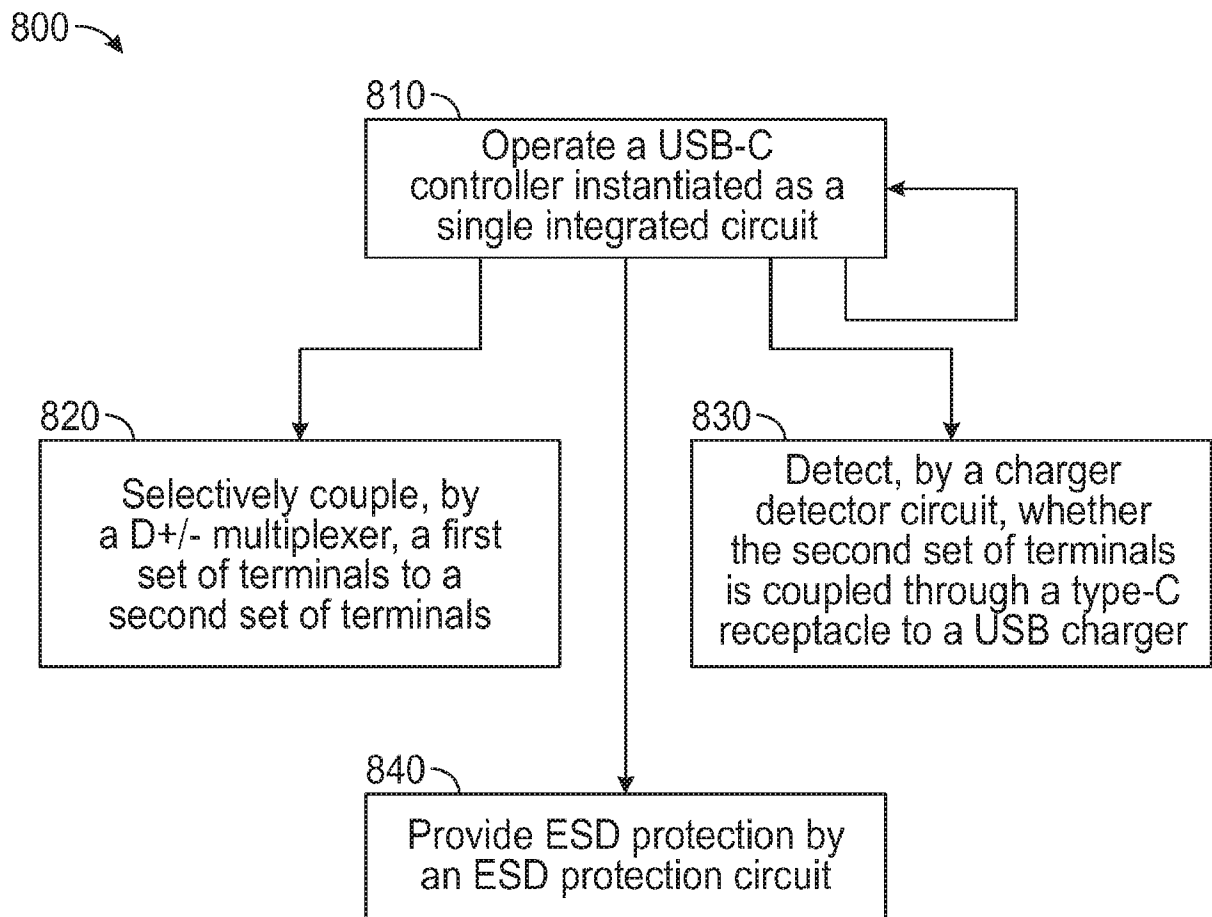


FIG. 7

**FIG. 8**

INTERNATIONAL SEARCH REPORT

International application No.

PCT/US2019/025949

A. CLASSIFICATION OF SUBJECT MATTER

IPC: G06F 1/26

CPC: G06F 1/3203, 1/26, 1/3296

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US 2016/0179648 A1 (SRIVASTAVA ET AL.) 23 June 2016 (23.06.2016) , entire document.	1-20
Y	US 2018/0062386 A1 (MALLIKARJUNASWAMY) 01 March 2018 (01.03.2018) , entire document.	1-20
Y	US 2017/0286360 A1 (SRIVASTAVA) 05 October 2017 (05.10.2017) , entire document.	3, 13

☐ Further documents are listed in the continuation of Box C.☐ See patent family annex.

* Special categories of cited documents:

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- "O" document referring to an oral disclosure, use, exhibition or other means
- "P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

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"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search

09 May 2019 (09.05.2019)

Date of mailing of the international search report

10 MAY 2019

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