



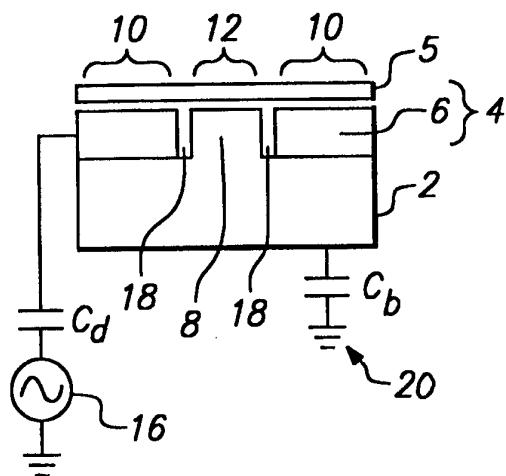
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(54) Title: POWER SEGMENTED ELECTRODE

(57) Abstract

A power segmented electrode useful as part of an upper electrode and/or substrate support for supporting a substrate such as a semiconductor wafer in a plasma reaction chamber such as a single wafer etcher. The power segmented electrode includes a plurality of electrodes which are supplied radiofrequency power in a manner which provides uniform processing of the substrate. The power to the electrodes can be supplied through a circuit incorporating interelectrode gap capacitance, one or more variable capacitors, one or more current sensors, a power splitter, one or more DC biasing sources, and/or power amplifier.



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POWER SEGMENTED ELECTRODE

FIELD OF THE INVENTION

The invention relates to an electrode for generating a plasma and/or local plasma density control in a plasma reaction chamber. The electrode can 5 be incorporated in an upper electrode and/or incorporated in a substrate support such as a chucking device for holding a substrate such as a semiconductor wafer, flat panel display, etc., during processing thereof in a plasma gas environment.

BACKGROUND OF THE INVENTION

10 Equipment for processing semiconductor wafers in a plasma gas environment typically couple radio frequency (RF) power from the plasma gas to the wafer to effect surface treatment of the wafer (e.g., etching, deposition, etc). For instance, U.S. Patent No. 4,617,079 discloses a parallel plate arrangement wherein a wafer is supported on a lower electrode, RF power from 15 a low frequency generator passes through a low frequency network, RF power from a high frequency generator is combined with the low frequency RF power in a high frequency matching and combining network, and the combined signals are applied across upper and lower electrodes. In this arrangement, the high frequency matching and combining circuit can include a high frequency trap (capacitor and inductor in parallel) tuned to the frequency of the high frequency source for preventing signals generated by the high frequency source from 20 being fed back to the low frequency source but allowing signals generated by the low frequency source to pass therethrough without being attenuated.

25 U.S. Patent No. 4,948,458 discloses a parallel plate arrangement wherein the upper electrode is in the form of an electrically conductive coil located outside the plasma reaction chamber and by inducing an RF current in the coil a magnetic field is produced in a planar region parallel to the plane of the coil. The coil is driven by an RF generator which supplies power to a matching circuit having a primary coil and a secondary loop. A variable 30 capacitor in series with the secondary loop adjusts the circuit resonant

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frequency with the frequency output of the RF generator and impedance matching maximizes efficiency of power transfer to the planar coil. An additional capacitor in the primary circuit cancels part of the inductive reactance of the coil in the circuit.

5 When processing semiconductor wafers in plasma gas environments, it is desired to uniformly process the entire surface of the wafer. For example, U.S. Patent No. 4,615,755 discloses a plasma etching technique wherein uniformity of the wafer temperature is achieved by He backcooling of a wafer supported on a bowed electrode. By bowing the wafer away from the lower 10 electrode with the cooling helium, cooling performance of the wafer is sacrificed in order to achieve etch uniformity. However, variations in the thickness of the wafer results in sub-standard control of the wafer bowing and thereby reduces the etch uniformity.

15 In plasma etching processes which use electrostatic (ESC) wafer clamping systems, the wafer cannot be bowed away from the surface of the electrode to control etch rate uniformity. Accordingly, other techniques are necessary for controlling the uniformity of the wafer surface treatment in plasma processing which are applied to ESC wafer clamping systems.

SUMMARY OF THE INVENTION

20 The invention provides a power segmented electrode for providing uniform processing of a substrate in a plasma reaction chamber. The power segmented electrode includes first and second electrodes and a capacitive network. The power segmented electrode is attachable to the plasma reaction chamber such that the first electrode is distributed across a first zone of the 25 plasma reaction chamber and the second electrode is distributed across a second zone of the plasma reaction chamber. The capacitive network controls distribution of radio frequency power in the first and second zones such that plasma coupled to a substrate supported in the plasma reaction chamber provides uniform processing across the substrate. In a preferred embodiment, 30 the substrate comprises a semiconductor wafer and the power segmented

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electrode is incorporated in an electrostatic chuck located in a plasma reaction etching chamber.

The power segmented electrode can be embodied in various ways. For instance, the first electrode can be separated from the second electrode by a gap 5 filled with dielectric material to form an interelectrode capacitor of the capacitive network. In a preferred embodiment, the first electrode surrounds the second electrode and is separated from the second electrode by a gap filled with dielectric material, the gap forming an interelectrode capacitor of the capacitive network. In this case, the first and second capacitors can form part 10 of the capacitive network and radio frequency power from a power source can pass sequentially through the first capacitor, through the first electrode, through the second capacitor, through the second electrode, and to an electrical ground.

According to another embodiment, the first and second electrodes form part of a concentric electrode arrangement comprising a plurality of spaced 15 apart annular electrodes, the electrodes being electrically connected to a radio frequency power source through variable capacitors forming part of the capacitive network and radio frequency power from the power source sequentially passing through each of the variable capacitors and to a respective one of the electrodes. In this case, current sensing mechanisms can be 20 provided for automatically adjusting capacitance of a respective one of the variable capacitors such that adjustment signals emitted therefrom compensate for deviations from uniformity of processing of the substrate in an annular zone of the substrate facing a respective one of the annular electrodes. The capacitive network can comprise first and second capacitors, the first capacitor 25 being connected to the first electrode and the second capacitor being connected to the second electrode, the first and second capacitors being electrically connected in parallel to a radio frequency power source. The power segmented electrode can include a third electrode, the first electrode surrounding the second electrode and the second electrode surrounding the third electrode, each 30 of the electrodes being electrically connected to a radio frequency power source, radio frequency power from the power source passing sequentially

through a power splitter and to a respective one of the electrodes.

Alternatively, the first electrode can surround only part of the second electrode.

The first and second electrodes can be incorporated in an electrostatic chuck and the electrodes can be electrically connected to direct current biasing sources

5 which allow the chuck to electrostatically clamp a substrate on the chuck. The radio frequency power can be supplied in phase or out of phase to the first and second electrodes. Also, a passive network can be used for supplying power and DC bias to the first and second electrodes.

According to another aspect of the invention, the power segmented
10 electrode can include a sine wave generator for generating a numerically sequenced sine wave, a biasing unit for generating a DC offset value, a summation unit for summing the numerically sequenced sine wave and the DC offset value, a digital/analog converter for converting the signal output from the summation unit to an analog summation signal, a low pass filter for filtering
15 predetermined low frequency portions of the analog summation signal, and a power amplifier for amplifying the analog summation signal filtered by the low pass filter and driving the first and second electrodes with the amplified signal. In this case, the first electrode completely surrounds the second electrode and the capacitive network supplies more power to the second electrode than to the
20 first electrode. The first electrode can surround the second electrode and power is supplied to the first and second electrodes by sequentially passing through the first electrode, an interelectrode capacitor formed by a dielectric material disposed in a gap between the first and second electrodes, the second electrode, a series of capacitors forming part of the capacitive network and an electrical
25 ground, the dielectric material providing the interelectrode capacitance to be less than that of the series of capacitors. The power segmented electrode can further comprise a voltage divider circuit electrically connected to the first electrode or the second electrode. The first electrode can be driven by a first active power driver and the second electrode can be driven by a second active
30 power driver, the first and second power drivers being operated independently of each other.

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The invention also provides a plasma processing system comprising a substrate support for clamping a substrate in a plasma reaction chamber of the plasma processing system, the substrate support including a plurality of electrodes associated with zones of the substrate support adjacent to the substrate and a power controller for controlling power supplied to the zones of the substrate support through the plurality of electrodes so that uniform processing is applied across an entire a surface of the substrate. In this case, the power controller includes a capacitive network connected to the plurality of electrodes for distributing power to the zones of the substrate chuck. Adjacent ones of the plurality of electrodes can be separated by gaps, and each of the gaps can be filled with dielectric material to form interelectrode capacitors of the capacitive network. The plurality of electrodes can be segmented into concentric annular rings and or provided in a pattern which compensates for process gas flow in the reaction chamber and provide uniform processing of the substrate.

BRIEF DESCRIPTION OF THE DRAWINGS

The present invention will become more fully understood from the detailed description given hereinbelow and the accompanying drawings which are given by way of illustration only, and thus are not limitative of the present invention, wherein:

FIG. 1(a) illustrates a bipolar type of electrostatic wafer clamping system used in an embodiment of the invention;

FIG. 1(b) illustrates an electrical schematic diagram of the electrostatic wafer clamping system illustrated in FIG. 1(a);

FIG. 2 illustrates an electrode segmented into a plurality of concentric annular rings in an embodiment of the invention;

FIG. 3 illustrates a segmented driving system used for the segmented electrodes in an embodiment of the invention;

FIG. 4 illustrates an asymmetrical pattern of segmented electrodes used in an embodiment of the invention;

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FIG. 5 illustrates an active mechanism for controlling the power delivered to zones of the segmented electrodes in an embodiment of the invention;

5 FIG. 6 illustrates a system for simultaneously coupling RF energy into both poles of an electrostatic wafer clamping system in an embodiment of the invention; and

FIG. 7 illustrates a voltage divider circuit and a capacitor network used to balance and adjust the RF voltage applied to the chuck surface in an embodiment of the invention.

10 **DETAILED DESCRIPTION OF THE INVENTION**

The invention provides a power segmented electrode of a plasma reaction chamber wherein density of the plasma can be locally enhanced or weakened to achieve desired substrate processing conditions. In the case of a semiconductor wafer, it is typically desired to achieve uniform processing of the exposed surface of the wafer from center to edge thereof. According to the invention, localized control of the plasma density is achieved with a capacitive network which balances RF power such that plasma coupled to the wafer in zones adjacent the exposed surface of the wafer provides uniform wafer processing, e.g., during etching a layer on the wafer or building up a layer on the wafer.

20 The power segmented electrode according to the invention can be incorporated in a mechanical or electrostatic chucking arrangement for holding a substrate such as a semiconductor wafer during processing thereof. The electrostatic chuck can comprise a bipolar chuck or other type of electrode arrangement. However, the power segmented electrode can also be incorporated in an upper electrode of a parallel plate electrode arrangement of a plasma reaction chamber.

25 In the case of processing a wafer, it is usually desired to provide a uniform plasma density above the exposed surface of the wafer to be processed. 30 However, depending on the treatment to be performed on the wafer surface,

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non-uniform plasma density can occur above the wafer surface. For instance, the plasma density may be greater at the wafer center than at the edge thereof or vice versa. The power segmented electrode of the invention can provide local plasma density control and thus achieve substantial improvement in 5 uniformity compared to previously known electrode arrangements.

The invention will now be described with reference to several embodiments thereof. In one embodiment, the power segmented electrode is incorporated in a bipolar chuck, as shown in FIG. 1(a). In another embodiment, the power segmented electrode includes three or more electrodes, 10 as shown in FIG. 2. In yet another embodiment, the electrodes of the power segmented electrode are arranged in a series and supplied RF power by a single RF power supply, as shown in FIG. 1(a). In another arrangement, the electrodes are arranged in parallel and supplied RF power by a single RF power supply, as shown in FIG. 5. In the latter case, the RF power can be passed 15 through individual variable capacitors, as shown in FIG. 5, or through a power splitter, as shown in FIG. 2. In addition, the electrodes can be electrically connected to current sensors and/or variable capacitors, as shown in FIG. 5.

In the arrangement shown in FIG. 1(a), a substrate S in the form of a semiconductor wafer is supported on a substrate support 2 in the form of a 20 wafer chuck system located in a plasma reaction chamber of a plasma reactor. The chuck system includes electrodes 4 which can be used to locally vary the amount of coupling of plasma to the wafer. The electrodes 4 include a first electrode 6 surrounding a second electrode 8, the first electrode 6 being located in a first zone 10 of the substrate support 2 and the second electrode being 25 located in a second zone 12 of the substrate support 2. The chuck system also includes an RF power source 16 which supplies balanced RF power in the first and second zones 10 and 12. In the embodiment shown, power from the RF power source 16 passes through the first electrode 6, through a gap 18 to the second electrode 8 and then to ground 20. The gap 18 is preferably filled with 30 a dielectric material and the size of the gap 18 is chosen to provide an interelectrode capacitance effective in balancing the RF power between the first

and second electrodes 6 and 8 such that plasma coupled to the wafer in the first and second zones 10 and 12 provides uniform processing from center to edge of the wafer.

In this embodiment, a bipolar type of ESC wafer clamping system is 5 illustrated to hold the wafer in a simple donut/base arrangement wherein the electrode is segmented into two zones. In this ESC arrangement, the wafer cannot be bowed away from the lower electrode and the helium can only be used to cool the backside of the wafer. FIG. 1(b) illustrates an electrical schematic diagram of this ESC wafer clamping system. A source capacitance 10 C_d is connected at the input to smooth the power applied to the first electrode 6 and the inherent capacitance between the second electrode 8 and ground is represented by C_b . The ratio between the capacitance of gap 18 (represented by C_g) and the base capacitance C_b determines the voltage applied to the first and second electrodes 6 and 8. Because the plasma processing is a function of 15 pressure, flow, power, temperature, gap size, gas, baffle design, material, RF frequency, and process latitude, the capacitors in this schematic diagram can be chosen to match the voltage requirements at each zone based on known RF phase and matching requirements. Thereby, the capacitor values are chosen to tailor the fields as desired to achieve plasma processing uniformity.

20 FIG. 2 illustrates another embodiment of the invention wherein an electrode is segmented into a plurality of concentric annular rings. FIG. 2 illustrates the electrode 4 segmented into first, second, and third concentric annular rings 4a, 4b, and 4c for allowing independent RF bias power zones which control the center-to-edge surface uniformity of the wafer. In this 25 embodiment, the electrode 4 is segmented into three zones. However, any number of concentric annular rings may be used for separating the electrode into zones in order to achieve the desired surface uniformity. The power source 16 may be connected to a power splitter 26 as illustrated in FIG. 2 for controlling the energy applied to each of the zones. Also, FIG. 2 illustrates a 30 DC bias source 28 connected to the concentric annular rings of the electrode for providing electrostatic clamping of the wafer. In addition, the annular zoned

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electrode controls the power applied to the surface of the wafer so that a symmetrical center-to-edge plasma processing is produced. The RF power and the DC bias delivered to each concentric annular ring of the first electrode 6 can be achieved in a conventional manner by a passive network in conjunction 5 with RF generators and high voltage power supplies.

In another embodiment of the invention the segments of the electrodes can also be driven by a numerically sequenced sine wave combined with a DC offset value as illustrated in FIG. 3. The sequenced sine wave is stored in a ROM 50 and the DC offset value is generated by a voltage source 52 in the 10 embodiment illustrated in FIG. 3. The outputs of the ROM 50 and the voltage generator 52 are summed by a summing circuit 54 and then input to a digital-to-analog converter 56 which outputs an analog signal. The analog signal output from the digital-to-analog converter 56 is low pass filtered by a low pass filter 58 and then the filtered signal output is amplified by a power amplifier 60 15 and applied to the segmented electrodes 4a, 4b, and 4c.

The electrodes may also be segmented into other patterns as desired to achieve processing uniformity requirements, and FIG. 4 illustrates another embodiment where an asymmetrical pattern of segmented electrodes is used. In the embodiment illustrated in FIG. 4, the electrode is segmented into four 20 zones. However, the electrodes can be designed to provide a pattern which compensates for the chamber geometry, gas delivery, or asymmetrical pumping of the plasma processing system.

FIG. 5 illustrates another embodiment of the invention wherein an active mechanism is used to control the power delivered to different zones of 25 electrodes. FIG. 5 illustrates a plurality of current sensors 24 and a plurality of variable capacitors 22 connected to the segmented electrodes. The current sensors 24 provide active control of the variable capacitors 22. This active mechanism is used to control the percentage of power sent to the electrode zones by a feedback loop through the current sensors 24 to the variable 30 capacitors 22.

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FIG. 6 illustrates another embodiment of the invention where two variable capacitors C1 and C2 are used to simultaneously couple RF energy into both poles of an ESC wafer clamping system. This embodiment helps to prevent any phase shift and charge imbalance across the portions of the chuck.

5 FIG. 7 illustrates another embodiment of the invention where a voltage divider circuit and a capacitor network balance and adjust the RF voltage applied to the chuck surface. In this embodiment, a parallel capacitance C_p to the base capacitance is varied to set up the voltage divider. The capacitance value is selected by running uniformity tests on patterned and unpatterned oxide
10 wafers and comparing the numerical data and diameter scans for result verification. Compared to prior art arrangements wherein wafer process uniformity (i.e., center-to-edge) was typically 5%, the power segmented electrode according to the invention provides significant improvement in that wafer process uniformities of 1.5% or even lower can be achieved.

15 The foregoing has described the principles, preferred embodiments and modes of operation of the present invention. However, the invention should not be construed as being limited to the particular embodiments discussed. Thus, the above-described embodiments should be regarded as illustrative rather than restrictive, and it should be appreciated that variations may be made in
20 those embodiments by workers skilled in the art without departing from the scope of the present invention as defined by the following claims.

WHAT IS CLAIMED IS:

1. A power segmented electrode attachable to a plasma reaction chamber and capable of providing uniform processing of a substrate in the plasma reaction chamber, comprising:
 - 5 first and second electrodes, the first electrode being distributed across a first zone and the second electrode being distributed across a second zone; and a capacitive network controlling distribution of radio frequency power in the first and second zones such that plasma coupled to a substrate supported in the plasma reaction chamber provides uniform processing across the substrate.
 - 10 2. The power segmented electrode of Claim 1, wherein the power segmented electrode is incorporated in a substrate support which supports a single semiconductor wafer and the substrate support is an electrostatic chuck located in a plasma etching chamber.
 - 15 3. The power segmented electrode of Claim 1, wherein the first electrode is separated from the second electrode by a gap, the gap being filled with dielectric material and forming an interelectrode capacitor of the capacitive network.
 - 20 4. The power segmented electrode of Claim 1, further comprising a radio frequency power source, first and second capacitors forming part of the capacitive network and an electrical ground, radio frequency power from the power source passing sequentially through the first capacitor, through the first electrode, through the second capacitor, through the second electrode, and to the electrical ground.
 - 25 5. The power segmented electrode of Claim 1, wherein the first and second electrodes form part of a concentric electrode arrangement comprising a plurality of spaced apart annular electrodes, the electrodes being electrically

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connected to a radio frequency power source through variable capacitors forming part of the capacitive network and radio frequency power from the power source sequentially passing through each of the variable capacitors and to a respective one of the electrodes.

5 6. The power segmented electrode of Claim 5, further comprising current sensing mechanisms for automatically adjusting capacitance of a respective one of the variable capacitors such that adjustment signals emitted therefrom compensate for deviations from uniformity of processing of the substrate in an annular zone of the substrate facing a respective one of the
10 annular electrodes.

7. The power segmented electrode of Claim 1, wherein the capacitive network comprises first and second capacitors, the first capacitor being connected to the first electrode and the second capacitor being connected to the second electrode, the first and second capacitors being electrically connected in
15 parallel to a radio frequency power source.

8. The power segmented electrode of Claim 1, further comprising a third electrode, the first electrode surrounding the second electrode and the second electrode surrounding the third electrode, each of the electrodes being electrically connected to a radio frequency power source, radio frequency
20 power from the power source passing sequentially through a power splitter and to a respective one of the electrodes.

9. The power segmented electrode of Claim 1, wherein the power segmented electrode is incorporated in an electrostatic chuck, the first and second electrodes being electrically connected to direct current biasing sources
25 which allow the chuck to electrostatically clamp a substrate on the chuck.

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10. The power segmented electrode of Claim 1, further comprising a source of radio frequency power supplied in phase or out of phase to the first and second electrodes.
11. The power segmented electrode of Claim 1, further comprising:
 - 5 a sine wave generator for generating a numerically sequenced sine wave;
 - a biasing unit for generating a DC offset value;
 - a summation unit for summing the numerically sequenced sine wave and the DC offset value;
 - a digital/analog converter for converting the signal output from the 10 summation unit to an analog summation signal;
 - a low pass filter for filtering predetermined low frequency portions of the analog summation signal; and
 - 15 a power amplifier for amplifying the analog summation signal filtered by the low pass filter and driving the first and second electrodes with the amplified signal.
12. The power segmented electrode of Claim 1, wherein the first electrode surrounds the second electrode and power is supplied to the first and second electrodes by sequentially passing through the first electrode, an interelectrode capacitor formed by a dielectric material disposed in a gap between the first and second electrodes, the second electrode, a series of capacitors forming part of the capacitive network and an electrical ground, the dielectric material providing the interelectrode capacitance to be less than that of the series of capacitors.
13. The power segmented electrode of Claim 1, further comprising a 25 voltage divider circuit electrically connected to the first electrode or the second electrode.

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14. The power segmented electrode of Claim 1, wherein the first electrode is driven by a first active power driver and the second electrode is driven by a second active power driver, the first and second power drivers being operated independently of each other.

5 15. A plasma processing system comprising:

a substrate support for clamping a substrate in a plasma reaction chamber of the plasma processing system, the substrate support including a plurality of electrodes associated with zones of the substrate support adjacent to the substrate; and

10 a power controller for controlling power supplied to the zones of the substrate support through the plurality of electrodes so that uniform processing is applied across an entire a surface of the substrate.

15 16. The plasma processing system according to Claim 15, wherein the power controller includes a capacitive network connected to the plurality of electrodes for distributing power to the zones of the substrate chuck.

17. The plasma processing system according to Claim 16, wherein adjacent ones of the plurality of electrodes are separated by gaps, and each of the gaps are filled with dielectric material to form interelectrode capacitors of the capacitive network and the plurality of electrodes are provided in a pattern 20 which compensates for process gas flow in the reaction chamber and provide uniform processing of the substrate.

18. A method for processing substrates in a plasma processing system, comprising the steps of:
25 (a) clamping a substrate to a substrate support in a plasma reaction chamber;

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(b) generating plasma in the plasma reaction chamber with a power segmented electrode having a plurality of electrodes associated with zones of the substrate; and

5 (c) controlling distribution of power supplied to the electrodes so that uniform processing is applied across a surface of the substrate to be processed.

19. The method according to Claim 18, wherein step (c) distributes the power to the zones of the substrate by a capacitive network connected to the plurality of electrodes.

10 20. The method according to Claim 18, wherein the plurality of electrodes are provided in a pattern which compensates for process gas flow in the reaction chamber and provide uniform processing a uniform surface of the substrate.

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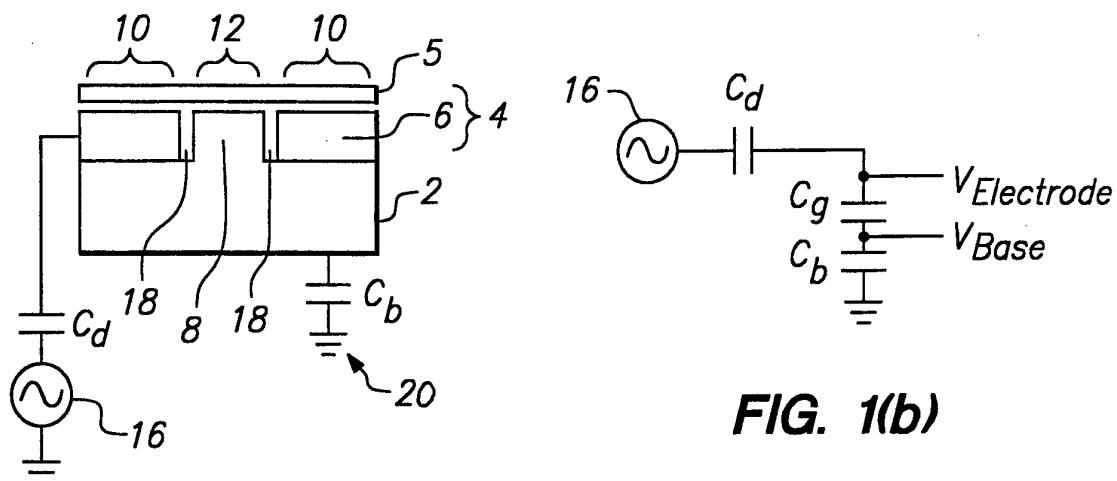
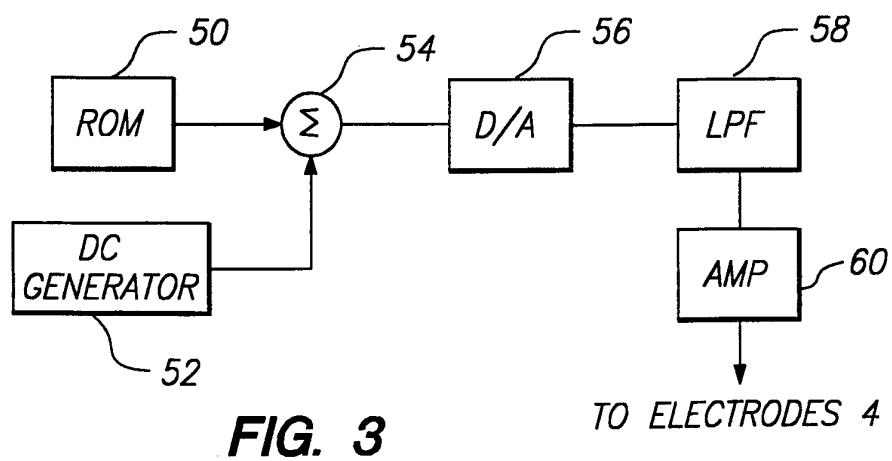
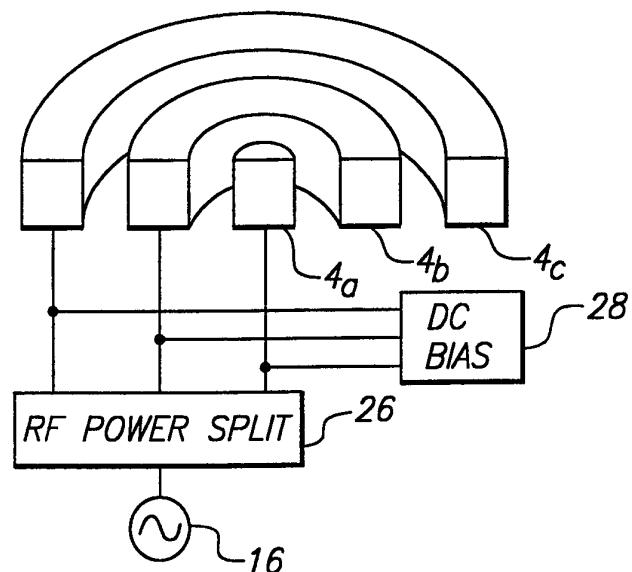


FIG. 1(a)



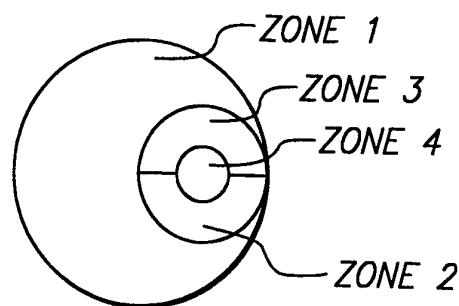


FIG. 4

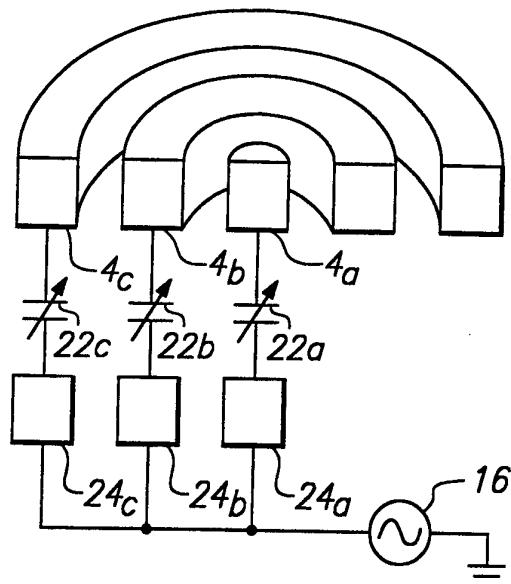


FIG. 5

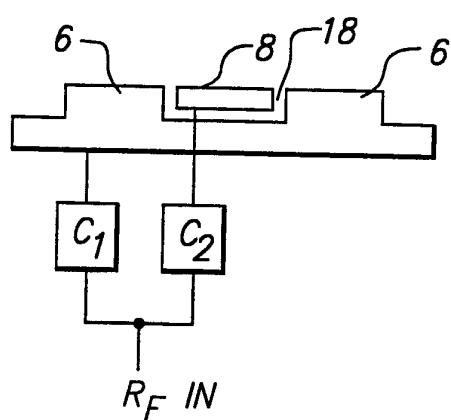


FIG. 6

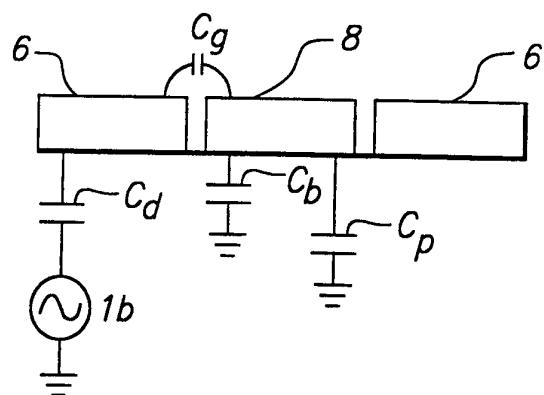


FIG. 7

INTERNATIONAL SEARCH REPORT

International Application No

PCT/US 96/10805

A. CLASSIFICATION OF SUBJECT MATTER

IPC 6 H01J37/32

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

IPC 6 H01J

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	EP,A,0 280 074 (IBM) 31 August 1988 see column 4, line 18 - column 5, line 15; figures --- IBM TECHNICAL DISCLOSURE BULLETIN, vol. 28, no. 1, June 1985, NEW YORK, US, pages 259-260, XP002014972 ANONYMOUS: "Electrode Arrangement for Plasma Etching" see the whole document --- DE,C,44 43 608 (SIEMENS AG) 21 March 1996 see page 4, line 51 - page 5, line 25; figure 4 --- -/-	1,3,5,8, 10,18,20 1,18 1,3,5-8, 18-20
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 Further documents are listed in the continuation of box C. Patent family members are listed in annex.

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Date of the actual completion of the international search

2 October 1996

Date of mailing of the international search report

14.10.96

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Schaub, G

INTERNATIONAL SEARCH REPORT

International Application No
PCT/US 96/10805

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	EP,A,0 578 011 (TEXAS INSTRUMENTS INC) 12 January 1994 see page 8, line 50 - page 9, line 1; figure 9 -----	1,18

INTERNATIONAL SEARCH REPORT

Information on patent family members

International Application No

PCT/US 96/10805

Patent document cited in search report	Publication date	Patent family member(s)		Publication date
EP-A-0280074	31-08-88	DE-D-	3854792	01-02-96
		JP-A-	63248130	14-10-88
		US-A-	4885074	05-12-89
DE-C-4443608	21-03-96	WO-A-	9618207	13-06-96
EP-A-0578011	12-01-94	US-A-	5286297	15-02-94
		JP-A-	6084812	25-03-94
		US-A-	5464499	07-11-95