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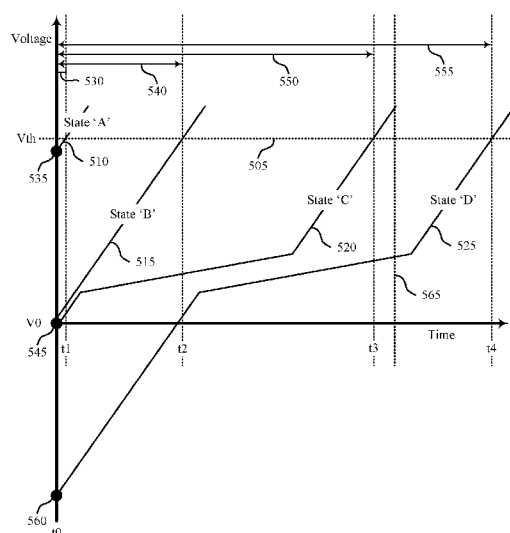


FIG. 5

(57) Abstract: Techniques, systems, and devices for time-resolved access of memory cells in a memory array are described herein. During a sense portion of a read operation, a selected memory cell may be charged to a predetermined voltage level. A logic state stored on the selected memory cell may be identified based on a duration between the beginning of the charging and when selected memory cell reaches the predetermined voltage level. In some examples, time-varying signals may be used to indicate the logic state based on the duration of the charging. In some examples, the duration of the charging may be based on a polarization state of the selected memory cell, a dielectric charge state of the selected state, or both a polarization state and a dielectric charge state of the selected memory cell.



TIME-BASED ACCESS OF A MEMORY CELL

CROSS REFERENCES

[0001] The present Application for Patent claims priority to U.S. Patent Application No. 15/619,163 by Di Vincenzo, entitled “Time-Based Access of a Memory Cell,” filed June 9, 2017, which is related to co-pending U.S. Patent Application Number 15/619,158 by Di Vincenzo, entitled “Time-Based Access of a Memory Cell,” filed June 9, 2017, assigned to the assignee hereof, each of which is expressly incorporated by reference herein.

BACKGROUND

[0002] The following relates generally to time-based access of a memory cell and more specifically to time-based sensing of a logic state of the memory cell.

[0003] Memory devices are widely used to store information in various electronic devices such as computers, wireless communication devices, cameras, digital displays, and the like. Information is stored by programing different states of a memory device. For example, binary devices have two states, often denoted by a logic “1” or a logic “0.” In other systems, more than two states may be stored. To access the stored information, a component of the electronic device may read, or sense, the stored state in the memory device. To store information, a component of the electronic device may write, or program, the state in the memory device.

[0004] Various types of memory devices exist, including magnetic hard disks, random access memory (RAM), read only memory (ROM), dynamic RAM (DRAM), synchronous dynamic RAM (SDRAM), ferroelectric RAM (FeRAM), magnetic RAM (MRAM), resistive RAM (RRAM), flash memory, phase change memory (PCM), and others. Memory devices may be volatile or non-volatile. Non-volatile memory, *e.g.*, FeRAM, may maintain their stored logic state for extended periods of time even in the absence of an external power source. Volatile memory devices, *e.g.*, DRAM, may lose their stored state over time unless they are periodically refreshed by an external power source. FeRAM may use similar device architectures as volatile memory but may have non-volatile properties due to the use of a ferroelectric capacitor as a storage device. FeRAM devices may thus have improved performance compared to other non-volatile and volatile memory devices.

[0005] Improving memory devices, generally, may include increasing memory cell density, increasing read/write speeds, increasing reliability, increasing data retention, reducing power consumption, or reducing manufacturing costs, among other metrics.

BRIEF DESCRIPTION OF THE DRAWINGS

- 5 [0006] FIG. 1 illustrates an example of a memory array that supports time-based access of a memory cell in accordance with embodiments of the present disclosure.
- [0007] FIG. 2 illustrates an example of a circuit that supports time-based access of a memory cell in accordance with embodiments of the present disclosure.
- [0008] FIG. 3 illustrates an example of hysteresis curves that support time-based access
10 of a memory cell in accordance with embodiments of the present disclosure.
- [0009] FIG. 4 illustrates an example of state diagrams that support time-based access of a memory cell in accordance with embodiments of the present disclosure.
- [0010] FIG. 5 illustrates an example of a timing diagram that supports time-based access of a memory cell in accordance with embodiments of the present disclosure.
- 15 [0011] FIG. 6 illustrates an example of a circuit that supports time-based access of a memory cell in accordance with embodiments of the present disclosure.
- [0012] FIG. 7 illustrates an example of a timing diagram that supports time-based access of a memory cell in accordance with embodiments of the present disclosure.
- [0013] FIG. 8 illustrates an example of a timing diagram that supports time-based access
20 of a memory cell in accordance with embodiments of the present disclosure.
- [0014] FIG. 9 illustrates an example of a timing diagram that supports time-based access of a memory cell in accordance with embodiments of the present disclosure.
- [0015] FIGs. 10 through 11 show block diagrams of a device that supports time-based access of a memory cell in accordance with embodiments of the present disclosure.
- 25 [0016] FIG. 12 illustrates a block diagram of a system including a memory controller that supports time-based access of a memory cell in accordance with embodiments of the present disclosure.

[0017] FIGs. 13 through 15 illustrate methods for time-based access of a memory cell in accordance with embodiments of the present disclosure.

DETAILED DESCRIPTION

[0018] Memory devices generally use voltages to distinguish between logic states stored on memory cells. For example, during a read operation of a memory cell, a memory controller may cause the memory cell to discharge a charge or a voltage onto an access line. The memory controller may identify the logic state stored on the memory cell based on a comparison between the voltage of the access line and a reference voltage. In some examples, using voltage levels to distinguish between logic states of memory cells may limit how many unique logic states may be stored on a memory cell.

[0019] Techniques, systems, and devices for time-resolved access of memory cells in a memory array are described herein. During a sense portion of a read operation, a selected memory cell may be charged to a predetermined voltage level. A logic state stored on the selected memory cell may be identified based on a duration between the beginning of the charging and when selected memory cell reaches the predetermined voltage level. In some examples, time-varying signals may be used to indicate the logic state based on the duration of the charging. In some examples, the duration of the charging may be based on a polarization state of the selected memory cell, a dielectric charge state of the selected state, or both a polarization state and a dielectric charge state of the selected memory cell.

[0020] A number of advantages may be realized using time-based sensing techniques during a read operation. In some examples, logic states may be distinguishable using time-based techniques that are not distinguishable using voltage-based techniques. In some examples, a pre-existing memory cell may be configured to store more logic states than is possible using voltage-based sensing techniques. Additional advantages of the techniques, systems, and devices described herein may be apparent based on the features described below.

[0021] Features of the disclosure introduced above are further described below in the context of FIGs. 1-12. These and other features of the disclosure are further illustrated by and described with reference to apparatus diagrams, system diagrams, and flowcharts that relate to time-based access of a memory cell.

[0022] FIG. 1 illustrates an example memory array 100 in accordance with various embodiments of the present disclosure. Memory array 100 may also be referred to as an electronic memory apparatus. Memory array 100 includes memory cells 105 that are programmable to store different states. Each memory cell 105 may be programmable to store two states, denoted as a logic 0 and a logic 1. In some cases, memory cell 105 is configured to store more than two logic states. A memory cell 105 may store a charge representative of the programmable states in a capacitor; for example, a charged and uncharged capacitor may represent two logic states, respectively. DRAM architectures may commonly use such a design, and the capacitor employed may include a dielectric material with linear or para-electric electric polarization properties as the insulator. By contrast, a ferroelectric memory cell may include a capacitor with a ferroelectric as the insulating material. Different levels of charge of a ferroelectric capacitor may represent different logic states. Ferroelectric materials have non-linear polarization properties; some details and advantages of a ferroelectric memory cell 105 are discussed below.

[0023] Operations such as reading and writing may be performed on memory cells 105 by activating or selecting access line 110 and digit line 115. Access lines 110 may also be known as word lines 110, and bit lines 115 may also be known digit lines 115. References to word lines and bit lines, or their analogues, are interchangeable without loss of understanding or operation. Activating or selecting a word line 110 or a digit line 115 may include applying a voltage to the respective line. Word lines 110 and digit lines 115 may be made of conductive materials such as metals (*e.g.*, copper (Cu), aluminum (Al), gold (Au), tungsten (W), *etc.*), metal alloys, carbon, conductively-doped semiconductors, or other conductive materials, alloys, compounds, or the like. In some examples, other lines (*e.g.*, plates lines – not shown in FIG. 1) also may be present.

[0024] According to the example of FIG. 1, each row of memory cells 105 is connected to a single word line 110, and each column of memory cells 105 is connected to a single digit line 115. By activating one word line 110 and one digit line 115 (*e.g.*, applying a voltage to the word line 110 or digit line 115), a single memory cell 105 may be accessed at their intersection. Accessing the memory cell 105 may include reading or writing the memory cell 105. The intersection of a word line 110 and digit line 115 may be referred to as an address of a memory cell. In some instances, the read operation of a memory cell 105 may be time-based. Meaning, the logic state of the memory cell 105 may be determined based on a duration to satisfy a condition rather than a voltage level satisfying a condition or a threshold.

For example, the memory controller 140 may determine the logic state of a memory cell 105 based on a duration it takes for the digit line to be charged to a predetermined voltage. In some examples, the memory cells 105 may be configured as a volatile memory cell, a non-volatile memory cell, or a partly volatile and partly non-volatile memory cell.

5 [0025] In some architectures, the logic storing device of a cell, *e.g.*, a capacitor, may be electrically isolated from the digit line by a selection component. The word line 110 may be connected to and may control the selection component. For example, the selection component may be a transistor and the word line 110 may be connected to the gate of the transistor. Activating the word line 110 results in an electrical connection or closed circuit between the
10 capacitor of a memory cell 105 and its corresponding digit line 115. The digit line may then be accessed to either read or write the memory cell 105.

[0026] Accessing memory cells 105 may be controlled through a row decoder 120 and a column decoder 130. For example, a row decoder 120 may receive a row address from the memory controller 140 and activate the appropriate word line 110 based on the received row
15 address. Similarly, a column decoder 130 receives a column address from the memory controller 140 and activates the appropriate digit line 115. For example, memory array 100 may include multiple word lines 110, labeled WL_1 through WL_M, and multiple digit lines 115, labeled DL_1 through DL_N, where M and N depend on the array size. Thus, by activating a word line 110 and a digit line 115, *e.g.*, WL_2 and DL_3, the memory cell 105 at
20 their intersection may be accessed.

[0027] Upon accessing, a memory cell 105 may be read, or sensed, by sense component 125 to determine the stored state of the memory cell 105. For example, after accessing the memory cell 105, the ferroelectric capacitor of memory cell 105 may discharge onto its corresponding digit line 115. Discharging the ferroelectric capacitor may result from biasing,
25 or applying a voltage, to the ferroelectric capacitor. The discharging may cause a change in the voltage of the digit line 115, which sense component 125 may compare to a reference voltage (not shown) in order to determine the stored state of the memory cell 105. For example, if digit line 115 has a higher voltage than the reference voltage, then sense component 125 may determine that the stored state in memory cell 105 was a logic 1 and vice
30 versa. Sense component 125 may include various transistors or amplifiers in order to detect and amplify a difference in the signals, which may be referred to as latching. The detected logic state of memory cell 105 may then be output through column decoder 130 as output

135. In some cases, sense component 125 may be part of a column decoder 130 or row decoder 120. Or, sense component 125 may be connected to or in electronic communication with column decoder 130 or row decoder 120. In some instances, the sense component 125 may be configured to activate a latch based on the duration for the digit line to be charged to the predetermined voltage. The logic state of the associated memory cell may be determined based on a value of a time-varying signal at the time the latch is activated. In some examples, the sense component 125 may include a decoder system 145. During an access operation (e.g., a read operation or a write operation), a plurality of digit lines 115 may be selected. The decoder system 145 may be configured to coordinate an access operation when multiple digit lines 115 are selected as part the access operation. In some instances, a pre-decoding system (not shown) may be positioned between the digit lines 115 and the sense component 125 to perform similar functions as the decoder system 145.

[0028] A memory cell 105 may be set, or written, by similarly activating the relevant word line 110 and digit line 115—i.e., a logic value may be stored in the memory cell 105.

Column decoder 130 or row decoder 120 may accept data, for example input/output 135, to be written to the memory cells 105. A ferroelectric memory cell 105 may be written by applying a voltage across the ferroelectric capacitor. This process is discussed in more detail below. In some instances, the memory cell 105 may be configured to store more than two logic states. For example, a ferroelectric memory cell may be configured to store at least three states by storing both a polarization state and a dielectric charge state. Using both of those states at least one of three logic states of the ferroelectric memory cell may be determined. In some cases, the polarization state and the dielectric charge state of the ferroelectric memory cell may be used to identify four or more logic states that may be stored on the memory cell. For example, the ferroelectric memory cell may be configured to store a plurality of polarization states and a plurality dielectric charge states. Various combinations of the polarization states and the dielectric charge states may define a plurality of logic states of the ferroelectric memory cell. In other examples, a dielectric memory cell may be configured to store a plurality of different dielectric charge states and thereby define more than two logic states. In other examples, a ferroelectric memory cell may be configured to store a plurality of different polarization states and thereby define more than two logic states.

[0029] In some memory architectures, accessing the memory cell 105 may degrade or destroy the stored logic state and re-write or refresh operations may be performed to return the original logic state to memory cell 105. In DRAM, for example, the capacitor may be

partially or completely discharged during a sense operation, corrupting the stored logic state. So the logic state may be re-written after a sense operation. Additionally, activating a single word line 110 may result in the discharge of all memory cells in the row; thus, several or all memory cells 105 in the row may need to be re-written. In some instances, a ferroelectric
5 memory cell may be configured to store both polarization states and dielectric charge states. As such, access operations, such as write operations, may be modified to store both a polarization state and a dielectric charge state on the ferroelectric memory cell.

[0030] Some memory architectures, including DRAM, may lose their stored state over time unless they are periodically refreshed by an external power source. For example, a
10 charged capacitor may become discharged over time through leakage currents, resulting in the loss of the stored information. The refresh rate of these so-called volatile memory devices may be relatively high, *e.g.*, tens of refresh operations per second for DRAM arrays, which may result in significant power consumption. With increasingly larger memory arrays, increased power consumption may inhibit the deployment or operation of memory arrays
15 (*e.g.*, power supplies, heat generation, material limits, *etc.*), especially for mobile devices that rely on a finite power source, such as a battery. As discussed below, ferroelectric memory cells 105 may have beneficial properties that may result in improved performance relative to other memory architectures.

[0031] The memory controller 140 may control the operation (*e.g.*, read, write, re-write, refresh, discharge, *etc.*) of memory cells 105 through the various components, for example, row decoder 120, column decoder 130, and sense component 125. In some cases, one or more of the row decoder 120, column decoder 130, and sense component 125 may be co-located with the memory controller 140. Memory controller 140 may generate row and column address signals in order to activate the desired word line 110 and digit line 115. Memory
20 controller 140 may also generate and control various voltages or currents used during the operation of memory array 100. For example, it may apply discharge voltages to a word line 110 or digit line 115 after accessing one or more memory cells 105. In general, the amplitude, shape, or duration of an applied voltage or current discussed herein may be adjusted or varied and may be different for the various operations discussed in operating memory array 100.
25
30 Furthermore, one, multiple, or all memory cells 105 within memory array 100 may be accessed simultaneously; for example, multiple or all cells of memory array 100 may be accessed simultaneously during a reset operation in which all memory cells 105, or a group of memory cells 105, are set to a single logic state. As is discussed in more detail below, access

operations (*e.g.*, read operation or write operation) performed by the memory controller 140 may be modified to account for time-based sensing and/or multiple logic states being stored on a memory cell 105.

[0032] FIG. 2 illustrates an example circuit 200 in accordance with various embodiments of the present disclosure. Circuit 200 includes a memory cell 105-a, word line 110-a, digit line 115-a, and sense component 125-a, which may be examples of a memory cell 105, word line 110, digit line 115, and sense component 125, respectively, as described with reference to FIG. 1. Memory cell 105-a may include a logic storage component, such as capacitor 205 that has a first plate, cell plate 230, and a second plate, cell bottom 215. Cell plate 230 and cell bottom 215 may be capacitively coupled through a ferroelectric material positioned between them. The orientation of cell plate 230 and cell bottom 215 may be flipped without changing the operation of memory cell 105-a. Circuit 200 also includes selection component 220 and reference line 225. Cell plate 230 may be accessed via plate line 210 and cell bottom 215 may be accessed via digit line 115-a. As described above, various states may be stored by charging or discharging capacitor 205. In some cases, the cell bottom 215 (or the cell plate 230 as the case may be) may cooperate with the selection component 220 to form a middle electrode 235. In some instances, the middle electrode 235 may store a charge. In some examples, the charge stored on the middle electrode 235 may contribute, at least in part, to the dielectric charge state of the memory cell 105-a.

[0033] The stored state of capacitor 205 may be read or sensed by operating various elements represented in circuit 200. Capacitor 205 may be in electronic communication with digit line 115-a. For example, capacitor 205 can be isolated from digit line 115-a when selection component 220 is deactivated, and capacitor 205 can be connected to digit line 115-a when selection component 220 is activated. Activating selection component 220 may be referred to as selecting memory cell 105-a. In some cases, selection component 220 is a transistor and its operation is controlled by applying a voltage to the transistor gate, where the voltage magnitude is greater than the threshold magnitude of the transistor. Word line 110-a may activate selection component 220; for example, a voltage applied to word line 110-a is applied to the transistor gate, connecting capacitor 205 with digit line 115-a. As discussed in more detail below, the logic state of a memory cell 105-a may be determined based on duration of time to charge the memory cell 105. Such a time-resolved sensing may enable the memory cell 105 to store additional logic states as compared to voltage-resolved sensing.

[0034] In other examples, the positions of selection component 220 and capacitor 205 may be switched, such that selection component 220 is connected between plate line 210 and cell plate 230 and such that capacitor 205 is between digit line 115-a and the other terminal of selection component 220. In this embodiment, selection component 220 may remain in electronic communication with digit line 115-a through capacitor 205. This configuration may be associated with alternative timing and biasing for read and write operations.

[0035] Due to the ferroelectric material between the plates of capacitor 205, and as discussed in more detail below, capacitor 205 may not discharge upon connection to digit line 115-a. In one scheme, to sense the logic state stored by ferroelectric capacitor 205, word line 110-a may be biased to select memory cell 105-a and a voltage may be applied to plate line 210. In some cases, digit line 115-a is virtually grounded and then isolated from the virtual ground, which may be referred to as “floating,” prior to biasing plate line 210 and word line 110-a. Biasing plate line 210 may result in a voltage difference (*e.g.*, plate line 210 voltage minus digit line 115-a voltage) across capacitor 205. The voltage difference may yield a change in the stored charge on capacitor 205, where the magnitude of the change in stored charge may depend on the initial state of capacitor 205—*e.g.*, whether the initial state stored a logic 1 or a logic 0. This may cause a change in the voltage of digit line 115-a based on the charge stored on capacitor 205. Operation of memory cell 105-a by varying the voltage to cell plate 230 may be referred to as “moving cell plate.” In some instances, the digit line 115-a may be charged to a predetermined voltage level during a read operation. A duration to perform such charging may be based on the logic state stored on the memory cell 105-a.

[0036] The change in voltage of digit line 115-a may depend on its intrinsic capacitance. That is, as charge flows through digit line 115-a, some finite charge may be stored in digit line 115-a and the resulting voltage depends on the intrinsic capacitance. The intrinsic capacitance may depend on physical characteristics, including the dimensions, of digit line 115-a. Digit line 115-a may connect many memory cells 105 so digit line 115-a may have a length that results in a non-negligible capacitance (*e.g.*, on the order of picofarads (pF)). The resulting voltage of digit line 115-a may then be compared to a reference (*e.g.*, a voltage of reference line 225) by sense component 125-a in order to determine the stored logic state in memory cell 105-a. Other sensing processes may be used. In some examples, determination of the stored logic state may be based, at least in part, on a duration of time to charge the digit line to a voltage level.

[0037] Sense component 125-a may include various transistors or amplifiers to detect and amplify a difference in signals, which may be referred to as latching. Sense component 125-a may include a sense amplifier that receives and compares the voltage of digit line 115-a and reference line 225, which may be a reference voltage. The sense amplifier output may be driven to the higher (*e.g.*, a positive) or lower (*e.g.*, negative or ground) supply voltage based on the comparison. For instance, if digit line 115-a has a higher voltage than reference line 225, then the sense amplifier output may be driven to a positive supply voltage. In some cases, the sense amplifier may additionally drive digit line 115-a to the supply voltage. Sense component 125-a may then latch the output of the sense amplifier and/or the voltage of digit line 115-a, which may be used to determine the stored state in memory cell 105-a, *e.g.*, logic 1. Alternatively, if digit line 115-a has a lower voltage than reference line 225, the sense amplifier output may be driven to a negative or ground voltage. Sense component 125-a may similarly latch the sense amplifier output to determine the stored state in memory cell 105-a, *e.g.*, logic 0. In some examples, determination of the state stored in the memory cell may depend, at least in part, on a duration of time to charge to a voltage level. The latched logic state of memory cell 105-a may then be output, for example, through column decoder 130 as output 135 with reference to FIG. 1. In some instances, the sense component 125-a may be configured to determine when the digit line 115-a is charged to a predetermined voltage level. In some examples, the sense component 125-a may activate a latch based on determining that the digit line has been charged to the predetermined voltage level. A logic state of the memory cell 105-a may be based on a value of a time-varying signal of the latch at the time the latch is activated.

[0038] To write memory cell 105-a, a voltage may be applied across capacitor 205. Various methods may be used. In one example, selection component 220 may be activated through word line 110-a in order to electrically connect capacitor 205 to digit line 115-a. A voltage may be applied across capacitor 205 by controlling the voltage of cell plate 230 (through plate line 210) and cell bottom 215 (through digit line 115-a). To write a logic 0, cell plate 230 may be taken high, that is, a positive voltage may be applied to plate line 210, and cell bottom 215 may be taken low, *e.g.*, virtually grounding or applying a negative voltage to digit line 115-a. The opposite process is performed to write a logic 1, where cell plate 230 is taken low and cell bottom 215 is taken high. In some examples, the write procedure may be modified to account for multiple bits being stored in a single memory cell.

[0039] FIG. 3 illustrates an example of non-linear electrical properties with hysteresis curves 300-a and 300-b for a ferroelectric memory cell that is operated in accordance with various embodiments of the present disclosure. Hysteresis curves 300-a and 300-b illustrate an example ferroelectric memory cell writing and reading process, respectively. Hysteresis curves 300-a and 300-b depict the charge, Q , stored on a ferroelectric capacitor (*e.g.*, capacitor 205 of FIG. 2) as a function of a voltage difference, V .

[0040] A ferroelectric material is characterized by a spontaneous electric polarization, *i.e.*, it maintains a non-zero electric polarization in the absence of an electric field. Example ferroelectric materials include barium titanate (BaTiO_3), lead titanate (PbTiO_3), lead zirconium titanate (PZT), and strontium bismuth tantalate (SBT). The ferroelectric capacitors described herein may include these or other ferroelectric materials. Electric polarization within a ferroelectric capacitor results in a net charge at the ferroelectric material's surface and attracts opposite charge through the capacitor terminals. Thus, charge is stored at the interface of the ferroelectric material and the capacitor terminals. Because the electric polarization may be maintained in the absence of an externally applied electric field for relatively long times, even indefinitely, charge leakage may be significantly decreased as compared with, for example, capacitors employed in DRAM arrays. This may reduce the need to perform refresh operations as described above for some DRAM architectures.

[0041] Hysteresis curves 300-a and 300-b may be understood from the perspective of a single terminal of a capacitor. By way of example, if the ferroelectric material has a negative polarization, positive charge accumulates at the terminal. Likewise, if the ferroelectric material has a positive polarization, negative charge accumulates at the terminal. Additionally, it should be understood that the voltages in hysteresis curves 300-a and 300-b represent a voltage difference across the capacitor and are directional. For example, a positive voltage may be realized by applying a positive voltage to the terminal in question (*e.g.*, a cell plate 230) and maintaining the second terminal (*e.g.*, a cell bottom 215) at ground (or approximately zero volts (0V)). A negative voltage may be applied by maintaining the terminal in question at ground and applying a positive voltage to the second terminal—*i.e.*, positive voltages may be applied to negatively polarize the terminal in question. Similarly, two positive voltages, two negative voltages, or any combination of positive and negative voltages may be applied to the appropriate capacitor terminals to generate the voltage difference shown in hysteresis curves 300-a and 300-b.

[0042] As depicted in hysteresis curve 300-a, the ferroelectric material may maintain a positive or negative polarization with a zero voltage difference, resulting, in some cases, in two possible memory states: memory state 305 (State B) and memory state 310 (State C). According to the example of FIG. 3, memory state 305 (State B) represents a logic 0 and memory state 310 (State C) represents a logic 1. In some examples, the logic values of the respective memory states may be reversed to accommodate other schemes for operating a memory cell.

[0043] A logic 0 or 1 may be written to the memory cell by controlling the electric polarization of the ferroelectric material by applying voltage. For example, applying a net positive biasing voltage 315 across the capacitor results in charge accumulation until a memory state 340 (State A) is reached. Upon removing the biasing voltage 315, the memory state 340 (State A) follows path 320 until it reaches the memory state 305 (State B) at zero voltage. Similarly, memory state 310 (State C) is written by applying a net negative biasing voltage 325, which results in a memory state 345 (State D). After removing negative voltage 325, memory state 345 (State D) follows path 330 until it reaches memory state 310 (State C) at zero voltage. Memory states 340 (State A) and 345 (State D) may also be referred to as the remnant polarization (P_r) values, *i.e.*, the polarization (or charge) that remains upon removing the external bias (*e.g.*, voltage). The coercive voltage is the voltage at which the charge (or polarization) is zero.

[0044] To read, or sense, the stored state of the ferroelectric capacitor, a voltage may be applied across the capacitor. In response, the stored charge, Q , changes, and the degree of the change depends on the initial charge state — *i.e.*, the final stored charge (Q) depends on whether memory state 305-a or 310-a was initially stored. For example, hysteresis curve 300-b illustrates two possible stored memory states 305-a and 310-a. Biasing voltage 335 may be applied across the capacitor as discussed with reference to FIG. 2. In other cases, a fixed voltage may be applied to the cell plate and, although depicted as a positive voltage, the biasing voltage 335 may be negative. In response to the biasing voltage 335, the memory state 305-a may follow path 350. Likewise, if memory state 310-a was initially stored, then it follows path 355. The final position of memory state 360 and memory state 365 depend on a number of factors, including the specific sensing scheme and circuitry.

[0045] In some cases, the final memory state may depend on the intrinsic capacitance of the digit line connected to the memory cell. For example, if the capacitor is electrically

connected to the digit line and voltage 335 is applied, the voltage of the digit line may rise due to its intrinsic capacitance. So a voltage measured at a sense component may not equal voltage 335 and instead may depend on the voltage of the digit line. The position of final memory states 360 and 365 on hysteresis curve 300-b may thus depend on the capacitance of the digit line and may be determined through a load-line analysis—*i.e.*, memory states 360 and 365 may be defined with respect to the digit line capacitance. As a result, the voltage of the capacitor, voltage 370 or voltage 375, may be different and may depend on the initial state of the capacitor.

[0046] By comparing the digit line voltage to a reference voltage, the initial state of the capacitor may be determined. The digit line voltage may be the difference between voltage 335 and the final voltage across the capacitor, voltage 370 or voltage 375—*i.e.*, (voltage 335 – voltage 370) or (voltage 335 – voltage 375). A reference voltage may be generated such that its magnitude is between the two possible voltages of the two possible digit line voltages in order to determine the stored logic state—*i.e.*, if the digit line voltage is higher or lower than the reference voltage. For example, the reference voltage may be an average of the two quantities, (voltage 335 – voltage 370) and (voltage 335 – voltage 375). Upon comparison by the sense component, the sensed digit line voltage may be determined to be higher or lower than the reference voltage, and the stored logic value of the ferroelectric memory cell (*i.e.*, a logic 0 or 1) may be determined. In some examples, the access procedures (*e.g.*, read or write) of the memory cell may be modified to account for multiple bits being stored in a single memory cell.

[0047] As discussed above, reading a memory cell that does not use a ferroelectric capacitor may degrade or destroy the stored logic state. A ferroelectric memory cell, however, may maintain the initial logic state after a read operation. For example, if memory state 305-a is stored, the memory state may follow path 350 to memory state 360 during a read operation and, after removing voltage 335, the charge state may return to initial memory state 305-a by following path 350 in the opposite direction.

[0048] In some instances, a ferroelectric memory cell may be configured to maintain more than two memory states. In some examples, to maintain more than two memory states, the ferroelectric memory cell may be configured to store a polarization state (*e.g.*, a stable state) and a dielectric charge state (*e.g.*, a volatile state). The polarization state may be associated with properties of the ferroelectric material (*i.e.*, polarization of the cell) and the

dielectric charge state may be associated with voltage or charge stored on the capacitor. The plurality of logic states of the memory cell may include a plurality of stable states, a plurality of volatile states, or combinations thereof.

[0049] For example, a ferroelectric memory cell may be configured to store four memory states: memory state 305 (State B), memory state 310 (State C), memory state 340 (State A), and memory state 345 (State D). In some examples, a logic value stored in the memory cell may be based on a combination of a polarization state (*e.g.*, stable state) and a dielectric charge (*e.g.*, volatile state). In some examples, the number of logic values that may be stored in a memory cell is based on a number of possible combinations of polarization states and dielectric charge states. The memory state 305 (State B) may be based on the memory cell having a positive polarization state and zero-value for the dielectric charge state. The memory state 310 (State C) may be based on the memory cell having a negative polarization state and zero-value for the dielectric charge state. The memory state 340 (State A) may be based on the memory cell having a positive polarization state and positive non-zero voltage or charge for the dielectric charge state. The memory state 345 (State D) may be based on the memory cell having a negative polarization state and negative non-zero voltage or charge for the dielectric charge state.

[0050] To store both a polarization state and a dielectric charge state on a memory cell, various operations of a memory array may be altered. For example, during a write operation a memory controller may not discharge the middle electrode of the memory cell. In such examples, the memory cell may maintain a non-zero dielectric charge state.

[0051] When a memory cell includes two memory states a single bit of logic may be stored by the memory cell. However, when a memory cell include more than two memory states, additional bits of logic may be stored by the memory cell. For example, if the memory cell includes four memory states, two bits of logic may be stored on memory cell. It should be appreciated that additional memory states may be stored on the memory cell based on different combinations of polarization state values and dielectric charge state values (*e.g.*, memory state 360 and memory state 365).

[0052] FIG. 4 illustrates an example of state diagrams 400 that support time-based access of a memory cell in accordance with various embodiments of the present disclosure. Time-based sensing may be used to identify a plurality of different types of memory states of a memory cell. For example, as shown in state diagram 400-a, a memory cell may include more

than two memory states that are based on polarization. In another example, as shown in the state diagram 400-b, a memory cell may include more than two memory states based on dielectric charges and, in some examples, memory states may be based on both polarization and dielectric charges.

5 **[0053]** State diagram 400-a illustrates memory states for a memory cell that includes that include a plurality of polarization memory states 405. The plurality of polarization memory states 405 may include a first memory state 410, a second memory state 415, a third memory state 420, and a fourth memory state 425. While only four memory states are depicted, a memory cell may include any number of memory states including two memory states, three
10 memory states, four memory states, *etc.* Each of the memory states 410, 415, 420, 425 may be based on a polarization of a ferroelectric memory cell. In some examples, each memory state 410, 415, 420, 425 may include zero dielectric charge. The memory states 410, 415, 420, 425 may be characterized by having a non-zero polarization value and a zero dielectric charge value.

15 **[0054]** To obtain the memory state 410, a biasing voltage may be applied to the ferroelectric memory cell to move the memory cell to point 430 of the hysteresis curve. After the biasing voltage is released, the ferroelectric memory cell may relax back to a zero dielectric charge state at memory state 410. Similarly, the memory state 425 may be obtained by applying a negative biasing voltage to the ferroelectric memory cell. To obtain the
20 memory states 415, 420, the biasing voltages and/or the timings of a write operation may be altered. For example, the memory cell may be biased to a point different from the point 435 on the hysteresis curve, and/or a sequence of negative and positive voltages may be applied. In some examples, the absolute value of the positive and negative voltage may decrease during the sequence of programming pulses. As discussed in more detail with regard to FIG.
25 5, time-based sensing techniques may be configured to distinguish between the memory states 410, 415, 420, 425.

[0055] State diagram 400-b illustrates memory states for a memory cell that include a plurality of dielectric charge memory states 440 and a plurality of combination polarization and dielectric charge memory states 445. The dielectric charge memory states 440 may
30 include a first memory state 450, a second memory state 455, a third memory state 460, and a fourth memory state 465. While only four memory states are depicted, a memory cell may include any number of memory states including two memory states, three memory states,

four memory states, *etc.* Each of the memory states may be based on a dielectric charge of the memory cell. In such examples, memory states with non-zero dielectric charge may have a corresponding voltage stored on the capacitor. In some cases, a linear relationship ($Q=CV$) may exist between charge and voltage. Line 490 represents an example of the linear

5 relationship for dielectric charge states. In some examples, the dielectric charge is stored on a capacitor of the memory cell. In some examples, the dielectric charge is stored on a middle electrode memory cell. In some examples, the dielectric charge is stored on both the capacitor and a middle electrode of a memory cell. In some examples, dielectric charge states may be associated with negative voltage and/or negative charge. Each of the memory states 450, 455,
10 460, 465 may be based on a dielectric charge of a memory cell. In some examples, each memory state 450, 455, 460, 465 may not be polarized. As such, either a dielectric capacitor (*e.g.*, DRAM) or a ferroelectric capacitor may be configured to store the memory states 450, 455, 460, 465. In some examples, a ferroelectric memory cell may be used as a pure DRAM memory cell. In the example depicted in state diagram 440-b, the ferroelectric memory cell
15 may differ from a pure DRAM cell in that a non-zero polarization state is present; however, this difference may be neglected in some examples of multi-level (volatile) storage operations of the memory cell.

[0056] To obtain one of the memory states 450, 455, 460, 465, voltage associated with the particular memory state may be applied to a capacitor of the memory cell. Different
20 voltages may be used to obtain different memory states. In some examples, after applying the voltage associated to a particular memory state, the memory cell may be deselected (*e.g.*, the capacitor may be isolated from the digit line).

[0057] The combination memory states 445 may include a first memory state 470, a second memory state 475, a third memory state 480, and a fourth memory state 485. While
25 only four memory states are depicted, a memory cell may include any number of memory states including two memory states, three memory states, four memory states, *etc.* Each of the memory states may be based on a both a polarization and a dielectric charge of the memory cell. Some memory states either the polarization or the dielectric charge may be a zero value.

[0058] To obtain one of the memory states 470, 475, 480, 485, one or more biasing
30 voltages associated with the particular memory state may be applied to a capacitor of the memory cell. Different biasing voltages and different timings may be used to obtain different memory states. In some examples, after applying the voltage associated to a particular

combined memory state, the memory cell may be deselected (*e.g.*, the capacitor may be isolated from the digit line), so that the capacitor stores the dielectric charge accumulated onto it.

5 [0059] In some examples, the dielectric charge memory states 440 and the combination memory states 445 may be associated with positive biasing voltages. In such examples, a single current generator may be configured to charge a digit line during a time-based read operation. In some examples, the dielectric charge memory states 440 and the combination memory states 445 may be associated with both negative and positive biasing voltages (*e.g.*, memory states 305, 310, 340, 345). In some of those examples, additional components may
10 be used to execute access operations on a memory cell.

[0060] As used herein, a memory state may refer to a state of a memory cell. For example, a memory state may include a polarization and a dielectric charge. As used herein, a logic state may refer to digital logic associated with a memory state of a memory cell. For example, a logic state may include a logical '0,' a logical '1,' a logical '00,' a logical '01,' a
15 logical '10,' a logical '11,' *etc.* Logic states may be mapped to memory states. In some examples, a one-to-one mapping exists between logic states and memory states. As used herein, the term memory state may be used interchangeably with the term logic state. As such, in some examples, a logic state may include a polarization state or a dielectric charge state or combinations thereof.

20 [0061] FIG. 5 illustrates an example of a timing diagram 500 that supports time-based access of a memory cell in accordance with various embodiments of the present disclosure. In some instances, a read operation of a memory cell may distinguish between logic states based on time and durations. For example, after biasing a memory cell 105 and/or its associated digit line 115, a sense component may detect different responses based on the memory state
25 of the memory cell. A logic state stored on a memory cell 105 (or a memory state of the memory cell 105) may be determined by detecting the duration between applying the biasing and when a voltage of the memory cell satisfies a voltage threshold 505.

[0062] The timing diagram 500 is associated with the memory states depicted and described with relation to hysteresis curve 300-a of FIG. 3. As such, the timing diagram 500
30 may be associated with memory states of a ferroelectric memory cell. However, it should be appreciated that other timing diagrams are encompassed by this disclosure based on the

memory states of the memory cell. For example, different timing diagrams may be associated with dielectric memory cells.

[0063] The illustrative timing diagram 500 includes a first response signal 510, a second response signal 515, a third response signal 520, and a fourth response signal 525. Each response signal may be associated with one of the memory states depicted in hysteresis curve 300-a. For example, the first response signal may be associated with a memory cell storing a memory state A (e.g., memory state 340 (State A)). The second response signal 515 may be associated with a memory cell storing a memory state B (e.g., memory state 305 (State B)). The third response signal 520 may be associated with a memory cell storing a memory state C (e.g., memory state 310 (State C)). The fourth response signal 525 may be associated with a memory cell storing a memory state D (e.g., memory state 345 (State D)).

[0064] During a read operation, a power source (e.g., a current generator) may charge the memory cell 105 to a predetermined voltage level. Based on the amount of time taken from the memory cell to reach a voltage threshold 505 associated with the predetermined voltage level, a memory controller 140 may be configured to determine what memory state is stored on the memory cell 105. In some examples, the predetermined voltage level may be the biasing voltage used to obtain the states (e.g., voltage 315). In some examples, the predetermined voltage level may be the dielectric charge voltage associated with the memory state A.

[0065] The duration needed to satisfy the voltage threshold 505 during a read operation may be based on the memory state of the memory cell. At time t_0 , a voltage or a current may be applied to the memory cell to charge the memory cell to the predetermined voltage level. At time t_1 , the first response signal 510 associated with the memory state A of a memory cell satisfies the voltage threshold 505. A duration 530 defined between time t_0 and time t_1 may be the duration used to determine whether the memory cell 105 is in the memory state A. In some examples, the memory state A starts at a positive voltage 535 because of the dielectric charge of the memory cell in the memory state A. In some examples, the predetermined voltage level to which the memory cell is charged is based on the positive voltage 535 associated with the memory state A. In some examples, the voltage threshold 505 is based on the positive voltage 535 associated with the memory state A. In such examples, the duration 530 may be quite small due to this relationship. In some examples, the duration 530 may be zero because the voltage threshold 505 is set to be less than the positive voltage 535.

[0066] When the memory cell is charged to the predetermined positive voltage level, the memory state A of the memory cell may advance along a hysteresis curve following path 350, as shown in hysteresis curve 300-b. Because the memory state A is positioned so close to the predetermined positive voltage level, the duration 530 may be small. In some examples, the duration 530 may be about zero nanoseconds.

[0067] At time t_2 , the second response signal 515 associated with the memory state B of the memory cell 105 may satisfy the voltage threshold 505. A duration 540 defined between time t_0 and time t_2 may be the duration used to determine whether the memory cell 105 is in the memory state B. In some examples, the memory state B starts at a zero voltage 545 because the memory cell storing the memory state B does not include any dielectric charge.

[0068] When the memory cell is charged to the predetermined positive voltage level, the memory state B of the memory cell may advance along a hysteresis curve following path 350, as shown in hysteresis curve 300-b. The duration 540 may be based at least in part on a length of the hysteresis curve the memory state B may travel before reaching the predetermined positive voltage level. In some examples, the duration 540 may be based at least in part on a constant current level used to charge the memory cell.

[0069] At time t_3 , the third response signal 520 associated with the memory state C of the memory cell 105 may satisfy the voltage threshold 505. A duration 550 defined between time t_0 and time t_3 may be the duration used to determine whether the memory cell 105 is in the memory state C. In some examples, the memory state C starts at the zero voltage 545 because the memory cell storing the memory state C does not include any dielectric charge.

[0070] When the memory cell is charged to the predetermined positive voltage level, the memory state C of the memory cell may advance along a hysteresis curve following path 355, as shown in hysteresis curve 300-b. The duration 550 may be based at least in part on a length of the hysteresis curve the memory state C may travel before reaching the predetermined positive voltage level. In some examples, the duration 550 may be based at least in part on a constant current level used to charge the memory cell. In some examples, the starting voltages for both the second response signal 515 and the third response signal 520 are the same but the duration 540 is different than the duration 550. Such a phenomenon may be the result of different polarization states. The memory state C may travel a different path along the hysteresis curve to reach the predetermined voltage level, and as such it may take longer for the digit line 115 to satisfy the voltage threshold 505 (*e.g.*, duration 550 may be

longer than duration 540). In some examples, if the memory cell is in memory state 310 (State C), some of the charge injected in the memory cell may be used to flip its polarization state and some of the charge may be used to charge the memory cell so that more charge (or time) may be used to satisfy the voltage threshold 505 with respond to a memory cell in
5 memory state 305 (State B).

[0071] At time t_4 , the fourth response signal 525 associated with the memory state D of the memory cell 105 may satisfy the voltage threshold 505. A duration 555 defined between time t_0 and time t_4 may be the duration used to determine whether the memory cell 105 is in the memory state D. In some examples, the memory state D starts at a negative voltage 560
10 because the memory cell storing the memory state D does includes a negative dielectric charge.

[0072] When the memory cell is charged to the predetermined positive voltage level, the memory state D of the memory cell may advance along a hysteresis curve following path 355, as shown in hysteresis curve 300-b and continue along the hysteresis curve to the
15 predetermined memory state. The duration 555 may be based at least in part on a length of the hysteresis curve the memory state D may travel before reaching the predetermined positive voltage level. In some examples, the duration 555 may be based at least in part on a constant current level used to charge the memory cell.

[0073] In some instances, a memory controller 140 may be configured to determine the
20 logic state stored on a memory cell 105 after time t_3 . For example, if the voltage threshold 505 has not been satisfied by time t_3 , the memory controller 140 may determine by inference that the memory cell 105 is in a memory state D. To make such inferences, in some examples, a memory controller 140 define a time threshold 565 for a read operation. If the
25 voltage threshold 505 is not satisfied when the time threshold 565 is satisfied, the memory controller 140 may determine (by inference) that the memory cell 105 is in a specific memory state. In the illustrative example of FIG. 5, the time threshold 565 may be set about at time t_3 or shortly after time t_3 and the time threshold 565 may be used to determine (by inference) that the memory cell 105 is in the memory state D. The use of a time threshold 565 may
30 reduce the amount of total time used to perform a read operation. For example, during a read operation, a memory controller 140 may reduce the amount of time it attempts to detect whether the voltage threshold 505 is satisfied based on the time threshold 565.

[0074] In some examples, a response signal (not shown in FIG. 5) may exist for any given memory state (*e.g.*, for any given point in the Q-V diagram representing all possible combinations of polarization states and dielectric charge state of a memory cell). For any given memory state, the response signal may have one or more linear portions associated with dielectric charging (and/or discharging) the memory cell capacitor and one or more other portions (typically with a slower slope) corresponding to a modification of the polarization of the capacitor. The duration of each portion (either dielectric charging or polarization) may be based at least in part on the initial memory state (*e.g.*, on the combination of the polarization and the dielectric charge stored on the capacitor) and/or on the current used to charge the memory cell to the predetermined voltage level.

[0075] FIG. 6 illustrates an example of a circuit 600 that supports time-based access of a memory cell in accordance with various embodiments of the present disclosure. The circuit 600 may be configured to perform time-based access operations (*e.g.*, read operations and write operations).

[0076] The circuit 600 may include a memory cell 602 coupled to a digit line 604 and a plate line 606. The memory cell 602 may include a capacitor 608 and a selection component 610. In some examples, a middle electrode may be defined between the capacitor 608 and the selection component 610. In some examples, the capacitor 608 may be a ferroelectric capacitor. In some examples, the capacitor 608 may be a dielectric capacitor. The selection component 610 may be coupled to an access line 612 (*e.g.*, word line) configured to activate the selection component 610 based on instructions received from a memory controller. The memory cell 602 may be an example of the memory cells described with reference to FIGs. 1-5. The digit line 604 may be an example of the digit lines 115 described with reference to FIGs. 1-5. The plate line 606 may be an example of the plate lines 210 described with reference to FIG. 2. The capacitor 608 may be an example of the capacitor 205 described with reference to FIG. 2. The selection component 610 may be an example of the selection component 220 described with reference to FIG. 2. The access line 612 may be an example of the word line 110 described with reference to FIGs. 1 and 2.

[0077] At a first node 620, the memory cell 602 may couple to the digit line 604. A charging component 622 may be coupled to the digit line 604 at the first node 620. The charging component 622 may be configured to charge the memory cell 602 and/or the digit line 604 to perform a time-based read operation. The charging component 622 may be

coupled to a control line 624. The control line 624 may communicate instructions from the memory controller 140 whether to charge the memory cell 602 or not. The charging component 622 may be activated based on the instructions from the memory controller 140. In some examples, the charging component 622 is current generator. In some examples, the charging component 622 is a cascode. In some examples, the charging component 622 may include one or more transistors.

[0078] An isolation component 626 may be coupled to the charging component 622 at a second node 628 (Node). The isolation component 626 may be configured to selectively couple the second node 628 to a voltage source 630 (V_{pp}) based on instructions received from the memory controller 140 by a control line 632. In some examples, the isolation component 626 may be an example of a transistor or other switching component.

[0079] A sense component 634 may be coupled to charging component 622. In some examples, the sense component 634 may be coupled to the second node 628. As is more described with reference to FIG. 7, the sense component 634 may be configured to detect when the digit line 604 at the first node 620 charges to a predetermined voltage level. The sense component 634 may be configured to detect when a voltage level at the second node 628 satisfies a threshold voltage. In some examples, the sense component 634 may be coupled to the voltage source 630. In some examples, the sense component 634 may be an inverter. In some examples, the sense component 634 may be components or circuitry configured to compare a voltage level of the second node 628 to a voltage threshold (e.g., voltage threshold 505). The sense component 634 may output a signal to a third node 636 based on the voltage level of the second node satisfying the threshold. In some examples, the sense component 634 may sense a voltage level at the second node 628. In some examples, the sense component 634 may be coupled to the digit line 604 at the first node 620.

[0080] A first latch 640 may be coupled to the sense component 634. In some examples, the first latch 640 may be coupled to the third node 636. The first latch 640 may be configured to output the value of the logic state stored on the selected memory cell 602. The first latch 640 may be used as part of a time-based read operation where the value output by the first latch 640 may be based on a duration since the read operation began or since the memory cell 602 began to be charged.

[0081] The first latch 640 may be coupled to a first time-varying signal 642 (the “F1 Signal”) by an access line. The first time-varying signal 642 may be configured to indicate a

logic state of the memory cell 602 based on the duration between beginning to charge the memory cell 602 or the digit line 604 and receiving a signal output from the sense component 634. The signal being output from the sense component 634 may be based on a voltage level satisfying a threshold. The first time-varying signal 642 may be configured to define at least three logic states. In some examples, the first time-varying signal 642 may be configured to define at least two logic states. In some examples, the first time-varying signal 642 may be configured to define at least four logic states, or some cases, more than four logic states.

[0082] In some examples, the memory controller 140 may apply the first time-varying signal 642 to the first latch 640 when the memory cell 602 or digit line 604 begins to be charged by the charging component 622. The first time-varying signal 642 may be a predetermined time-varying signal based on the expected logic states of the memory cell 602. The first time-varying signal 642 may vary in a predetermined manner over a predetermined time interval. In some examples, the first time-varying signal 642 may be received from a memory controller 140.

[0083] The first time-varying signal 642 may define a mapping between memory states of the memory cell 602 and logic states of the memory cell 602. During a read operation, the charging component 622 may charge the memory cell 602. Based on the memory state of the memory cell 602 (*e.g.*, its polarization and/or dielectric charge), it will take a certain time duration for a voltage associated with the memory cell 602 to satisfy a voltage threshold (*e.g.*, voltage threshold 505). The first time-varying signal 642 may be configured to cycle through the possible logic states of the memory cell 602. If the memory cell 602 is in a first memory state A, the first time-varying signal 642 may be configured to represent a first logic state associated with the first memory state A for a subinterval of time. The subinterval of time being associated with an expected duration for the memory cell 602 to charge when the memory state A. The first time-varying signal 642 may define a logic state for each memory state of the memory cell 602 for a subinterval of the total overall interval. For example, the first time-varying signal 642 may include a first subinterval defining a logic state associated with the memory state A. After the first subinterval, the first time-varying signal 642 may include a second subinterval defining a logic state associated with the memory state B. Such a pattern may continue until the memory states/logic states of the memory cell 602 are represented by the first time-varying signal 642. In some examples, the subintervals are substantially equal in duration. However, in other examples, the subintervals may be different durations based on the expected charging durations of the memory cell 602.

[0084] In some examples, a second latch 644 may cooperate with the first latch 640 to define the logic states of the memory cell 602. The second latch 644 may be coupled to the third node 636 and to a second time-varying signal 646 (F2 Signal). The second time-varying signal 646 may cooperate with the first time-varying signal 642 to define the logic states of the memory cell 602. Such an example, is described in more detail with reference to FIG. 8. In some examples, additional latches (not shown in FIG. 6) may be present. The additional latches may cooperate with the first latch and the second latch to define more logic states of the memory cell by dividing the reading time duration in finer granularity time subintervals.

[0085] A controller 660 may be coupled to the first latch 640 by a data line 648 and to the second latch 644 by a data line 650. The controller 660 may be configured to identify the logic state of the memory cell 602 based on the value of the first time-varying signal 642 received from the first latch 640. In some examples, identifying the logic state of the memory cell 602 may be based on both the first time-varying signal 642 and the second time-varying signal 646 received from the second latch 644. The controller 660 may also be configured to execute a write back operation as part of the read operation. In some examples, the controller 660 may be configured to identify a first bit of the logic state prior to identifying a second bit of the logic state. For example, if the memory cell 602 is capable of storing four logic states (00, 01, 10, 11), the controller 660 may be configured to identify whether the most-significant bit of a memory identifier is a logical '1' or a logical '0' prior to identifying the value of the other bit.

[0086] The controller 660 may also operate the switching components 662, 664, 666 to perform a write back portion of a read operation. In some examples, the controller 660 may be configured to perform write operations as part a normal write operation. The controller 660 may be coupled to the switching components 662, 664 by a first control line 668. The controller 660 may be coupled to the switching component 666 by a second control line 670. In some examples, any number of control lines may be used by the controller 660 to operate the switching components 662, 664, 666.

[0087] The switching component 662 may be coupled to a voltage source 672 (V_o). The switching component 662 may be configured to bias the plate line 606 high (e.g., to the voltage source 672) during a write operation or a write back operation. The switching component 662 may be a transistor or other type of switching component.

[0088] The switching component 664 may be coupled to a ground 674. The switching component 664 may be configured to bias the plate line 606 low (*e.g.*, to ground) during a write operation or a write back operation. In some examples, the ground 674 may be a ground or a virtual ground that is a voltage source at a V_{ss} .

5 [0089] In the instances when the same control line is used to control both the switching component 662 and the switching component 664 (*e.g.*, first control line 668), the switching component 662 may be configured to be activated when the switching component 664 is deactivated. As such, the switching component 662 may be configured to be activated based on a low signal, while the switching component 664 may be configured to be activated based
10 on a high signal, or vice versa.

[0090] The switching component 666 may be coupled to the ground 674. The switching component 664 may be configured to bias the digit line 604 low (*e.g.*, to ground or virtual ground) during a write operation or a write back operation. In some examples, the controller may be configured the word line 612 during a write or write-back operation. Such control of
15 the word line 612 may be used when the word line 612 is deactivated after the dielectric charging of the memory cell 602.

[0091] In some examples, the controller 660 may be coupled to another switching component to bias the digit line 604 high during a write or write back operation. In some examples, the charging component 622 may be operated to bias the digit line 604 high during
20 a write or write back operation.

[0092] In some instances, the controller 660 may be an example of the memory controller 140. In some instances, the controller 660 may be a dedicated component, a dedicated circuit, or dedicated logic configured to perform the functions described herein. In some instances, the controller 660 may be coupled to the memory controller 140 and may be configured to
25 cooperate with the memory controller 140 to perform the various functions described herein. For example, the controller 660 may perform some portions of the functions described herein and the memory controller 140 may perform the other portions of the functions described herein, in some examples.

[0093] FIG. 7 illustrates an example of a timing diagram 700 that supports time-based
30 access of a memory cell in accordance with various embodiments of the present disclosure. The timing diagram 700 illustrates a digit line voltage signal 705 of the digit line 604 at the first node 620 and a node voltage signal 710 at the second node 628 of the circuit 600. The

digit line voltage signal 705 and the node voltage signal 710 may represent voltages during a read operation of a memory cell 602. More specifically, the signals 705, 710 may represent voltages during a sense portion of the read operation.

[0094] A read operation performed on the memory cell 602 may include a

5 preconditioning portion, a sense portion, a write back operation, and a precharge portion. At time t_0 , a memory controller 140 may initiate a sense portion of the read operation. To develop the signal from the memory cell 602, the memory controller 140 may activate the charging component 622 to charge the memory cell 602 or the digit line 604 to the predetermined voltage level 715 as represented by V_{dl} in FIG. 7. The voltage level of the
10 memory cell 602 rises from a starting voltage level 720 (represented by V_{st} in FIG. 7) to the predetermined voltage level 715 (V_{dl}).

[0095] The voltage level of the second node 628, as represented by the node voltage signal 710, also rises from a starting voltage level based on the memory cell 602 being charged. The starting voltage level of the second node 628 may be based on the starting

15 voltage level of the digit line 604 and/or memory cell 602. In some examples, the starting voltage level of the second node 628 may be the same as the starting voltage level of the digit line 604 and/or memory cell 602. In some examples, the starting voltage level of the second node 628 may be different from the starting voltage level of the digit line 604 and/or memory cell 602. In some examples, the starting voltage varies based on a memory state of the
20 memory cell 602 being charged.

[0096] A voltage threshold 725 may be defined for the voltage level of the second node 628 (represented by node voltage signal 710). The voltage threshold 725 may be associated with when the voltage level of the digit line 604 and/or memory cell 602 reaches the predetermined voltage level 715. The voltage threshold 725 may be selected based on an

25 identified relationship between the voltage level of the second node 628 and a voltage level of the first node 620. In some examples, the voltage threshold 725 may be an example of the voltage threshold 505 described with reference to FIG. 5.

[0097] At time t_1 , the voltage level at the second node 628 may satisfy the voltage threshold 725. The circuit 600 may make this determination using the sense component 634

30 in some examples. In some instances, the sense component 634 may compare the voltage level detected at the second node 628 to a reference voltage to identify with the voltage threshold 725 is satisfied. At time t_1 , the sense component 634 may output a signal to the

latch 640 based on the voltage level at the second node 628 satisfying the voltage threshold 725. The voltage threshold 725 may be modified or altered based on circuit operation or changes in the access operations.

[0098] A duration 730 may be defined between the beginning of charging the digit line 604 and/or memory cell 602 at time t_0 and when the voltage level satisfies the voltage threshold 725 at time t_1 . The duration 730 may correspond to one of the durations described with reference to FIG. 5. The duration 730 may vary based on the memory state of the memory cell 602 at time t_0 when the charging begins. The starting voltage levels of both the digit line 604 and the second node 628 may also vary based on the memory state of the memory cell 602 at time t_0 when the charging begins. For example, the starting voltage levels for memory state A (described with reference to FIGs. 3 and 5) may be higher than memory state D (described with reference to FIGs. 3 and 5). In some examples, the signals 705, 710 may vary based on the memory state of the memory cell 602 at time t_0 when the charging begins.

[0099] In some examples, the sense component 634 of the circuit 600 may be coupled to the digit line 604 at the first node 620. In those examples, the voltage threshold 725 may be set to be at or around the predetermined voltage level 715 that the digit line 604 and/or the memory cell 602 are being charged. It should be appreciated that the elements of the sense component 634 may be modified when the sense component 634 is coupled to digit line 604 to perform the functions described herein.

[0100] In some examples, the digit line 604 may be biased prior to starting the read operation. Biasing the digit line 604 may reduce disturbances of the logic state of unselected memory cells also coupled to the digit line 604. Biasing the digit line 604 before performing the read operation, in some cases, may not alter the durations taken to charge the digit line 604 during a sense portion of a read operation.

[0101] In some instances, a time-based read operation may be performed on a memory cell 602 without a latch and/or time-varying signals. In some instances, the controller 660 or memory controller 140 may determine a duration between beginning to charge the memory cell 602 and when the voltage threshold 725 is satisfied. The controller 660 or memory controller 140 may compare the duration to values of a look-up table. The look-up table may be configured to map durations to a particular logic state. In some examples, a timer may be initiated when the memory cell 602 begins to be charged. The duration of the sense portion of

the read operation may be based on a value of the timer when the voltage threshold is satisfied.

[0102] A write back portion of the read operation may begin after the logic state of the memory cell 602 is identified. The controller 660 may identify the logic state of the memory cell 602 about or after time t1. The controller 660 may then determine what memory state should be written to the memory cell based on the identified logic state. In some examples, the memory state to be written back is the same memory state that was identified by the controller 660.

[0103] During a sense portion of a time-based read operation, the digit line 604 may be charged or biased to a high voltage. To write memory states to the memory cell 602, the memory cell 602 may be biased by the digit line 604 and the plate line 606. To write some memory states to the memory cell 602, the digit line 604 may be high and the plate line 606 may be low. To write other memory states to the memory cell 602, the digit line 604 may be low and the plate line 606 may be high.

[0104] As such, to write some memory states to the memory cell 602, the controller 660 may activate the switching component 664 to couple the plate line 606 to ground 674. Because the digit line 604 may already be high due to the charging during the sense portion of the read operation, the memory cell 602 may be biased to write back certain memory state to the memory cell 602.

[0105] In some instances, the digit line 604 may not be high at the beginning of a write operation or a write back portion of a read operation. In such instances, the controller 660 may activate one or more switching components (not shown) to couple the digit line 604 to a voltage source and the switching component 664 may be activated to couple the plate line 606 to ground. For example, during a normal write operation, the digit line 604 may be at a low value at the beginning of the write operation. In another example, the digit line 604 may be coupled to ground after the sense component detects that the threshold has been satisfied. Switching the memory cell 602 off during portions of the read operation may reduce the stress on the memory cell 602. In such examples, the digit line 604 may be coupled to one or more switching components that selectively couple the digit line 604 to ground.

[0106] To write other memory states to the memory cell 602, the controller 660 may activate the switching component 662 to couple the plate line 606 to a voltage source and may activate the switching component 666 to couple the digit line 604 to ground 674. In

some cases, prior to activating the switching component 666, the charging component 622 may be deactivated.

[0107] In some examples, the controller 660 may deactivate the selection component 610 during a write operation or a write back operation. In such examples, the selection component 610 may be deactivated while the plate line 606 or the digit line 604 is high. Deactivating the selection component 610 may cause the middle electrode of the memory cell 602 to store a dielectric charge. In some examples, deactivating the selection component 610 may cause the capacitor 608 to store a dielectric charge. In some examples, a ferroelectric memory cell may be configured to store both a polarization state and a dielectric charge state by not discharging the middle electrode after a write operation or a write back operation.

[0108] In some examples, the memory cell 602 may be configured to store a plurality of memory states. As such, the controller 660 may be coupled to a plurality of switching components coupled to a plurality of voltage sources. Various combinations of these voltage sources may be used to obtain the proper biasing for the memory cell 602. For example, a memory cell 602 may be written with a memory state by coupling the digit line 604 to a first voltage and coupling the plate line 606 to a second voltage different from the voltage. The first and second voltage may be any voltage. The circuit 600 may include any number of control lines and switching components to properly write various memory states to the memory cell 602.

[0109] FIG. 8 illustrates an example of a timing diagram 800 that supports time-based access of a memory cell in accordance with various embodiments of the present disclosure. The timing diagram 800 illustrates an examples of time-varying signals input into at least one latch (*e.g.*, latch 640). The timing diagram 800 includes a first time-varying signal 805 and a second time-varying signal 810. In some examples, the time-varying signals 805, 810 may be input into a single latch (*e.g.*, first latch 640). In some examples, the time-varying signals 805, 810 may be input into two latches (*e.g.*, first latch 640 and second latch 644). The first time-varying signal 805 may be an example of the first time-varying signal 642 described with reference to FIG. 6. The second time-varying signal 810 may be an example of the second time-varying signal 646 described with reference to FIG. 6. In some examples, the amplitude of the signals 805, 810 may be varied over time. In other examples, other characteristics of the signals 805, 810 may be varied over time.

[0110] The first and second time-varying signals 805, 810 may be configured to define logic states stored on a memory cell 602. The first and second time-varying signals 805, 810 may be configured to represent logical '1s' and logical '0s' based on high and low voltage values. For example, a high voltage value of the time-varying signals 805, 810 may represent a logical '1' and a low voltage value may represent a logical '0.'

[0111] In a time-based read operation, the duration between the beginning of charging the memory cell 602 to a predetermined voltage level (*e.g.*, voltage level 715) and satisfying a voltage threshold (*e.g.*, voltage threshold 725) may be used to activate one or more latches (*e.g.*, latches 640, 644). The value of the time-varying signals 805, 810 at the time the latches are activated may be used to identify the logic state of the memory cell 602. For example, if the charging of the memory cell 602 begins at time t_0 and the voltage threshold is satisfied at time t_1 , the value of the first time-varying signal 805 may indicate that the first bit of a logic state of the memory cell 602 is a logical '0' and the second bit is a logical '0.'

[0112] The first and second time-varying signals 805, 810 may cooperate to map a logic state of the memory cell 602 to an associated memory state of the memory cell 602 based on the duration to charge the memory cell 602 during a read operation. Such time-based read operations may be used to distinguish between memory states not previously distinguishable in other memory cells. For example, a time-based read operation may be able to distinguish between a first memory state defined by zero polarization and a first level of dielectric charge and a second memory state defined by a first polarization and the first level of dielectric charge. In some examples, time-based read operations may be configured to distinguish between different levels of dielectric charge alone or different levels of polarization alone, or change in both.

[0113] The first and second time-varying signals 805, 810 may be based on expected durations of charging associated with different memory states of a memory cell 602. As used in FIG. 8, the time t_1 may represent the time at which the voltage satisfies the voltage threshold during a read operation when the memory cell 602 stores the memory state A. A duration 815 defined between time t_0 and time t_1 may correspond to duration 530 described with reference to FIG. 5. As used in FIG. 8, the time t_2 may represent the time at which the voltage satisfies the voltage threshold during a read operation when the memory cell 602 stores the memory state B. A duration 820 defined between time t_0 and time t_2 may correspond to duration 540 described with reference to FIG. 5. As used in FIG. 8, the time t_3

may represent the time at which the voltage satisfies the voltage threshold during a read operation when the memory cell 602 stores the memory state C. A duration 825 defined between time t0 and time t3 may correspond to duration 550 described with reference to FIG. 5. As used in FIG. 8, the time t4 may represent the time at which the voltage satisfies the voltage threshold during a read operation when the memory cell 602 stores the memory state D. A duration 830 defined between time t0 and time t4 may correspond to duration 555 described with reference to FIG. 5.

[0114] The first and second time-varying signals 805, 810 may be configured to extend for an overall interval 835. The overall interval 835 may include a number of subintervals.

Each subinterval may define a unique logic state of the memory cell 602. For instance, in the examples where the memory cell 602 is configured to store four memory states, the first and second time-varying signals 805-, 810 may define four subintervals. Each subinterval may be associated with a separate memory state of the memory cell 602. Each subinterval may be associated with an expected duration for charging for a separate memory state of the memory cell 602.

[0115] A subinterval may represent a time period during which a single logic state of the memory cell 602 is represented by one or more time-varying signals. In the illustrative example, two time-varying signals are used to represent the possible logical states of a memory cell 602. However, in other examples, other number of time-varying signals may be

used to represent the possible logical states of a memory cell 602 (*e.g.*, one time-varying signal, three time-varying signals, *etc.*). The first and second time-varying signals 805, 810 may include a first subinterval 840, a second subinterval 845, a third subinterval 850, and fourth subinterval 855. In the representative example of FIG. 8, the first subinterval 840 may represent a logical '00,' the second subinterval 845 may represent a logical '01,' the third subinterval 850 may represent a logical '10,' and a fourth subinterval 855 may represent a logical '11.' In some examples, the first time-varying signal 805 may represent a most-significant bit of a logic state identifier and the second time-varying signal 810 may represent a least-significant bit of a logic state identifier. In some examples, a single time-varying signal may represent more two or more bits of a logic state identifier.

[0116] Each subinterval may be separated by a transition. A transition may refer to a change in the voltage level of one of the time-varying signals or both of the time-varying signals. The change in the voltage level may represent a change in the logic state be

represented by the one or more time-varying signals. The first subinterval may extend between an initial transition at time t_0 (*e.g.*, the beginning of applying the time-varying signal) and a first transition 860. The second subinterval 845 may extend between the first transition 860 and a second transition 865. The third subinterval 850 may extend between the second transition 865 and a third transition 870. The fourth subinterval 855 may extend between the third transition 870 and a fourth transition 875 or an ending transition.

[0117] At the first transition 860, the first time-varying signal 805 may not alter its voltage value and the second time-varying signal 810 may alter its voltage value from a low voltage value to a high voltage value. At the second transition 865, the first time-varying signal 805 may alter its voltage value from low to high and the second time-varying signal 810 may alter its voltage value from high to low. At the third transition 870, the first time-varying signal 805 may not alter its voltage value and the second time-varying signal 810 may alter its voltage value from low to high. At the fourth transition 875, the first time-varying signal 805 may alter its voltage value from high to low and the second time-varying signal 810 may alter its voltage value from high to low.

[0118] In some examples, the subintervals may span equal lengths of time. However, in other examples, the subintervals may span different lengths of the time. The transitions of the time-varying signals between logical states may be positioned to distinguish between memory states of the memory cell 602. Because a read operation may not produce equally spaced apart durations for satisfying voltage thresholds, similarly the thresholds between logical states may not be equally spaced.

[0119] The first and second time-varying signals 805, 810 may be used in conjunction with the memory states A-D shown and described with reference to FIGs. 3 and 5. In such an example, the subinterval 840 may be associated with the memory state A (*e.g.*, memory state 340 (State A)), the subinterval 845 may be associated with the memory state B (*e.g.*, memory state 305 (State B)), the subinterval 850 may be associated with the memory state C (*e.g.*, memory state 310 (State C)), and the subinterval 855 may be associated with the memory state D (*e.g.*, memory state 345 (State D)). As such, in this example, memory state A may be mapped to a logical '00,' memory state B may be mapped to a logical '01,' memory state C may be mapped to a logical '10,' and memory state D may be mapped to a logical '11.' In some examples, the time-varying signals may be configured to map the memory states to any logic state. The mapping shown FIG. 8 is provided for illustrative purposes only.

[0120] In some examples, the time-varying signal(s) may be configured such that a first bit of a logic state identifier may be identified after a first duration shorter than a second duration to determine a second bit of the logic state identifier. For example, at transition 865 the controller 660 may be able to determine whether one of the bits is a logical '1' or a logical '0.' If the voltage threshold has not been satisfied by the transition 865, then the controller 660 may determine that the first bit is a logical '1.' This type of determination may be accomplished through an inference. In some examples, if the voltage threshold has not been satisfied by the transition 870, the controller 660 may determine that logical state identifier is a logical '11.' Such a determination may be done by inference because during the time-based sense there is no longer any ability to determine that any of the other three logic states represented in the timing diagram 800 is stored by the memory cell 602. In some examples, the overall interval 835 of the time-varying signals may terminate at transition 870. As such, the time-varying signals may include three subintervals 840, 845, 850 and not include subinterval 855. In other examples, however, the time-varying signals extend to the transition 875 to identify whether an error has occurred during a read operation. If the voltage threshold is never satisfied during the interval 835, then the controller 660 may determine that an error in the read operation occurred.

[0121] FIG. 9 illustrates an example of timing diagrams 900 that support time-based access of a memory cell in accordance with various embodiments of the present disclosure.

The timing diagrams 900 represent expected durations for charging for various memory state of the memory cell 602. The timing diagram 900-a may represent the expected durations for charging when the charging component 622 applies a constant current to the digit line 604 as part of the read operation. The timing diagram 900-b may represent the expected durations for charging when the charging component 622 applies a time-varying current to the digit line 604 as part of the read operation.

[0122] The duration of time taken to charge the digit line 604 and/or the memory cell 602 may be based on the characteristics of the components of the memory device. Because characteristics of components (*e.g.*, capacitance) of the memory device are fixed, the duration to charge the memory cell 602 may be based on the memory state of the memory cell 602 and how that memory state interacts with the other fixed characteristics of the components of the circuit.

[0123] For example, if the capacitances associated with the circuit are fixed and the charging component applies a constant current or a constant power supply during charging, expected values of the durations associated with each memory state may be determined. At time t0, the charging of the memory cell 602 as part of a sense portion of a read operation begins. At time t1, a memory cell 602 having the memory state A (e.g., memory state 340 (State A)) satisfies the voltage threshold. In some examples, a duration 905 defined between time t0 and time t1 is about zero nanoseconds. In some instances, the duration 905 may be more than zero nanoseconds such as 0.2 nanoseconds, 0.4 nanoseconds, 0.6 nanoseconds, 0.8 nanoseconds, 1.0 nanoseconds, *etc.* Frequently, the voltage threshold and the predetermined voltage for charging may be set based on one of the memory states of the memory cell 602. As such, one of the memory states of the memory cell 602 may satisfy the voltage threshold quickly, and sometimes instantaneously after charging begins. Time t1 is shown as different from time t0 for illustrative purposes only. In some examples, time t1 occurs at or directly after time t0.

[0124] At time t2, a memory cell 602 having the memory state B (e.g., memory state 305 (State B)) satisfies the voltage threshold. In some examples, a duration 910 defined between time t0 and time t2 is about ten nanoseconds. In some instances, the duration 910 may range between 7 nanoseconds and 13 nanoseconds, 7.5 nanoseconds and 12.5 nanoseconds, 8 nanoseconds and 12 nanoseconds, 8.5 nanoseconds and 11.5 nanoseconds, 9.0 nanoseconds and 11 nanoseconds, or 9.5 nanoseconds and 10.5 nanoseconds.

[0125] At time t3, a memory cell 602 having the memory state C (e.g., memory state 310 (State C)) satisfies the voltage threshold. In some examples, a duration 615 defined between time t0 and time t3 is about forty-two nanoseconds. In some instances, the duration 915 may range between 35 nanoseconds and 49 nanoseconds, 36 nanoseconds and 48 nanoseconds, 37 nanoseconds and 47 nanoseconds, 38 nanoseconds and 46 nanoseconds, 39 nanoseconds and 45 nanoseconds, 40 nanoseconds and 44 nanoseconds, 41.0 nanoseconds and 43 nanoseconds, or 41.5 nanoseconds and 42.5 nanoseconds.

[0126] At time t4, a memory cell 602 having the memory state D (e.g., memory state 345 (State D)) satisfies the voltage threshold. In some examples, a duration 920 defined between time t0 and time t4 is about fifty-two nanoseconds. In some instances, the duration 920 may range between 45 nanoseconds and 59 nanoseconds, 46 nanoseconds and 58 nanoseconds, 47 nanoseconds and 57 nanoseconds, 48 nanoseconds and 56 nanoseconds, 49 nanoseconds and

55 nanoseconds, 50 nanoseconds and 54 nanoseconds, 51.0 nanoseconds and 53 nanoseconds, or 51.5 nanoseconds and 52.5 nanoseconds.

[0127] The relationships between the durations 910, 915, 920 may be based on the capacitances of the circuit. Because the design of the circuit and the characteristics of those circuit components is relatively constant, applying a constant current may yield predictable durations for charging the memory cell 602 based on the memory states. The durations and range values described above may be based on a value of the current used to charge the memory cell 602 and/or the digit line 604. Thus, in some cases, a high higher may result in less time to satisfy the threshold (*e.g.*, twice the current may result in half the time to satisfy the threshold).

[0128] As should be appreciated, the durations of timing diagram 900-a may make distinguishing between some memory states to be more difficult than distinguishing between other memory states. A first sense window 925 based on time between memory state A (time t_1) and memory state B (time t_2) may be about ten nanoseconds, in this example. A second sense window 930 based on time between memory state B (time t_2) and memory state C (time t_3) may be about thirty-two nanoseconds. A third sense window 935 based on time between memory state C (time t_3) and memory state D (time t_4) may be about ten nanoseconds.

[0129] Because of the relative durations of the sense windows 925, 930, 935, it may be more difficult or less difficult to distinguish between memory states in a time-based read operation. For example, because the first sense window 925 is about ten nanoseconds and the second sense window 930 is about three times the size of the first sense window, it may be easier to distinguish between memory state B and memory state C than it is to distinguish between memory state A and memory state B.

[0130] In some examples, the current or power source applied to the memory cell 602 during a sense portion of a read operation may be varied over time. Such a time-varying current may be configured to distribute the durations for charging in a predetermined manner. For example, a time-varying current applied by the charging component 622 may be configured to provide equally sized sense windows based on time. In some examples, the amplitude of the current may be varied over time. In other examples, other characteristics of the current may be varied over time.

[0131] The timing diagram 900-b illustrates durations and sense windows associated with a sense portion of a time-based read operation. In the read operation, a time-varying current is applied. The time-varying current is configured to change the charge times associated different memory states. For example, a duration 950 associated with memory state B may be longer than a duration 910. In another example, a duration 955 associated with memory state C may be shorter than the duration 915. In some examples, the duration 960 associated with memory state D may be different than the duration 920. In some examples, the time-varying current may be configured to make the duration 960 shorter than the duration 920 and thereby reduce the overall time taken during a sense portion of a read operation. In some examples, the time-varying current may be configured to provide predetermined sense windows, and as such the duration 960 may be longer than the duration 920.

[0132] The sense windows 965, 970, 975 in the timing diagram 900-b may be about equal in length of time. The length of time of the sense windows 965, 970, 975 may be based on the configuration of the time-varying current applied while charging the memory cell 602. In some examples, other configurations of durations and sense windows may be based on different current profiles of the time-varying current applied while charging the memory cell 602.

[0133] FIG. 10 shows a block diagram 1000 of a memory array 1005 that supports time-based access of a memory cell in accordance with various embodiments of the present disclosure. Memory array 1005 may be referred to as an electronic memory apparatus, and may be an example of a component of a memory controller 140 as described with reference to FIG. 1.

[0134] Memory array 1005 may include one or more memory cells 1010, a memory controller 1015, a word line 1020, a plate line 1025, a reference component 1030, a sense component 1035, a digit line 1040, and a latch 1045. These components may be in electronic communication with each other and may perform one or more of the functions described herein. In some cases, memory controller 1015 may include biasing component 1050 and timing component 1055. In some examples, the memory controller 1015 may be an example of a memory controller 140 as described with reference to FIG. 1. In some examples, the memory controller 1015 may be an example of a controller 660 as described with reference to FIG. 6. In some examples, the memory controller 1015 may be an example of both the memory controller 140 and the controller 660.

[0135] Memory controller 1015 may be in electronic communication with word line 1020, digit line 1040, sense component 1035, and plate line 1025, which may be examples of word line 110, digit line 115, sense component 125, and plate line 210 described with reference to FIGs. 1, and 2. Memory array 1005 may also include reference component 1030 and latch 1045. The components of memory array 1005 may be in electronic communication with each other and may perform portions of the functions described with reference to FIGs. 1 through 9. In some cases, reference component 1030, sense component 1035, and latch 1045 may be components of memory controller 1015.

[0136] In some examples, digit line 1040 is in electronic communication with sense component 1035 and a ferroelectric capacitor of ferroelectric memory cells 1010. A ferroelectric memory cell 1010 may be writable with a logic state (*e.g.*, a first or second logic state). Word line 1020 may be in electronic communication with memory controller 1015 and a selection component of ferroelectric memory cell 1010. Plate line 1025 may be in electronic communication with memory controller 1015 and a plate of the ferroelectric capacitor of ferroelectric memory cell 1010. Sense component 1035 may be in electronic communication with memory controller 1015, digit line 1040, latch 1045, and reference line 1060. Reference component 1030 may be in electronic communication with memory controller 1015 and reference line 1060. Sense control line 1065 may be in electronic communication with sense component 1035 and memory controller 1015. These components may also be in electronic communication with other components, both inside and outside of memory array 1005, in addition to components not listed above, via other components, connections, or busses.

[0137] Memory controller 1015 may be configured to activate word line 1020, plate line 1025, or digit line 1040 by applying voltages to those various nodes. For example, biasing component 1050 may be configured to apply a voltage to operate memory cell 1010 to read or write memory cell 1010 as described above. In some cases, memory controller 1015 may include a row decoder, column decoder, or both, as described with reference to FIG. 1. This may enable memory controller 1015 to access one or more memory cells 105. Biasing component 1050 may also provide voltage potentials to reference component 1030 in order to generate a reference signal for sense component 1035. Additionally, biasing component 1050 may provide voltage potentials for the operation of sense component 1035.

[0138] In some cases, memory controller 1015 may perform its operations using timing component 1055. For example, timing component 1055 may control the timing of the various

word line selections or plate biasing, including timing for switching and voltage application to perform the memory functions, such as reading and writing, discussed herein. In some cases, timing component 1055 may control the operations of biasing component 1050. In some examples, the timing component 1055 may cooperate to generate the F1 signal and/or the F2 signal.

[0139] Reference component 1030 may include various components to generate a reference signal for sense component 1035. Reference component 1030 may include circuitry configured to produce a reference signal. In some cases, reference component 1030 may be implemented using other ferroelectric memory cells 105. Sense component 1035 may compare a signal from memory cell 1010 (through digit line 1040) with a reference signal from reference component 1030. Upon determining the logic state, the sense component may then store the output in latch 1045, where it may be used in accordance with the operations of an electronic device that memory array 1005 is a part. Sense component 1035 may include a sense amplifier in electronic communication with the latch and the ferroelectric memory cell.

[0140] Memory controller 1015 may be an example of portions of the memory controller 1215 described with reference to FIG. 12. Memory controller 1015 and/or at least some of its various sub-components may be implemented in hardware, software executed by a processor, firmware, or any combination thereof. If implemented in software executed by a processor, the functions of the memory controller 1015 and/or at least some of its various sub-components may be executed by a general-purpose processor, a digital signal processor (DSP), an application-specific integrated circuit (ASIC), an field-programmable gate array (FPGA) or other programmable logic device, discrete gate or transistor logic, discrete hardware components, or any combination thereof designed to perform the functions described in the present disclosure. The memory controller 1015 and/or at least some of its various sub-components may be physically located at various positions, including being distributed such that portions of functions are implemented at different physical locations by one or more physical devices. In some examples, memory controller 1015 and/or at least some of its various sub-components may be a separate and distinct component in accordance with various embodiments of the present disclosure. In other examples, memory controller 1015 and/or at least some of its various sub-components may be combined with one or more other hardware components, including but not limited to an I/O component, a transceiver, a network server, another computing device, one or more other components described in the

present disclosure, or a combination thereof in accordance with various embodiments of the present disclosure.

[0141] Memory controller 1015 may charge a digit line coupled to a memory cell to a first voltage level, determine a duration for the digit line to charge to the first voltage level, and identify a logic state of the memory cell based on the duration for the digit line to reach the first voltage level. The memory controller 1015 may also force a current into a ferroelectric memory cell coupled to a digit line, the ferroelectric memory cell configured to store at least three logic states, sense a voltage at a node different from the digit line, the voltage based on a first voltage level of the digit line, and identify a logic state of the ferroelectric memory cell from the at least three logic states based on the voltage satisfying a voltage threshold. The memory controller 1015 may also apply a time-varying signal to a latch after initiating a read operation on a memory cell, activate the latch based on a digit line that is coupled to the memory cell charging to a first voltage level as part of the read operation, and identify a logic state of the memory cell based on a value of the time-varying signal present at the latch when the latch is activated. The memory controller 1015 may also sense a first state of a ferroelectric capacitor in a ferroelectric memory cell, sense a second state of the ferroelectric capacitor different from the first state, and identify a logic state of the ferroelectric memory cell from at least three logic states based on the first state and the second state. The memory controller 1015 may also activate a selection component of a ferroelectric memory cell, modify a first state of a ferroelectric capacitor of the ferroelectric memory cell based on a voltage being applied to the ferroelectric memory cell while the selection component is activated, deactivate the selection component, and modify a second state of the ferroelectric capacitor based on the selection component being deactivated while the voltage is applied to the ferroelectric memory cell.

[0142] In some cases, the memory array 1005 may include various means for operating the memory array 1005. For example, the memory array 1005 and/or the memory controller 1015 may include means for performing the functions described above with reference to FIG. 13.

[0143] The memory array 1005 may include means for charging a digit line coupled to a memory cell to a first voltage level, means for determining a duration for the digit line to charge to the first voltage level, and means for identifying a logic state of the memory cell based at least in part on the duration for the digit line to reach the first voltage level.

[0144] Some examples of the memory array 1005 described above may further include processes, features, means, or instructions for varying an amplitude of a current applied to the digit line over time, wherein the duration is based at least in part on the time-varying current. Some examples of the memory array 1005 described above may further include processes,
5 features, means, or instructions for selecting the memory cell from a plurality of memory cells based at least in part on a read operation being initiated.

[0145] Some examples of the memory array 1005 described above may further include processes, features, means, or instructions for initiating a timer based at least in part on performing a read operation on the memory cell, wherein the duration may be determined
10 based at least in part on the timer. In some examples of the memory array 1005 described above, the duration may be determined based at least in part on an amount of time that elapses between initiating a timer and the digit line charging to the first voltage level.

[0146] Some examples of the memory array 1005 described above may further include processes, features, means, or instructions for determining that a second voltage level at a
15 node different from the digit line satisfies a voltage threshold, wherein the duration may be based at least in part on the second voltage level satisfying the voltage threshold.

[0147] Some examples of the memory array 1005 described above may further include processes, features, means, or instructions for sensing, by a sense component, the second voltage level at the node, wherein the logic state may be identified based at least in part on
20 the second voltage level satisfying the threshold. In some examples of the memory array 1005 described above, the voltage threshold may be less than a biasing voltage used to generate a stable state of the memory cell.

[0148] Some examples of the memory array 1005 described above may further include processes, features, means, or instructions for identifying a value of a time-varying signal
25 based at least in part on the duration, wherein the logic state may be based at least in part on the value of the time-varying signal. Some examples of the memory array 1005 described above may further include processes, features, means, or instructions for biasing the digit line prior to charging the digit line with the first voltage level.

[0149] Some examples of the memory array 1005 described above may further include
30 processes, features, means, or instructions for identifying a first bit of the logic state after a second duration less than the duration. Some examples of the memory array 1005 described above may further include processes, features, means, or instructions for identifying a second

bit of the logic state after the duration. In some examples of the memory array 1005 described above, the first voltage level to which the digit line may be charged may be a predetermined voltage level based at least in part on at least one of a plurality of possible charge states of the memory cell.

5 **[0150]** In some examples of the memory array 1005 described above, the digit line may be charged by a cascode coupled to the digit line and to a sense component. In some examples of the memory array 1005 described above, the duration may be based at least in part on a stable state of a capacitor of the memory cell and a volatile state of the capacitor of the memory cell.

10 **[0151]** In some examples of the memory array 1005 described above, the memory cell includes a ferroelectric capacitor. In some examples of the memory array 1005 described above, the memory cell includes a dielectric capacitor. In some examples of the memory array 1005 described above, the memory cell may be configured to store at least three logic states. In some examples of the memory array 1005 described above, the memory cell may be
15 configured to store two logic states.

[0152] The memory array 1005 may include means for applying a current to a ferroelectric memory cell coupled to a digit line, the ferroelectric memory cell configured to store at least three logic states, means for sensing a voltage at a node different from the digit line, the voltage based at least in part on a first voltage level of the digit line, and means for
20 identifying a logic state of the ferroelectric memory cell from the at least three logic states based at least in part on the voltage satisfying a voltage threshold.

[0153] Some examples of the memory array 1005 described above may further include processes, features, means, or instructions for identifying a duration for a second voltage level present on the node to satisfy the voltage threshold, wherein the logic state may be
25 identified based at least in part on the duration.

[0154] In some examples of the memory array 1005 described above, the duration may be based at least in part on a total charge stored on a ferroelectric capacitor of the ferroelectric memory cell. In some examples of the memory array 1005 described above, the total charge comprises a volatile charge of the ferroelectric capacitor and a stable charge of the
30 ferroelectric capacitor.

[0155] Some examples of the memory array 1005 described above may further include processes, features, means, or instructions for identifying the logic state of the ferroelectric memory cell may be based at least in part on a polarization state of a ferroelectric capacitor of the ferroelectric memory cell and a charge state of the ferroelectric capacitor of the ferroelectric memory cell.

[0156] Some examples of the memory array 1005 described above may further include processes, features, means, or instructions for outputting, by a sense component, a signal based at least in part on the voltage satisfying the voltage threshold. Some examples of the memory array 1005 described above may further include processes, features, means, or instructions for activating a first latch based at least in part on the voltage satisfying the voltage threshold. Some examples of the memory array 1005 described above may further include processes, features, means, or instructions for activating a second latch different from the first latch based at least in part on the voltage satisfying the voltage threshold.

[0157] Some examples of the memory array 1005 described above may further include processes, features, means, or instructions for applying a first time-varying signal to the first latch. Some examples of the memory array 1005 described above may further include processes, features, means, or instructions for applying a second time-varying signal to the second latch different from the first time-varying signal, wherein the logic state of the ferroelectric memory cell may be based at least in part on values of the first time-varying signal and the second time-varying signal when the first latch and the second latch may be activated.

[0158] Some examples of the memory array 1005 described above may further include processes, features, means, or instructions for activating a selection component of the ferroelectric memory cell, wherein the current may be forced based at least in part on the selection component being activated.

[0159] Some examples of the memory array 1005 described above may further include processes, features, means, or instructions for activating a selection component of the ferroelectric memory cell while a plate line and the digit line coupled to the ferroelectric memory cell may be grounded or virtually grounded.

[0160] Some examples of the memory array 1005 described above may further include processes, features, means, or instructions for performing a write-back operation on the ferroelectric memory cell based at least in part on the identified logic state of the ferroelectric

memory cell. In some examples of the memory array 1005 described above, the current may be forced based at least in part on performing a read operation on the ferroelectric memory cell.

[0161] Some examples of the memory array 1005 described above may further include processes, features, means, or instructions for charging, by a current generator, the digit line to the first voltage level based at least in part on applying the current. In some examples of the memory array 1005 described above, the current may be forced by a current generator coupled to the digit line and the node.

[0162] The memory array 1005 may include means for applying a time-varying signal to a latch after initiating a read operation on a memory cell, means for activating the latch based at least in part on a digit line that is coupled to the memory cell charging to a first voltage level as part of the read operation, and means for identifying a logic state of the memory cell based at least in part on a value of the time-varying signal present at the latch when the latch is activated.

[0163] Some examples of the memory array 1005 described above may further include processes, features, means, or instructions for isolating the memory cell from the latch after the digit line charges to the first voltage as part of the read operation.

[0164] In some examples of the memory array 1005 described above, the memory cell may be configured to store at least three logic states. In some examples of the memory array 1005 described above, the identified logic state of the memory cell may be selected from the at least three logic states.

[0165] Some examples of the memory array 1005 described above may further include processes, features, means, or instructions for applying a second time-varying signal to a second latch based at least in part on performing the read operation on the memory cell, the second time-varying signal different from the time-varying signal, the second latch different from the latch.

[0166] Some examples of the memory array 1005 described above may further include processes, features, means, or instructions for activating the second latch based at least in part on the digit line that may be coupled to the memory cell charging to the first voltage level, wherein identifying the logic state of the memory cell may be based at least in part on the

time-varying signal present at the latch and the second time-varying signal present at the second latch when the latch and the second latch may be activated.

[0167] In some examples of the memory array 1005 described above, a configuration of the second time-varying signal may be based at least in part on a configuration of the time-varying signal, wherein the time-varying signal and the second time-varying signal cooperate to define at least three logic states. Some examples of the memory array 1005 described above may further include processes, features, means, or instructions for charging the digit line of the memory cell as part of the read operation, wherein the time-varying signal may be applied when charging the digit line begins.

[0168] Some examples of the memory array 1005 described above may further include processes, features, means, or instructions for sensing a second voltage level at a node different from the digit line, wherein the latch may be activated based at least in part on the second voltage level satisfying a voltage threshold. Some examples of the memory array 1005 described above may further include processes, features, means, or instructions for outputting a signal based at least in part on the second voltage level satisfying the voltage threshold, wherein the latch may be activated based at least in part on the signal.

[0169] Some examples of the memory array 1005 described above may further include processes, features, means, or instructions for determining that a duration of the read operation satisfies a time threshold, wherein identifying the logic state of the memory cell may be based at least in part on the latch not activating prior to the duration satisfying the time threshold.

[0170] In some examples of the memory array 1005 described above, a configuration of the time-varying signal may be based at least in part on an expected charge of the memory cell and the first voltage level. In some examples of the memory array 1005 described above, the configuration of the time-varying signal may be based at least in part on a number of logic states the memory cell may be capable of storing.

[0171] In some examples of the memory array 1005 described above, the configuration of the time-varying signal may be based at least in part on a number of latches used in the read operation. In some examples of the memory array 1005 described above, a configuration of the time-varying signal and an interval of the time-varying signal may be predetermined. In some examples of the memory array 1005 described above, a value of the time-varying signal varies in a predetermined manner over a predetermined interval of the time-varying signal.

[0172] The memory array 1005 may include means for sensing a first state of a ferroelectric capacitor in a ferroelectric memory cell, means for sensing a second state of the ferroelectric capacitor different from the first state, and means for identifying a logic state of the ferroelectric memory cell from at least three logic states based at least in part on the first state and the second state. In some examples, sensing a first state of the ferroelectric capacitor and sensing a second state of the ferroelectric capacitor may comprise sensing a combined state of the sensing capacitor. In some cases, the combined state may be a combination (or superposition) of a polarized state and a dielectric charge state.

[0173] In some examples of the memory array 1005 described above, the first state of the ferroelectric capacitor may be associated with a polarization of the ferroelectric capacitor. In some examples of the memory array 1005 described above, the second state of the ferroelectric capacitor may be associated with a dielectric charge stored on the ferroelectric capacitor.

[0174] Some examples of the memory array 1005 described above may further include processes, features, means, or instructions for identifying a first bit of the logic state based at least in part on the first state. Some examples of the memory array 1005 described above may further include processes, features, means, or instructions for identifying a second bit of the logic state based at least in part on the second state.

[0175] Some examples of the memory array 1005 described above may further include processes, features, means, or instructions for activating at least two latches based at least in part on a voltage level of a node different from a digit line satisfying a voltage threshold.

[0176] Some examples of the memory array 1005 described above may further include processes, features, means, or instructions for applying a first time-varying signal to one of the at least two latches. Some examples of the memory array 1005 described above may further include processes, features, means, or instructions for applying a second time-varying signal different from the first time-varying signal to another of the at least two latches, wherein the logic state may be identifying based at least in part on values of the first time-varying signal and the second time-varying signal when activating the at least two latches.

[0177] Some examples of the memory array 1005 described above may further include processes, features, means, or instructions for identifying a duration for a first voltage level of a digit line to satisfy a voltage threshold during an access operation, the duration based at

least in part on the first state of the ferroelectric capacitor, the second state of the ferroelectric capacitor, and a voltage applied to the digit line.

[0178] Some examples of the memory array 1005 described above may further include processes, features, means, or instructions for identifying a duration for a second voltage level of a node different from a digit line to satisfy a voltage threshold, the duration based at least in part on the first state of the ferroelectric capacitor and the second state of the ferroelectric capacitor.

[0179] The memory array 1005 may include means for activating a selection component of a ferroelectric memory cell, means for modifying a first state of a ferroelectric capacitor of the ferroelectric memory cell based at least in part on a voltage being applied to the ferroelectric memory cell while the selection component is activated, means for deactivating the selection component, and means for modifying a second state of the ferroelectric capacitor based at least in part on the selection component being deactivated while the voltage is applied to the ferroelectric memory cell.

[0180] Some examples of the memory array 1005 described above may further include processes, features, means, or instructions for activating the selection component while a plate line and a digit line coupled to the ferroelectric memory cell may be grounded or virtually grounded. In some examples of the memory array 1005 described above, modifying the first state of the ferroelectric capacitor comprises: applying a first voltage to the ferroelectric capacitor.

[0181] In some examples of the memory array 1005 described above, applying the first voltage to the ferroelectric capacitor comprises: applying a second voltage to a digit line coupled to the ferroelectric memory cell. Some examples of the memory array 1005 described above may further include processes, features, means, or instructions for applying a third voltage to a plate line coupled to the ferroelectric memory cell, the third voltage different from the second voltage, wherein the first voltage may be based at least in part on the second voltage and the third voltage. In some examples of the memory array 1005 described above, modifying the second state of the ferroelectric capacitor comprises: applying a fourth voltage to the ferroelectric capacitor.

[0182] In some examples of the memory array 1005 described above, applying the fourth voltage to the ferroelectric capacitor comprises: applying a fifth voltage to a digit line coupled to the ferroelectric memory cell, the selection component may be deactivated while

the fifth voltage is applied to the ferroelectric memory cell, wherein the selection component may be positioned between the ferroelectric capacitor and a plate line coupled to the ferroelectric memory cell.

[0183] In some examples of the memory array 1005 described above, applying the fourth voltage to the ferroelectric capacitor comprises: applying a sixth voltage to a plate line coupled to the ferroelectric memory cell, the selection component may be deactivated while the sixth voltage is applied to the ferroelectric memory cell, wherein the selection component may be positioned between the ferroelectric capacitor and a digit line coupled to the ferroelectric memory cell.

[0184] In some examples of the memory array 1005 described above, the ferroelectric memory cell may be configured to store at least three logic states based at least in part on the first state of the ferroelectric capacitor and the second state of the ferroelectric capacitor. In some examples of the memory array 1005 described above, the first state may be a polarization state of the ferroelectric capacitor. In some examples of the memory array 1005 described above, the second state may be a dielectric charge state of the ferroelectric capacitor.

[0185] FIG. 11 shows a block diagram 1100 of a memory controller 1115 that supports time-based access of a memory cell in accordance with various embodiments of the present disclosure. The memory controller 1115 may be an example of portions of a memory controller 1215 described with reference to FIGs. 1, 10, and 12. The memory controller 1115 may include biasing component 1120, timing component 1125, charging component 1130, sensing manager 1135, logic determiner 1140, signal manager 1145, latch manager 1150, cell manager 1155, timing manager 1160, and threshold manager 1165. Each of these modules may communicate, directly or indirectly, with one another (*e.g.*, via one or more buses).

[0186] Biasing component 1120 may bias the digit line prior to charging the digit line with the first voltage level.

[0187] Timing component 1125 may be configured to determine durations associated with read operation of a memory cell. For example, the timing component may be configured to determine a duration between beginning to charge a digit line of a memory cell and the firing of a latch. In some cases, the duration is determined based on an amount of time that elapses between initiating a timer and the digit line charging to the first voltage level.

[0188] Charging component 1130 may charge a digit line coupled to a memory cell to a first voltage level, vary a current applied to the digit line over time to charge the digit line, the time-varying current configured to modify a time interval associated with a specific logic state of the memory cell, force a current into a ferroelectric memory cell coupled to a digit line, the ferroelectric memory cell configured to store at least three logic states, charge, by a current generator, the digit line to the first voltage level based on applying the current, and charge the digit line of the memory cell as part of the read operation, where the time-varying signal is applied when charging the digit line begins. In some cases, the first voltage level to which the digit line is charged is a predetermined voltage level based on at least one of a set of possible charge states of the memory cell. In some cases, the digit line is charged by a cascode coupled to the digit line and to a sense component. In some cases, the current is forced based on performing a read operation on the ferroelectric memory cell. In some cases, the current is forced by a current generator coupled to the digit line and the node.

[0189] Sensing manager 1135 may determine a duration for the digit line to charge to the first voltage level, sense a voltage at a node different from the digit line, the voltage based on a first voltage level of the digit line, output, by a sense component, a signal based on the voltage satisfying the voltage threshold, sense a second voltage level at a node different from the digit line, where the latch is activated based on the second voltage level satisfying a voltage threshold, output a signal based on the second voltage level satisfying the voltage threshold, where the latch is activated based on the signal, sense a first state of a ferroelectric capacitor in a ferroelectric memory cell, and sense a second state of the ferroelectric capacitor different from the first state.

[0190] Logic determiner 1140 may identify a logic state of the memory cell based on the duration for the digit line to reach the first voltage level, identify a value of a time-varying signal based on the duration, where the logic state is based on the value of the time-varying signal, identify a first bit of the logic state after a second duration less than the duration, identify a second bit of the logic state after the duration, identify a logic state of the ferroelectric memory cell from the at least three logic states based on the voltage satisfying a voltage threshold, identify the logic state of the ferroelectric memory cell is based on a polarization state of a ferroelectric capacitor of the ferroelectric memory cell and a charge state of the ferroelectric capacitor of the ferroelectric memory cell, identify a logic state of the memory cell based on a value of the time-varying signal present at the latch when the latch is activated, identify a logic state of the ferroelectric memory cell from at least three logic states

based on the first state and the second state, identify a first bit of the logic state based on the first state, and identify a second bit of the logic state based on the second state.

[0191] Signal manager 1145 may apply a time-varying signal to a latch after initiating a read operation on a memory cell, apply a second time-varying signal to a second latch based on performing the read operation on the memory cell, the second time-varying signal different from the time-varying signal, the second latch different from the latch, apply a first time-varying signal to one of the at least two latches, and apply a second time-varying signal different from the first time-varying signal to another of the at least two latches, where the logic state is identifying based on values of the first time-varying signal and the second time-varying signal when activating the at least two latches. In some cases, a configuration of the second time-varying signal is based on a configuration of the time-varying signal, where the time-varying signal and the second time-varying signal cooperate to define at least three logic states. In some cases, a configuration of the time-varying signal is based on an expected charge of the memory cell and the first voltage level. In some cases, the configuration of the time-varying signal is based on a number of logic states the memory cell is capable of storing. In some cases, the configuration of the time-varying signal is based on a number of latches used in the read operation. In some cases, a configuration of the time-varying signal and an interval of the time-varying signal is predetermined. In some cases, a value of the time-varying signal varies in a predetermined manner over a predetermined interval of the time-varying signal.

[0192] Latch manager 1150 may activate a first latch based on the voltage satisfying the voltage threshold, activate a second latch different from the first latch based on the voltage satisfying the voltage threshold, apply a first time-varying signal to the first latch, apply a second time-varying signal to the second latch different from the first time-varying signal, where the logic state of the ferroelectric memory cell is based on values of the first time-varying signal and the second time-varying signal when the first latch and the second latch are activated, activate the latch based on a digit line that is coupled to the memory cell charging to a first voltage level as part of the read operation, activate the second latch based on the digit line that is coupled to the memory cell charging to the first voltage level, where identifying the logic state of the memory cell is based on the time-varying signal present at the latch and the second time-varying signal present at the second latch when the latch and the second latch are activated, and activate at least two latches based on a voltage level of a node different from a digit line satisfying a voltage threshold.

[0193] Cell manager 1155 may select the memory cell from a set of memory cells based on a read operation being initiated, activate a selection component of the ferroelectric memory cell, where the current is forced based on the selection component being activated, activate a selection component of the ferroelectric memory cell while a plate line and the digit line coupled to the ferroelectric memory cell are grounded or virtually grounded, perform a write-back operation on the ferroelectric memory cell based on the identified logic state of the ferroelectric memory cell, isolate the memory cell from the latch after the digit line charges to the first voltage as part of the read operation, modify a first state of a ferroelectric capacitor of the ferroelectric memory cell based on a voltage being applied to the ferroelectric memory cell while the selection component is activated, deactivate the selection component, modify a second state of the ferroelectric capacitor based on the selection component being deactivated while the voltage is applied to the ferroelectric memory cell, activate the selection component while a plate line and a digit line coupled to the ferroelectric memory cell are grounded or virtually grounded, apply a third voltage to a plate line coupled to the ferroelectric memory cell, the third voltage different from the second voltage, where the first voltage is based on the second voltage and the third voltage, and activate a selection component of a ferroelectric memory cell. In some cases, the second state is a dielectric charge state of the ferroelectric capacitor. In some cases, the memory cell includes a ferroelectric capacitor. In some cases, the memory cell includes a dielectric capacitor. In some cases, the memory cell is configured to store at least three logic states. In some cases, the memory cell is configured to store two logic states. In some cases, the memory cell is configured to store at least three logic states. In some cases, the identified logic state of the memory cell is selected from the at least three logic states. In some cases, the first state of the ferroelectric capacitor is associated with a polarization of the ferroelectric capacitor. In some cases, the second state of the ferroelectric capacitor is associated with a dielectric charge stored on the ferroelectric capacitor. In some cases, the duration is based on a stable state of a capacitor of the memory cell and a volatile state of the capacitor of the memory cell. In some cases, modifying the first state of the ferroelectric capacitor includes: applying a first voltage to the ferroelectric capacitor. In some cases, applying the first voltage to the ferroelectric capacitor includes: applying a second voltage to a digit line coupled to the ferroelectric memory cell. In some cases, modifying the second state of the ferroelectric capacitor includes: applying a fourth voltage to the ferroelectric capacitor. In some cases, applying the fourth voltage to the ferroelectric capacitor includes: applying a fifth voltage to a digit line coupled to the ferroelectric memory cell, the selection component being deactivated while the

fifth voltage is applied to the ferroelectric memory cell, where the selection component is positioned between the ferroelectric capacitor and a plate line coupled to the ferroelectric memory cell. In some cases, applying the fourth voltage to the ferroelectric capacitor includes: applying a sixth voltage to a plate line coupled to the ferroelectric memory cell, the selection component being deactivated while the sixth voltage is applied to the ferroelectric memory cell, where the selection component is positioned between the ferroelectric capacitor and a digit line coupled to the ferroelectric memory cell. In some cases, the ferroelectric memory cell is configured to store at least three logic states based on the first state of the ferroelectric capacitor and the second state of the ferroelectric capacitor. In some cases, the first state is a polarization state of the ferroelectric capacitor.

[0194] Timing manager 1160 may initiate a timer based on performing a read operation on the memory cell, where the duration is determined based on the timer, identify a duration for a second voltage level present on the node to satisfy the voltage threshold, where the logic state is identified based on the duration, determine that a duration of the read operation satisfies a time threshold, where identifying the logic state of the memory cell is based on the latch not activating prior to the duration satisfying the time threshold, identify a duration for a first voltage level of a digit line to satisfy a voltage threshold during an access operation, the duration based on the first state of the ferroelectric capacitor, the second state of the ferroelectric capacitor, and a voltage applied to the digit line, and identify a duration for a second voltage level of a node different from a digit line to satisfy a voltage threshold, the duration based on the first state of the ferroelectric capacitor and the second state of the ferroelectric capacitor. In some cases, the duration is based on a total charge stored on a ferroelectric capacitor of the ferroelectric memory cell. In some cases, the total charge includes a volatile charge of the ferroelectric capacitor and a stable charge of the ferroelectric capacitor.

[0195] Threshold manager 1165 may determine that a second voltage level at a node different from the digit line satisfies a voltage threshold, where the duration is based on the second voltage level satisfying the voltage threshold and sense, by a sense component, the second voltage level at the node, where the logic state is identified based on the second voltage level. In some cases, the voltage threshold is less than a biasing voltage used to generate a stable state of the memory cell.

[0196] FIG. 12 shows a diagram of a system 1200 including a device 1205 that supports time-based access of a memory cell in accordance with various embodiments of the present disclosure. Device 1205 may be an example of or include the components of memory controller 1015 as described above, *e.g.*, with reference to FIG. 10. Device 1205 may include components for bi-directional voice and data communications including components for transmitting and receiving communications, including memory controller 1215, memory cells 1220, basic input/output system (BIOS) component 1225, processor 1230, I/O controller 1235, and peripheral components 1240. These components may be in electronic communication via one or more busses (*e.g.*, bus 1210). Memory cells 1220 may store information (*i.e.*, in the form of a logical state) as described herein.

[0197] BIOS component 1225 be a software component that includes BIOS operated as firmware, which may initialize and run various hardware components. BIOS component 1225 may also manage data flow between a processor and various other components, *e.g.*, peripheral components, input/output control component, *etc.* BIOS component 1225 may include a program or software stored in read only memory (ROM), flash memory, or any other non-volatile memory.

[0198] Processor 1230 may include an intelligent hardware device, (*e.g.*, a general-purpose processor, a DSP, a central processing unit (CPU), a microcontroller, an ASIC, an FPGA, a programmable logic device, a discrete gate or transistor logic component, a discrete hardware component, or any combination thereof). In some cases, processor 1230 may be configured to operate a memory array using a memory controller. In other cases, a memory controller may be integrated into processor 1230. Processor 1230 may be configured to execute computer-readable instructions stored in a memory to perform various functions (*e.g.*, functions or tasks supporting time-based access of a memory cell).

[0199] I/O controller 1235 may manage input and output signals for device 1205. I/O controller 1235 may also manage peripherals not integrated into device 1205. In some cases, I/O controller 1235 may represent a physical connection or port to an external peripheral. In some cases, I/O controller 1235 may utilize an operating system such as iOS®, ANDROID®, MS-DOS®, MS-WINDOWS®, OS/2®, UNIX®, LINUX®, or another known operating system. In other cases, I/O controller 1235 may represent or interact with a modem, a keyboard, a mouse, a touchscreen, or a similar device. In some cases, I/O controller 1235

may be implemented as part of a processor. In some cases, a user may interact with device 1205 via I/O controller 1235 or via hardware components controlled by I/O controller 1235.

[0200] Peripheral components 1240 may include any input or output device, or an interface for such devices. Examples may include disk controllers, sound controller, graphics controller, Ethernet controller, modem, universal serial bus (USB) controller, a serial or parallel port, or peripheral card slots, such as peripheral component interconnect (PCI) or accelerated graphics port (AGP) slots.

[0201] FIG. 13 shows a flowchart illustrating a method 1300 for time-based access of a memory cell in accordance with various embodiments of the present disclosure. The operations of method 1300 may be implemented by a memory controller 1015 or its components as described herein. For example, the operations of method 1300 may be performed by a memory controller as described with reference to FIGs. 10 through 12. In some examples, a memory controller 1015 may execute a set of codes to control the functional elements of the device to perform the functions described below. Additionally or alternatively, the memory controller 1015 may perform portions of the functions described below using special-purpose hardware.

[0202] At block 1305 the memory controller 1015 may apply a time-varying signal to a latch after initiating a read operation on a memory cell. The operations of block 1305 may be performed according to the methods described with reference to FIGs. 1 through 9. In certain examples, portions of the operations of block 1305 may be performed by a signal manager as described with reference to FIGs. 10 through 12.

[0203] At block 1310 the memory controller 1015 may activate the latch based at least in part on a digit line that is coupled to the memory cell charging to a first voltage level as part of the read operation. The operations of block 1310 may be performed according to the methods described with reference to FIGs. 1 through 9. In certain examples, portions of the operations of block 1310 may be performed by a latch manager as described with reference to FIGs. 10 through 12.

[0204] At block 1315 the memory controller 1015 may identify a logic state of the memory cell based at least in part on a value of the time-varying signal present at the latch when the latch is activated. The operations of block 1315 may be performed according to the methods described with reference to FIGs. 1 through 9. In certain examples, portions of the

operations of block 1315 may be performed by a logic determiner as described with reference to FIGs. 10 through 12.

[0205] In some cases, a value of the time-varying signal varies in a predetermined manner over a predetermined interval of the time-varying signal. In some cases, the memory cell is configured to store at least three logic states. In some cases, the identified logic state of the memory cell is selected from the at least three logic states. In some cases, a configuration of the second time-varying signal is based at least in part on a configuration of the time-varying signal, wherein the time-varying signal and the second time-varying signal cooperate to define at least three logic states. In some cases, a configuration of the time-varying signal is based at least in part on an expected charge of the memory cell and the first voltage level. In some cases, the configuration of the time-varying signal is based at least in part on a number of logic states the memory cell is capable of storing. In some cases, the configuration of the time-varying signal is based at least in part on a number of latches used in the read operation. In some cases, a configuration of the time-varying signal and an interval of the time-varying signal is predetermined.

[0206] An apparatus for performing the method 1300 is described. The apparatus may include means for applying a time-varying signal to a latch after initiating a read operation on a memory cell, means for activating the latch based at least in part on a digit line that is coupled to the memory cell charging to a first voltage level as part of the read operation, and means for identifying a logic state of the memory cell based at least in part on a value of the time-varying signal present at the latch when the latch is activated.

[0207] In examples of the method 1300 and apparatus described above may further include processes, features, means, or instructions for isolating the memory cell from the latch after the digit line charges to the first voltage as part of the read operation. In some examples of the method 1300 and apparatus described above, the memory cell is configured to store at least three logic states and the identified logic state of the memory cell is selected from the at least three logic states.

[0208] In some examples of the method 1300 and apparatus described above may further include processes, features, means, or instructions for applying a second time-varying signal to a second latch based at least in part on performing the read operation on the memory cell, the second time-varying signal different from the time-varying signal, the second latch different from the latch. Some examples of the method 1300 and apparatus described above

may further include processes, features, means, or instructions for activating the second latch based at least in part on the digit line that is coupled to the memory cell charging to the first voltage level. In some cases, identifying the logic state of the memory cell is based at least in part on the time-varying signal present at the latch and the second time-varying signal present at the second latch when the latch and the second latch are activated.

[0209] In some examples of the method 1300 and apparatus described above, a configuration of the second time-varying signal is based at least in part on a configuration of the time-varying signal. In some cases, the time-varying signal and the second time-varying signal cooperate to define at least three logic states.

[0210] In some examples of the method 1300 and apparatus described above may further include processes, features, means, or instructions for charging the digit line of the memory cell as part of the read operation. In some cases, the time-varying signal is applied when charging the digit line begins. In some examples of the method 1300 and apparatus described above may further include processes, features, means, or instructions for sensing a second voltage level at a node different from the digit line. In some cases, the latch is activated based at least in part on the second voltage level satisfying a voltage threshold.

[0211] In some examples of the method 1300 and apparatus described above may further include processes, features, means, or instructions for outputting a signal based at least in part on the second voltage level satisfying the voltage threshold. In some cases, the latch is activated based at least in part on the signal. In some examples of the method 1300 and apparatus described above may further include processes, features, means, or instructions for determining that a duration of the read operation satisfies a time threshold. In some cases, identifying the logic state of the memory cell is based at least in part on the latch not activating prior to the duration satisfying the time threshold.

[0212] In some examples of the method 1300 and apparatus described above, a configuration of the time-varying signal is based at least in part on an expected charge of the memory cell and the first voltage level. In some examples of the method 1300 and apparatus described above, the configuration of the time-varying signal is based at least in part on a number of logic states the memory cell is capable of storing.

[0213] In some examples of the method 1300 and apparatus described above, the configuration of the time-varying signal is based at least in part on a number of latches used in the read operation. In some examples of the method 1300 and apparatus described above,

the value of the time-varying signal varies in a predetermined manner over a predetermined interval of the time-varying signal.

[0214] FIG. 14 shows a flowchart illustrating a method 1400 for time-based access of a memory cell in accordance with various embodiments of the present disclosure. The operations of method 1400 may be implemented by a memory controller 1015 or its components as described herein. For example, the operations of method 1400 may be performed by a memory controller as described with reference to FIGs. 10 through 12. In some examples, a memory controller 1015 may execute a set of codes to control the functional elements of the device to perform the functions described below. Additionally or alternatively, the memory controller 1015 may perform portions of the functions described below using special-purpose hardware.

[0215] At block 1405 the memory controller 1015 may sense a first state of a ferroelectric capacitor in a ferroelectric memory cell. The operations of block 1405 may be performed according to the methods described with reference to FIGs. 1 through 9. In certain examples, portions of the operations of block 1405 may be performed by a sensing manager as described with reference to FIGs. 10 through 12.

[0216] At block 1410 the memory controller 1015 may sense a second state of the ferroelectric capacitor different from the first state. The operations of block 1410 may be performed according to the methods described with reference to FIGs. 1 through 9. In certain examples, portions of the operations of block 1410 may be performed by a sensing manager as described with reference to FIGs. 10 through 12.

[0217] At block 1415 the memory controller 1015 may identify a logic state of the ferroelectric memory cell from at least three logic states based at least in part on the first state and the second state. The operations of block 1415 may be performed according to the methods described with reference to FIGs. 1 through 9. In certain examples, portions of the operations of block 1415 may be performed by a logic determiner as described with reference to FIGs. 10 through 12.

[0218] In some cases, the first state of the ferroelectric capacitor is associated with a polarization of the ferroelectric capacitor. In some cases, the second state of the ferroelectric capacitor is associated with a dielectric charge stored on the ferroelectric capacitor. In some examples, sensing a first state of the ferroelectric capacitor and sensing a second state of the ferroelectric capacitor may comprise sensing a combined state of the sensing capacitor. In

some cases, the combined state may be a combination (or superposition) of a polarized state and a dielectric charge state.

[0219] An apparatus for performing the method 1400 is described. The apparatus may include means for sensing a first state of a ferroelectric capacitor in a ferroelectric memory cell, means for sensing a second state of the ferroelectric capacitor different from the first state, and means for identifying a logic state of the ferroelectric memory cell from at least three logic states based at least in part on the first state and the second state.

[0220] In some examples of the method 1400 and apparatus described above, the first state of the ferroelectric capacitor is associated with a polarization of the ferroelectric capacitor. In some examples of the method 1400 and apparatus described above, the second state of the ferroelectric capacitor is associated with a dielectric charge stored on the ferroelectric capacitor.

[0221] In some examples of the method 1400 and apparatus described above may further include processes, features, means, or instructions for identifying a first bit of the logic state based at least in part on the first state and identifying a second bit of the logic state based at least in part on the second state. Some examples of the method 1400 and apparatus described above may further include processes, features, means, or instructions for activating at least two latches based at least in part on a voltage level of a node different from a digit line satisfying a voltage threshold.

[0222] In some examples of the method 1400 and apparatus described above may further include processes, features, means, or instructions for applying a first time-varying signal to one of the at least two latches, and applying a second time-varying signal different from the first time-varying signal to another of the at least two latches. In some cases, the logic state is identifying based at least in part on values of the first time-varying signal and the second time-varying signal when activating the at least two latches.

[0223] In some examples of the method 1400 and apparatus described above may further include processes, features, means, or instructions for identifying a duration for a first voltage level of a digit line to satisfy a voltage threshold during an access operation, the duration based at least in part on the first state of the ferroelectric capacitor, the second state of the ferroelectric capacitor, and a voltage applied to the digit line.

[0224] In some examples of the method 1400 and apparatus described above may further include processes, features, means, or instructions for identifying a duration for a second voltage level of a node different from a digit line to satisfy a voltage threshold, the duration based at least in part on the first state of the ferroelectric capacitor and the second state of the ferroelectric capacitor.

[0225] FIG. 15 shows a flowchart illustrating a method 1500 for time-based access of a memory cell in accordance with various embodiments of the present disclosure. The operations of method 1500 may be implemented by a memory controller 1015 or its components as described herein. For example, the operations of method 1500 may be performed by a memory controller as described with reference to FIGs. 10 through 12. In some examples, a memory controller 1015 may execute a set of codes to control the functional elements of the device to perform the functions described below. Additionally or alternatively, the memory controller 1015 may perform portions of the functions described below using special-purpose hardware.

[0226] At block 1505 the memory controller 1015 may activate a selection component of a ferroelectric memory cell. The operations of block 1505 may be performed according to the methods described with reference to FIGs. 1 through 9. In certain examples, portions of the operations of block 1505 may be performed by a cell manager as described with reference to FIGs. 10 through 12.

[0227] At block 1510 the memory controller 1015 may modify a first state of a ferroelectric capacitor of the ferroelectric memory cell based at least in part on a voltage being applied to the ferroelectric memory cell while the selection component is activated. The operations of block 1510 may be performed according to the methods described with reference to FIGs. 1 through 9. In certain examples, portions of the operations of block 1510 may be performed by a cell manager as described with reference to FIGs. 10 through 12.

[0228] At block 1515 the memory controller 1015 may deactivate the selection component. The operations of block 1515 may be performed according to the methods described with reference to FIGs. 1 through 9. In certain examples, portions of the operations of block 1515 may be performed by a cell manager as described with reference to FIGs. 10 through 12.

[0229] At block 1520 the memory controller 1015 may modify a second state of the ferroelectric capacitor based at least in part on the selection component being deactivated

while the voltage is applied to the ferroelectric memory cell. The operations of block 1520 may be performed according to the methods described with reference to FIGs. 1 through 9. In certain examples, portions of the operations of block 1520 may be performed by a cell manager as described with reference to FIGs. 10 through 12.

5 **[0230]** In some cases, the second state is a dielectric charge state of the ferroelectric capacitor. In some cases, modifying the first state of the ferroelectric capacitor comprises: applying a first voltage to the ferroelectric capacitor. In some cases, applying the first voltage to the ferroelectric capacitor comprises: applying a second voltage to a digit line coupled to the ferroelectric memory cell. In some cases, modifying the second state of the ferroelectric
10 capacitor comprises: applying a fourth voltage to the ferroelectric capacitor.

[0231] In some cases, applying the fourth voltage to the ferroelectric capacitor comprises: applying a fifth voltage to a digit line coupled to the ferroelectric memory cell while the selection component is deactivated, wherein the selection component is positioned between the ferroelectric capacitor and a plate line coupled to the ferroelectric memory cell.

15 **[0232]** In some cases, applying the fourth voltage to the ferroelectric capacitor comprises: applying a sixth voltage to a plate line coupled to the ferroelectric memory cell while the selection component is deactivated, wherein the selection component is positioned between the ferroelectric capacitor and a digit line coupled to the ferroelectric memory cell.

[0233] In some cases, the ferroelectric memory cell is configured to store at least three
20 logic states based at least in part on the first state of the ferroelectric capacitor and the second state of the ferroelectric capacitor. In some cases, the first state is a polarization state of the ferroelectric capacitor.

[0234] An apparatus for performing the method 1500 is described. The apparatus may include means for activating a selection component of a ferroelectric memory cell, means for
25 modifying a first state of a ferroelectric capacitor of the ferroelectric memory cell based at least in part on a voltage being applied to the ferroelectric memory cell while the selection component is activated, means for deactivating the selection component, and means for modifying a second state of the ferroelectric capacitor based at least in part on the selection component being deactivated while the voltage is applied to the ferroelectric memory cell.

30 **[0235]** In some examples of the method 1500 and apparatus described above may further include processes, features, means, or instructions for activating the selection component

while a plate line and a digit line coupled to the ferroelectric memory cell are grounded or virtually grounded. In some examples of the method 1500 and apparatus described above may further include processes, features, means, or instructions for applying a first voltage to the ferroelectric capacitor.

5 **[0236]** In some examples of the method 1500 and apparatus described above may further include processes, features, means, or instructions for applying a second voltage to a digit line coupled to the ferroelectric memory cell and applying a third voltage to a plate line coupled to the ferroelectric memory cell, the third voltage different from the second voltage. In some cases, the first voltage is based at least in part on the second voltage and the third
10 voltage.

[0237] In some examples of the method 1500 and apparatus described above may further include processes, features, means, or instructions for applying a fourth voltage to the ferroelectric capacitor. Some examples of the method 1400 and apparatus described above may further include processes, features, means, or instructions for applying a fifth voltage to
15 a digit line coupled to the ferroelectric memory cell, the selection component being deactivated while the fifth voltage is applied to the ferroelectric memory cell. In some cases, the selection component is positioned between the ferroelectric capacitor and a plate line coupled to the ferroelectric memory cell.

[0238] In some examples of the method 1500 and apparatus described above may further
20 include processes, features, means, or instructions for applying a sixth voltage to a plate line coupled to the ferroelectric memory cell, the selection component being deactivated while the sixth voltage is applied to the ferroelectric memory cell. In some cases, the selection component is positioned between the ferroelectric capacitor and a digit line coupled to the ferroelectric memory cell.

25 **[0239]** In some examples of the method 1500 and apparatus described above, the ferroelectric memory cell is configured to store at least three logic states based at least in part on the first state of the ferroelectric capacitor and the second state of the ferroelectric capacitor.

[0240] In some examples of the method 1500 and apparatus described above, the first
30 state is a polarization state of the ferroelectric capacitor and the second state is a dielectric charge state of the ferroelectric capacitor.

[0241] It should be noted that the methods described above describe possible implementations, and that the operations and the steps may be rearranged or otherwise modified and that other implementations are possible. Furthermore, embodiments from two or more of the methods may be combined.

5 [0242] Information and signals described herein may be represented using any of a variety of different technologies and techniques. For example, data, instructions, commands, information, signals, bits, symbols, and chips that may be referenced throughout the above description may be represented by voltages, currents, electromagnetic waves, magnetic fields or particles, optical fields or particles, or any combination thereof. Some drawings may
10 illustrate signals as a single signal; however, it will be understood by a person of ordinary skill in the art that the signal may represent a bus of signals, where the bus may have a variety of bit widths.

[0243] As used herein, the term “virtual ground” refers to a node of an electrical circuit that is held at a voltage of approximately zero volts (0V) but that is not directly connected
15 with ground. Accordingly, the voltage of a virtual ground may temporarily fluctuate and return to approximately 0V at steady state. A virtual ground may be implemented using various electronic circuit elements, such as a voltage divider consisting of operational amplifiers and resistors. Other implementations are also possible. “Virtual grounding” or “virtually grounded” means connected to approximately 0V.

20 [0244] The term “electronic communication” and “coupled” refer to a relationship between components that support electron flow between the components. This may include a direct connection between components or may include intermediate components. Components in electronic communication or coupled to one another may be actively exchanging electrons or signals (*e.g.*, in an energized circuit) or may not be actively
25 exchanging electrons or signals (*e.g.*, in a de-energized circuit) but may be configured to and operable to exchange electrons or signals upon a circuit being energized. By way of example, two components physically connected via a switch (*e.g.*, a transistor) are in electronic communication or may be coupled regardless of the state of the switch (*i.e.*, open or closed).

[0245] As used herein, the term “substantially” means that the modified characteristic (*e.g.*, a
30 verb or adjective modified by the term substantially) need not be absolute but is close enough so as to achieve the advantages of the characteristic.

[0246] As used herein, the term “electrode” may refer to an electrical conductor, and in some cases, may be employed as an electrical contact to a memory cell or other component of a memory array. An electrode may include a trace, wire, conductive line, conductive layer, or the like that provides a conductive path between elements or components of memory array

100.

[0247] The term “isolated” refers to a relationship between components in which electrons are not presently capable of flowing between them; components are isolated from each other if there is an open circuit between them. For example, two components physically connected by a switch may be isolated from each other when the switch is open.

[0248] As used herein, the term “shorting” refers to a relationship between components in which a conductive path is established between the components via the activation of a single intermediary component between the two components in question. For example, a first component shorted to a second component may exchange electrons with the second component when a switch between the two components is closed. Thus, shorting may be a dynamic operation that enables the flow of charge between components (or lines) that are in electronic communication.

[0249] The devices discussed herein, including memory array 100, may be formed on a semiconductor substrate, such as silicon, germanium, silicon-germanium alloy, gallium arsenide, gallium nitride, *etc.* In some cases, the substrate is a semiconductor wafer. In other cases, the substrate may be a silicon-on-insulator (SOI) substrate, such as silicon-on-glass (SOG) or silicon-on-sapphire (SOP), or epitaxial layers of semiconductor materials on another substrate. The conductivity of the substrate, or sub-regions of the substrate, may be controlled through doping using various chemical species including, but not limited to, phosphorous, boron, or arsenic. Doping may be performed during the initial formation or growth of the substrate, by ion-implantation, or by any other doping means.

[0250] A transistor or transistors discussed herein may represent a field-effect transistor (FET) and comprise a three terminal device including a source, drain, and gate. The terminals may be connected to other electronic elements through conductive materials, *e.g.*, metals. The source and drain may be conductive and may comprise a heavily-doped, *e.g.*, degenerate, semiconductor region. The source and drain may be separated by a lightly-doped semiconductor region or channel. If the channel is n-type (*i.e.*, majority carriers are electrons), then the FET may be referred to as a n-type FET. If the channel is p-type (*i.e.*,

majority carriers are holes), then the FET may be referred to as a p-type FET. The channel may be capped by an insulating gate oxide. The channel conductivity may be controlled by applying a voltage to the gate. For example, applying a positive voltage or negative voltage to an n-type FET or a p-type FET, respectively, may result in the channel becoming conductive.

5 A transistor may be “on” or “activated” when a voltage greater than or equal to the transistor’s threshold voltage is applied to the transistor gate. The transistor may be “off” or “deactivated” when a voltage less than the transistor’s threshold voltage is applied to the transistor gate.

[0251] The description set forth herein, in connection with the appended drawings,
10 describes example configurations and does not represent all the examples that may be implemented or that are within the scope of the claims. The term “exemplary” used herein means “serving as an example, instance, or illustration,” and not “preferred” or “advantageous over other examples.” The detailed description includes specific details for the purpose of providing an understanding of the described techniques. These techniques,
15 however, may be practiced without these specific details. In some instances, well-known structures and devices are shown in block diagram form in order to avoid obscuring the concepts of the described examples.

[0252] In the appended figures, similar components or features may have the same reference label. Further, various components of the same type may be distinguished by
20 following the reference label by a dash and a second label that distinguishes among the similar components. If just the first reference label is used in the specification, the description is applicable to any one of the similar components having the same first reference label irrespective of the second reference label.

[0253] Information and signals described herein may be represented using any of a
25 variety of different technologies and techniques. For example, data, instructions, commands, information, signals, bits, symbols, and chips that may be referenced throughout the above description may be represented by voltages, currents, electromagnetic waves, magnetic fields or particles, optical fields or particles, or any combination thereof.

[0254] The various illustrative blocks and modules described in connection with the
30 disclosure herein may be implemented or performed with a general-purpose processor, a DSP, an ASIC, an FPGA or other programmable logic device, discrete gate or transistor logic, discrete hardware components, or any combination thereof designed to perform the

functions described herein. A general-purpose processor may be a microprocessor, but in the alternative, the processor may be any conventional processor, controller, microcontroller, or state machine. A processor may also be implemented as a combination of computing devices (e.g., a combination of a digital signal processor (DSP) and a microprocessor, multiple microprocessors, one or more microprocessors in conjunction with a DSP core, or any other such configuration).

[0255] The functions described herein may be implemented in hardware, software executed by a processor, firmware, or any combination thereof. If implemented in software executed by a processor, the functions may be stored on or transmitted over as one or more instructions or code on a computer-readable medium. Other examples and implementations are within the scope of the disclosure and appended claims. For example, due to the nature of software, functions described above can be implemented using software executed by a processor, hardware, firmware, hardwiring, or combinations of any of these. Features implementing functions may also be physically located at various positions, including being distributed such that portions of functions are implemented at different physical locations. Also, as used herein, including in the claims, “or” as used in a list of items (for example, a list of items prefaced by a phrase such as “at least one of” or “one or more of”) indicates an inclusive list such that, for example, a list of at least one of A, B, or C means A or B or C or AB or AC or BC or ABC (*i.e.*, A and B and C). Also, as used herein, the phrase “based on” shall not be construed as a reference to a closed set of conditions. For example, an exemplary step that is described as “based on condition A” may be based on both a condition A and a condition B without departing from the scope of the present disclosure. In other words, as used herein, the phrase “based on” shall be construed in the same manner as the phrase “based at least in part on.”

[0256] Computer-readable media includes both non-transitory computer storage media and communication media including any medium that facilitates transfer of a computer program from one place to another. A non-transitory storage medium may be any available medium that can be accessed by a general purpose or special purpose computer. By way of example, and not limitation, non-transitory computer-readable media can comprise RAM, ROM, electrically erasable programmable read only memory (EEPROM), compact disk (CD) ROM or other optical disk storage, magnetic disk storage or other magnetic storage devices, or any other non-transitory medium that can be used to carry or store desired program code means in the form of instructions or data structures and that can be accessed by a general-

purpose or special-purpose computer, or a general-purpose or special-purpose processor.

Also, any connection is properly termed a computer-readable medium. For example, if the software is transmitted from a website, server, or other remote source using a coaxial cable, fiber optic cable, twisted pair, digital subscriber line (DSL), or wireless technologies such as infrared, radio, and microwave, then the coaxial cable, fiber optic cable, twisted pair, digital subscriber line (DSL), or wireless technologies such as infrared, radio, and microwave are included in the definition of medium. Disk and disc, as used herein, include CD, laser disc, optical disc, digital versatile disc (DVD), floppy disk and Blu-ray disc where disks usually reproduce data magnetically, while discs reproduce data optically with lasers. Combinations of the above are also included within the scope of computer-readable media.

[0257] The description herein is provided to enable a person skilled in the art to make or use the disclosure. Various modifications to the disclosure will be readily apparent to those skilled in the art, and the generic principles defined herein may be applied to other variations without departing from the scope of the disclosure. Thus, the disclosure is not limited to the examples and designs described herein, but is to be accorded the broadest scope consistent with the principles and novel features disclosed herein.

CLAIMS

What is claimed is:

- 1 1. An apparatus, comprising:
2 a memory cell in electronic communication with a digit line;
3 a sense component coupled to the memory cell, the sense component
4 configured to output a signal that is based at least in part on a duration of time for a voltage
5 level input into the sense component to satisfy a voltage threshold; and
6 a first latch coupled to the sense component, the first latch configured to
7 output a value of a first signal indicative of a logic state of the memory cell based at least in
8 part on the signal received from the sense component.
- 1 2. The apparatus of claim 1, further comprising:
2 a controller to identify the logic state of the memory cell based at least in part
3 on the value of the first signal when the voltage level input into the sense component satisfies
4 the voltage threshold.
- 1 3. The apparatus of claim 1, wherein:
2 the memory cell is configured to store at least three logic states.
- 1 4. The apparatus of claim 3, further comprising:
2 a second latch coupled to the sense component, the second latch configured to
3 receive a second signal indicative of a first bit of a logic state identifier associated with the
4 memory cell, wherein the first signal is indicative of a second bit of the logic state identifier.
- 1 5. The apparatus of claim 4, further comprising:
2 a controller to identify the logic state of the memory cell based at least in part
3 on the first bit and the second bit of the logic state identifier.
- 1 6. The apparatus of claim 1, further comprising:
2 a cascode having a first node coupled to the digit line and a second node
3 coupled to the sense component, the cascode being configured to apply a voltage to the digit
4 line during a read operation.
- 1 7. The apparatus of claim 1, wherein the memory cell comprises:

2 a ferroelectric capacitor configured to store a polarization state and a dielectric
3 charge state.

1 8. The apparatus of claim 1, wherein:
2 the sense component in an inverter.

1 9. The apparatus of claim 1, wherein:
2 the first latch is activated by the signal output from the sense component.

1 10. A method, comprising:
2 applying a time-varying signal to a latch after initiating a read operation on a
3 memory cell;
4 activating the latch based at least in part on a digit line that is coupled to the
5 memory cell charging to a first voltage level as part of the read operation; and
6 identifying a logic state of the memory cell based at least in part on a value of
7 the time-varying signal present at the latch when the latch is activated.

1 11. The method of claim 10, further comprising:
2 isolating the memory cell from the latch after the digit line charges to the first
3 voltage as part of the read operation.

1 12. The method of claim 10, wherein:
2 the memory cell is configured to store at least three logic states; and
3 the identified logic state of the memory cell is selected from the at least three
4 logic states.

1 13. The method of claim 12, further comprising:
2 applying a second time-varying signal to a second latch based at least in part
3 on performing the read operation on the memory cell, the second time-varying signal
4 different from the time-varying signal, the second latch different from the latch.

1 14. The method of claim 13, further comprising:
2 activating the second latch based at least in part on the digit line that is
3 coupled to the memory cell charging to the first voltage level, wherein identifying the logic
4 state of the memory cell is based at least in part on the time-varying signal present at the latch

5 and the second time-varying signal present at the second latch when the latch and the second
6 latch are activated.

1 15. The method of claim 13, wherein:
2 a configuration of the second time-varying signal is based at least in part on a
3 configuration of the time-varying signal, wherein the time-varying signal and the second
4 time-varying signal cooperate to define at least three logic states.

1 16. The method of claim 10, further comprising:
2 charging the digit line of the memory cell as part of the read operation,
3 wherein the time-varying signal is applied when charging the digit line begins.

1 17. The method of claim 10, further comprising:
2 sensing a second voltage level at a node different from the digit line, wherein
3 the latch is activated based at least in part on the second voltage level satisfying a voltage
4 threshold.

1 18. The method of claim 17, further comprising:
2 outputting a signal based at least in part on the second voltage level satisfying
3 the voltage threshold, wherein the latch is activated based at least in part on the signal.

1 19. The method of claim 10, further comprising:
2 determining that a duration of the read operation satisfies a time threshold,
3 wherein identifying the logic state of the memory cell is based at least in part on the latch not
4 activating prior to the duration satisfying the time threshold.

1 20. The method of claim 10, wherein:
2 a configuration of the time-varying signal is based at least in part on an
3 expected charge of the memory cell and the first voltage level.

1 21. The method of claim 20, wherein:
2 the configuration of the time-varying signal is based at least in part on a
3 number of logic states the memory cell is capable of storing.

1 22. The method of claim 21, wherein:
2 the configuration of the time-varying signal is based at least in part on a
3 number of latches used in the read operation.

1 23. The method of claim 10, wherein:
2 the value of the time-varying signal varies in a predetermined manner over a
3 predetermined interval of the time-varying signal.

1 24. An apparatus, comprising:
2 a ferroelectric memory cell comprising:
3 a selection component in electronic communication with an access
4 line;
5 a ferroelectric capacitor coupled to the selection component, the
6 ferroelectric capacitor configured to store a polarization state and a charge state; and
7 a controller operable to identify a logic state of the ferroelectric memory cell
8 from a set of at least three logic states based at least in on the polarization state and the
9 charge state.

1 25. The apparatus of claim 24, further comprising:
2 a sense component coupled to the ferroelectric memory cell, the sense
3 component configured to output a signal based at least in part on a voltage satisfying a
4 voltage threshold.

1 26. The apparatus of claim 24, further comprising:
2 at least two latches coupled to the ferroelectric memory cell, the at least two
3 latches configured to output a value of a first time-varying signal and a value of a second
4 time-varying signal based at least in part on receiving a signal indicative that a voltage
5 satisfies a voltage threshold.

1 27. The apparatus of claim 24, further comprising:
2 a cascode coupled to a digit line, the cascode configured to apply a first
3 voltage to the digit line during an access operation.

1 28. The apparatus of claim 27, further comprising:
2 a sense component coupled to a node of the cascode different from the digit
3 line, the sense component configured to detect a second voltage present on the node, wherein
4 the second voltage is based at least in part on a voltage level of the digit line.

1 29. The apparatus of claim 28, further comprising:

2 a first latch coupled to an output of the sense component, the first latch
3 configured to receive a signal indicative that the second voltage present on the node satisfies
4 a voltage threshold.

1 30. The apparatus of claim 29, further comprising:
2 a second latch coupled to the output of the sense component, the second latch
3 configured to receive the signal.

1 31. The apparatus of claim 30, wherein:
2 the controller is coupled to outputs of the first latch and the second latch; and
3 the controller is operable to identify the logic state of the ferroelectric memory
4 cell based at least in part a first output signal received from the first latch and a second output
5 signal received from the second latch.

1 32. The apparatus of claim 30, wherein:
2 the first latch is configured to receive a first time-varying signal to indicate at
3 least in part the logic state of the ferroelectric memory cell; and
4 the second latch is configured to receive a second time-varying signal to
5 indicate at least in part the logic state of the ferroelectric memory cell, the second time-
6 varying signal different from the first time-varying signal.

1 33. The apparatus of claim 32, wherein:
2 the first latch is configured to output a value of the first time-varying signal
3 based at least in part on receiving the signal indicative of the second voltage satisfying the
4 voltage threshold; and
5 the second latch is configured to output a value of the second time-varying
6 signal based at least in part on receiving the signal indicative of the second voltage satisfying
7 the voltage threshold.

1 34. The apparatus of claim 24, wherein:
2 the access line is a plate line or a digit line.

1 35. The apparatus of claim 24, wherein:
2 the ferroelectric capacitor is coupled to a second access line different from the
3 access line.

1 36. The apparatus of claim 24, wherein:
2 the polarization state stored on the ferroelectric capacitor is in a stable state.

1 37. The apparatus of claim 24, wherein:
2 the charge state stored on the ferroelectric capacitor is in a volatile state.

1 38. A method, comprising:
2 sensing a first state of a ferroelectric capacitor in a ferroelectric memory cell;
3 sensing a second state of the ferroelectric capacitor different from the first
4 state; and
5 identifying a logic state of the ferroelectric memory cell from at least three
6 logic states based at least in part on the first state and the second state.

1 39. The method of claim 38, wherein:
2 the first state of the ferroelectric capacitor is associated with a polarization of
3 the ferroelectric capacitor.

1 40. The method of claim 38, wherein:
2 the second state of the ferroelectric capacitor is associated with a dielectric
3 charge stored on the ferroelectric capacitor.

1 41. The method of claim 38, further comprising:
2 identifying a first bit of the logic state based at least in part on the first state;
3 and
4 identifying a second bit of the logic state based at least in part on the second
5 state.

1 42. The method of claim 38, further comprising:
2 activating at least two latches based at least in part on a voltage level of a node
3 different from a digit line satisfying a voltage threshold.

1 43. The method of claim 42, further comprising:
2 applying a first time-varying signal to one of the at least two latches; and
3 applying a second time-varying signal different from the first time-varying
4 signal to another of the at least two latches,

5 wherein the logic state is identifying based at least in part on values of the first
6 time-varying signal and the second time-varying signal when activating the at least two
7 latches.

1 44. The method of claim 38, further comprising:
2 identifying a duration for a first voltage level of a digit line to satisfy a voltage
3 threshold during an access operation, the duration based at least in part on the first state of the
4 ferroelectric capacitor, the second state of the ferroelectric capacitor, and a voltage applied to
5 the digit line.

1 45. The method of claim 38, further comprising:
2 identifying a duration for a second voltage level of a node different from a
3 digit line to satisfy a voltage threshold, the duration based at least in part on the first state of
4 the ferroelectric capacitor and the second state of the ferroelectric capacitor.

1 46. A method, comprising:
2 activating a selection component of a ferroelectric memory cell;
3 modifying a first state of a ferroelectric capacitor of the ferroelectric memory
4 cell based at least in part on a voltage being applied to the ferroelectric memory cell while the
5 selection component is activated;
6 deactivating the selection component; and
7 modifying a second state of the ferroelectric capacitor based at least in part on
8 the selection component being deactivated while the voltage is applied to the ferroelectric
9 memory cell.

1 47. The method of claim 46, further comprising:
2 activating the selection component while a plate line and a digit line coupled
3 to the ferroelectric memory cell are grounded or virtually grounded.

1 48. The method of claim 46, wherein modifying the first state of the
2 ferroelectric capacitor comprises:
3 applying a first voltage to the ferroelectric capacitor.

1 49. The method of claim 48, wherein applying the first voltage to the
2 ferroelectric capacitor comprises:
3 applying a second voltage to a digit line coupled to the ferroelectric memory
4 cell; and
5 applying a third voltage to a plate line coupled to the ferroelectric memory
6 cell, the third voltage different from the second voltage, wherein the first voltage is based at
7 least in part on the second voltage and the third voltage.

1 50. The method of claim 46, wherein modifying the second state of the
2 ferroelectric capacitor comprises:
3 applying a fourth voltage to the ferroelectric capacitor.

1 51. The method of claim 50, wherein applying the fourth voltage to the
2 ferroelectric capacitor comprises:
3 applying a fifth voltage to a digit line coupled to the ferroelectric memory cell,
4 the selection component being deactivated while the fifth voltage is applied to the
5 ferroelectric memory cell, wherein the selection component is positioned between the
6 ferroelectric capacitor and a plate line coupled to the ferroelectric memory cell.

1 52. The method of claim 50, wherein applying the fourth voltage to the
2 ferroelectric capacitor comprises:
3 applying a sixth voltage to a plate line coupled to the ferroelectric memory
4 cell, the selection component being deactivated while the sixth voltage is applied to the
5 ferroelectric memory cell, wherein the selection component is positioned between the
6 ferroelectric capacitor and a digit line coupled to the ferroelectric memory cell.

1 53. The method of claim 46, wherein:
2 the ferroelectric memory cell is configured to store at least three logic states
3 based at least in part on the first state of the ferroelectric capacitor and the second state of the
4 ferroelectric capacitor.

1 54. The method of claim 46, wherein:
2 the first state is a polarization state of the ferroelectric capacitor; and
3 the second state is a dielectric charge state of the ferroelectric capacitor.

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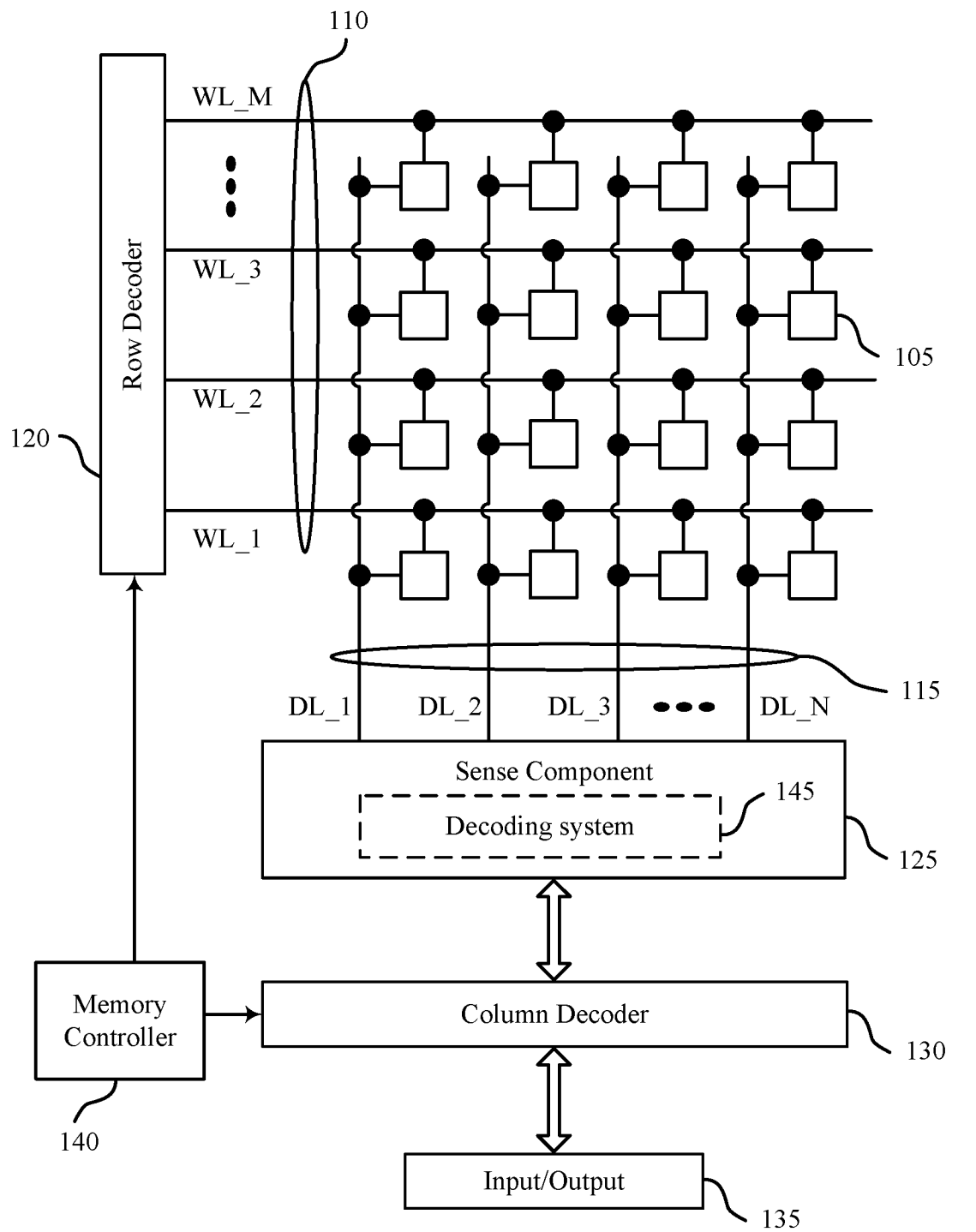


FIG. 1

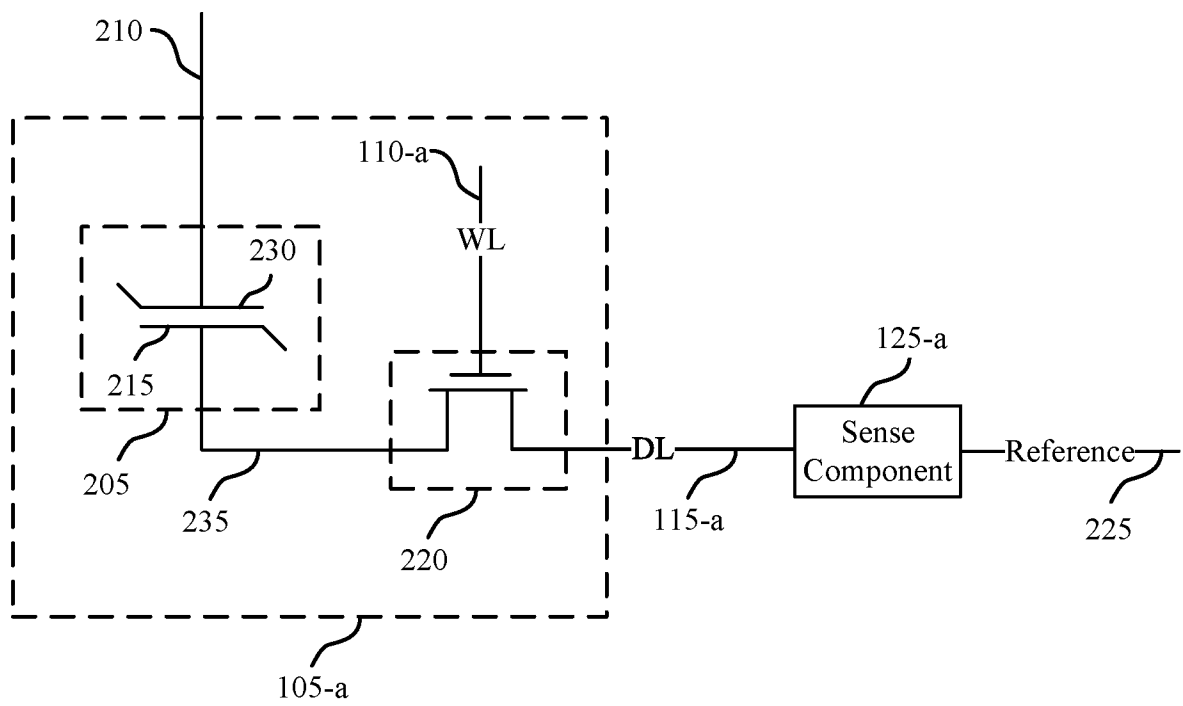


FIG. 2

200

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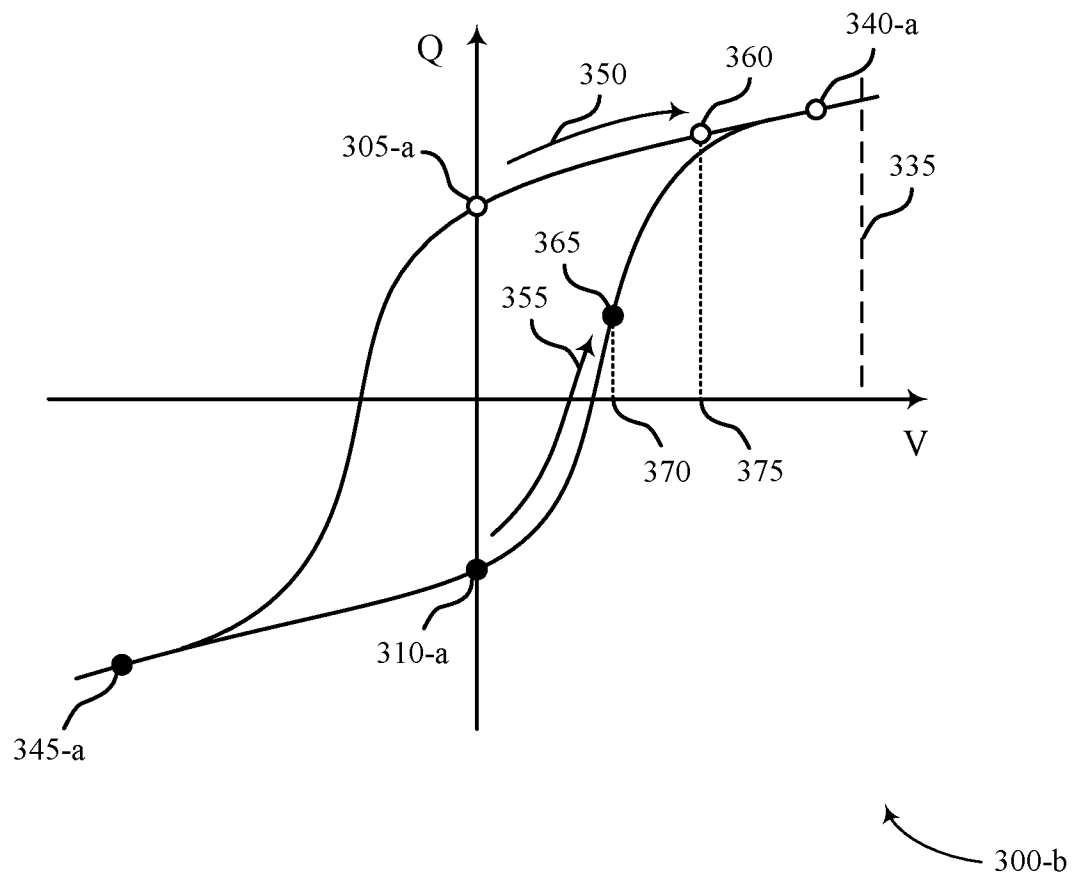
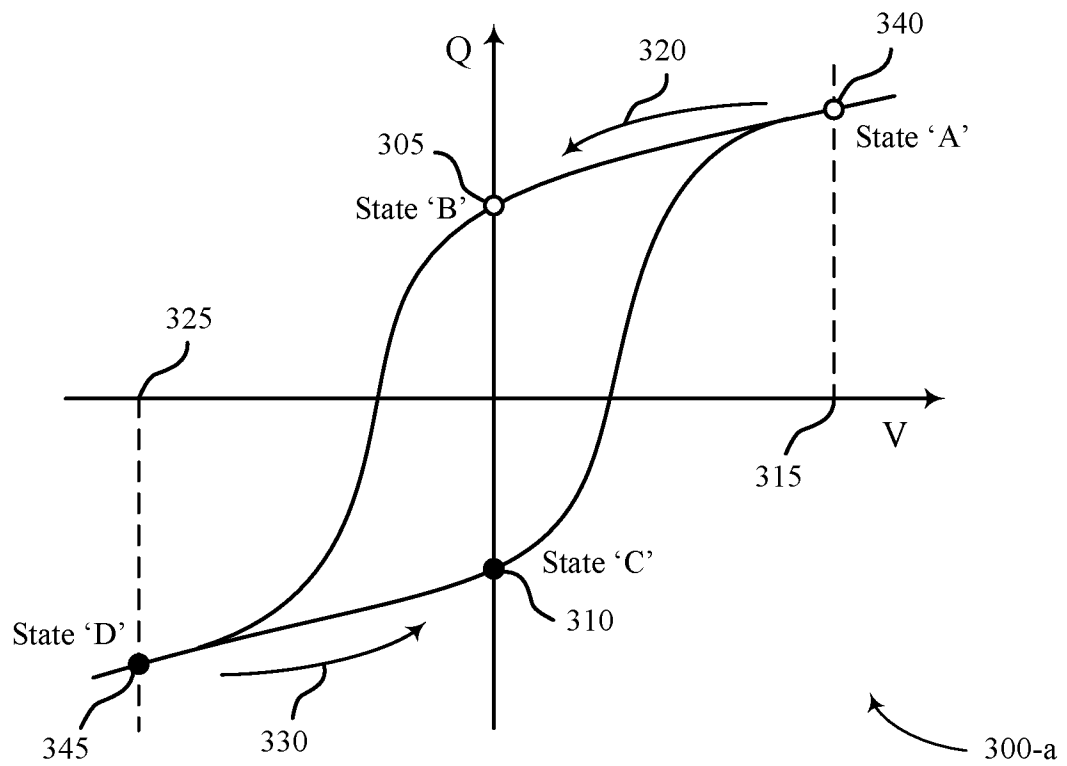


FIG. 3

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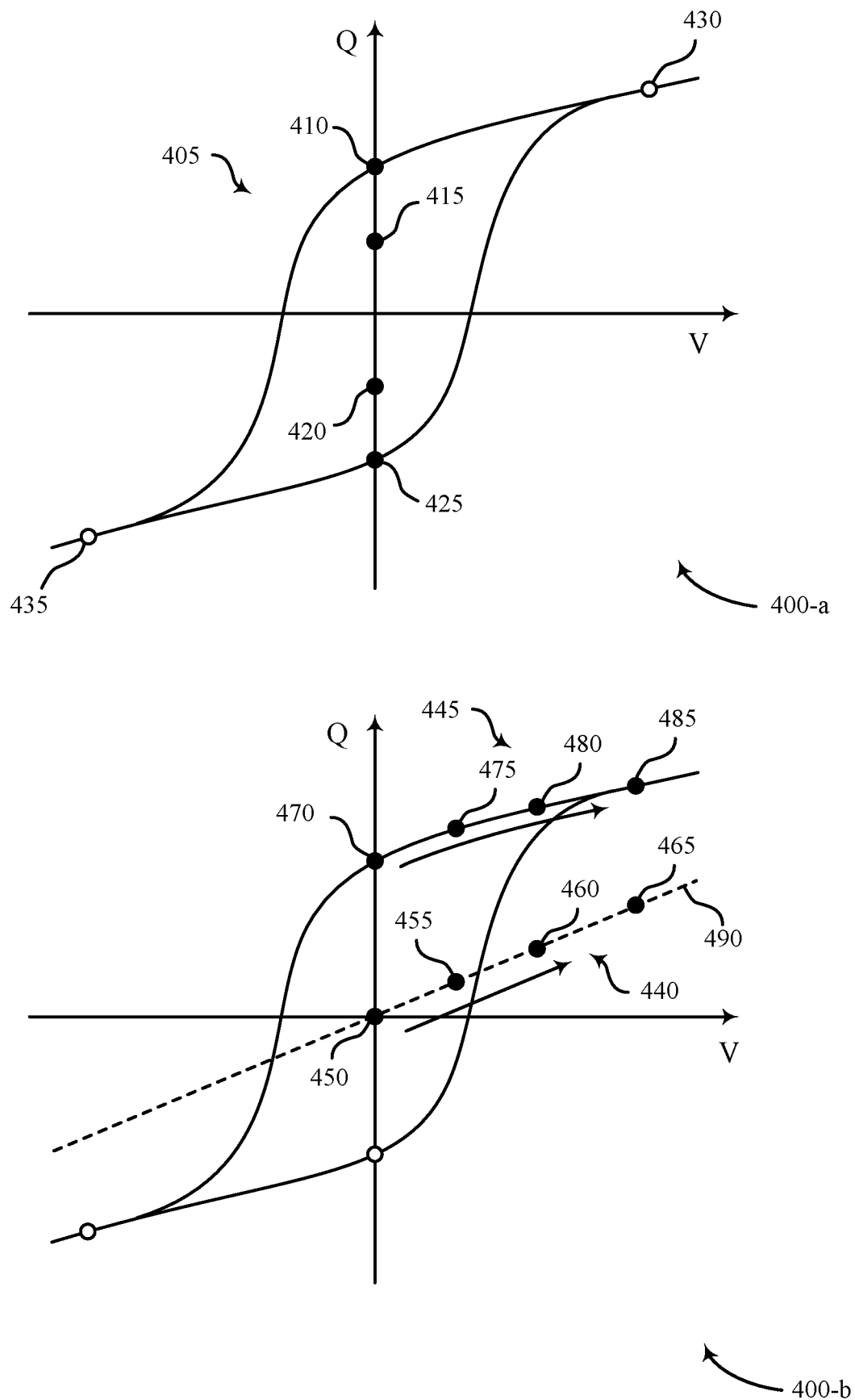


FIG. 4

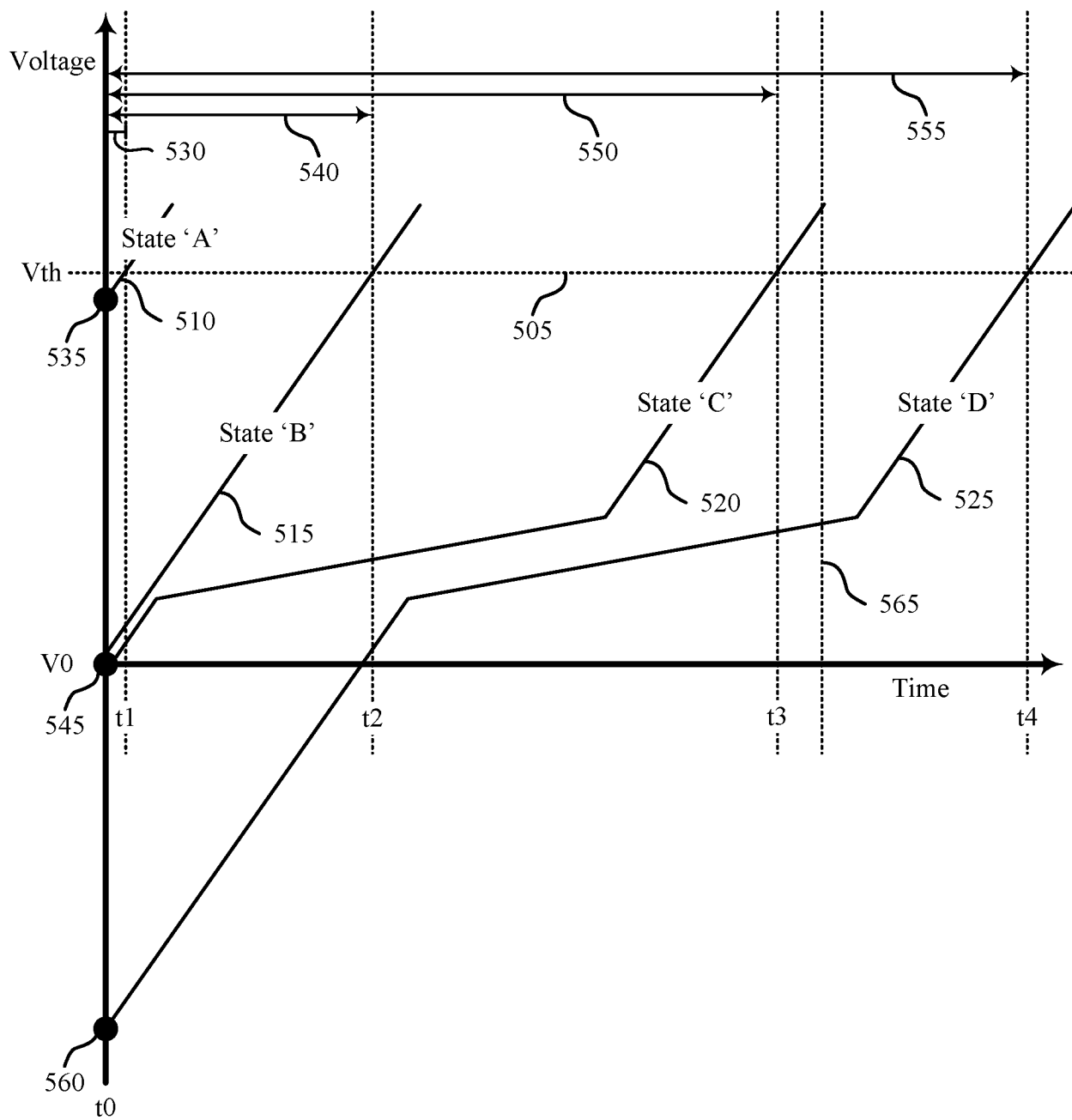


FIG. 5

500

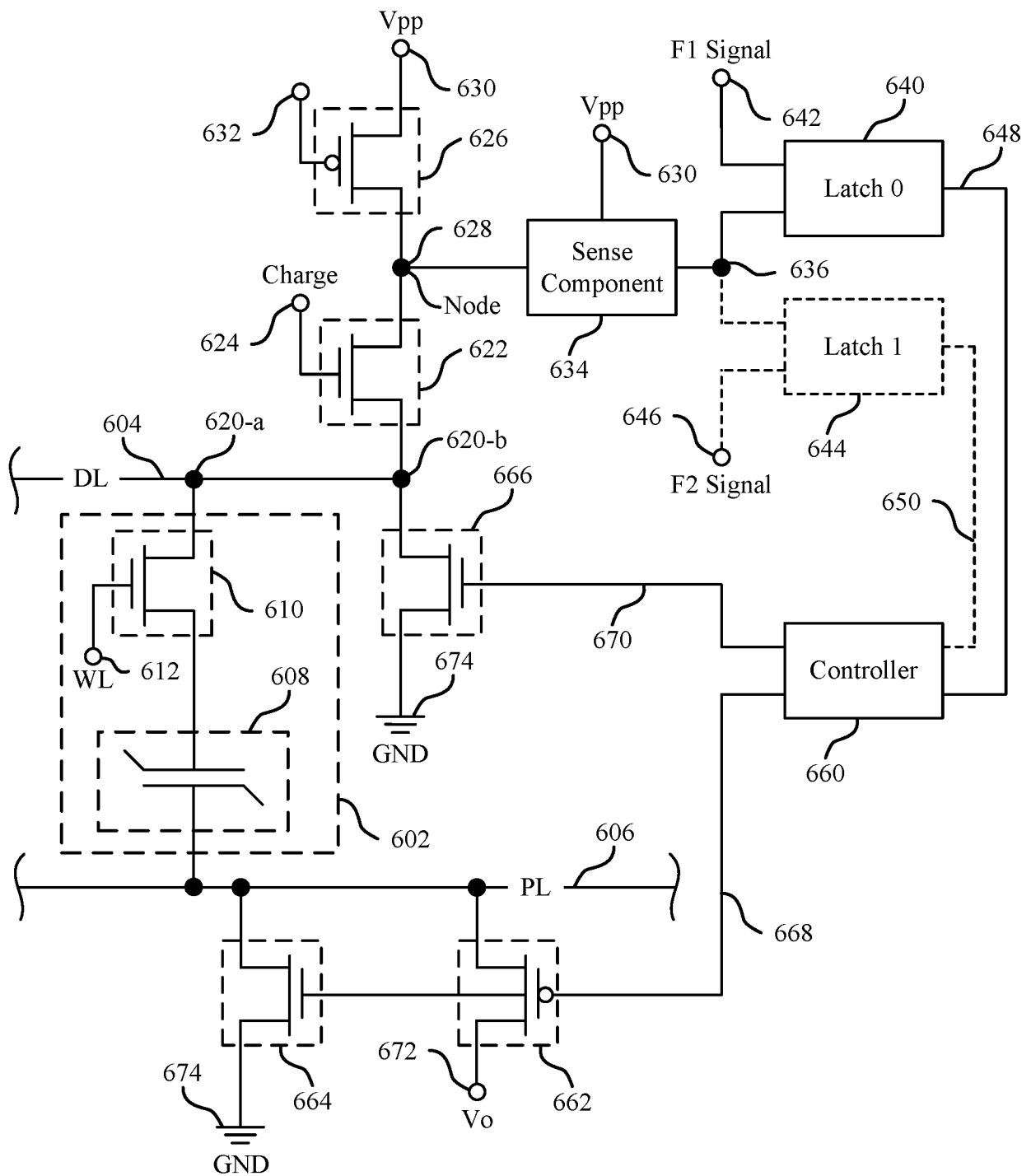


FIG. 6

600

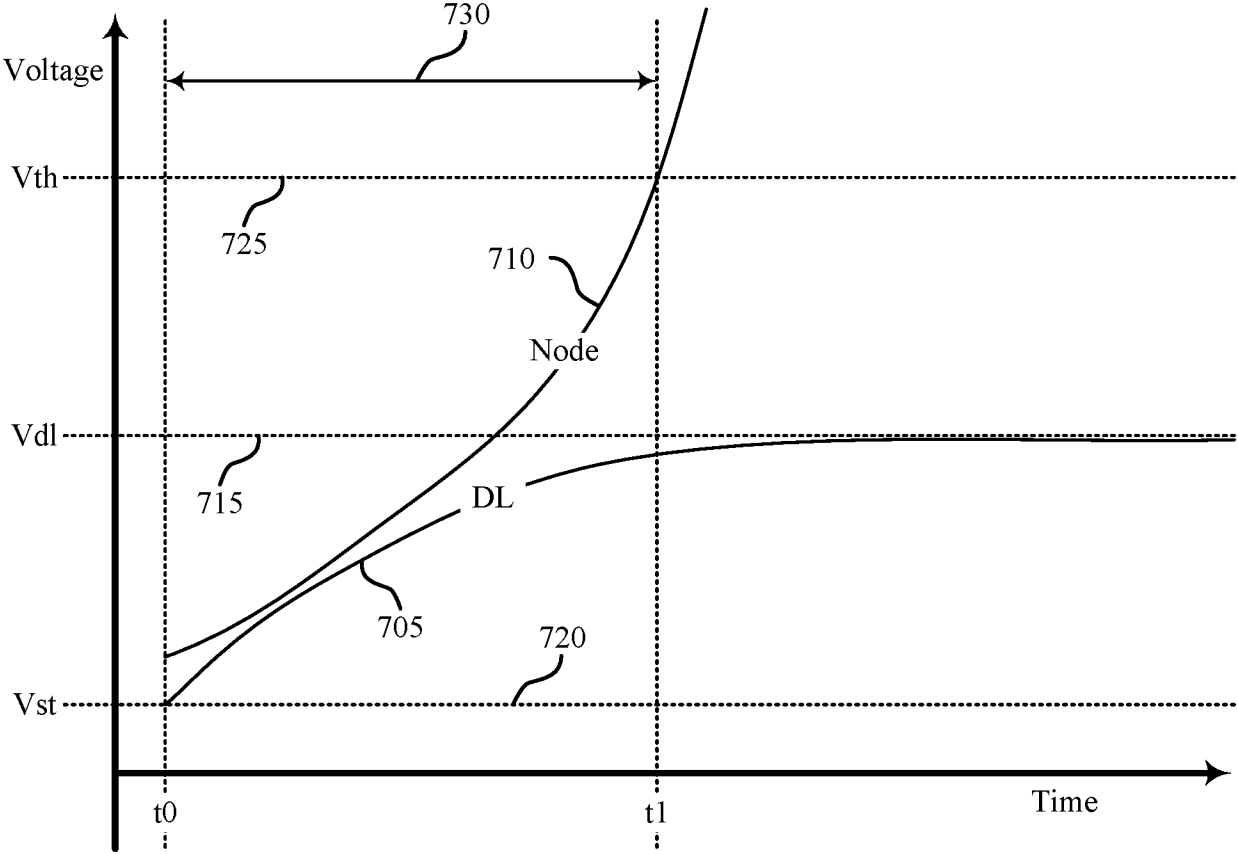


FIG. 7

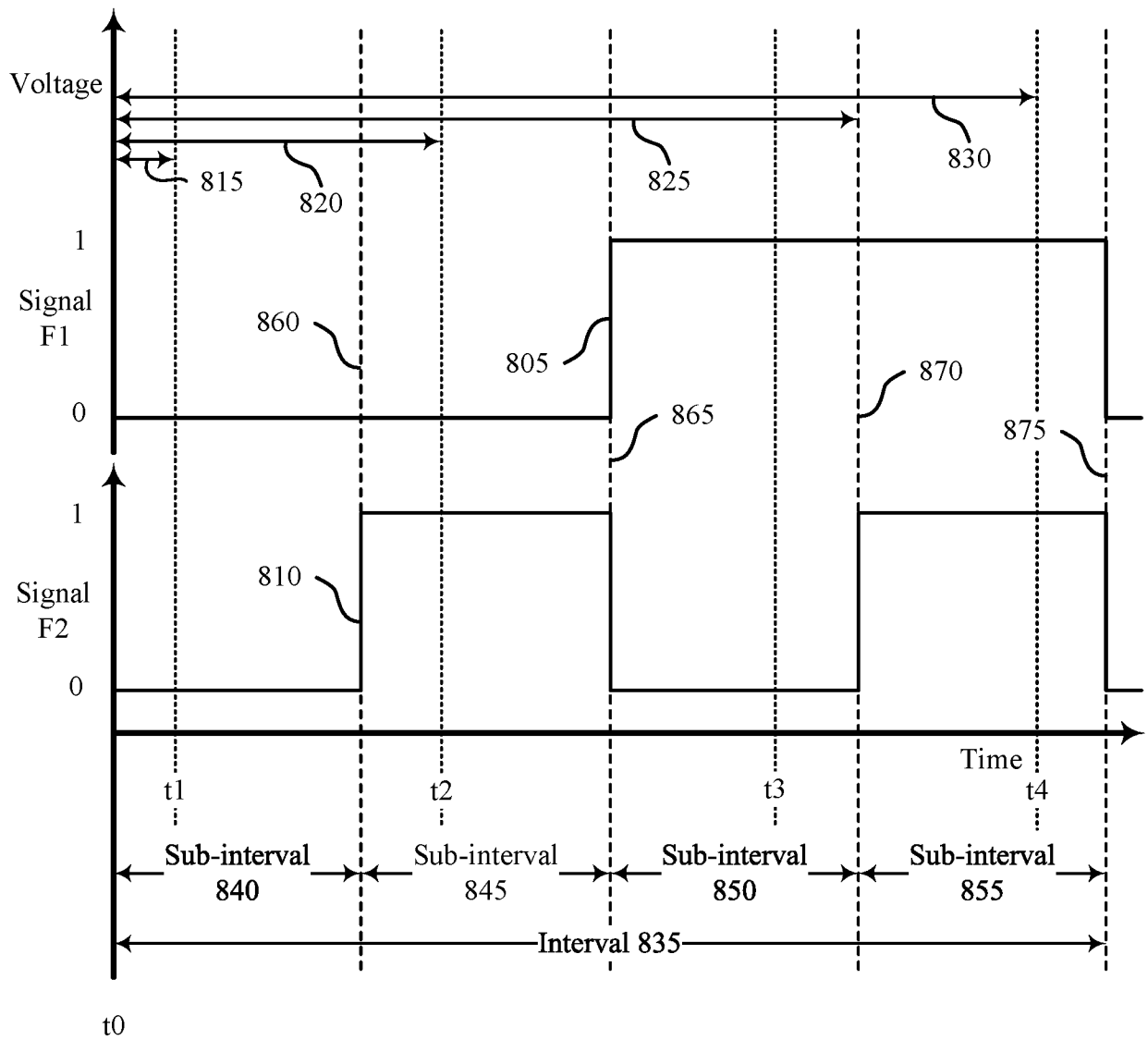


FIG. 8

800

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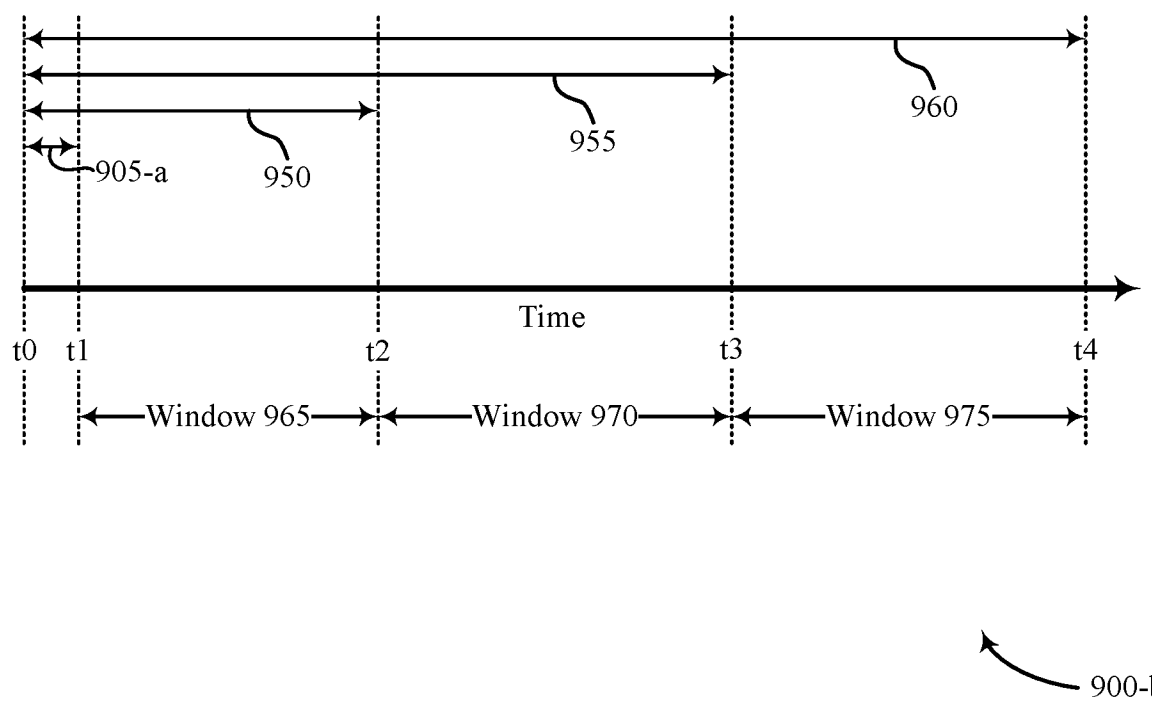
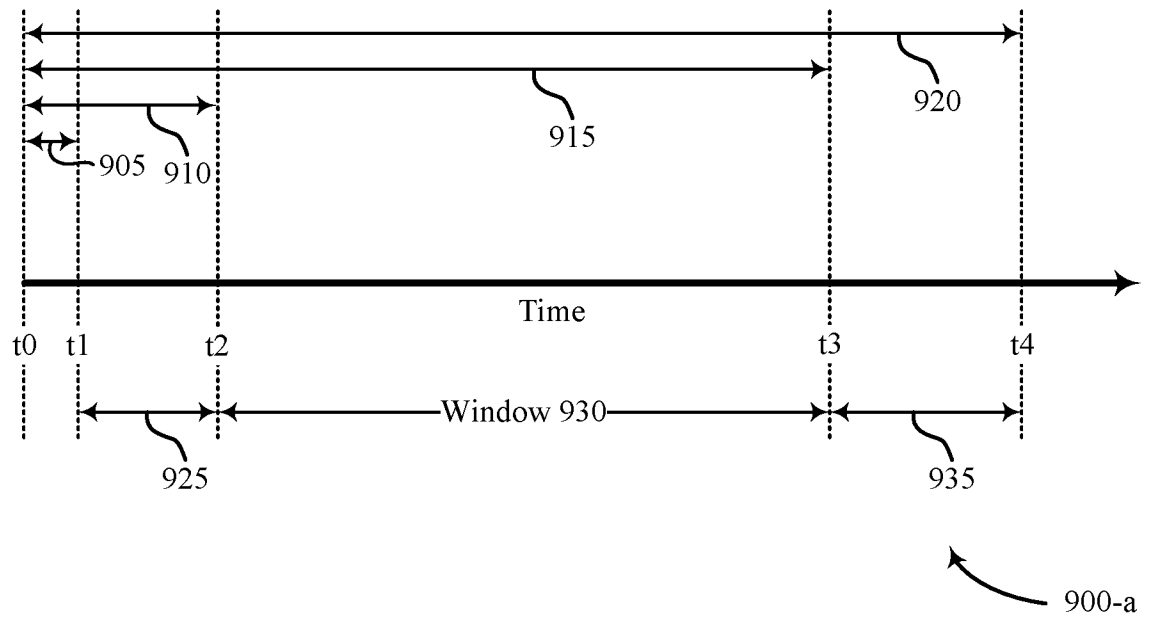


FIG. 9

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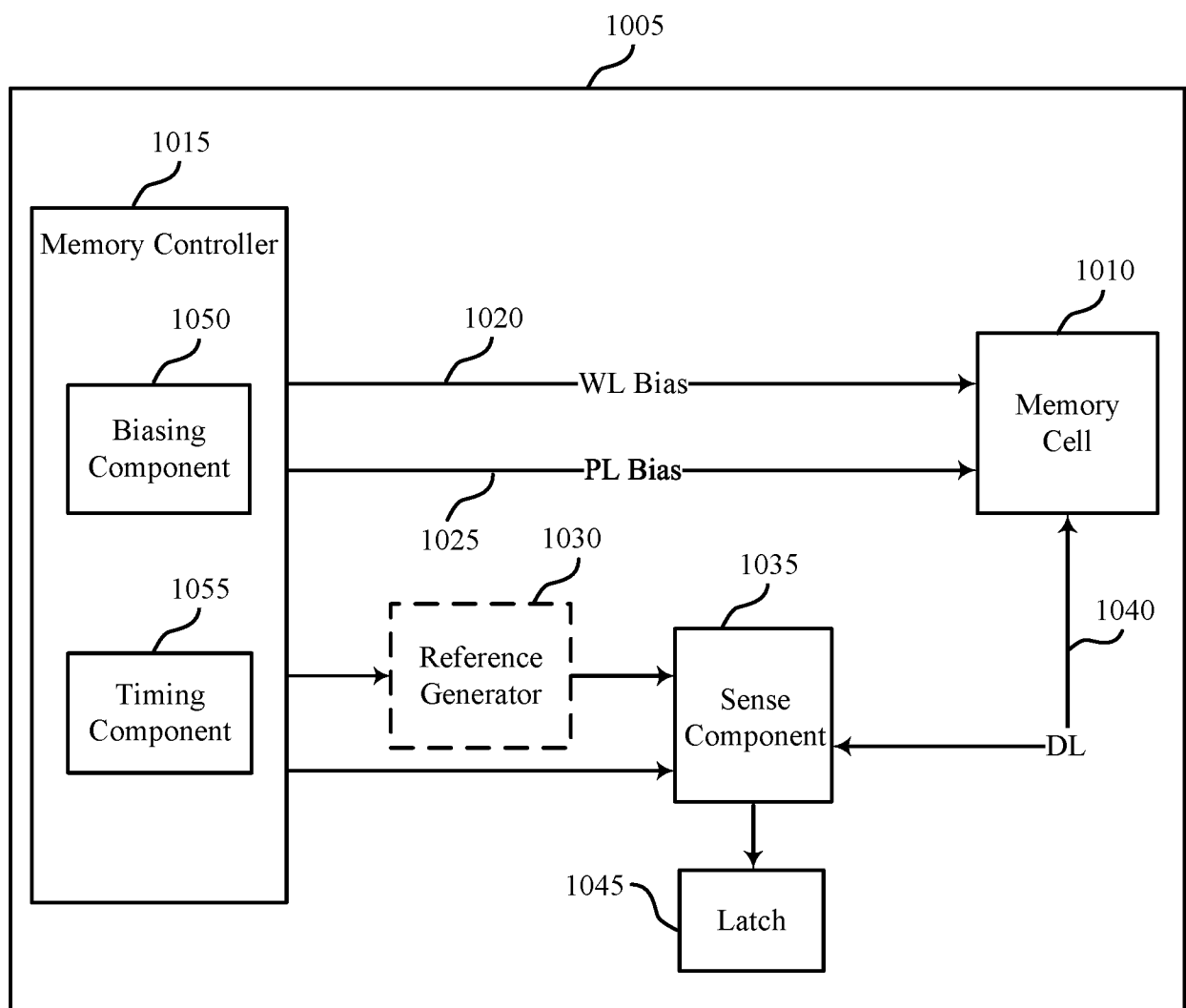


FIG. 10

1000

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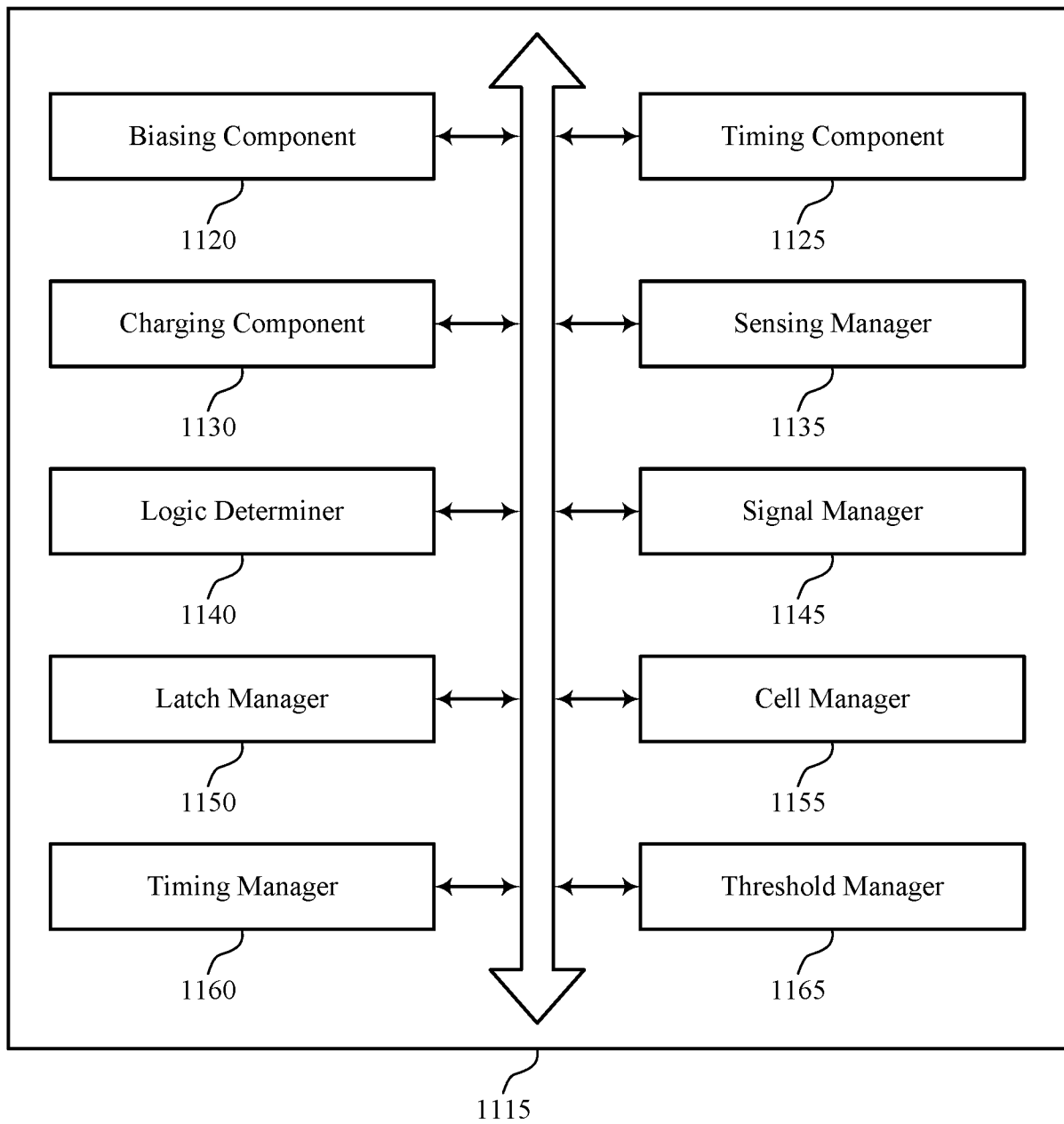


FIG. 11

1100

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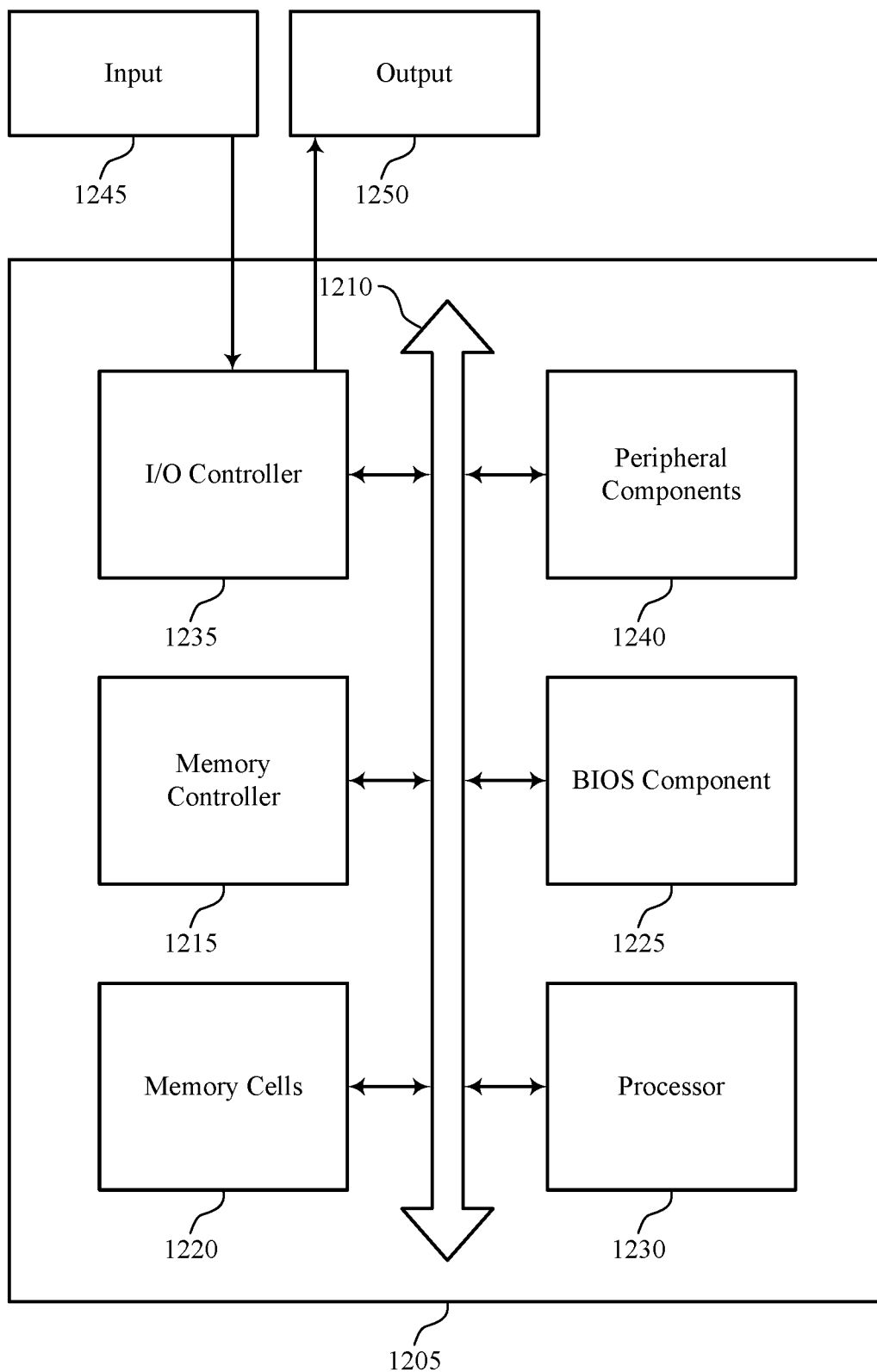


FIG. 12

1200

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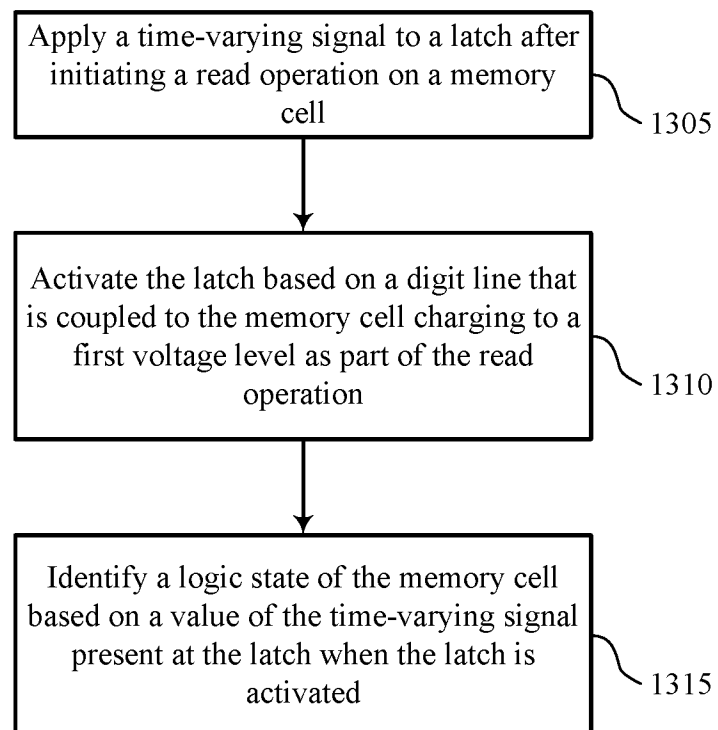


FIG. 13

1300

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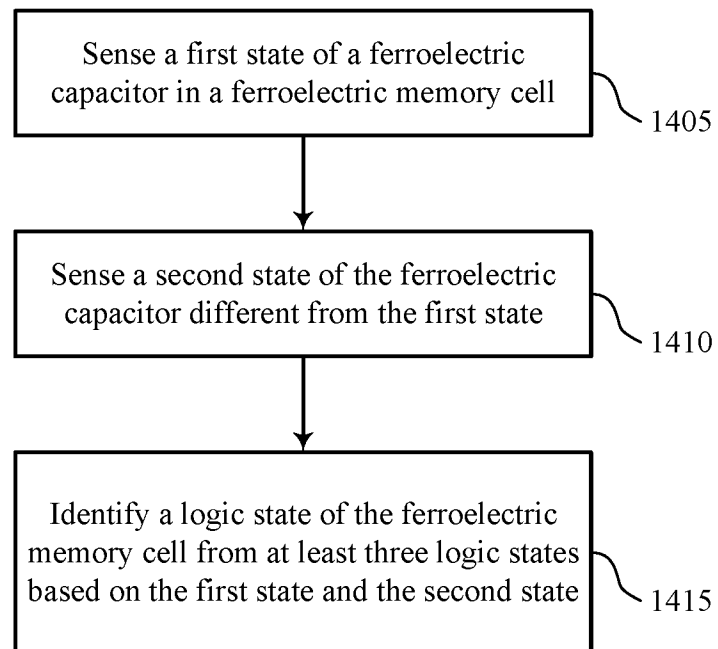


FIG. 14

1400

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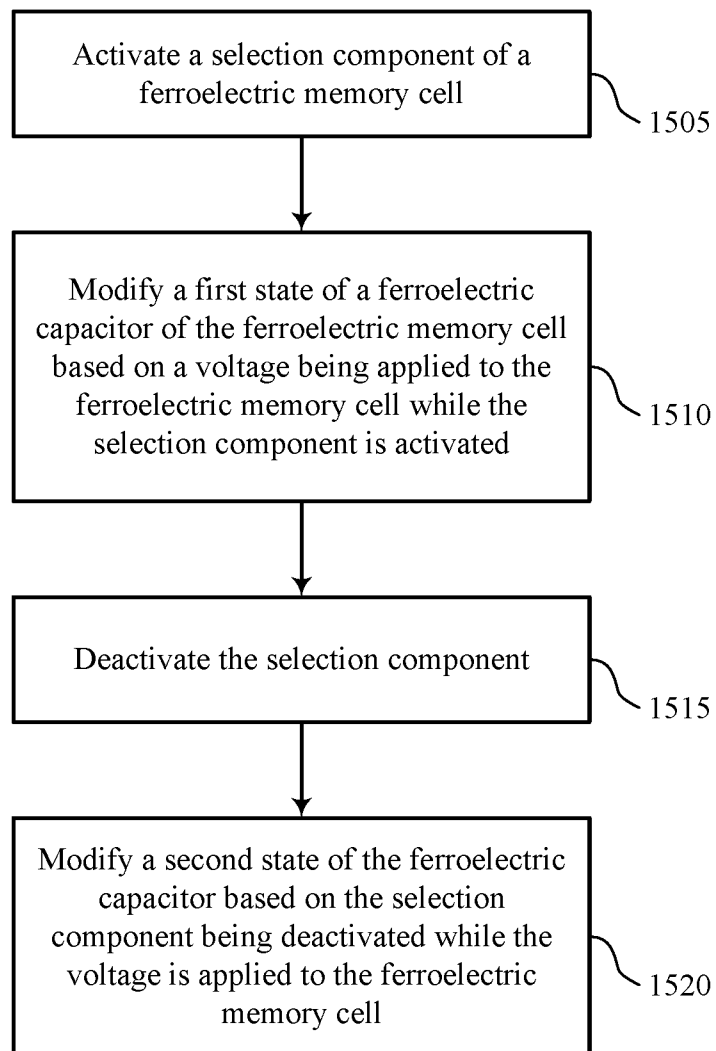


FIG. 15

1500

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2018/035089**A. CLASSIFICATION OF SUBJECT MATTER****G11C 11/22(2006.01)i**

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

G11C 11/22; G06F 12/00; H01L 27/115

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Korean utility models and applications for utility models

Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

eKOMPASS(KIPO internal) & Keywords: ferroelectric, memory, capacitor, sensing, multi-logic, multi-level, polarization, charge, state, and similar terms.

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 2004-0233744 A1 (JOHN ANTHONY RODRIGUEZ et al.) 25 November 2004 See paragraphs [0008], [0014], [0050]-[0051]; and claims 18, 20-21, 24.	1-54
A	US 2003-0198077 A1 (MICHIHITO UEDA et al.) 23 October 2003 See paragraphs [0113]-[0167]; and figures 1-18.	1-54
A	US 2014-0233296 A1 (TAE WON NOH et al.) 21 August 2014 See paragraphs [0048]-[0073]; and figures 1-3.	1-54
A	US 2005-0219892 A1 (SHENG CHIH LAI et al.) 06 October 2005 See paragraphs [0019]-[0031]; and figures 1-7.	1-54
A	US 2007-0260817 A1 (CHANG WAN HA) 08 November 2007 See paragraphs [0031]-[0053]; and figures 4-9.	1-54



Further documents are listed in the continuation of Box C.



See patent family annex.

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"P" document published prior to the international filing date but later than the priority date claimed

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"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search

30 October 2018 (30.10.2018)

Date of mailing of the international search report

30 October 2018 (30.10.2018)

Name and mailing address of the ISA/KR

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INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.

PCT/US2018/035089

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