

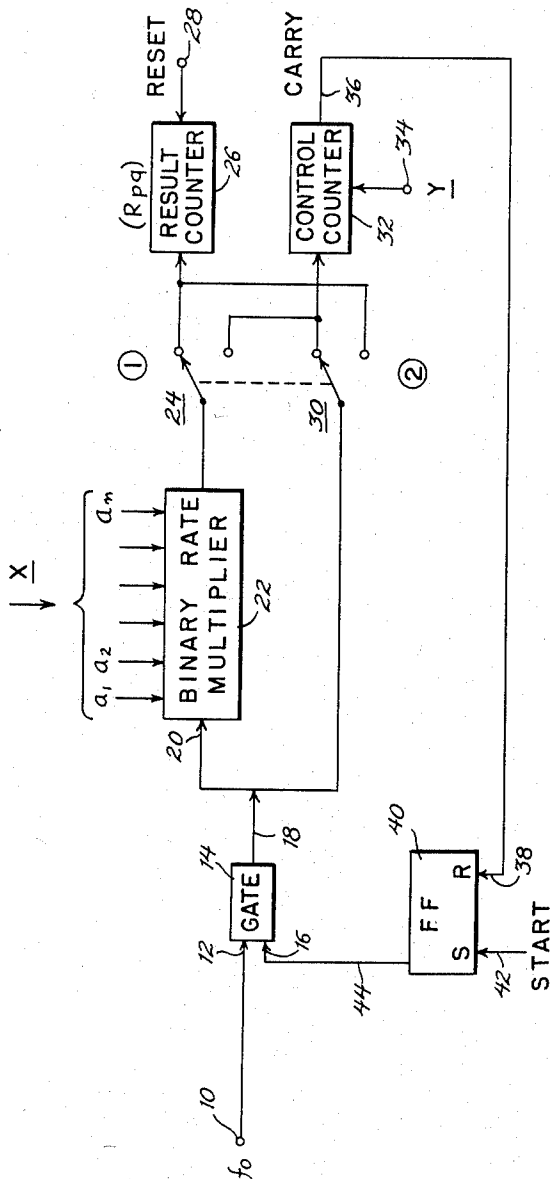
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COUNTING DEVICE

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SWITCH IN POSITION ②

$$R_{pq} = f_0 t$$

$$f_0 X t = Y$$

$$t = \frac{Y}{f_0 X}$$

$$R_q = \frac{Y}{X}$$

SWITCH IN POSITION ①

$$R_{pq} = f_0 X t$$

$$f_0 t = Y$$

$$R_p = X Y$$

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2,926,848

COUNTING DEVICE

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11 Claims. (Cl. 235—164)

The invention relates to counting devices, and more particularly to counting devices for performing multiplying and dividing operations.

Heretofore computers have used complex devices and circuits for performing multiplying and dividing operations. Such devices have also required separate circuits for performing either multiplying or dividing functions. This of course has increased the complexities and number of circuits required thereby increasing the costs of manufacturing and reducing the efficiency of operation and maintenance.

It is therefore a primary object of this invention to provide a new and improved counting device for performing multiplying operations.

Another object of the invention is to provide a new and improved counting device for performing dividing operations.

Another object of the invention is to provide a new and improved counting device selectively performing multiplying and dividing operations utilizing the same components.

Another object of the invention is to provide a new and improved counting device for multiplying and dividing operations which is simple in construction, low in cost and efficient in operation.

Another object of the invention is to provide a new and improved counting device which may be made entirely electrical in operation.

Another object of the invention is to provide a new and improved counting device having high operating speed and efficiency.

Another object of the invention is to provide a new and improved counting device which may be switched from a multiplying operation to a dividing operation at great speed.

Another object of the invention is to provide a new and improved counting device which is highly adaptable to various design circumstances and requirements.

The above objects of the invention as well as other objects will be apparent when the following description is read in conjunction with the drawing annexed hereto showing the invention in block form.

The input terminal 10 receives a train of actuating pulse signals which may occur at a frequency f_0 . The input terminal 10 is connected to the first input 12 of a gate 14 which has a second input 16 and an output 18.

When the second input 16 is energized, the gate 14 passes pulse signals from the terminal 10 to the output 18.

The output 18 of the gate 14 is connected to the input

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lead 20 of a rate multiplier 22. The rate multiplier 22 receives an information signal having a value X. The rate multiplier 22 may be of the binary type having a number of information rate control leads $A_1, A_2, \dots, A_n$ which receive the input information X in binary parallel form. Such a binary rate multiplier has been described in the article entitled "Special Purpose Digital Data Processing Computers" by Bernard M. Gordon and R. N. Nicola in the proceedings of the Association of Computing Machinery dated May 1952, and therefore shall not be described in detail herein.

The output from the multiplier 22 is delivered to the armature of the two position switch 24. In its first position which is shown by the drawing, the switch 24 delivers the output signal from the multiplier 22 to a result counter 26. The counter 26 may be of the cascade binary type. Although the switch 24 is shown in mechanical form for simplicity, it may take the form of a high speed electronic switching device, many of which are well known in the art.

The output signals of the rate multiplier 22 comprise a train or sequence of pulse signals having a frequency or occurrence rate $f_0 X$ which is the product of the rate f_0 of the input signals at the lead 20 and the input information signal X at the rate control leads $A_1, A_2, \dots, A_n$. The value X equals 0.7 may be represented in binary form by 0111, in which a zero (0) represents the absence of a signal and a one (1) represents the presence of a signal on respective control leads $A_1, A_2, \dots, A_n$ of the multiplier 22. Similarly the value X equals zero may be represented by 0000 in binary form and X equals 1.0 may be represented by 1010 as is well known in the art.

As also will be clearly evident from Figure 8 of the above published article of the inventor, when the information signal X to the rate multiplier is equal to zero (0), the rate of the output signals will also be zero. When the signal X has another value such as 0.2 (or 0010 in binary form) the rate of output signals will be $0.2f_0$, where f_0 is the rate of input actuating signals. Thus the value of the information signal X to the rate control leads $A_1, A_2, \dots, A_n$ of the rate multiplier unit 22 controls the rate of its output pulse signals. The rate of the output signals, therefore, may be represented as the product $f_0 X$.

The result counter 26 may be reset to its starting or zero position by a signal delivered to its input terminal 28 before the initiation of a multiplying or dividing operation. During the multiplying or dividing operation the result counter 26 registers the count of the signals delivered to it.

The signals from the output 18 of the gate 14 are also delivered to the armature of a two position switch 30 which is linked to operate unitarily with the switch 24. In its first position (shown by the drawing), the switch 30 delivers the output signals from the gate 14 to a control counter 32.

The control counter 32 is provided with a preset input terminal 34 which adjusts the counter 32 so that it delivers an output carry signal over its output line 36 upon the receipt by the control counter 32 of input signals of a predetermined number Y.

The output line 36 of the control counter 32 delivers a

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carry signal to the input terminal 38 of a bi-stable or flip-flop circuit 40 placing it in its reset condition.

The flip-flop 40 is also provided with an input lead 42 for placing it in its set condition. The output line 44 of the flip-flop 40 is energized only when the flip-flop 40 is in its set condition and delivers a gating signal to the second input 16 of the gate 14.

When the switches 24, 30 are in their first positions they condition the counting device for a multiplying operation.

When the switches 24, 30 are placed in their second positions, the counting device is conditioned for a dividing operation. In their second positions, the switches 24, 30 interchange the connections of the input leads of the result counter 26 and the control counter 32. Thus, in the second position, the output signal from the multiplier 22 is delivered to the input of the control counter 32, while the output from the gate 18 is delivered to the input of the result counter 26.

In the operation of the counting device, the result counter 26 is first reset by a reset or clear signal delivered to its input terminal 28. An information signal Y is delivered to the input terminal 34 which presets the control counter 32. Thus, if the control counter 32 is a backward-forward binary counter, a series of input pulses on the input terminal 34 representing the value Y may be delivered to its backward input terminal causing it to deliver a carry output signal only upon the delivery of Y signals to its forward input terminal.

The flip-flop 40 which has been in its reset state, is now placed in its set condition by a start signal delivered to its input terminal 42. This results in the delivery of a gating signal to the second input 16 of the gate 14 allowing the passage of a series of impulses from the input terminal 10 to the binary rate multiplier 22 as well as to the control counter 32.

The output signals from the multiplier 22 are delivered to the counter 26 which registers their number. As soon as the control counter 32, however, has received Y pulses it delivers a carrying signal, resetting the flip-flop 40 and preventing passage of impulse signals through the gate 14. This terminates the counting operation.

The number registered in the result counter 26 is the product or quotient of the input information signals X and Y depending upon the position of the switches 24, 30.

In a multiplying operation when the switches 24, 30 are placed in their first position, the result R registered in the counter 26 equals the frequency f_0 of pulse signals delivered to the input terminal 10 multiplied by the rate control value signal X delivered to the multiplier 22 multiplied by the period of time t during which the gate 14 passes pulse signals. Bearing in mind that the frequency of actuating pulses f_0 multiplied by the period t during which they pass through the gate 14 is equal to the information signal Y, by substitution, it is evident that the result R in counter 26 equals the product XY of the information signals delivered to the multiplier 22 and the information signals presetting the control counter 32.

When the counting device is set to perform a dividing operation with its control switches 24, 30 in their second position, the number R registered by the result counter 26 equals the frequency f_0 of signals passing through the gate 14 multiplied by the period of time t during which they pass through the gate 14. The rate f_0 of impulse actuating signals multiplied by the information signal X (controlling the multiplier 22) multiplied by the time t during which the actuating signals pass through the gate 14 equals the number Y by which the control counter 32 is preset. The time t during which signals pass through the gate 14 equals Y divided by the product of f_0 and X. By substitution the number R registered in the counter 22 equals the product of f_0 and Y divided

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by the product of f_0 and X. By cancellation of f_0 , R is equal to Y divided by X.

Although counting device is illustrated using an actuating signal f_0 at its input terminal 10 having a predetermined constant frequency, the device will also operate and in the same manner when the frequency f_0 varies and is not constant, and will produce the same results R in the counter 26.

Although the invention has been illustrated with regard to a particular embodiment, it will be evident to those skilled in the art that appropriate modifications may be made in accordance with design requirements without departing from the spirit of the invention.

What is claimed is:

1. A counting device comprising an input terminal for receiving actuating signals, a binary rate multiplier unit controllably connected with said input terminal and adapted to receive rate control information signals in parallel binary form to deliver output signals having a rate which is the product of the rate of said actuating signals and the quantity represented by said signals in parallel binary form, a first counter excited by the output of said multiplier unit, and a second counter responsive to said actuating signals for controlling the period of delivery of actuating signals from said input terminal to said binary rate multiplier unit.

2. A counting device comprising an input terminal for receiving actuating signals, a binary rate multiplier unit controllably connected with said input terminal and adapted to receive rate control information signals in parallel binary form to deliver output signals having a rate which is the product of the rate of said actuating signals and the quantity represented by said signals in parallel binary form, a result counter excited by the output of said multiplier unit, and a control counter having an input lead controllably connected with said input terminal, said control counter controlling the period of delivery of actuating signals from said input terminal to its input lead and to said multiplier unit.

3. A counting device comprising an input terminal for receiving actuating signals, a binary rate multiplier unit controllably connected with said input terminal and adapted to receive rate control information signals in parallel binary form to deliver output signals having a rate which is the product of the rate of said actuating signals and the quantity represented by said signals in parallel binary form, a result counter excited by the output of said multiplier unit, and a presettable control counter having an input lead controllably connected with said input terminal, said control counter controlling the period of delivery of actuating signals from said input terminal to its input lead and to said multiplier unit.

4. A counting device comprising an input terminal for receiving actuating signals, a binary rate multiplier unit adapted to receive rate control information signals in parallel binary form to deliver output signals having a rate which is the product of the rate of said actuating signal and the quantity represented by said signals in parallel binary form, a result counter excited by the output of said multiplier unit, a presettable control counter providing a carry signal in response to a predetermined number of said actuating signals, and a signal gating unit actuated by said control counter carry signal for terminating the delivery of said actuating signals to said multiplier unit and said control counter.

5. A counting device comprising an input terminal for receiving pulse signals; a gate circuit having a first input connected with said terminal, a second input, and an output; a binary rate multiplier unit having a pulse input lead, a plurality of rate control leads for receiving information signals in parallel binary form, and an output lead; a result counter connected with the output lead of said multiplier unit; a control counter having an input count line connected with the output of said gate circuit, a preset control line, and an output carry line; and a

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flip-flop circuit having a set lead, a reset lead joined with the output carry line of said control counter, and an output line joined with the second input of said gate circuit, the output of said rate multiplier unit delivering a train of output pulse signals having a rate which is the product of the rate of the pulse signals received at its pulse input lead and the quantity represented by said information signals received at said rate control leads.

6. A counting device comprising a first set of input terminals for receiving a first information signal in parallel binary form, a second input terminal for receiving a second information signal, a third input terminal for receiving actuating signals, a binary rate multiplier unit joined with said first set of input terminals and controllably connected with said third terminal and having an output lead, a result counter connected with the output lead of said multiplier unit for registering the product of the information signals delivered by said first and second terminals, a control counter joined with said second terminal for presetting its count and controllably connected with said third terminal, said control counter responsive to said actuating signals for controlling the connection of said third terminal with said multiplier unit and said control counter, the output lead of said rate multiplier unit delivering a train of signals having a rate which is the product of the rate of said actuating signals received from said third terminal and the quantity represented by said information signals received at said first set of input terminals.

7. A multiplying device comprising a first set of input terminals for receiving first information signals in parallel binary form representing a value X; a second input terminal for receiving second information signals representing a value Y; a third input terminal for receiving actuating pulse signals; a binary rate multiplier unit joined with said first set of terminals for receiving said information signals, and having an input lead and an output lead; a result counter connected with the output lead of said multiplier unit for registering the product XY of the information signals delivered by said first and second terminals, and having an input conductor for clearing the counter; a control counter joined with said second terminal for presetting its count to deliver a carry signal after receiving Y signals from said third input terminal; a flip-flop circuit having a set lead, a reset lead energized by the carry signal from said control counter, and an output lead energized when the circuit is in its set condition; and a gate circuit having a first input connected with said third terminal, a second input connected with the output lead of said flip-flop circuit, and an output lead for delivering signals to said multiplier unit and said control counter, the output lead of said rate multiplier unit delivering a train of output pulse signals which is the product of the rate of said actuating signals received by its input lead and said value X represented by said information signals in parallel binary form.

8. A dividing means comprising a first set of input terminals for receiving first information signals representing a value X in parallel binary form; a second input terminal for receiving second information signals representing a value Y; a third input terminal for receiving actuating signals having a rate f_0 ; a binary rate multiplier unit joined with said first set of terminals, and having an input lead and an output lead; a result counter for registering the quotient Y/X of the information signals delivered by said first and second terminals, and having an input conductor for clearing the counter; a control counter joined with said second terminal for presetting its count to deliver a carry signal after receiving Y signals from the output lead of said multiplier unit; a flip-flop circuit having a set lead, a reset lead energized by the carry signal from said control counter, and an output lead energized when the circuit is in its set condition; and a gate circuit having a first input connected with

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said third terminal, a second input connected with the output lead of said flip-flop circuit, and an output lead for delivering pulse signals to said multiplier unit and said result counter, the output lead of said rate multiplier unit delivering a train of signals having a rate $f_0 X$ which is the product of the actuating signals received by its input lead and the information signal of value X received from said first set of terminals.

9. A counting apparatus comprising an input terminal for receiving pulse signals; a gate circuit having a first input connected with said terminal, a second input, and an output; a binary rate multiplier unit having a pulse input lead, a plurality of rate control leads, and an output lead; a result counter having an input lead; a control counter having an input count line, a preset control line, and an output carry line; a flip-flop circuit having a set lead joined with the output carry line of said control counter, and an output line joined with the second input of said gate circuit; and switching means having a first position connecting the output of said multiplier unit with the input lead of said result counter and the output of said gate circuit with the input count line of said control counter, and a second position connecting the output of said multiplier unit with the input count line of said control counter and the output of said gate circuit with the input lead of said result counter.

10. A multiplying-dividing apparatus comprising a first set of input terminals for receiving first information signals representing a value X; a second input terminal for receiving second information signals representing a value Y; a third input terminal for receiving actuating pulse signals; a binary rate multiplier unit joined with said first set of terminals, and having an input lead and an output lead; a result counter for registering selectively the product XY and the quotient Y/X of the information signals delivered by said first and second terminals and having an input lead; a control counter having an output line, a first input line, a second input line joined with said second terminal for presetting its count to deliver an output signal upon receiving Y pulse signals at its first input line; a flip-flop circuit having a set lead, a reset lead connected with the output line of said control counter, and an output lead energized when the circuit is in its set condition; a gate circuit having a first input connected with said third terminal, a second input connected with the output lead of said flip-flop circuit, and an output lead; and switching means having a first position connecting the output lead of said multiplier unit with the input lead of said result counter and the output lead of said gate circuit with the first input line of said control counter causing said result counter to register the product XY, and a second position connecting the output lead of said multiplier unit with the first input line of said control counter and the output lead of said gate circuit with the input lead of said result counter causing said result counter to register the quotient Y/X .

11. Apparatus for providing a digital output indication of the combination of a first quantity represented by a first signal in parallel binary form with a second quantity represented by a second input signal comprising gating means having first and second inputs and an output, a source of a reference signal having a reference rate, means for coupling said reference signal source to said gating means first input, a binary rate multiplier having a rate input terminal coupled to said gating means output, an output terminal and rate control leads, means for applying a conditioning signal to said gating means second input to couple said reference signal from said source to said binary rate multiplier rate input through said gating means, means for applying said first signal in parallel binary form to said rate control leads to alter said reference rate whereby the rate of the signal on

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said binary rate multiplier output equals the product of said reference rate with said first quantity, a result counter having an input, a control counter having an advancing input, a preset input, and delivering a carry pulse after a predetermined number of signals are received at said advancing input, means for applying said second signal to the preset input of said control counter to select said predetermined number, selective means for coupling the output of said binary rate multiplier and the output of said gating means to respective ones of said result counter input and said control counter input, and means responsive to a carry pulse delivered from the output of said control counter for removing said conditioning signal from said gating means second input.

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