PCT

WORLD INTELLECTUAL PROPERTY ORGANIZATION
International Bureau

INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(51) International Patent Classification 5 :
H05B 41/36, 37/04, 37/03, 39/10, 41/46, 37/02

A1

(11) International Publication Number: **WO 94/14302**

(43) International Publication Date: 23 June 1994 (23.06.94)

(21) International Application Number: PCT/AU93/00639

(22) International Filing Date: 10 December 1993 (10.12.93)

(30) Priority Data:
PL 6287 11 December 1992 (11.12.92) AU

(71) Applicant (*for all designated States except US*): NEWTRONICS PTY. LTD. [AU/AU]; 149-159 Capel Street, North Melbourne, VIC 3051 (AU).

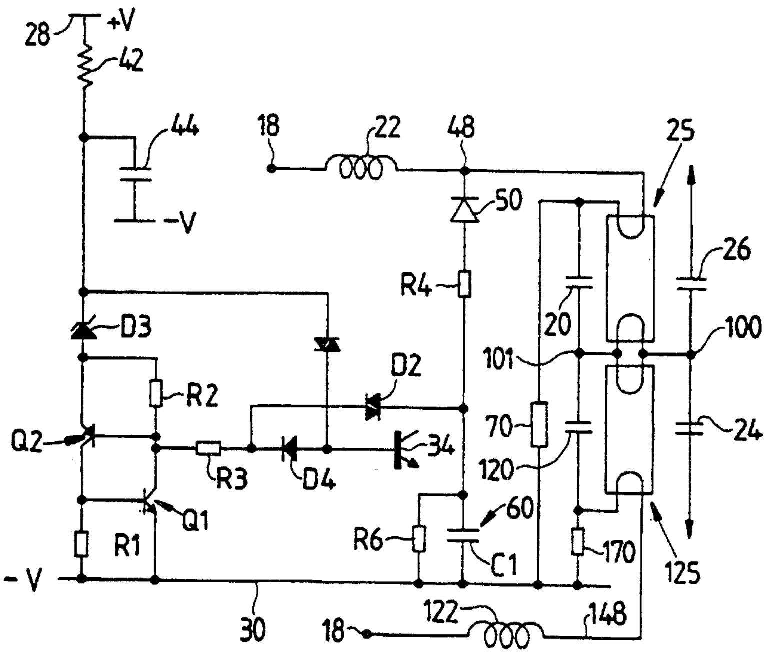
(72) Inventor; and
(75) Inventor/Applicant (*for US only*): BRUCE, David, John [GB/AU]; 71 Macedon Street, Sunbury, VIC 3429 (AU).

(74) Agents: LESLIE, Keith et al.; Davies Collison Cave, 1 Little Collins Street, Melbourne, VIC 3000 (AU).

(81) Designated States: AT, AU, BB, BG, BR, BY, CA, CH, CZ, DE, DK, ES, FI, GB, HU, JP, KP, KR, KZ, LK, LU, LV, MG, MN, MW, NL, NO, NZ, PL, PT, RO, RU, SD, SE, SK, UA, US, UZ, VN, European patent (AT, BE, CH, DE, DK, ES, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, ML, MR, NE, SN, TD, TG).

Published
With international search report.

(54) Title: ELECTRIC CIRCUIT FOR GAS DISCHARGE LAMP



(57) Abstract

A circuit for controlling electricity delivered to a load, in particular a gas discharge lamp (25, 125). A high frequency ballast inverter (14) outputs a high frequency oscillating signal to drive a gas discharge lamp (25, 125). A resonant circuit is coupled to the lamp and inverter (14) to act as a voltage multiplier to aid in starting the lamp (i.e. to reach gas ionisation). If the lamp does no start within a certain time, or if the lamp fails during operation, a timer circuit disables output from the inverter (14) so as to protect the driving components from extended exposure to high currents/voltage experienced during starting. Reset circuitry is also provided to re-enable the inverter (14) upon removal and replacement of the faulty lamp. In one form a capacitor (120), which forms part of the resonant circuit, charges during removal of the lamp, and the resulting discharge upon lamp replacement effects resetting of the timer circuit and restart of the inverter (14).

Electric Circuit for gas discharge lamp

This invention relates to an electric circuit of the kind which produces in use an output which cyclically varies about a first reference voltage, the magnitude of which output, relative to the first reference voltage, is, during normal operation of the circuit, such as not to exceed a predetermined value for more than a predetermined time, but which in abnormal operation does exceed the predetermined value for a predetermined time.

Exemplary circuits of the above kind include various forms of DC-AC converter used for operating fluorescent lamps via ballast circuits. Ballast circuits for fluorescent lamps, as used in these applications, are commonly arranged such that, on initial application of output from the inverter, a high voltage is generated and applied through the ballast circuitry to the lamp in order to ionise gas in the lamp to initiate operation. Once, however, the ionisation occurs and the lamp commences operation, a relatively low voltage only is required to sustain operation, and the ballast circuitry is effective to apply a much lower voltage from the inverter to the lamp. The principles of ballast circuits for performing this function are well known, simple circuits employing a capacitor connected across the lamp and a series inductor between one end of the lamp and one of the ballast inverter outputs. In the non-operative state, the lamp essentially constitutes an open circuit and the ballast inverter output is applied to a substantially reactive load of low impedance, constituted by the series connected capacitor and inductor. When the lamp is operating, a substantially resistive load is presented by the lamp in parallel with the capacitor so that the effective impedance of the circuit is much increased. In this way, the voltage applied from the ballast inverter to the lamp is automatically changed from the start condition at which a relatively high voltage is applied to the lamp to a run condition where a relatively low voltage is applied.

Whilst, in the start condition of the ballast and lamp, the load presented by the ballast and lamp is predominantly reactive in nature, the inductance naturally exhibits some resistive component. In these conditions, the voltage applied across the lamp may be of the order of several times the normal operating voltage and substantial current flows will occur through the inductor in view of the low load impedance then presented.

Similarly, output components of the inverter, such as output semi-conductor devices, are subjected to heavy current. At least in the interests of economy, it is generally not viable to so design the inverter and inductance such that these are capable, indefinitely, of sustaining without damage the heavy power dissipation which thus occurs under the start condition.

It might be considered possible to provide a means for directly measuring the voltage across the lamp and, responsive to the measured voltage, to prevent continued application of voltage from the ballast inverter to the ballast circuit and lamp under the condition where starting is not established. However, generally speaking, arrangements sensitive to voltage per se involve some complexity, particularly in cases such as above described where the voltage to be sensed is high.

In accordance with the invention, there is provided a protective electric circuit for a gas discharge lamp circuit which includes a driving means for generating a voltage signal for application across the electrodes of a gas discharge lamp, the voltage signal, during normal operation of the lamp, being of an amplitude so as to be of one polarity with respect to a reference voltage, the protective circuit comprising means responsive to a condition in which the voltage signal is the other polarity with respect to the reference voltage, and means to generate a fault signal when the time period during which the voltage signal is said other polarity persists for more than a predetermined time period.

By this arrangement, it is not necessary to particularly provide magnitude discriminating circuitry, simply to provide for polarity detection to generate the fault signal.

The fault signal may be applied as required, such as to automatically turn off operation of the circuit.

The invention also provides a circuit for driving a gas discharge lamp, the lamp being detachable from the circuit for removal and replacement, comprising:

a ballast inverter for generating a high frequency output signal for application to the electrodes of the lamp;

a resonant circuit portion for multiplying said output signal whilst the lamp is inactive;

a timing means for determining the time period during which the lamp is inactive on the basis of the multiplied output signal, and for issuing a hold signal when the time period exceeds a predetermined period; and

latch means for preventing the inverter from generating said output signal after issuance of said hold signal.

In another aspect, the invention provides a circuit for driving a gas discharge lamp, the lamp being detachable from the circuit for removal and replacement, comprising:

an inverter circuit for generating a high frequency output signal for starting and energising the lamp;

a protection circuit for disabling the inverter circuit on detection of a faulty lamp; and

a reset circuit for resetting the protection circuit to re-enable generating of the output signal upon replacement of the lamp.

In an embodiment of the invention, the circuit further comprises a resonant circuit which includes a charge storage element coupled, in use, between terminals of respective electrodes of the lamp, and wherein removal of the lamp causes the charge storage element to charge and replacement of said lamp effects a discharge of the element which effects resetting of the protection circuit.

The invention is further described by way of example only with reference to the accompanying drawings in which:

Figure 1 is a diagram of a drive arrangement for a fluorescent lamp;

Figure 2 is a circuit diagram of part of a ballast inverter incorporated at the arrangement of Figure 1;

Figure 3 is a circuit diagram of a protection circuit incorporated into the ballast inverter;

Figure 4 is a diagram of a current transformer incorporated into the ballast inverter of Figure 2; and

Figure 5 is a modified form of the protection circuit of Figure 3.

Referring firstly to Figure 1, the circuit arrangement shown includes a line filter 10 arranged to be connected, for example, to a mains AC supply to produce a filtered AC signal, a rectifier 12 which produces a rectified DC voltage from the filtered AC signal, a ballast inverter 14, which receives the DC voltage from the rectifier 12 and generates therefrom a high frequency AC signal (for example of 40 kHz frequency), and a ballast circuit 16 which couples the inverter 14 to a fluorescent lamp 25.

The fluorescent lamp 25 comprises an envelope 25a containing a suitable low pressure gas or vapour having, at opposite ends thereof, electrodes 25b, 25c, these being formed as heater elements. In normal operation, the lamp 25 has an alternating electric supply applied thereacross so that there is an ionisation current through the lamp which causes a fluorescent layer on the envelope 25a to emit light. In normal operation then, the elements 25b, 25c simply serve the purpose of electrodes to which the drive supply is applied. During initial start up, however, current is passed through the elements 25b, 25c, which are of low resistance, to excite electrons which are used to ionise the gas or vapour in the envelope 25 so as to start operation.

First ends of each of the elements 25b, 25c are interconnected by a capacitor 20. The other end of element 25b is connected to the output 18 of inverter 14 via an inductance 22. The other end of element 25c is connected on the one hand to negative supply for the apparatus via a capacitor 24 and on the other hand to positive supply by an equal capacitor 26.

During initial operation, the high frequency output of the inverter 14 is applied from an output 18 via the inductance 22 through the element 25b, capacitor 20 and element 25c to the junction between capacitors 24, 26. Because the lamp 25 is not conducting, the load presented to the inverter 14 is essentially reactive, comprising the capacitive reactance of the capacitor 20 in series with the inductance 22, the resistances of the elements 25b, 25c being small. In the result, substantial current flow occurs through the elements 25b, 25c to cause these elements to be heated as is required for initial operation. Furthermore, the nature of the resonant circuit comprised of the inductance 22 and capacitor 20 is such that a relatively high voltage is generated across the lamp 25 ie between the elements 25b, 25c so that, in conjunction with the heating of the elements 25b, 25c, ionisation of gas or vapour within the envelope 25a occurs and start up of the operation of the lamp likewise occurs. Once the ionisation current is established in the lamp 25, however, the lamp itself presents a significant impedance which may be treated as being resistive in nature so that the total impedance presented to the output 18 of the ballast inverter 14 is substantially increased. Thus, whereas a relatively high voltage is applied on initial start up, this voltage drops to a much lower level once ionisation and normal operation of the lamp is established. Typically, the magnitude of the AC voltage applied during start up may rise to the order of one thousand volts as compared with a magnitude of, say 150 to 200 volts once normal operation has been established. This principle of ballasting fluorescent lamps is well known.

It would of course be possible to apply the AC drive voltage from the ballast inverter 14 directly to the ballast circuit 16. However, it is necessary, in most applications to provide for DC decoupling of the output of the inverter to the circuit 16. This may be achieved in various ways but in the present instance is shown as being achieved by coupling the output 18 from the inverter 14, as mentioned, to the inductance 22 and, also as mentioned, by coupling the element 25c to positive and negative rails via the two capacitors 24, 26.

The output 18 from the inverter 14 is an oscillatory voltage about a first reference voltage which is midway between the positive and negative supply rails. The positive and negative supply rails may be arranged such that there is a voltage difference of four hundred volts therebetween so that the output 18 oscillates around a voltage which is more or less constant with reference to the positive and negative supply rails and midway therebetween. So, the voltage at the output 18 will oscillate about a mean voltage of about two hundred volts.

The ballast inverter 14 may take one of many forms. One form is described in Australian Patent Specification 30314/89 (PCT/EP88/01211). Figure 2 is a simplified circuit diagram of an arrangement which is somewhat similar. The positive and negative supply rails are designated by reference numerals 28, 30. These are derived from the rectifier 12.

Two transistor switches 32, 34 are provided, connected in series across the rails 28, 30. Output is taken from a junction between the emitter of transistor 32 and the collector of transistor 34. This output is passed through the winding 40a of a current transformer 40 (Figure 4) to the inductance 22 of the circuit 16. Suitable drive arrangements are provided for turning on and off of the transistors 32, 34 so that transistor 34 is cyclically turned on and off with transistor 34 being turned on and off in a complementary fashion so that at any one time only one of the two transistors is in an on condition. The switching rate is arranged to provide the required high frequency output to the inductance 22. Reference may be had to the aforementioned prior patent specification for a detailed explanation as to an exemplary method of control. Generally, however, the bases of the transistors 32, 34 are connected into circuitry including windings 40b, 40c of the current transformer 40 to provide triggering signals of the required polarity for on and off switching, these signals being generated, essentially, in accordance with the flow of current through the winding 40a. Winding 40b is connected from the negative rail 30 to the base of transistor 34 via a resistor 53, and winding 40c is connected from the junction between the collector of transistor 34 and the emitter of transistor 32 to the base of transistor 32 via a resistor 55.

Insofar as the present invention is concerned, it is noted that the input lines to the inverter 14 have coupled thereacross a series connected resistor 42 and capacitor 44. The junction between these is connected via a diac 49 to the base of transistor 34. When the arrangement of Figure 1 is initially turned on and DC voltage appears at the output of rectifier 12 and at the input to the ballast inverter 14, capacitor 44 charges through resistor 42 until a voltage sufficient to cause break over of the diac 49 occurs, at which time a current is injected into the base of transistor 34 which causes the transistor 34 to turn on and initiate operation of the inverter. Circuitry of a nature similar to this is generally needed because the inverter 14 will not self start without such circuitry. In particular, the transistors 32, 34 will otherwise be in a stable state at turn on, control via induced voltages in the windings 40b, 40c being dependent on the existence of changing current flow through the winding 40a which will not occur until, for example, one of the transistors 32, 34 is turned on. Each time transistor 34 is turned on, capacitor 44 is discharged via diode 51 in readiness for the next cycle of operation.

If the inverter 14 comprised no more than the circuitry shown in Figure 2, the aforementioned problem concerning prolonged power dissipation in the inductance 22 would occur if the lamp 25 did not begin satisfactory operation on initial turn on of the arrangement. In particular, if the lamp does not strike when the inverter 14 begins operation, there will be a high current flow through the inductance 22 which if allowed to continue for a substantial period of time will cause the inductance 22 to possibly overheat and cause damage to it. Similarly, the output transistors 32, 34 are subjected to substantial current flows and again substantial and possibly damaging temperature rises will occur if the start up condition prevails for too long. In accordance with this embodiment of the invention, then, the circuitry shown in Figure 3 is additionally incorporated into the ballast inverter 14.

Under normal operating conditions, in the case described where the potential difference between rails 28, 30 is 400 volt positive, and the output reference voltage 100 is plus 200 volts, the voltage across the lamp 25 will swing in accordance with the voltage on line 18 about the same reference voltage with an amplitude of about 150 volts, that is somewhat less than half the voltage between the rails 28, 30. If, as described, the voltage of rail 28 is positive with reference to the voltage on rail 30, the voltage across the lamp 25 will never be negative relative to rail 30, being always somewhat positive relative thereto. On the other hand, during initial operation, since the voltage across the lamp 25 may have an amplitude rising to of the order of 1000 volts about the same 200 volt positive reference, then the voltage will swing, on negative peaks of the applied voltage across the lamp 18, very substantially negative relative to the rail 30.

The circuitry shown in Figure 3 is connected to the same ground rail 30 as the remainder of the circuitry of the inverter and to the same positive rail 28. Lamp voltage, such as at the point 48 in Figure 1 circuitry is applied via a diode 50 and resistor R4 to a timing circuit 60 comprised of the parallel connected capacitor C1 and resistor R6 shown. So long as the voltage at the point 48 is positive, no current flow can occur through diode 50 because of the reverse bias of these through the circuit 60 to the line 30. On the other hand, when the voltage at the point 48 is negative relative to the rail 30, current flow can occur so as to charge the capacitor C1 via diode 50 and resistor R4, the charging rate being controlled by selecting the values of resistor R6 and capacitor C1. As mentioned, this condition applies only during initial start up operation or in abnormal operation, since it is only in this condition that peaks of the voltage applied across the lamp 25 exceed an amplitude of 200 volts.

Thus, the capacitor C1 will charge only under start up conditions or in abnormal operation. The values of the capacitor C1 and of the resistors R6 and R4 are chosen such that a predetermined threshold voltage across the capacitor C1 is reached only after a predetermined time limit from application of the start up voltage across the lamp 25. Typically this may be of the order of 5 seconds. If the time for start up of the lamp 25 is less than this predetermined time, the voltage at the point 48 assumes a positive value and the capacitor C1 discharges through the resistor R6. If however, a threshold voltage is reached, a diac D2 becomes conductive and an error signal is generated indicating that start up has not occurred within the predetermined time or an abnormal condition has existed for a predetermined time. Typically, diac D2 may be a 32 volt diac so that break over or conduction occurs when a voltage of 32 volts is reached across the capacitor C1. The diac D2 is connected from capacitor C1 through resistor R3 to a latching circuit comprised of transistors Q1, Q2 and resistors R1 and R2 connected as shown. In particular, the side of the diac D2 not connected to capacitor C1 is coupled by the resistor R3 to the base of transistor Q2 so that when break over occurs the transistor Q2 is turned on followed by resultant turn on of transistor Q1. Transistor Q1 is in this case latched in the on condition. The emitter–collector junction of transistor Q2 is connected in series with a resistor R1 to rail 30, the emitter itself being connected via a zener diode D3 and the resistor 42 mentioned in relation to Figure 2 to the positive supply rail 28. The junction between the zener diode D3 and resistor 42 is connected to the negative supply rail 30 by capacitor 44 also shown in Figure 2. Zener diode D3 is chosen to have a lower zener voltage than the break over voltage of diacs 49 and D2, such as being 12 volt where the break over voltage is 32 volt.

The diac 49 shown in Figure 2 is shown in Figure 3, this being connected from the junction between the resistor 42 and zener diode D3 to the junction between diac D2 and resistor R3 via a diode D4 as shown. The junction between diode D4 and the diac 49 is connected to the base of transistor 34.

In normal operation, when the voltage on capacitor C1 does not rise to the point where diac D2 conducts, the voltage across the diac 49 can as aforedescribed reach the necessary 32 volts in order to initiate operation of the inverter. However, if after initiation of operation, charging of capacitor C1 continues to the point where diac D2 breaks over, the junction between diode D4 and resistor R3 is then pulled to a negative value (point 48 peaking at a value which is negative with respect to rail 30) with the result that the transistor 34 is decisively turned off due to the connection of the last mentioned junction to the base of the transistor 34 via the diode D4. Operation of inverter 14 then ceases. This clamping condition is arranged to prevail for several cycles of operation of the inverter 14 since if the clamping were removed immediately, restarting may occur due to ringing in the circuit comprised of the inverter 14 and ballast circuit 16.

Also, when clamping of the base of transistor 34 occurs, transistors Q1, Q2 are turned on due to break over of diac D2, and current flow occurs through zener diode D3. The voltage across capacitor 44 is then limited to the zener voltage so that diac 49 can no longer conduct, and drive to base of transistor 34 is prevented. Thus, further starting of the inverter 14 is inhibited.

Figure 5 illustrates an extended form of the protection and drive circuitry illustrated in Figure 3 and described hereinbefore. The modified circuit is constructed to allow two fluorescent lamps 25, 125 to be operated in parallel by a single protection circuit. In order to achieve this, parallel inductors 22, 122 are provided to couple the output 18 from the inverter 14 to respective first terminals of the lamps 25, 125. As in Figure 3, the elements of the lamps 25, 125 are interconnected by respective capacitors 20, 120, with the remaining element terminal of the lamps 25, 125 each being connected between the negative and positive supply rails via capacitors 24 and 25 respectively.

As described above, the oscillator comprising transistors 32, 34 and related drive components (Figure 2) provides a high frequency output signal at the output terminal 48. Considering lamp 25, and neglecting the voltage drops across the cathodes thereof, the output load comprises essentially an LC series resonant circuit of inductor 22 and capacitor 20. Therefore, before the lamp 25 starts, the unloaded output LC filter acts as a voltage multiplier dependant upon the circuit quality factor (Q) in normal operation, the voltage across capacitors 20 and 120, and hence across the elements of lamps 25 and 125, reaches a sufficient magnitude to begin ionisation within the tubes 25, 125. Once the lamps 25, 125 are conducting, a low impedance is presented across capacitors 20, 120, which acts to damp the LC resonant circuit. The voltage across capacitors 20, 120 then drops to a level defined by the operation of the lamps 25, 125 and the output of inductors 22, 122.

However, in the event that lamp 25 is faulty and does not reach ionisation, the voltage across capacitor 20 remains high and the circuit currents are much higher than during normal operation. This causes excessive power dissipation requirements and can lead to circuit overload, as discussed above, necessitating some form of preventative protection circuit to limit this condition.

Output terminals 48, 148 (Figure 5) have a DC level defined by the rectifier circuitry, and under normal operation has a peak to peak voltage swing of a magnitude such that the voltage at terminal 48 does not exceed that of the supply rails. However, under startup condition (ie. before ionisation of the gas in lamps 25, 125) the high voltages achieved from the LC resonant circuit exceeds that of the supply rail, causing diode 50 to conduct so as to charge capacitor C1. If the threshold voltage of diac D2 is achieved before the lamp 25 starts, then a hold signal is issued by diac D2 conducting current to the base of transistor Q2, thus causing the latch comprising transistors Q1 and Q2 to operate. Operation of the latch in turn causes the base of transistor 34 to be clamped low via diode D4, thus preventing further operation of the inverter whilst the latch is set. In this event, however, the latch circuit can only be reset by removal of input power to the circuit.

In the circuits thus far described, as mentioned above, supply power to the protection circuit must be cut, once the circuit has latched, in order to start a new lamp tube. This requirement can be a significant drawback in large installations where a large number of lamp tubes may be controlled by a single power switch, and/or where the lamps run continuously for extended periods of time. In such an installation it may be very inconvenient or disadvantageous to require that the supply power be cut to all of the lamp circuits in order to replace and restart only one of them. In order to alleviate this problem, it has been found that a resistor 70 coupled from the junction of capacitor 20 and lamp electrode 25B to the negative supply rail 30 can effect resetting of the protection circuitry upon replacement of the faulty lamp tube.

Referring to Figure 5, there is shown a resistor 70 coupled from one end of capacitor 20, and resistor 170 coupled to an end of capacitor 120, the other ends of the capacitors 20, 120 being coupled together at a cathode terminal of lamp tubes 25, 125. As described hereinabove, if one of the lamp tubes 25, 125 is faulty and does not start, the latch arrangement of transistors Q1 and Q2 latches so as to prevent further low impedance current draw through the resonant starting circuits. In this condition, the transistor 34 (see Figure 2) is latched off, and thus resistor 39 (Figure 2) forms a voltage divider with resistors 70 and 170 by way of inductors 22 and 122, respectively. Preferably the resistance values of each of resistors 70 and 170 are larger than the resistance value of resistor 39, such that the quiescent voltage at terminal 101 (the junction between the cathode terminals of lamps 25 and 125) is around 250 to 300 volts. This provides a quiescent charge on capacitors 20 and 120 of around 50 to 100 volts, since mid point 100 between capacitors 24 and 26 is stabilised at around 200 volts, between the upper and lower rail voltages. If faulty lamp tube 125 is then removed so as to replace it with an operational tube, then the cathode connections of tube 125 are left open circuit. This alters the conditions of capacitor 120, whereby the terminal of capacitor 120 coupled to resistor 170 is drawn to ground potential, whilst the other end thereof is drawn to 200 volts potential, creating a charge voltage across capacitor 120 of about 200 volts. When an operational tube is replaced as lamp tube 125, the charge in capacitor 120 must revert to its former state, ie. –50 volts compared to the +200 volt charge with tube 125 removed, which requires a redistribution of charge in the protection circuit. Advantageously, charge current is drawn from capacitor 44 through diode 51, inductor 122 and a cathode of lamp tube 125 so as to equalise the charge in capacitor 120 with that of capacitor 20. In doing so, the charge voltage across capacitor 44 drops slightly below the 14 volts or so required for zener diode D3 to conduct, which unlatches the transistor arrangement of Q1 and Q2 by momentarily ceasing current flow thereto. In effect this constitutes a reset signal, brought about by discharge of capacitor 20 upon replacement of the lamp tube, which causes the latch to reset by momentarily preventing current flow thereto. Therefore, by releasing the latch of transistors Q1, Q2, the drive transistor 34 is able to conduct once again so as to drive the lamp tubes 25 and 125, as described above. Since the circuit is symmetrical with respect to lamp tubes 25 and 125, the operation of the circuit in the instance in which tube 25 is faulty rather than tube 125, is the same except with respect to capacitor 20 and resistor 70 rather than capacitor 120 and resistor 170.

In the case of a circuit arranged to drive only a single lamp tube, such as that illustrated in Figures 1 and 3, an additional resistor 69 may be introduced in order to encourage discharge of capacitor 20 whilst the faulty lamp tube 25 is removed and replaced. Thus, as in the case of the dual lamp circuit, the capacitor 20 must be recharged upon insertion of the lamp tube 25, which draws current from capacitor 44, so as to momentarily prevent conduction of zener diode D3 which has the effect of resetting the latch arrangement of transistors Q1 and Q2. The additional resistor 69 may be coupled in parallel across the terminals of tube cathode 25C, between one end of capacitor 20 and the mid point 100 between capacitors 24 and 26. Additionally, the resistor 69 may be of a relatively high resistance value, eg. 100 kilooams, so as to substantially prevent disturbance to the remainder of the circuit.

The described arrangement generates an error signal when a time period has elapsed during which lamp start up has not occurred or when a fault condition exists for such time period. As mentioned, this time interval may be determined by selection of components, particularly capacitor C1 in the circuit of Figure 3. When the error signal is generated, the ballast inverter is disabled. The time period allowed from initiation of operation of the inverter before disabling occurs, if start up does occur, can easily be selected to be such that operation of the inverter is not permitted for a period likely to damage to the inductance 22 and internal components of the inverter, particularly the transistors 32 and 34. The error signal could however be applied otherwise to disable the inverter or need not be applied to actually disable the inverter at all, simply to provide a suitable warning to enable manual disabling of the inverter or otherwise to permit control action to be taken.

The described construction has been advanced merely by way of explanation, and many modifications and variations may be made thereto without departing from the spirit and scope of the invention defined by the claims appended hereto.

CLAIMS:

1. A protective electric circuit for a gas discharge lamp circuit which includes a driving means for generating a voltage signal for application across the electrodes of a gas discharge lamp, the voltage signal, during normal operation of the lamp, being of an amplitude so as to be of one polarity with respect to a reference voltage, the protective circuit comprising means responsive to a condition in which the voltage signal is the other polarity with respect to the reference voltage, and means to generate a fault signal when the time period during which the voltage signal is said other polarity persists for more than a predetermined time period.

2. A protective circuit as claimed in claim 1, including a latch means which is coupled to said driving means and which is responsive to said fault signal to assume a state effective to prevent the driving means from generating said voltage signal.

3. A protective circuit as claimed in claim 2 wherein the latch means is further responsive to a reset signal effective to reset the state of the latch means so as to re-enable the driving means to generate said voltage signal.

4. A protective circuit as claimed in claim 3 wherein the latch means includes a charge storage device which, in use of the circuit, is charged to a threshold level whilst the latch means is in its set state, said reset signal being effective to at least momentarily reduce the charge of the storage device to below said threshold level.

5. A protective circuit as claimed in claim 4 wherein the latch means further includes a threshold device coupled with said charge storage device such that when the charge of the storage device is drawn below said threshold level by the reset signal the threshold device prevents current flow to the latch means so as to reset same.

6. A protective circuit as claimed in claim 3, 4 or 5 wherein the lamp is removable from the driving means and protective circuit for replacement of the lamp, wherein the action of removal and replacement of the lamp causes issuance of said reset signal.

7. A circuit for driving a gas discharge lamp, the lamp being detachable from the circuit for removal and replacement, comprising:

a ballast inverter for generating a high frequency output signal for application to the electrodes of the lamp;

a resonant circuit portion for multiplying said output signal whilst the lamp is inactive;

a timing means for determining the time period during which the lamp is inactive on the basis of the multiplied output signal, and for issuing a hold signal when the time period exceeds a predetermined period; and

latch means for preventing the inverter from generating said output signal after issuance of said hold signal.

8. A circuit as claimed in claim 7, further comprising means for resetting said latch means in response to a reset signal, after issuance of said hold signal, so as to allow the inverter to generate said output signal.

9. A circuit as claimed in claim 8, wherein removal and replacement of said lamp is effective to initiate the issuance of said reset signal to the resetting means to reset the latch means.

10. A circuit as claimed in claim 9, wherein the resonant circuit portion includes a charge storage element coupled, in use, between terminals of respective electrodes of the lamp, and wherein removal of the lamp causes the charge storage element to charge and replacement of said lamp effects a discharge of the element constituting said reset signal.

11. A circuit as claimed in claim 10 wherein current is supplied to said latch means by way of a threshold device, the reset signal being effective to, at least momentarily, reduce the voltage across the threshold device to below its threshold so as to block current flow to the latch means and reset same.

12. A circuit as claimed in claim 7 wherein the lamp comprises first and second dual terminal heatable electrodes, and wherein the resonant circuit portion comprises an

inductive element having one end coupled to one terminal of the first lamp electrode and the other end coupled to receive the output signal from the inverter, and a first capacitive element coupled from the other terminal of the first electrode to one terminal of the second electrode, with the other terminal of the second electrode being coupled to a substantially constant voltage source, and wherein the timing means comprises a parallel resistive and capacitive arrangement having one end coupled to said one terminal of the first lamp electrode via a first threshold device.

13. A circuit as claimed in claim 12 wherein the said end of the RC arrangement is coupled to the latch means via a second threshold device, such that when the capacitive element of the RC arrangement level above the threshold of the second threshold device the second threshold device conducts an electrical current constituting said hold signal.

14. A circuit as claimed in claim 13 wherein said latch means comprises a bistable transistor arrangement which, in its latched condition, is supplied with current via a third threshold device.

15. A circuit as claimed in claim 14, further including a resistive element which couples an end of the first capacitive element to ground such that, on removal of the lamp the first capacitive element charges between said voltage source and ground whereby, on replacement of the lamp, said first capacitive element at least partially discharges so as to at least momentarily reduce said third threshold device below its threshold whereby to cut current flow there through and reset the latch means.

16. A circuit for driving a gas discharge lamp, the lamp being detachable from the circuit for removal and replacement, comprising:

an inverter circuit for generating a high frequency output signal for starting and energising the lamp;

a protection circuit for disabling the inverter circuit on detection of a faulty lamp; and

a reset circuit for resetting the protection circuit to re-enable generating of the output signal upon replacement of the lamp.

17. A circuit according to claim 16, further comprising a resonant circuit which includes a charge storage element coupled, in use, between terminals of respective electrodes of the lamp, and wherein removal of the lamp causes the charge storage element to charge and replacement of said lamp effects a discharge of the element which effects resetting of the protection circuit.

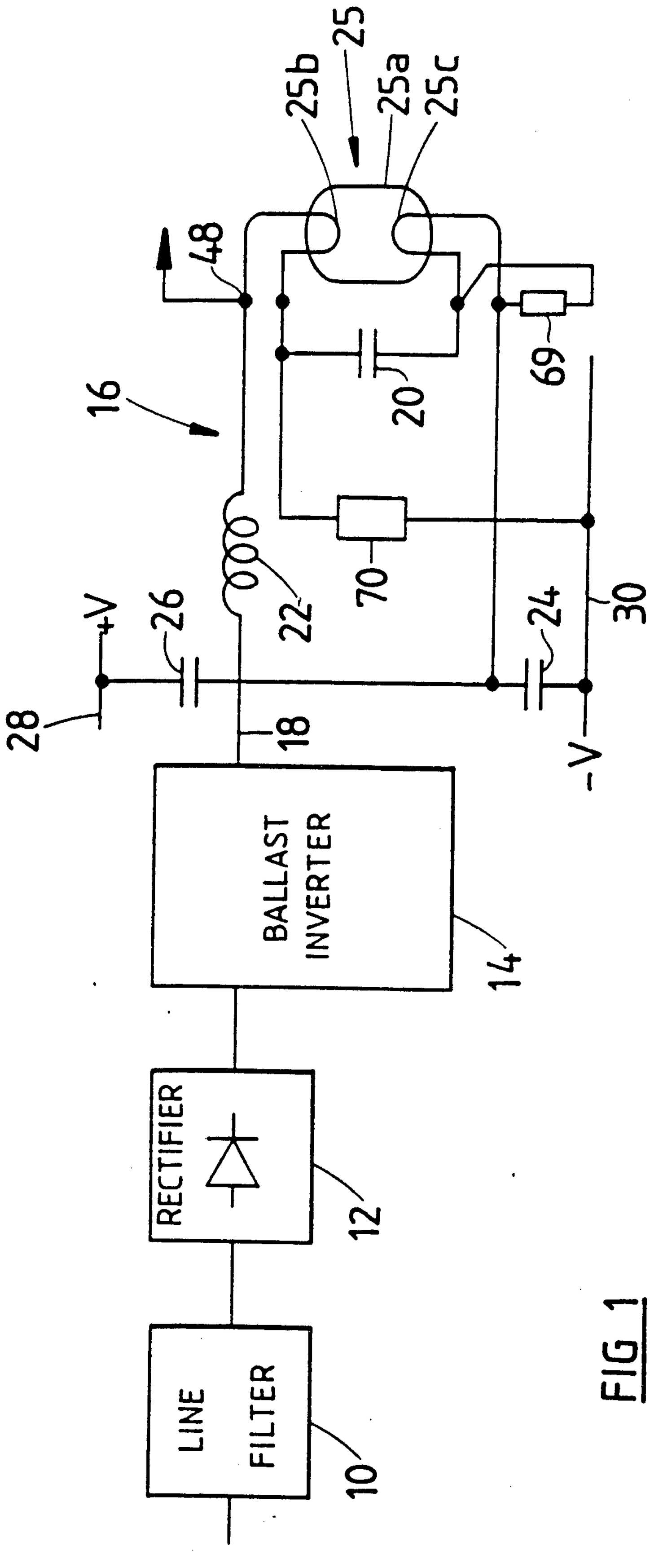

LINE
FILTER
10
RECTIFIER
12
BALLAST
INVERTER
14
18
28
+V
26
22
16
48
20
25b
25
25a
25c
69
70
24
30
-V

FIG 1

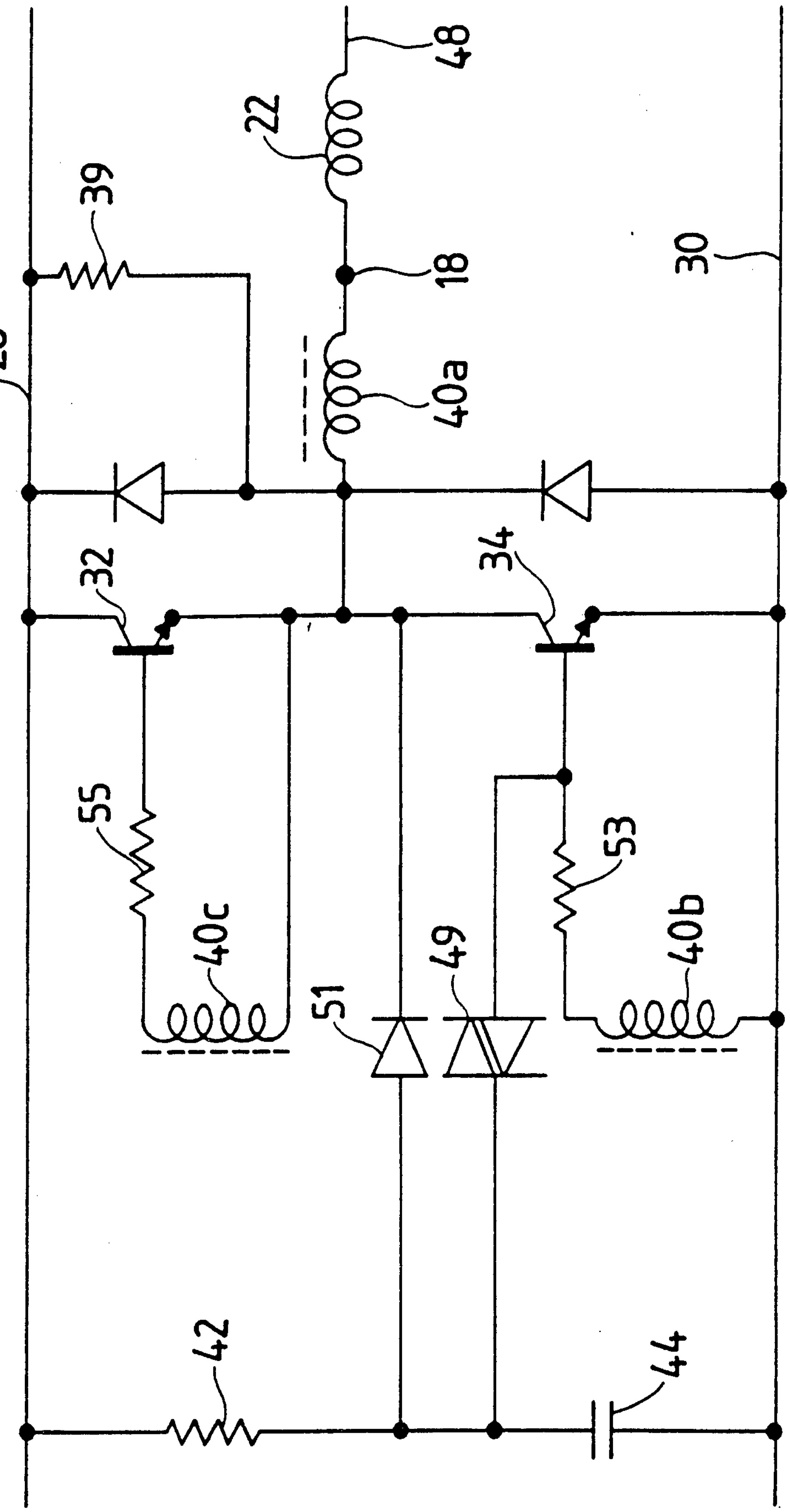


FIG 2

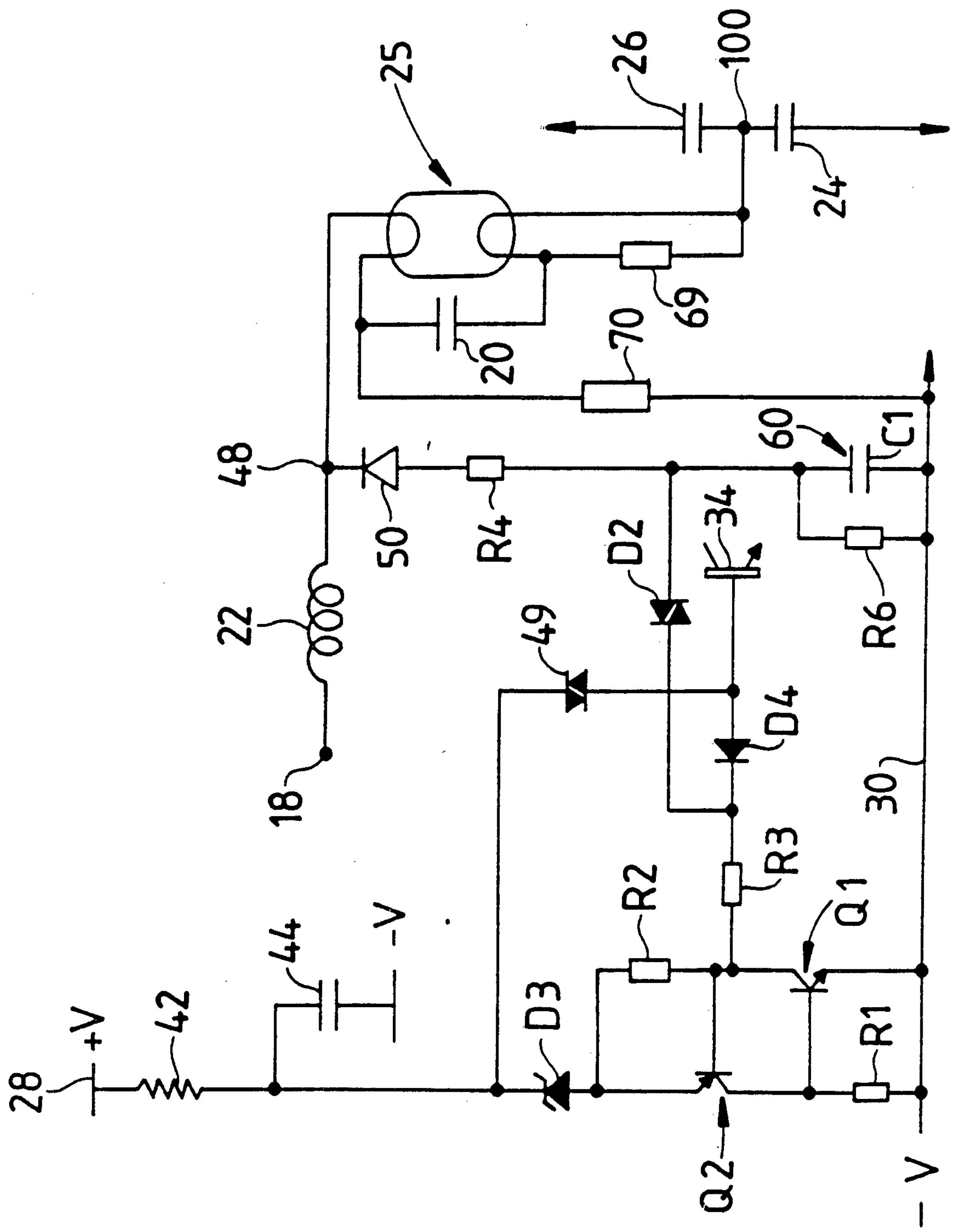

25
26
100
24
69
70
20
48
50
R4
D2
34
60
C1
R6
22
49
D4
18
30
R3
R2
Q1
28
+V
42
44
-V
D3
R1
Q2
– V

FIG 3

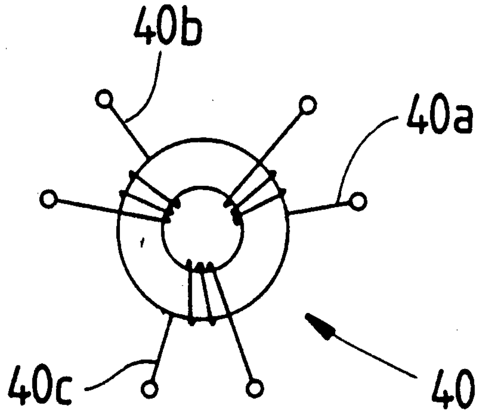


FIG 4

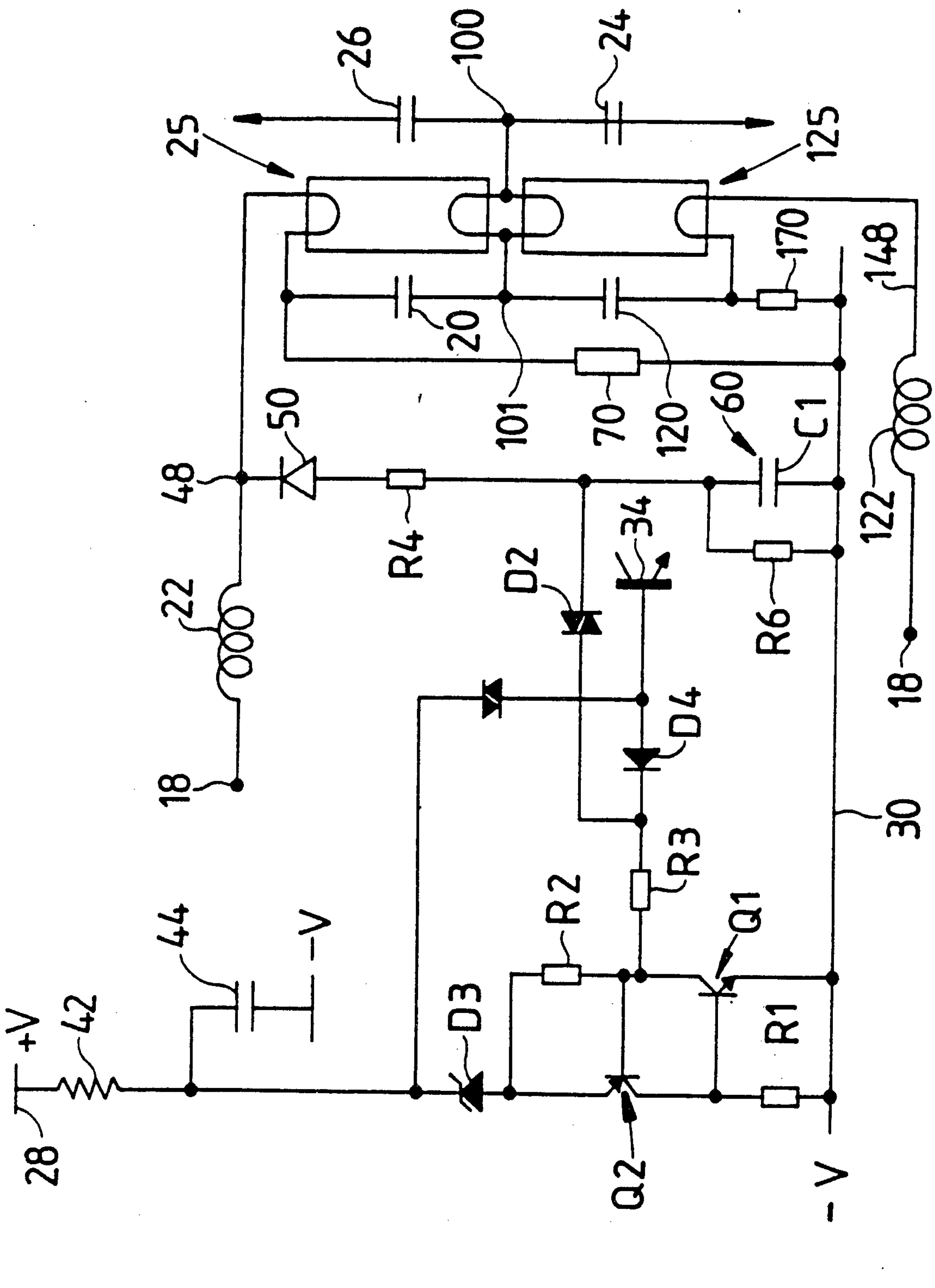

26
100
24
25
125
170
148
20
101
70
120
60
C1
50
48
R4
34
D2
22
R6
122
18
D4
18
R3
30
R2
Q1
44
-V
+V
42
D3
R1
28
Q2
-V

FIG 5

INTERNATIONAL SEARCH REPORT

International application No.
PCT/AU 93/00639

A. CLASSIFICATION OF SUBJECT MATTER

Int. Cl.5 H05B 41/36, 37/04, 37/03, 39/10, 41/46, 37/02

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC H05B 41/36, 37/04, 37/03, 39/10, 41/46, 37/02

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
AU : IPC as above

Electronic data base consulted during the international search (name of data base, and where practicable, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to Claim No.
X	US,A, 4598232 (NILSSEN) 1 July 1986 (01.07.86) See figure 2 and column 3 line 22 - column 4 line 68	7
X	US,A, 4207500 (Duve et al.) 10 June 1980 (10.06.80) See column 5 lines 27-35 and column 2 lines 8-30	16
X	Patent Abstracts of Japan, E-1182, page 66, JP,A, 3-289092 (HITACHI LIGHTING LTD) 19 December 1991 (19.12.91)	16
A	US,A, 4902938 (LINDQUIST) 20 February 1990 (20.02.90) See figure 1 and abstract	

[X] Further documents are listed in the continuation of Box C.

[X] See patent family annex.

* Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
24 March 1993 (24.03.93)	30 March 1994 (30.03.94)

Name and mailing address of the ISA/AU	Authorized officer
AUSTRALIAN INDUSTRIAL PROPERTY ORGANISATION PO BOX 200 WODEN ACT 2606 AUSTRALIA	R. TOLHURST
Facsimile No. 06 2853929	Telephone No. (06) 2832187

C(Continuation).	DOCUMENTS CONSIDERED TO BE RELEVANT	
Category*	Citation of document, with indication, where appropriate of the relevant passages	Relevant to Claim No.
A	WO,A, 84/00463 (STROEDE) 2 February 1984 (02.02.84) See figure 1 and pages 3 and 4	
A	GB,A, 2199204 (HUBBELL INCORPORATED) 29 June 1988 (29.06.88) See abstract and figure 1	
A	US,A, 5070279 (GARBOWICZ et al) 3 December 1991 (03.12.91) See abstract and figure 1	

Box I **Observations where certain claims were found unsearchable (Continuation of Item 1 of first sheet)**

This international search report has not established in respect of certain claims under Article 17(2)(a) for the following reasons:

1. ☐ Claims Nos.:
because they relate to subject matter not required to be searched by this Authority, namely:

2. ☐ Claim Nos.:
because they relate to parts of the international application that do not comply with the prescribed requirements to such an extent that no meaningful international search can be carried out, specifically:

3. ☐ Claims Nos.:
because they are dependent claims and are not drafted in accordance with the second and third sentences of Rule 6.4(a).

Box II **Observations where unity of invention is lacking (Continuation of item 2 of first sheet)**

This International Searching Authority found multiple inventions in this international application, as follows:

1. Claims 1-6

Protective electric circuit which generates a fault signal if drive voltage changes polarity with respect to a reference voltage and exceeds a predetermined time period.

Claims 7-15

Protective electric cirucit which disables the ballast invertes when the lamp is inactive, on the basis of the multiplied inverter output signal, for a predetermined time period.

2. Claims 16-17

Protective electric circuit which disables the inverter circuit when a faulty lamp is detected and having a resetting means to reset the protection circuit upon replacement of the lamp.

1. ☐ As all required additional search fees were timely paid by the applicant, this international search report covers all searchable claims

2. ☒ As all searchable claims could be searched without effort justifying an additional fee, this Authority did not invite payment of any additional fee.

3. ☐ As only some of the required additional search fees were timely paid by the applicant, this international search report covers only those claims for which fees were paid, specifically
claims Nos.:

4. ☐ No required additional search fees were timely paid by the applicant. Consequently, this international search report is restricted to the invention first mentioned in the claims; it is covered by claims Nos.:

Remark on Protest

☐ The additional search fees were accompanied by the applicant's protest.

☐ No protest accompanied the payment of additional search fees.

This Annex lists the known "A" publication level patent family members relating to the patent documents cited in the above-mentioned international search report. The Australian Patent Office is in no way liable for these particulars which are merely given for the purpose of information.

Patent Document Cited in Search Report		Patent Family Member					
WO	8400463	AU	17764/83	BR	8307637	DK	1172/84
		EO	121520	FI	843048	NO	840803
		SE	8207101	US	4570108		
GB	2199204	CA	1273051	JP	63143795	US	4810936
		AU	78939/87				
US	5070279	CA	2047505				

END OF ANNEX