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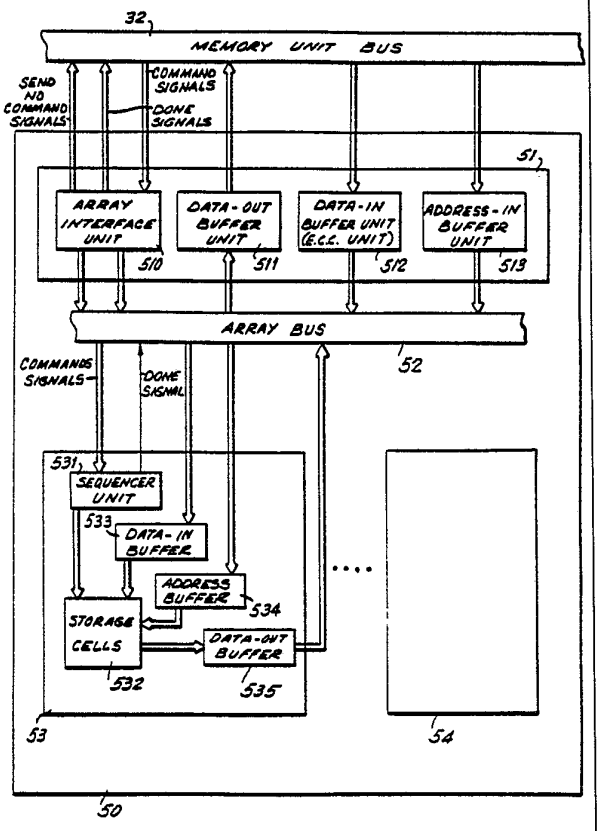
(54) Title: APPARATUS AND METHOD FOR PROVIDING DISTRIBUTED CONTROL IN A MAIN MEMORY UNIT OF A DATA PROCESSING SYSTEM

(57) Abstract

For use in a data processing system, a main memory subsystem includes a plurality of memory boards for storing groups of logic signals. Each memory board includes a plurality of array units. Each array unit is adapted to store a group of logic signals that is equivalent in size to the field of data logic signals transferred on the system bus and has an address structure so that each addressable data signal group can be stored in a signale array. The address field of each array unit is further adapted so that the probability of interfering activity in each array is low. The arrays are adapted to process data signal groups independently, thus, activity involving several arrays can take place simultaneously. The memory subsystem is structured to provide a pipeline type of overlapping activity so that activity involving several array units can be in progress simultaneously. Because the manipulation of the storage cells requires the most amounts of time in the memory unit, and because the arrays are performing this activity independently for each signal group, then the memory unit can be adapted to process the signal groups applied sequentially to the system without delay in nonexceptional circumstances, the most general exceptional circumstance being the masked write operation.



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APPARATUS AND METHOD FOR PROVIDING DISTRIBUTED CONTROL IN A MAIN MEMORY UNIT OF A DATA PROCESSING SYSTEM

BACKGROUND OF THE INVENTION

1. Field of the Invention

This invention relates generally to data processing systems and more particularly to the main memory unit storing the signal groups required for the current operation of the data processing system. The present invention provides for distributed control in the main memory unit as contrasted with the centralization of the memory unit control function in typical data processing subsystems.

2. Description of the Related Art

Referring to Figure 1, a typical data processing system configuration is shown. The data processing system includes at least one central processing unit 10 (or 11), at least one input/output device 13 (or 14), a memory unit 15 and a system bus 19 coupling the plurality of units or subsystems of the data processing system. The central processing unit processes groups of logic signals according to software and/or firmware instructions. The logic signal groups to be processed as well as the currently executing program are typically stored in the memory unit 15. A console unit 12 can be coupled to the central processing unit(s) and includes the apparatus and stored instructions to initialize the

system. The console unit 12 can also act as a terminal during the operation of the data processing system. The input/output unit(s) 13 (or 14) provide the interface to the remainder of the data processing system to terminal units, mass storage units, communication units, and any other units to be coupled to the data processing system. The detailed function of the units coupled to the system bus is less important than the fact that these units operate autonomously and communicate with the remainder of the data processing units by means of the system bus. In particular, the system bus is used to store signal groups into and to retrieve signal groups from the memory subsystem by the other subsystems.

Referring next to Figure 2, a block diagram of a typical main memory subsystem 15 found in the related art is shown. The main memory unit 15 includes a memory interface unit 21 that exchanges signals with the system bus 19. The memory interface unit 21 is coupled to an array bus 22 and the array bus 22 has at least one memory array unit 23 coupled thereto. The memory array units 23 (through 25) are comprised of a plurality of logic signal storage elements organized in groups so that each group of storage elements can be accessed by a unique address logic signal group. The memory interface unit 21 includes the apparatus for controlling the exchange of logic

signal groups, identified by an address logic signal group, between the memory array units 23 through 25 and the system bus 19. The memory interface unit 21 includes apparatus for identifying signal activity on the system bus 19 directed to the memory unit 15 as well as apparatus for returning logic signal groups to the subsystems transmitting requests for the signal groups. Buffering of the data signal groups, error correction and generation of control signal are also typically performed in the memory interface unit 21 in the related art.

The foregoing main memory architecture limits the amount of activity that can be performed in the main memory subsystem, because the activity must be performed under the control of the memory interface unit 21, to a single activity unless parallel apparatus is included for simultaneous processing of a plurality of signal groups.

A need has therefore been felt for apparatus and method of operation for the main memory subsystem that can permit a multiplicity of simultaneous operations involving the memory subsystem. This requirement is particularly stringent in the computer systems referred to as "write through" data processing systems in which each group of data signals from the central processing system is immediately stored or written into the main memory

subsystem. The memory activity resulting from this type of data processing system requirement can result in performance deterioration unless the memory subsystem is designed to accommodate the increased activity.

SUMMARY OF THE INVENTION

It is an object of the present invention to provide an improved data processing unit.

It is a further object of the present invention to provide an improved main memory subsystem for a data processing system.

It is yet another object of the present invention to provide a plurality of storage cell arrays in a main memory subsystem, each array capable of functioning independently of the other storage cell arrays.

It is a still further object of the present invention to provide an array unit bus, wherein a plurality of storage cell arrays are coupled to the array unit bus and wherein an interface unit couples the array unit bus with the system bus.

The aforementioned and other objects are accomplished, according to the present invention, by providing a main memory subsystem that includes a plurality of storage cell array units for storing groups of logic signals, an array bus coupled to the storage cell array units, and a memory array

interface unit for coupling the array bus and the system bus. The storage cell array units each have control apparatus associated therewith controlling the operation of the storage cells associated with the storage cell array. The control apparatus also serves the function of communicating the status of the storage cell array unit to the memory array interface unit to prevent inconsistent activity in the storage cell array units.

These and other features of the present invention will be understood upon reading of the following description along with the drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a block diagram of the components of a data processing system capable of utilizing the present invention.

FIG. 2 is a block diagram of a main memory unit typically provided in related data processing systems.

FIG. 3 is a block diagram of a main memory unit according to the present invention.

FIG. 4 is a block diagram of the apparatus providing the interface, in the main memory unit, between the memory boards and the data processing system.

FIG. 5 is a block diagram of apparatus comprising the memory boards according to the present

invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

1. Detailed Description of the Figures

Figure 1 and Figure 2 have been previously described with reference to data processing systems of the related art.

Referring next to Figure 3, the basic structure of the main memory subsystem 15 according to the present invention is shown. The main memory subsystem 15 includes a memory interface unit 40 that couples the main memory subsystem 15 to the system bus 19. The memory interface unit 40 is coupled to and exchanges signals with the memory unit bus 32. The memory unit bus 32, in turn, exchanges logic signal groups with a plurality of memory boards, memory boards 50 and 50" shown as an example of the relationship of the memory boards with respect to the remainder of the main memory subsystem. Each memory board 50 includes a board interface unit 51 that exchanges logic signals with the memory unit bus 32. The board interface unit 51, in turn, exchanges groups of logic signals with array bus 52 on board 50, while an plurality of memory arrays units, 53 through 54, also on board 50, are coupled to the array bus 52.

Referring next to Figure 4, a block diagram of the memory interface unit 21 is shown. A system bus

interface unit 401 controls the exchange of signals, including control signals between the system bus and the rest of the main memory unit. Of particular interest is the control signal labelled Memory Busy. With respect to the logic signal groups representing data, the data-in buffer unit 402 provides a temporary storage for data signals to be stored in the memory arrays 53 through 54. From the data-in buffer unit 402, the data signal groups are transferred to the memory unit bus 32. The data-out buffer unit 403 provides a temporary storage for data signal groups from the main memory unit that are to be transferred to a subsystem requesting the signal groups. A data path for data signal groups via memory bus 32 from the memory arrays 53 through 54 to the data-in buffer 402 is provided for the masked write operation, i.e. an operation in which the data signal group at a predetermined location (address) is only partially replaced with data from other subsystems. ECC generator unit 406, ECC comparison unit 405 and error correction apparatus 404 are included to verify the accuracy of the data being transferred from the memory subsystem to another portion of the data processing system. The memory interface unit also includes an address buffer unit 420 for temporary storage of address signal groups of data signal groups being stored in or retrieved from

the memory unit. The address buffer unit 420 is coupled to the system bus interface unit 401 and to the memory unit bus 32 to implement the transfer of address signal groups between the memory arrays 53 through 54 and the system bus 19.

Included in the memory interface unit 21 are also a multiplicity of units for controlling and monitoring the operation of the memory subsystem. The array status unit 410 receives signals from and applies signals to the memory control sequencer 411. The array status unit 410 also receives Data Ready/Done and Send No Command signals from the memory boards. The command buffer unit 412 provides a temporary storage for commands that are received from and applied to the system bus interface unit 401. The command buffer unit 412 also applies control signals to logic unit 414. Logic unit 414 also receives signals from the masked write control unit 413. The memory control sequencer 411 applies signals to the memory unit bus 32 and to the read command buffer 416 for temporary storage. The read command buffer 416 applies signals to the read command execution unit 417; the read command execution unit 417 in turn applies signals to the memory unit bus 32 and to the masked write control unit 413.

As stated above, the array status unit 410 receives Data Ready/Done signals and Send No Command

signals from the memory arrays. The Send No Command signals are used to insure that each array unit 53 through 54 is processing only one read command or a refresh operation. The Data Ready/Done signals are used to control status bits in the array status unit 410. The Data Ready/Done signals are asserted by the memory array prior to its being capable of processing another read operation, the data signal group having not been removed. The Send No Command signal is asserted and remains asserted prior to the assertion of the Data Ready/Done signal and remains asserted until the memory interface unit 21 has removed the data signal groups. Logic components (not shown) in the memory interface unit 21 insure that the commands are not sent to the the memory arrays 53 through 54 between the time that the memory interface unit 21 begins removing the data signal group and completes the data signal group removal.

It will be clear that numerous interconnections between the components of the memory interface unit that are typically used by a memory interface unit and have a standard functionality have not been explicitly illustrated. However, several signal lines that are useful in the explanation of the operation of the present invention are specifically shown. Busy Request lines couple control signals from the data-in buffer unit 402, the address buffer unit

420, and the command buffer unit 412 to the system bus interface unit 401. The presence of appropriate signals on these lines can result in a Memory Busy signal being applied to the system bus 19 (i.e. for use with a system bus arbitration unit). Similarly, the array status unit 410 receives Data Ready/Done signals and Send No Command signals, described above, from the memory boards.

Referring next to Figure 5, the apparatus implementing the memory boards, e.g. 50, according to the present invention is shown. The board interface unit 51 includes an array interface unit 510 that receives command signals from the memory unit bus 32 and applies status signals to the memory unit bus 32. The array interface unit 510 applies command signals to the array bus 52 and receives (Done) status signals from the array bus. The board interface unit 51 also includes a data-out buffer unit 511 for temporary storage of data signal groups applied to the array bus from the memory arrays 53 through 54, an address-in buffer unit 513 for temporary storage of address signals to be applied to the array bus 52 and data-in buffer unit 512 for temporary storage of data signals to be stored in the storage cells of the array. The data-in buffer unit 512 also includes ECC bit generation apparatus for storage with the data signal group.

The memory array units 53 through 54, illustrated in Figure 5, each include a sequencer unit 531 for receiving commands from the array bus 52 and for applying status (Done) signals to the array bus 52. The sequencer unit 531 controls the operation of the associated array of storage cells 532 within the memory array unit in response to the command signals received from the array bus. The memory array unit also includes a data-in buffer unit 533 for temporary storage of signal groups to be stored in the storage cell array 532, an address buffer unit 534 for temporary storage of signals determining the location in the storage cell array 532 to be manipulated by the sequencer unit 531 and a data-out buffer unit 535 for temporary storage of the signal groups being retrieved from the storage cell array 532. In the preferred embodiment, the data-in lines and buffer are also used as the data-out lines and buffer.

2. Operation of the Preferred Embodiment

Referring once again to Figures 3 and 5, the storage cells comprising the memory array units 53 through 54 on a memory board are implemented in such a manner that the number of logic signals that are transferred in parallel on the system bus, sometimes designated as a word or longword, can be stored in a group of associated related storage cells in one of

the memory array units. That is, the word or long associated with an address signal group can be completely stored in the memory array unit responding to the associated address signal group so that each group of signals transferred on the system bus is related to a single memory array unit. The memory array units are typically implemented in a technology that is considerably slower than the technology implementing the remainder of the signal processing circuits of the data processing system. As a result, the time to perform an operation involving the array can occupy multiple system clock cycles. To minimize the impact of the relatively slow speed of the memory arrays, the addresses can be arranged so that each array contains an address that is in consecutive sequence with the addresses of other arrays on the board. Furthermore, the addresses of the boards are also adapted so that the same array will not receive a second address in a consecutive sequence of addresses until all the other arrays have been addressed.

In a typical embodiment, the memory unit can include 8 boards and each board can include 4 memory arrays. In this situation, each memory array can be adapted to respond to every 32^{nd} address in the consecutive memory array address sequence (wherein each memory address can be associated with a

plurality of signal groups addressable by other subsystems of the data processing unit), although this capability may not be necessary in practice. However, the memory boards as described in the typical embodiment can support four write commands being processed simultaneously, or one read command being processed.

In the preferred embodiment, the address signal group can be applied to the arrays approximately three clock cycles after the address/command cycle is begun on the system bus. During this period of time, the determination is made in the memory interface unit 21 that the address signal group is valid, that a memory command is involved, and that the array unit that will process the command is available. Thus, the memory unit has the apparatus to transfer the signal groups to the appropriate array unit with sufficient rapidity so as not to limit the memory activity under normal circumstances.

The Busy Request signals can be generated by the command buffer unit 412, the address buffer unit 420 and the data-in buffer unit 402 when these units are in danger of being unable to process in-coming signal groups in an appropriate manner. The Busy Request signals are applied to the system interface unit 401 and the system interface unit can apply a Memory Busy signal to the system bus or to dedicated signal

paths. In the preferred embodiment, the Memory Busy signal, generated as a result of an earlier transaction, may be used to inform a data processing subsystem that an attempted later transaction was not successful prior to the notification of such a result by the means of the Confirmation Busy signal. In this manner, the data processing subsystem can begin attempting to reinitiate the transaction sooner. The Memory Busy signal is also used to prevent the arbitration unit from awarding access to the system bus for a transaction that may not be successful.

It will be clear that control signals exchanged between memory boards 50 and the memory interface unit 21, which permit the memory arrays to function independently, similarly permit the boards 50 etc. to function independently from the other memory boards and from the memory interface unit itself. As a result, memory boards with arrays which operate at different speeds can be used interchangeably in the board positions of the memory unit 15 of the present invention.

The foregoing description is included to illustrate the operation of the preferred embodiment and is not meant to limit the scope of the invention. The scope of the invention is to be limited only by the following claims. From the foregoing description, many variations will be apparent to those skilled in

the art that would yet be encompassed by the spirit and scope of the invention.

What is Claimed is:

1. A data processing system comprising:

a system bus;

at least one data processing unit coupled to said system bus; and,

a memory subsystem coupled to said system bus, said memory subsystem including:

a memory array interface unit coupled to said system bus; and,

a plurality of storage cell array units, each of said storage cell array units including a array of storage units and apparatus for controlling the operation of said array of storage units, wherein a plurality of said array units can process data signal groups simultaneously.

2. The data processing system of Claim 1 wherein said array units are coupled in groups, each of said array unit groups capable of processing memory operations at different rates.

3. The data processing system of Claim 1 wherein said memory subsystem further includes means for generating a signal when said subsystem can no longer process incoming data.

4. A memory board for use in a data processing system having a memory subsystem with a system bus interface unit and a plurality of said memory boards coupled thereto, said memory board comprising:

at least one array means for storing data signal groups;

sequencer means for controlling operation of said array means, said sequencer means including apparatus for generating a first signal when said array has completed a memory operation; and

interface means for applying a first and a second signal to said system bus interface unit, said first signal indicating that said array can process no commands, said second signal indicating that an array activity is complete.

5. The memory board of Claim 4 further comprising a bus means for distributing signal groups to said array means.

6. The memory board of Claim 4 further comprising means for coupling to a bus in said memory subsystem, said coupling means providing operation independent of other memory boards coupled to said memory subsystem bus.

7. The memory board of Claim 4 further comprising:

an array bus means for distributing signals to a plurality of array means coupled to said memory board; and

means coupled to each array for simultaneously processing a write operation in each of said plurality of arrays.

8. A method for storing data signal bits in a main memory of a data processing system comprising the steps of:

providing a plurality of semiconductor arrays, said plurality of arrays being coupled in groups of arrays;

coupling said groups of arrays to a remainder of said data processing unit through an interface unit; and

operating each of said groups of arrays to process transactions in said each array independently of transactions in other of said groups of arrays.

9. The method for storing data signal groups of Claim 8 wherein said operating step includes the step of operating each of said arrays to permit each array of a group of arrays to process a write operation simultaneously, said write operation of said array group being independent of the operation of other

arrays.

10. The method for storing data signal groups in Claim 9 wherein said operating step includes the step of performing one read operation by a one of said boards independently of the operation of said other array groups.

11. A memory subsystem for use with said data processing system comprising:

memory unit bus means;

interface means for transferring signal groups between said memory unit bus means and said data processing system;

at least one memory board coupled to said memory system bus;

plurality of memory arrays coupled to said board; and

control means associated with each memory board for permitting each memory board to operate independently of other memory boards, said control means enabling each memory array coupled to said memory board to process a data signal storage operation simultaneously.

AMENDED CLAIMS

[received by the International Bureau on 03 August 1987 (03.08.87); original claims 2–11 cancelled; claim 1 unchanged; new claims 2–12 added (4 pages)]

1. A data processing system comprising:

a system bus;

at least one data processing unit coupled to said system bus; and

a memory subsystem coupled to said system bus, said memory subsystem including:

a memory array interface unit coupled to said system bus; and

a plurality of storage cell array units, each of said storage cell array units including an array of storage units and apparatus for controlling the operation of said array of storage units, wherein a plurality of said array units can process data signal groups simultaneously.

2. A data processing system comprising:

(a) a system bus;

(b) at least one data processing unit coupled to said system bus; and

(c) a memory subsystem coupled to said system bus communication with said data processing unit, said memory subsystem comprising:

(i) a memory subsystem bus;

(ii) a memory interface means connecting said memory subsystem bus to said system bus; and

(iii) a plurality of memory boards connected to said memory subsystem bus, each memory board comprising an array bus, a board interface means for connecting said array bus to said memory subsystem bus, and a plurality of memory array means connected to said array bus, each memory array means including a plurality of storage cells and means for controlling the operation of said storage cells,

wherein a plurality of said memory array means can process data signal groups simultaneously.

3. The data processing system as defined in claim 2, wherein said plurality of memory boards includes a first memory board the memory array means of which operate at a first speed and a second memory board the memory array means of which operate at a second speed, said second speed being different than said first speed.

4. The data process system as defined in claim 2, wherein said memory interface means transmits a busy signal to said system bus when said memory subsystem is unable to process incoming data.

5. A memory board for use in a data processing system having a memory subsystem connected to a system bus, said memory subsystem including a memory subsystem bus and memory interface means for connecting said system bus and said memory subsystem bus, said memory board being connected to said memory subsystem bus and comprising a first memory array means for storing data signal groups, said first memory array means including a plurality of storage cells and sequencer means for controlling operation of said storage cells, said sequencer means comprising means for generating a DONE signal indicating said first memory array means has completed a memory operation, and said memory board further comprising board interface means for applying to said memory subsystem bus a signal indicating that said first memory array means can process no commands and a signal indicating that an array operation is complete.

6. The memory board as defined in claim 5, further comprising an array bus for connecting said board interface means and said first memory array means.

7. The memory board as defined in claim 6, wherein said board interface means comprises array interface means for receiving command signals from

said memory subsystem bus.

8. The memory board as defined in claim 5, further comprising second memory array means and an array bus for connecting said board interface means and said first and second memory array means, wherein each of said first and second memory array means comprises means for simultaneously writing data signal groups in storage cells of said first and second memory array means.

9. A method for storing data signal bits in a main memory of a data processing system comprising the steps of:

providing a plurality of semiconductor arrays, said plurality of arrays being coupled in groups of arrays;

coupling said groups of arrays to a system bus of said data processing system through an interface unit; and

operating each of said groups of arrays to process transactions in any one of said groups of arrays independently of transactions in other of said groups of arrays.

10. The method for storing data signal groups as defined in claim 9, wherein said operating step includes the step of operating each of said arrays to permit each array of any group of arrays to process a write operation simultaneously, said write operation of said group of arrays being independent of the operation of other groups of arrays.

11. The method for storing data signal groups as defined in claim 10, wherein said operating step includes the step of performing one read operation in one of said groups of arrays independently of the operation of said other groups of arrays.

12. A memory subsystem for use with a data processing system said memory subsystem comprising:

memory subsystem bus means;

interface means for transferring signal groups between said memory subsystem bus means and a

system bus of said data processing system;

a plurality of memory boards coupled to said memory subsystem bus means, each memory board comprising a plurality of memory arrays; and

control means associated with each memory board for permitting each memory board to operate independently of other memory boards, said control means enabling each memory array of a memory board to process a data signal storage operation simultaneously.

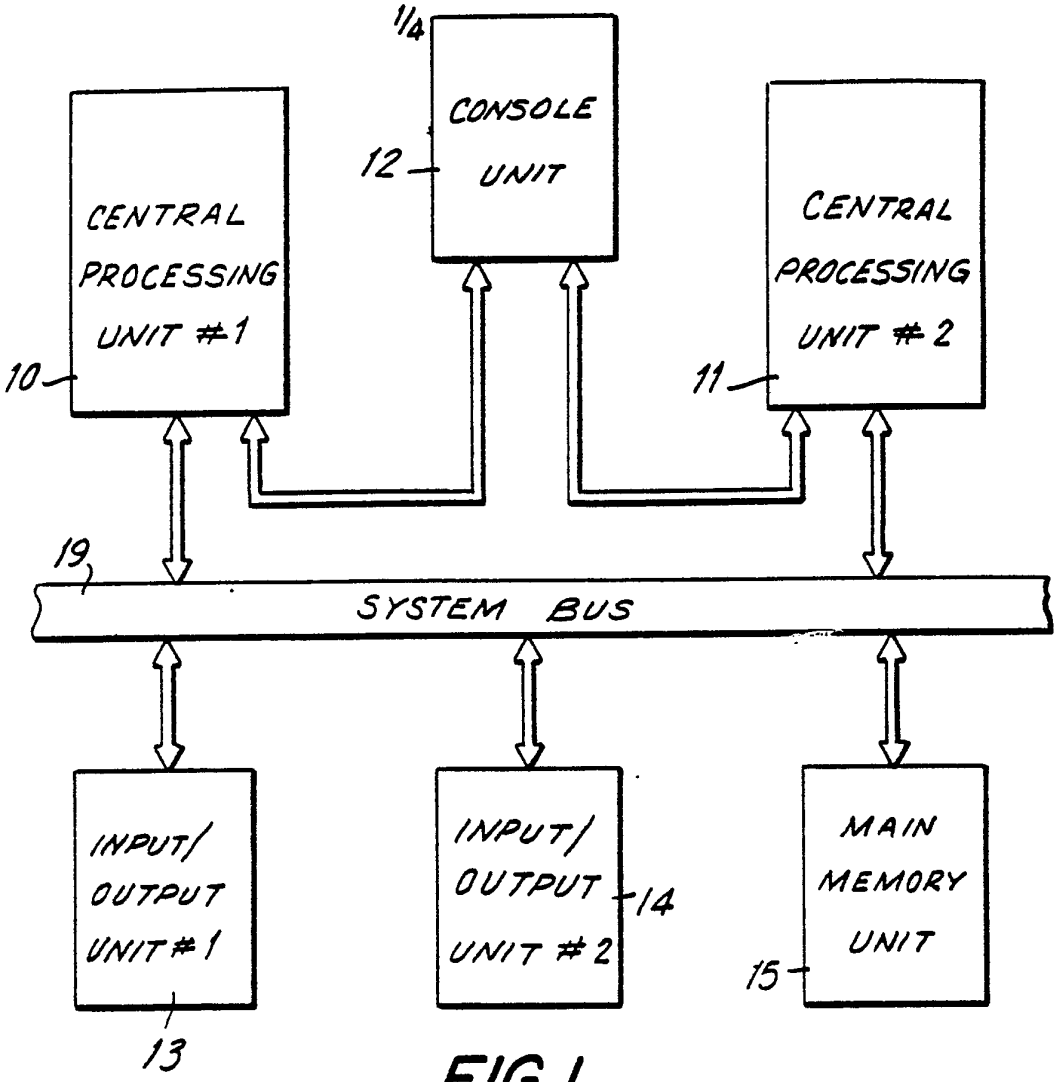

1/4
CONSOLE UNIT
12
CENTRAL PROCESSING UNIT #1
10
CENTRAL PROCESSING UNIT #2
11
19
SYSTEM BUS
INPUT/ OUTPUT UNIT #1
13
INPUT/ OUTPUT UNIT #2
14
MAIN MEMORY UNIT
15

FIG. 1

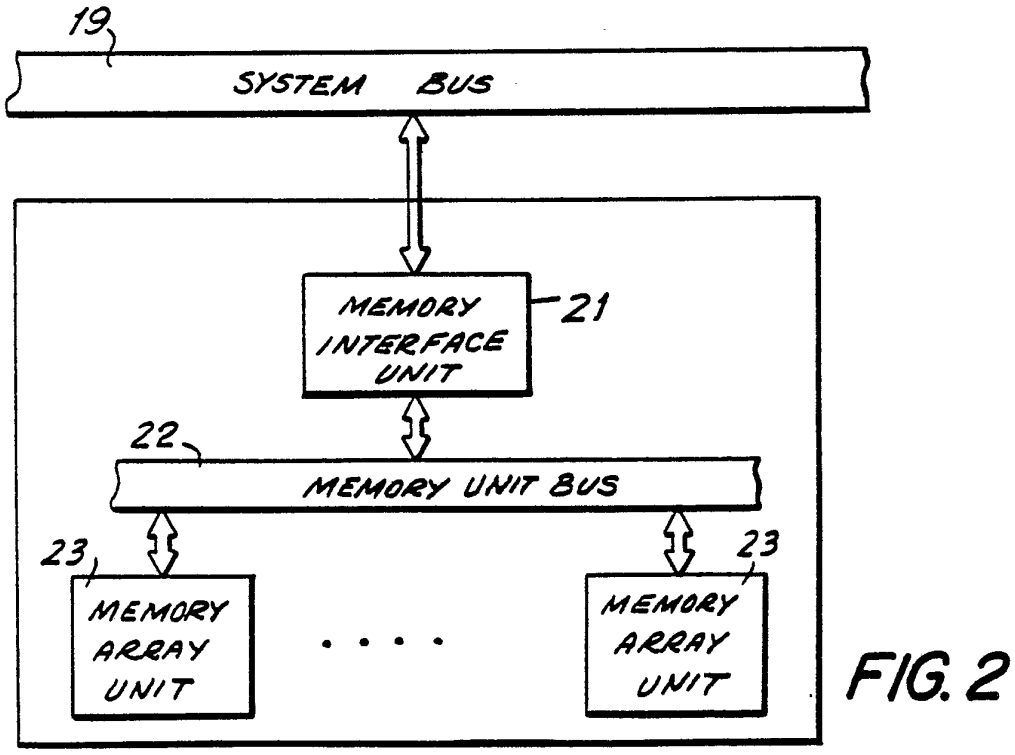

19
SYSTEM BUS
MEMORY INTERFACE UNIT
21
22
MEMORY UNIT BUS
23
MEMORY ARRAY UNIT
. . . .
23
MEMORY ARRAY UNIT

FIG. 2

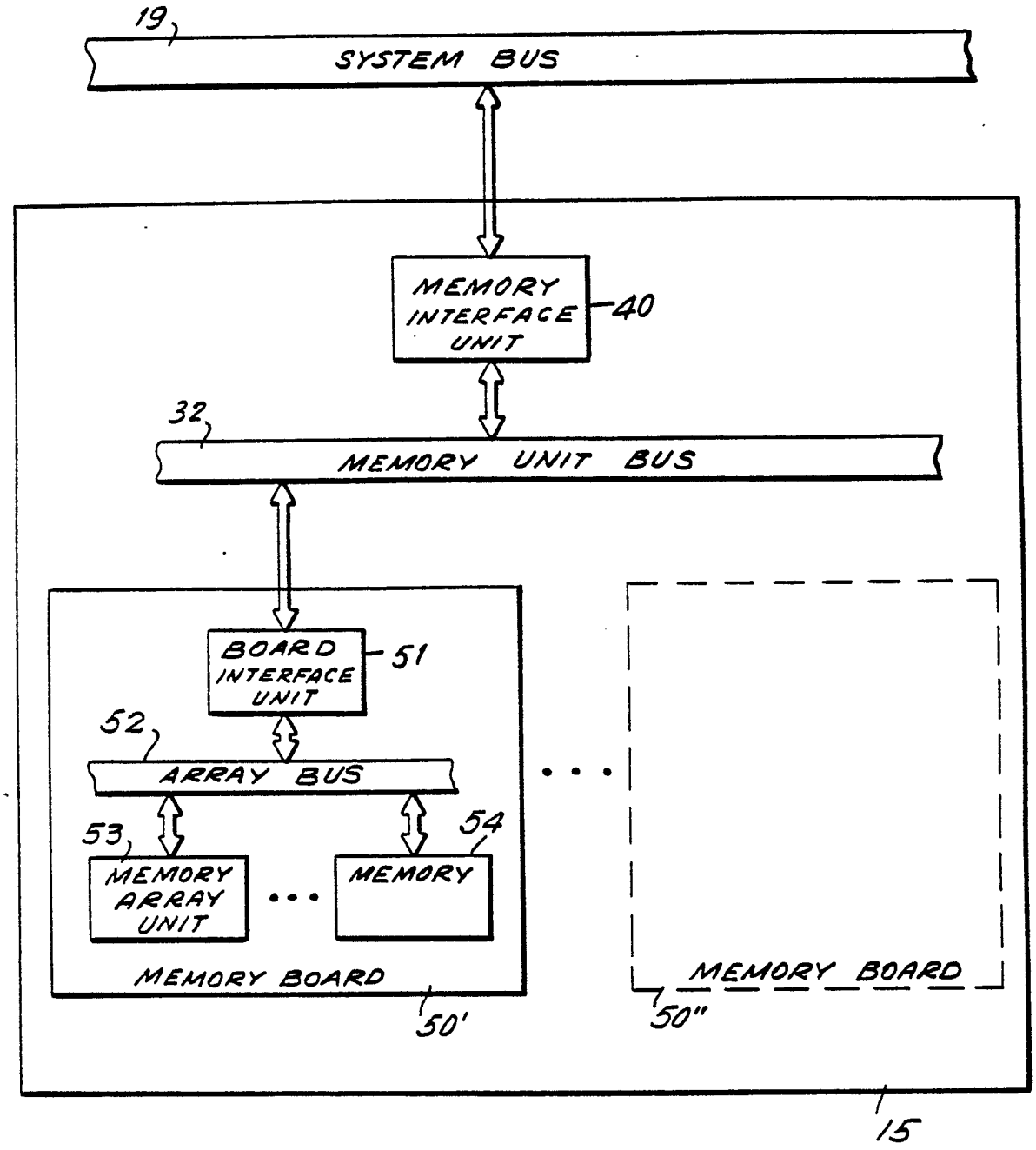

19
SYSTEM BUS
MEMORY INTERFACE UNIT
40
32
MEMORY UNIT BUS
BOARD INTERFACE UNIT
51
52
ARRAY BUS
53
54
MEMORY ARRAY UNIT
MEMORY
MEMORY BOARD
50'
MEMORY BOARD
50"
15

FIG. 3

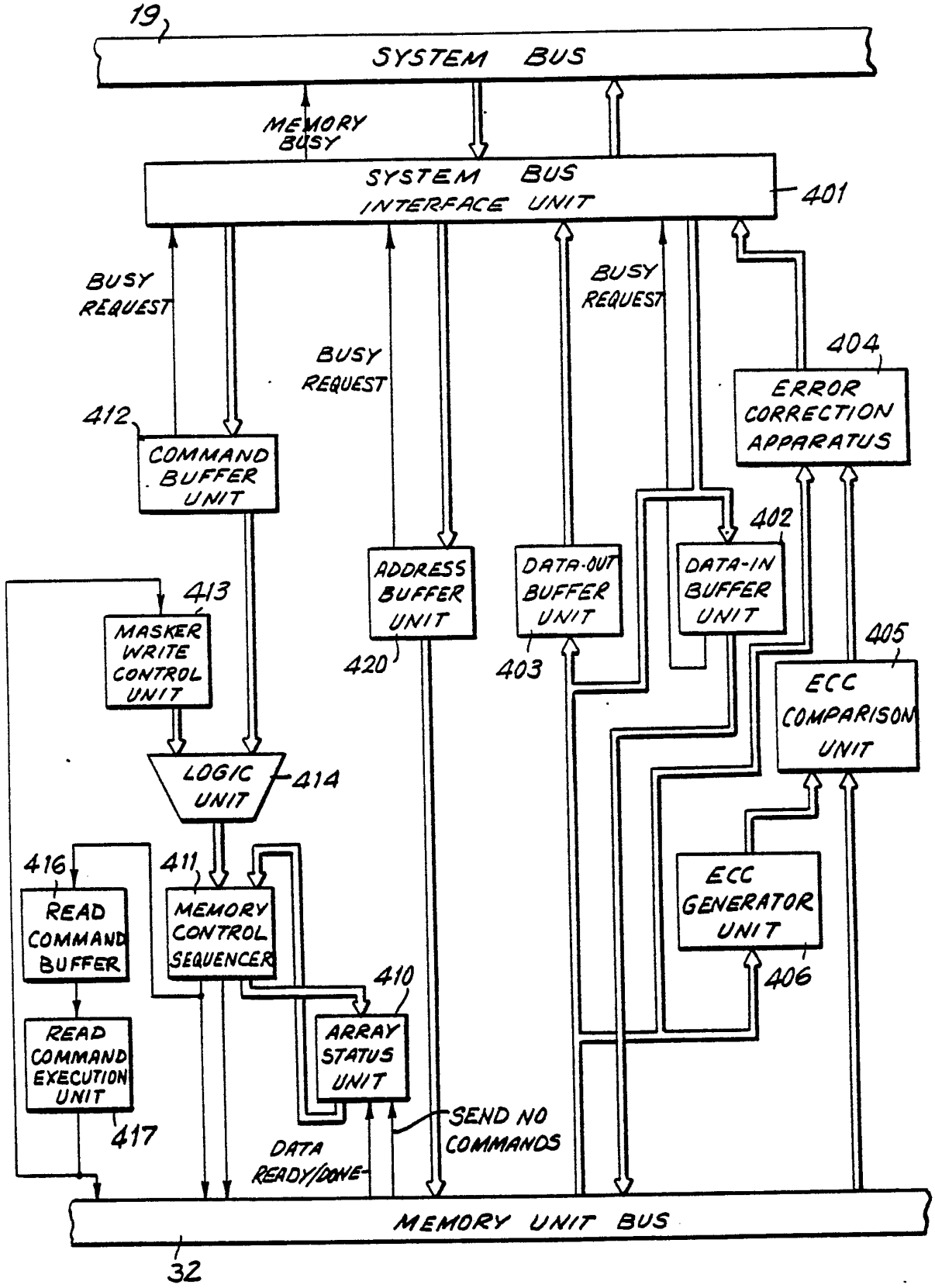
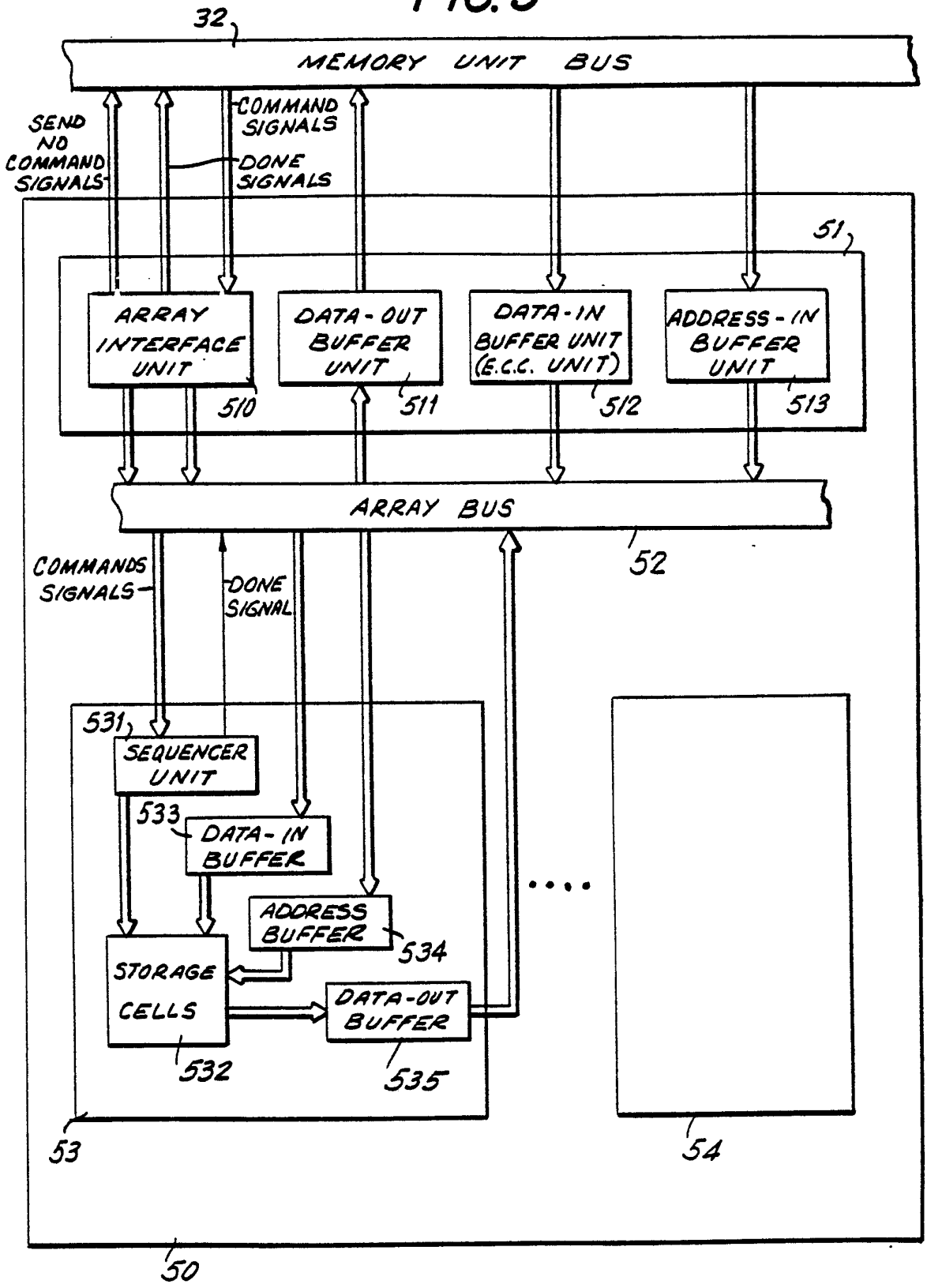

19
SYSTEM BUS
MEMORY BUSY
SYSTEM BUS INTERFACE UNIT
401
BUSY REQUEST
BUSY REQUEST
BUSY REQUEST
404
ERROR CORRECTION APPARATUS
412
COMMAND BUFFER UNIT
ADDRESS BUFFER UNIT
420
DATA-OUT BUFFER UNIT
403
DATA-IN BUFFER UNIT
402
413
MASKER WRITE CONTROL UNIT
405
ECC COMPARISON UNIT
LOGIC UNIT
414
416
READ COMMAND BUFFER
411
MEMORY CONTROL SEQUENCER
ECC GENERATOR UNIT
406
410
ARRAY STATUS UNIT
READ COMMAND EXECUTION UNIT
417
SEND NO COMMANDS
DATA READY/DONE
MEMORY UNIT BUS
32

FIG. 4

FIG. 5


32
MEMORY UNIT BUS
SEND NO COMMAND SIGNALS
COMMAND SIGNALS
DONE SIGNALS
51
ARRAY INTERFACE UNIT
510
DATA-OUT BUFFER UNIT
511
DATA-IN BUFFER UNIT (E.C.C. UNIT)
512
ADDRESS-IN BUFFER UNIT
513
ARRAY BUS
52
COMMANDS SIGNALS
DONE SIGNAL
531
SEQUENCER UNIT
533
DATA-IN BUFFER
ADDRESS BUFFER
534
STORAGE CELLS
532
DATA-OUT BUFFER
535
53
54
50

INTERNATIONAL SEARCH REPORT

International Application No PCT/US 87/00185

I. CLASSIFICATION OF SUBJECT MATTER (if several classification symbols apply, indicate all) [6]

According to International Patent Classification (IPC) or to both National Classification and IPC

IPC[4]: G 06 F 13/16

II. FIELDS SEARCHED

Minimum Documentation Searched [7]

Classification System	Classification Symbols
IPC[4]	G 06 F 13/16; G 06 F 13/18

Documentation Searched other than Minimum Documentation to the Extent that such Documents are Included in the Fields Searched [8]

III. DOCUMENTS CONSIDERED TO BE RELEVANT [9]

Category [10]	Citation of Document, [11] with indication, where appropriate, of the relevant passages [12]	Relevant to Claim No. [13]
X	DE, A, 2537787 (WOEHL) 3 March 1977, see page 4, lines 24-30; page 5, lines 1-29; page 7, lines 26-34; page 8, lines 8-22; page 9, lines 1-7; figures 2,3	1,8,9,11
A		4-7
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X	US, A, 3343140 (RICHMOND) 19 September 1967, see column 2, lines 14-20,46-60; column 25, lines 40-54; figures 1,2	1,8,11
A		4,7,9
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A	US, A, 4245303 (DURVASULA) 13 January 1981, see column 16, lines 7-23; column 25, lines 57-68; column 26, lines 1-11; figures 1,11	1

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* Special categories of cited documents: [10]

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IV. CERTIFICATION

Date of the Actual Completion of the International Search	Date of Mailing of this International Search Report
7th May 1987	01 JUN 1987
International Searching Authority	**Signature of Authorized Officer**
EUROPEAN PATENT OFFICE	M. VAN MOL

ANNEX TO THE INTERNATIONAL SEARCH REPORT ON

INTERNATIONAL APPLICATION NO. PCT/US 87/00185 (SA 16032)

This Annex lists the patent family members relating to the patent documents cited in the above-mentioned international search report. The members are as contained in the European Patent Office EDP file on 15/05/87

The European Patent Office is in no way liable for these particulars which are merely given for the purpose of information.

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
DE-A- 2537787	03/03/77	None	
US-A- 3343140		NL-A- 6509725	28/04/66
		BE-A- 667374	16/11/65
		DE-A- 1499194	30/10/69
		FR-A- 1453946	
		GB-A- 1069480	
US-A- 4245303	13/01/81	None	