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(54) **Title:** PROGRAMMABLE LOOP FILTER FOR USE WITH A SIGMA DELTA ANALOG-TO-DIGITAL CONVERTER

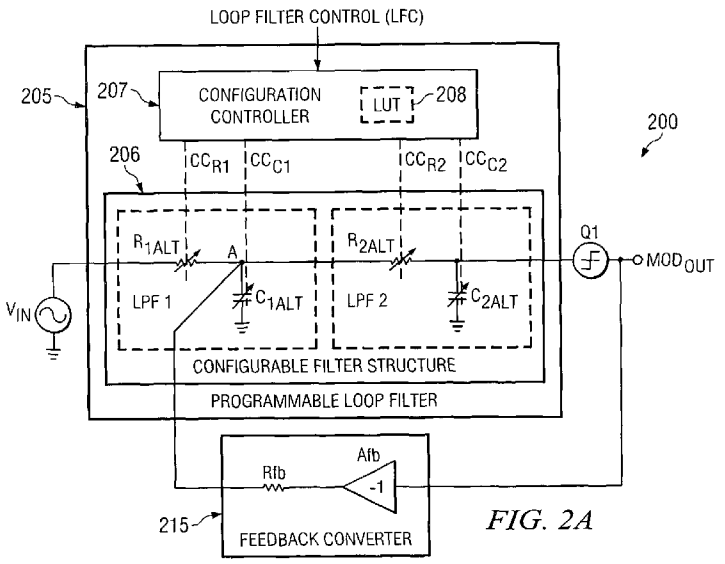


FIG. 2A

(57) **Abstract:** The present invention is directed to a programmable loop filter, a method of programming the same and a sigma delta analog-to-digital converter (ADC) incorporating the programmable loop filter or the method. In one embodiment, the programmable loop filter (205) includes: (1) a configurable filter structure (206) containing selectably interconnectable alternative filter elements LPF1, LPF2 and (2) a configuration controller (207) coupled to the configurable filter structure (206) and operable to interconnect at least a selected one of the filter elements LPF1, LPF2 to determine a transfer characteristic of the configurable filter structure (206) and set an operating condition of the sigma delta ADC.

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PROGRAMMABLE LOOP FILTER FOR USE WITH A SIGMA DELTA ANALOG-TO-DIGITAL CONVERTER

TECHNICAL FIELD OF THE INVENTION

[0001] The present invention is directed, in general, to analog-to-digital converters (ADCs) and, more specifically, to a programmable loop filter for use with a sigma delta ADC and a method of programming the same.

BACKGROUND OF THE INVENTION

[0002] An analog input signal can be converted into a digital output word using an analog-to-digital converter (ADC), which contains a mixture of analog and digital circuitry. The speed, resolution and linearity of the conversion affects the accuracy with which the digital output word represents the analog input signal. The conversion speed must be high enough to sample the shortest analog input signal period (highest analog signal frequency) at least twice. The conversion resolution is determined by the number of bits in the digital output word and must be large enough to resolve the maximum peak-to-peak analog input signal into a required degree of granularity. The conversion linearity must be sufficient to operate at, or preferably below, a required maximum level of distortion associated with the conversion process.

[0003] Several different algorithms and architectures exist that may be employed to accomplish a conversion. These include sigma delta, successive approximation, pipeline and flash ADCs, in increasing order of bandwidth capability. Of particular interest is the sigma delta ADC, which typically provides a reasonable trade-off between sampling rate and bits of

resolution, while providing a low component count that benefits cost of production, size and reliability.

[0004] The sigma delta ADC employs sigma delta modulation techniques that digitize an input signal using very low resolution (one-bit) and a very high sampling rate (often in the megahertz range). Oversampling and the use of digital filters increases the resolution to as many as twenty or more bits. It is especially useful for high resolution conversion of low to moderate frequency signals as well as low distortion conversion of signals containing audio frequencies due to its inherent qualities of good linearity and high accuracy.

[0005] In its basic form, the sigma delta ADC employs an input modulator and an output digital filter and decimator. The input modulator operates by accepting an input signal through an input summing junction, which feeds a loop filter. The loop filter basically provides an integrated value of this signal to a comparator, which acts as a one-bit quantizer. The comparator output signal is fed back to the input summing junction through a circuit acting as a one-bit digital-to-analog converter. The feedback loop forces the average of the feedback signal to be substantially equal to the input signal. The density of "ones" in the comparator output signal is proportional to the value of the input signal. The input modulator oversamples the input signal by clocking the comparator at a rate that is higher than the Nyquist rate. Then, the output digital filter and decimator produce output data words at a data rate appropriate to the conversion.

[0006] Quantization noise (or quantization error) is one of the factors that limits the dynamic range of an ADC. When an analog input signal is quantized, the quantization error is actually the "round off" error that occurs and has a magnitude that is typically one-half the value represented by the

conversions least significant bit. The quantization error is usually random and therefore may be treated as white noise. An input signal sampled at the Nyquist rate has its associated quantization noise folded into the input signal bandwidth.

[0007] Oversampling the input signal causes the quantization noise to be spread over a wider bandwidth, thereby reducing the level of quantization noise in the signal bandwidth by the oversampling ratio (oversampling rate/Nyquist rate). Additionally, the oversampled modulator also redistributes energy from the signal bandwidth to higher frequencies, thereby providing further advantageous noise shaping.

[0008] General purpose sigma delta ADCs are often designed to be employed in a spectrum of applications having differing input signal bandwidth requirements. For example, one application may only require that a bandwidth of 10 kHz be accommodated, while another application may require a bandwidth of 100 kHz. For this case, the input modulator of the sigma delta ADC would have to accommodate an input signal bandwidth of at least 100 kHz. Accommodating this 100 kHz bandwidth establishes an equivalent noise level and thereby a dynamic range for the ADC. Unfortunately, this dynamic range is less than a dynamic range that the sigma delta ADC could provide for an input signal bandwidth of only 10 kHz.

[0009] Accordingly, what is needed in the art is a way for a general purpose sigma delta ADC to provide a dynamic range commensurate with an input signal bandwidth.

SUMMARY OF THE INVENTION

[0010] To address the above-discussed deficiencies of the prior art, the present invention provides a programmable loop filter, a method of programming the same, and a sigma delta analog-to-digital converter (ADC) incorporating the programmable loop filter or the method. In one embodiment, the programmable

loop filter includes: (1) a configurable filter structure containing selectably interconnectable alternative filter elements; and (2) a configuration controller coupled to the configurable filter structure and operable to interconnect at least a selected one of the filter elements to determine a transfer characteristic of the configurable filter structure and set an operating condition of the sigma delta ADC.

[0011] In another aspect, the present invention provides a method of programming a loop filter for use with a sigma delta analog-to-digital converter (ADC). The method includes: (1) selecting, from a configurable filter structure containing selectably interconnectable alternative filter elements, at least one of the filter elements; and (2) interconnecting the at least one of the filter elements to determine a transfer characteristic of the configurable filter structure and set an operating condition of the sigma delta ADC.

[0012] The present invention also provides, in yet another aspect, a modulator for use with a sigma delta analog-to-digital converter (ADC). The modulator includes an input signal summing junction and a programmable loop filter, coupled to an output of the summing junction. The programmable loop filter has a configurable filter structure that contains selectably interconnectable alternative filter elements, and a configuration controller, coupled to the configurable filter structure, that operates to interconnect at least a selected one of the filter elements to determine a transfer characteristic of the configurable filter structure and set an operating condition of the sigma delta ADC. The modulator also includes a one-bit quantizer coupled to an output of the programmable loop filter, and a one-bit digital-to-analog converter coupled between an output of the one-bit quantizer and the summing junction.

BRIEF DESCRIPTION OF THE DRAWINGS

[0013] FIG. 1 illustrates an embodiment of a sigma delta analog-to-digital converter (ADC) employing a programmable loop filter constructed in accordance with the principles of the present invention;

[0014] FIG. 2A illustrates an embodiment of a modulator employing a programmable loop filter constructed in accordance with the principles of the present invention;

[0015] FIG. 2B illustrates an alternative embodiment of a modulator employing an alternative programmable loop filter constructed in accordance with the principles of the present invention; and

[0016] FIG. 3 illustrates a flow diagram of an embodiment of a method of programming a loop filter carried out in accordance with the principles of the present invention.

DETAILED DESCRIPTION

[0017] Referring initially to FIG. 1, illustrated is a diagram of an embodiment of a sigma delta analog-to-digital converter (ADC), generally designated 100, employing a modulator 105 constructed in accordance with the principles of the present invention. The sigma delta ADC 100 includes the modulator 105 that receives an input signal voltage Vin, a digital filter and decimator module 115 that provides a converter output signal ADCout and a converter control module 120. The modulator 105 includes a summing junction 106, a programmable loop filter 110, a one-bit quantizer 113 and a one-bit digital-to-analog converter (DAC) 114. The programmable loop filter 110 includes a configuration filter structure 111 and a configuration controller 112.

[0018] The sigma delta ADC 100 converts the input signal voltage Vin into the converter output signal ADCout. The modulator 105 quantizes the input signal voltage Vin and provides a modulator output signal 107, which is an oversampled digital

signal, to the digital filter and decimator module 115. An oversampling frequency Kfs for the one-bit quantizer 113 and a sampling frequency fs for the digital filter and decimator module 115 are provided by the converter control module 120. These are determined by a required bit-resolution of the conversion and a highest frequency associated with the input signal voltage Vin, respectively. The modulator output signal 107 provides a serial bitstream that produces one bit for each period of the oversampling frequency Kfs. This is transformed for the converter output signal ADCout into a parallel digital word having N bits for each period of the sampling frequency fs, where N is the number of bits associated with the conversion.

[0019] The modulator 105 receives the input signal voltage Vin employing the summing junction 106, as shown. The output of the summing junction 106 provides an average error signal between the input signal voltage Vin and the output of the one-bit DAC 114, which reflects the inverse of the state of the oversampled digital signal 107. The programmable loop filter 110 processes this average error signal for quantization by the one-bit quantizer 113.

[0020] The programmable loop filter 110 employs the configurable filter structure 111, which contains selectably interconnectable alternative filter elements, to form a transfer characteristic that includes a low pass frequency response. Additionally, the programmable loop filter 110 couples the configuration controller 112 to the configurable filter structure 111 and interconnects at least one of the filter elements thereby determining at least one pole of the transfer characteristic of the configurable filter structure 111. This action is initiated by a loop filter control signal LFC from the converter control module 120 and sets an operating condition of the sigma delta ADC 100. The operating condition may

accommodate a particular application employing an industry standard, such as Bluetooth support in a Global System for Mobile Communications (GSM) receiver. Additionally, one or more industry standards may also be employed to tune the sigma delta ADC 100 for best performance within a desired bandwidth. Generally, by changing the transfer characteristic of the programmable loop filter 110, the signal-to-quantization noise ratio of the sigma delta ADC 100 may be enhanced thereby increasing its overall signal-to-noise ratio and dynamic range for the particular application.

[0021] Alternative embodiments of a sigma delta ADC may be constructed in accordance with the principles of the present invention. In one embodiment, the feedback employed may be multi-bit using a multi-bit DAC wherein the associated bit stream may become a symbol stream. In another embodiment, more than one feedback loop may be employed wherein the feedback provided is single bit, multi-bit or a combination of the two. Additionally, the configurable filter structure may employ one or more low pass or bandpass filters wherein at least a selected one the filter elements is operable to be interconnected by a configuration controller. In yet another embodiment, a plurality of summing junctions or summing nodes may be employed that are typically separated by one or more programmable filters. In general, the programmable filters employed in an embodiment may have passive or active components or a combination of both.

[0022] Turning now to FIG. 2A, illustrated is a diagram of an embodiment of a modulator, generally designated 200, employing a programmable loop filter 205 constructed in accordance with the principles of the present invention. The modulator 200 may be used with a sigma delta ADC and includes the programmable loop filter 205 coupled to an input signal Vin, a quantizer Q1 having

a modulator output signal MODout and a feedback converter 215 having a feedback amplifier Afb and a feedback resistor Rfb. The programmable loop filter 205 includes a configurable filter structure 206 and a configuration controller 207. The configurable filter structure 206 includes first and second low pass filters LPF1, LPF2. The configuration controller 207 includes a look-up table 208.

[0023] Operation of the modulator 200 parallels that of the modulator 105 discussed with respect to FIG. 1. The modulator output signal MODout provides one bit per oversampled quantization period having a bipolar output state, as before. The feedback converter 115 employs the feedback amplifier Afb to invert the modulator output signal MODout and apply it using the feedback resistor Rfb. A summing node A replaces the summing junction 106 of FIG. 1 to produce an error signal for the modulator 200.

[0024] The first and second low pass filters LPF1, LPF2 contain selectably interconnectable alternative filter elements. The first low pass filter LPF1 includes first alternative resistive filter elements R_{1ALT} and first alternative capacitive filter elements C_{1ALT}. Similarly, the second low pass filter LPF2 includes second alternative resistive filter elements R_{2ALT} and second alternative capacitive filter elements C_{2ALT}. The configuration controller 207 receives a loop filter control command LFC that provides a general instruction regarding a transfer characteristic required to enhance a particular application.

[0025] In response, the configuration controller 207 provides first filter resistive and capacitive control commands CC_{R1}, CC_{C1} and second filter resistive and capacitive control commands CC_{R2}, CC_{C2}. These commands respectively select the appropriate filter elements to determine the required transfer characteristic for

the low pass frequency responses associated with the first and second low pass filters LPF1, LPF2. In the illustrated embodiment, the look-up table 208 is employed to determine at least one of the filter elements. Alternatively, an appropriate polynomial equation may be employed instead of the look-up table 208. This action determines at least one pole of the configurable filter structure 206 and sets an operating condition of the sigma delta ADC that enhances a signal to noise ratio for the application.

[0026] In the illustrated embodiment, the configurable filter structure 206 may employ a passive implementation using cascaded IIR filter stages having either switched capacitor passive filter stages, cascaded RC filter stages or a combination of both. The programmable loop filter 205 may also be employed in multiple applications (corresponding to multiple industry standards) wherein its poles are determined by selecting appropriate capacitance ratios in the switched capacitor implementation or varying a capacitor size in the continuous time-domain implementation. Of course, other passive implementations may be employed, as well as an active filter implementation as appropriate to a particular sigma delta ADC design. Additionally, selection of the poles may also be employed to tune a dynamic range of the sigma delta ADC to compensate for component tolerances within a particular application.

[0027] Table 1, below, indicates the effect of various filter pole locations on the signal-to-noise (S/N) ratio for several bandwidths. As shown, positioning of these filter poles may result in a significant difference in the S/N ratio and therefore the dynamic range of the associated sigma delta ADC.

Table 1: S/N ratio for a sinusoidal 100 KHz tone

LPF1 Pole (KHz)	LPF2 Pole (KHz)	S/N Ratios for Bandwidths Shown (N = Thermal + Quantization)		
		200 KHz	1 MHz	3 MHz
325	3300	62.52	55.10	40.71
1000	3300	63.07	58.20	47.95
2000	3300	62.52	57.33	49.97
3000	3300	61.77	55.83	49.43
325	5000	63.53	54.82	41.41
1000	5000	62.99	57.38	47.86
2000	5000	61.63	55.62	48.71
3000	5000	59.33	53.35	47.34

[0028] Turning now to FIG. 2B, illustrated is an alternative embodiment of a modulator, generally designated 250, employing an alternative programmable loop filter 255 constructed in accordance with the principles of the present invention. The modulator 250 may also be used with a sigma delta ADC and includes the alternative programmable loop filter 255 coupled to an input signal Vin, a quantizer Q1 having a modulator output signal MODout and a feedback converter 265 having first and second feedback amplifiers Afb1, Afb2 respectively coupled to first and second feedback resistors Rfb1, Rfb2. The programmable loop filter 255 includes a configurable filter structure 256 and a configuration controller 257. The configurable filter structure 256 includes first and second, low pass filters LPF1, LPF2, as before, and third and fourth low pass filters LPF3, LPF4, which are coupled by an active coupling element G. The configuration controller 257 includes a look-up table 258, but an appropriate polynomial equation may also be employed, as

before.

[0029] Operation of the modulator 250 generally parallels the operation of the modulator 200, as was discussed with respect to FIG. 2A. However, the modulator 250 employs two summing nodes A and B to accommodate the two outputs from the first and second feedback resistors R_{fb1}, R_{fb2} in the feedback converter 265, as shown. The first and second feedback resistors R_{fb1}, R_{fb2} may be scaled to accommodate needed signal magnitudes at the two summing nodes A and B. The configuration controller 257 provides additional third and fourth resistive control commands CC_{R3}, CC_{R4} and third and fourth capacitive control commands CC_{C3}, CC_{C4} to the third and fourth low pass filters LPF3, LPF4, respectively. The configurable filter structure 256 employs the active coupling element G to maintain a required signal level between the second and third low pass filters LPF2, LPF3. Of course, bandpass filters may also be employed in the configurable filter structure 256, as may be appropriate to a particular requirement.

[0030] Turning now to FIG. 3, illustrated is a flow diagram of an embodiment of a method of programming a loop filter, generally designated 300, carried out in accordance with the principles of the present invention. The method 300 may be used with a sigma delta ADC and starts in a step 310 with an intent to provide a loop filter response that will enhance a dynamic range of the sigma delta ADC for a particular application based on an industry standard. Then an appropriate filter transfer response for the application, which includes a low pass frequency response, is determined in a step 310.

[0031] The corresponding poles, associated with the low pass frequency response, are then determined in a step 315. One or more filter elements are selected from a configurable filter structure containing alternative filter elements that are

selectably interconnectable, in the step 315. These alternative filter elements may be selected from the group consisting of analog filter elements and digital filter elements. These selections may employ a look-up table to facilitate the selecting process. Alternatively, the method 300 may calculate the required one or more filter elements and their interconnections needed to generate the poles of the required filter transfer characteristic. Then, in a step 325, the one or more filter elements are interconnected to determine the required filter transfer characteristic. This action sets an operating condition that improves a S/N ratio for the particular application of the sigma delta ADC. The method 300 ends in a step 330.

[0032] While the method disclosed herein has been described and shown with reference to particular steps performed in a particular order, it will be understood that these steps may be combined, subdivided, or reordered to form an equivalent method without departing from the teachings of the present invention. Accordingly, unless specifically indicated herein, the order and/or the grouping of the steps are not limitations of the present invention.

[0033] In summary, embodiments of the present invention employing a programmable loop filter and method of programming a loop filter have been presented. Advantages include the ability to select at least one filter pole and determine a filter transfer characteristic that enhances the performance of an associated sigma delta ADC. The programmable loop filter and method may also be employed to tune or enhance a filter response that would otherwise be de-tuned due to component tolerances.

CLAIMS

1. A programmable loop filter for use with a sigma delta analog-to-digital converter (ADC), comprising:

a configurable filter structure containing selectably interconnectable alternative filter elements; and

a configuration controller coupled to said configurable filter structure and operable to interconnect at least a selected one of said filter elements to determine a transfer characteristic of said configurable filter structure and set an operating condition of said sigma delta ADC.

2. The programmable loop filter recited in Claim 1, wherein said alternative filter elements determine at least one pole of said configurable filter structure.

3. The programmable loop filter recited in Claim 1 or 2, wherein a look-up table is employed to determine said at least a selected one of said filter elements.

4. The programmable loop filter recited in Claim 1, wherein said transfer characteristic includes a low pass frequency response.

5. A method of programming a loop filter for use with a sigma delta analog-to-digital converter (ADC), comprising:

selecting, from a configurable filter structure containing selectably interconnectable alternative filter elements, at least one of said filter elements; and

interconnecting said at least one of said filter elements to determine a transfer characteristic of said configurable filter structure and set an operating condition of said sigma

delta ADC.

6. The method as recited in Claim 5, wherein said alternative filter elements determine at least one pole of said configurable filter structure.

7. The method as recited in Claim 5 or 6, wherein said selecting comprises employing a look-up table.

8. The method as recited in Claim 5, wherein said transfer characteristic includes a low pass frequency response.

9. A modulator for use with a sigma delta analog-to-digital converter (ADC), comprising:

a summing junction coupled to an input signal;

a programmable loop filter, coupled to an output of said summing junction, including:

a configurable filter structure that contains selectably interconnectable alternative filter elements, and

a configuration controller coupled to said configurable filter structure that operates to interconnect at least a selected one of said filter elements to determine a transfer characteristic of said configurable filter structure and set an operating condition of said sigma delta ADC;

a one-bit quantizer coupled to an output of said programmable loop filter; and

a one-bit digital-to-analog converter coupled between an output of said one-bit quantizer and said summing junction.

10. The modulator as recited in Claim 9, wherein said alternative filter elements determine at least one pole of said configurable filter structure.

11. The modulator as recited in Claim 9 or 10, wherein a look-up table is employed to determine said at least said selected one of said filter elements.

12. The modulator as recited in Claim 9, wherein said transfer characteristic includes a low pass frequency response.

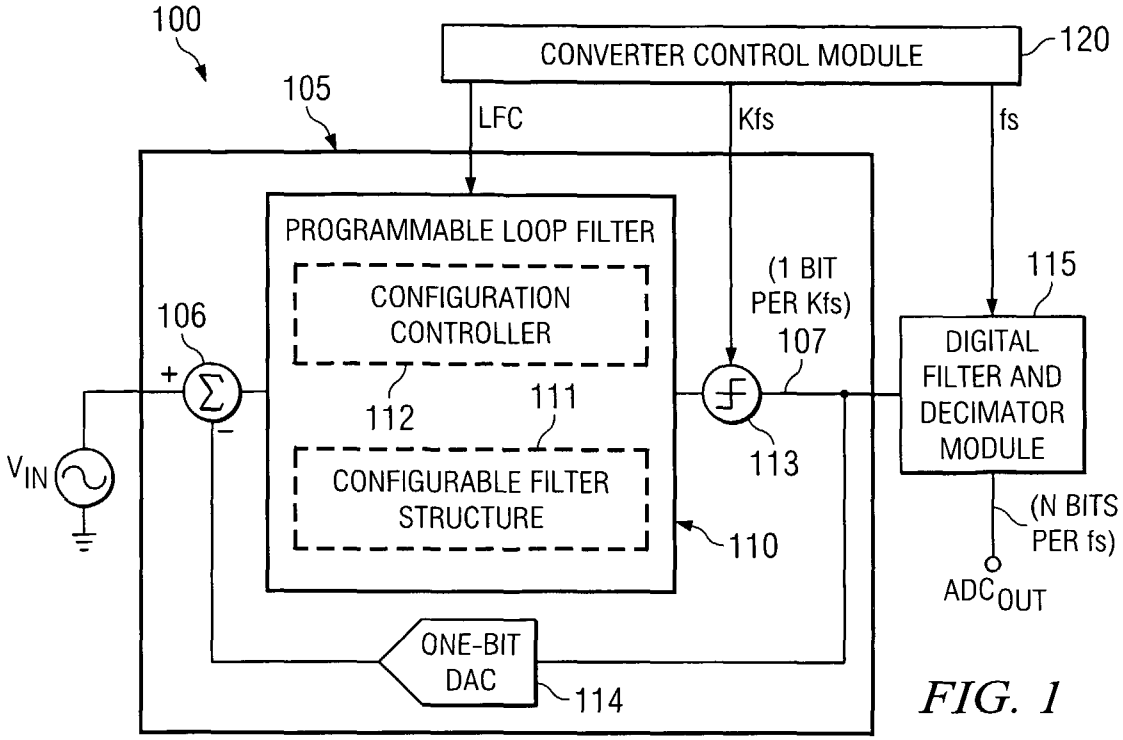

100
105
CONVERTER CONTROL MODULE
120
LFC
Kfs
fs
PROGRAMMABLE LOOP FILTER
CONFIGURATION CONTROLLER
112
111
CONFIGURABLE FILTER STRUCTURE
110
106
+
Σ
−
VIN
(1 BIT PER Kfs)
107
113
115
DIGITAL FILTER AND DECIMATOR MODULE
(N BITS PER fs)
ADCOUT
ONE-BIT DAC
114

FIG. 1

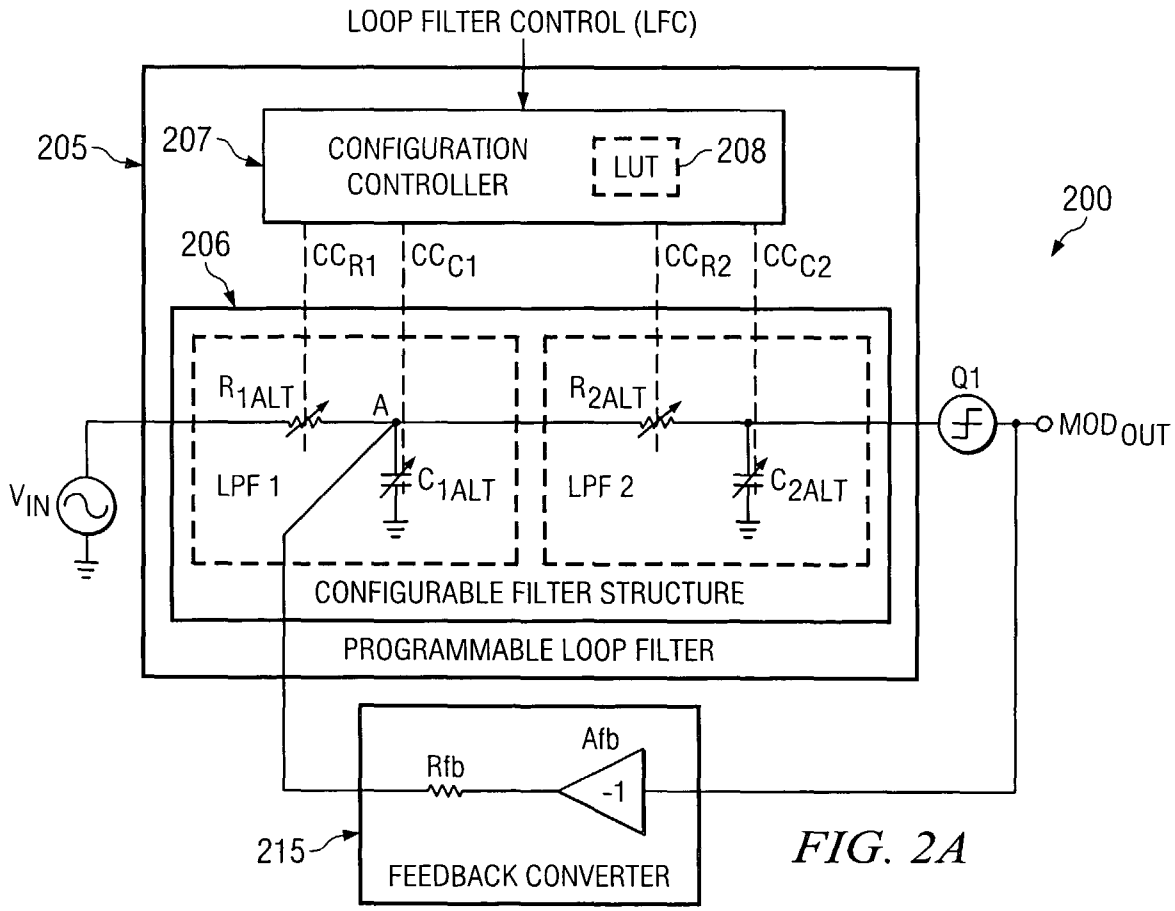

LOOP FILTER CONTROL (LFC)
205
207
CONFIGURATION CONTROLLER
LUT
208
200
206
CCR1
CCC1
CCR2
CCC2
R1ALT
A
R2ALT
Q1
MODOUT
VIN
LPF 1
C1ALT
LPF 2
C2ALT
CONFIGURABLE FILTER STRUCTURE
PROGRAMMABLE LOOP FILTER
Afb
Rfb
-1
215
FEEDBACK CONVERTER

FIG. 2A

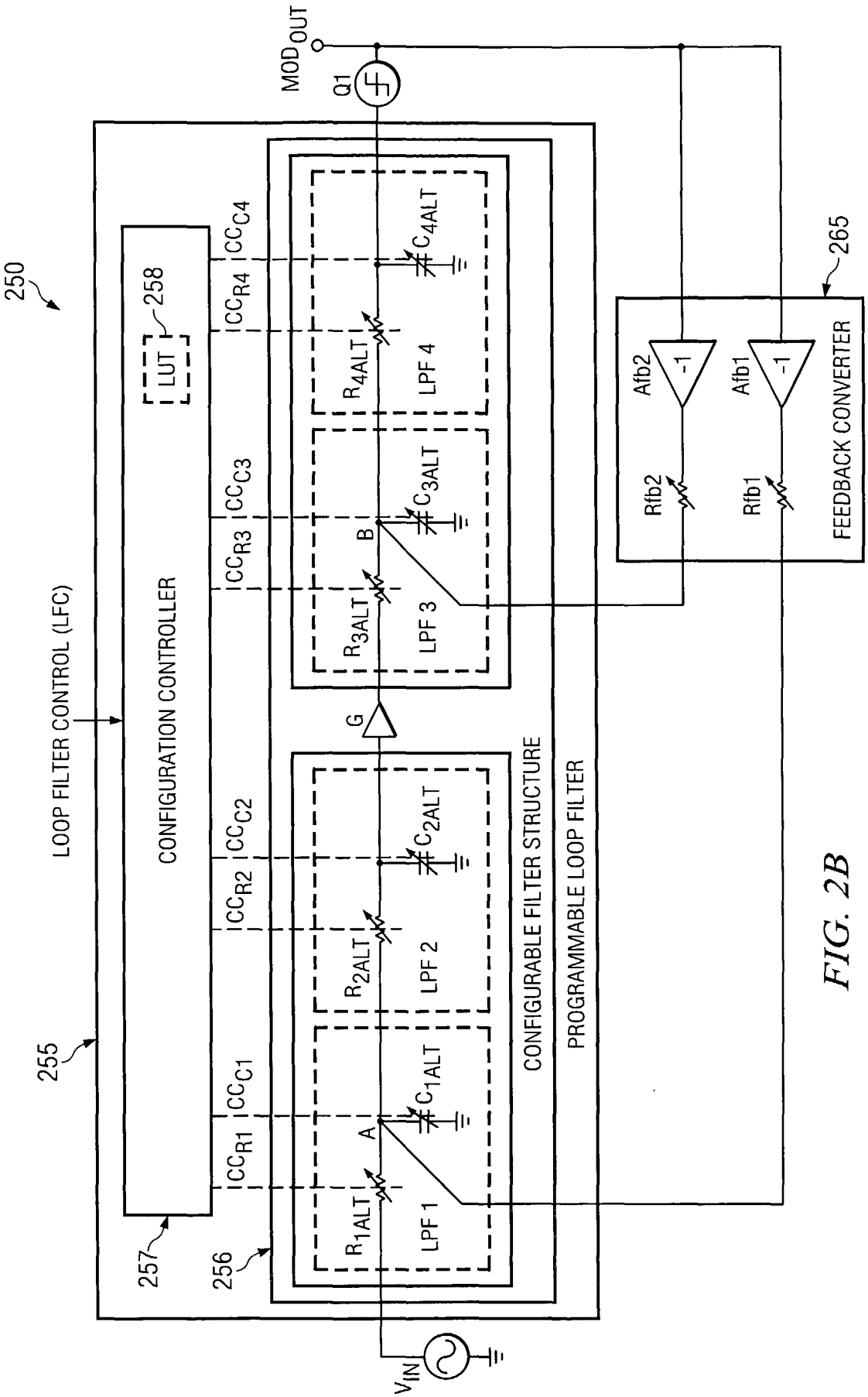
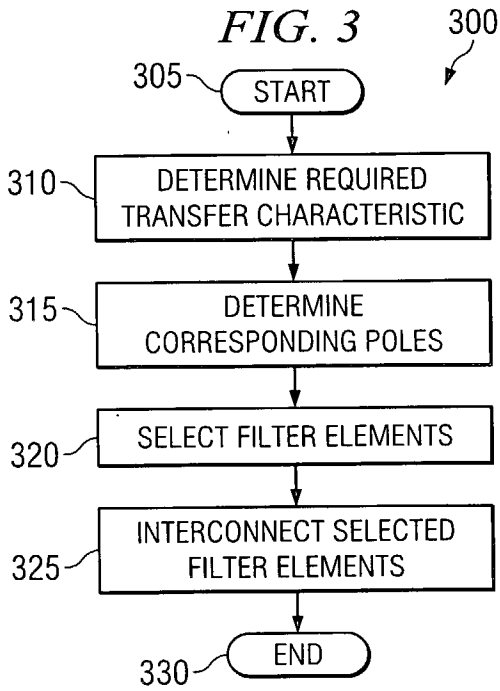

250
255
256
257
258
265
LOOP FILTER CONTROL (LFC)
CONFIGURATION CONTROLLER
LUT
CONFIGURABLE FILTER STRUCTURE
PROGRAMMABLE LOOP FILTER
FEEDBACK CONVERTER
MOD OUT
Q1
V IN
G
A
B
CC C1
CC R1
CC R2
CC C2
CC R3
CC C3
CC R4
CC C4
R 1ALT
C 1ALT
LPF 1
R 2ALT
C 2ALT
LPF 2
R 3ALT
C 3ALT
LPF 3
R 4ALT
C 4ALT
LPF 4
Afb2
Afb1
-1
-1
Rfb2
Rfb1

FIG. 2B

FIG. 3


300
305
START
310
DETERMINE REQUIRED TRANSFER CHARACTERISTIC
315
DETERMINE CORRESPONDING POLES
320
SELECT FILTER ELEMENTS
325
INTERCONNECT SELECTED FILTER ELEMENTS
330
END

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US05/13490

A. CLASSIFICATION OF SUBJECT MATTER
IPC(8) - H03M 3/02
USPC - 341/143
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

USPC: 341/126, 142, 143

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
NONE

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

Delphion ; Patent Cafe collections

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 6,577,258 B2 (RUHA et al) 10 June 2003 (10.06.2003), col. 3, lines 48-60 and col. 4, lines 23-54.	1-12
A	US 5,103,228 A (VOORMAN et al) 07 April 1992 (07.04.1992), claims 1-4.	1-12
A	US 5,471,209 A (SUTTERLIN et al) 28 November 1995 (28.11.1995) see entire document.	1-12
A	US 5,124,705 A (VOORMAN) 23 June 1992 (23.06.1992), col. 2, lines 52-65 and claim 1.	1-12
A	US 2002/0180629 A1 (LIU et al) 05 December 2002 (05.12.2002), abstract.	1-12

☐ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

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Date of the actual completion of the international search	Date of mailing of the international search report
21 December 2005 (21.12.2005)	06 FEB 2006
Name and mailing address of the ISA/US Mail Stop PCT, Attn: ISA/US, Commissioner for Patents P.O. Box 1450, Alexandria, Virginia 22313-1450 Facsimile No. 571-273-3201	Authorized officer: Blaine R. Copenheaver Telephone No. 571-272-7774

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