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(71) Applicant: **ALCATEL LUCENT** [FR/FR]; 148/152 Route de la Reine, 92100 Boulogne-Billancourt (FR).

(72) Inventors: **VAN VEEN, Doutje**; 600-700 Mountain Avenue, Murray Hill, NJ 07974-0636 (US). **HOUTSMA, Vincent**; 600-700 Mountain Avenue, Murray Hill, NJ 07974-0636 (US).

(74) Agent: **WYSE, Stephen, J.**; Alcatel-Lucent USA Inc., Att: Docket Administrator-room 3B-212F, 600-700 Mountain Avenue, Murray Hill, NJ 07974-0636 (US).

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(54) Title: CLOCK AND DATA RECOVERY CIRCUIT FOR DETECTION OF MULTI-LEVEL INPUT SIGNALS

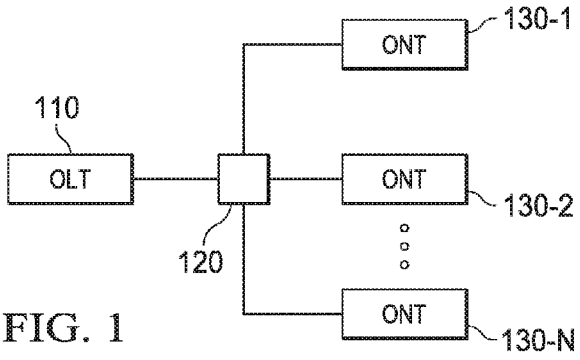

FIG. 1

(57) Abstract: A multi-level modulated signal receiver front-end, a method of receiving an optical signal and a multi-level modulated optical signal receiver front-end, In one embodiment, the receiver front-end includes: (1) a power splitter configured to split the multi-level modulated signal into a plurality of signal portions, (2) a plurality of two-level clock-and-data-recovery circuits configured to receive and recover distinct clock and data signals from corresponding ones of the plurality of signal portions and (3) logic circuitry configured to generate a recovered signal from the distinct clock and data signals.

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CLOCK AND DATA RECOVERY CIRCUIT FOR DETECTION OF MULTI-LEVEL INPUT SIGNALS

TECHNICAL FIELD

This application is directed, in general, to data communication and, more specifically, to a clock-and-data-recovery (CDR) circuit for detection of multi-level input signals, typically in the context of a network, such as a passive optical network (PON).

BACKGROUND

Electrical ("copper") computer and telecommunication networks have long existed. Optical telecommunication networks have been widely built out in recent years and are gaining in popularity. Optical fibers are capable of carrying a high volume of traffic at a reasonable cost. Although previously the "last mile" between an optical communication network and the end user was still spanned with copper wire, now fiber optic cables are often run directly up to houses, apartment complexes, and business locations. One arrangement for spanning this portion of the communication link is referred to as a PON.

Generally speaking, a PON includes an optical line termination (OLT), typically located in a central office, which communicates via a fiber-optic cable system with one or more optical network units (ONUs), with each ONU

being located on or near a customer premises. An optical network termination (ONT) is an ONU that typically serves a single user and may, for example, be located at the user's residence. A multi-dwelling unit (MDU) is an ONU that serves a multi-dwelling unit such as an apartment complex or small business. Each ONU is capable of segregating the downstream signals from the OLT and directing them to the proper user, and of transmitting upstream signals back to the OLT. In addition to forming a part of one or more PONs, the OLT is also connected to the larger telecommunication system through which the various services such as telephony, Internet access, and broadcast media are accessible so that they can be made available to the users associated with the OLT.

Standards have been promulgated for PON operations. For example, many current implementations are configured in accordance with a family of specifications including ITU-T G.984 and related standards. Such systems currently provide for transmission speeds of up to (approximately) 2.5 Gbps in the downstream direction and 1.24 Gbps upstream. The directional difference in transmission speeds is due in part to practical consideration of the cost of facilitating higher upstream transmission speeds, coupled with the fact that, as a

general rule, more content needs to be transmitted downstream than back to the OLT.

The modulation format of current deployed passive optical networks is based on a two-level, non-return-to-zero (NRZ) line code. NRZ line code is a binary code in which ones are represented by one significant condition (usually a positive voltage), and zeroes are represented by some other significant condition (usually a negative voltage), with no other neutral or rest condition. To increase the data rate, a multi-level signal, such as polybinary (*e.g.*, duobinary) or pulse-amplitude modulation (PAM), can be used. Polybinary is a form of signal modulation where proximal bits are added to result in more than two different voltage levels (*e.g.*, 1,0,-1). PAM is a form of signal modulation where the message information is encoded by using different voltage amplitudes. For instance, PAM-4 has four levels of different amplitude voltages (usually 1,1/3,-1/3,-1), so the data rate can increase by a factor of two compared to NRZ at the same baud-rate.

SUMMARY

One aspect provides a multi-level modulated signal receiver front-end. In one embodiment, the receiver front-end includes: (1) a power splitter configured to

split a multi-level modulated signal into a plurality of signal portions, (2) a plurality of two-level CDR circuits configured to receive and recover distinct clock and data signals from corresponding ones of the plurality of signal portions and (3) logic circuitry configured to generate a recovered signal from the distinct clock and data signals.

Another aspect provides a method of receiving an optical signal. In one embodiment, the method includes: (1) converting the optical signal into an electrical signal, (2) splitting the electrical signal into a plurality of electrical signal portions, (3) recovering distinct clock and data signals from each of the plurality of electrical signal portions and (4) generating a recovered electrical signal based on the distinct clock and data signals.

BRIEF DESCRIPTION OF THE DRAWINGS

Reference is now made to the following descriptions taken in conjunction with the accompanying drawings, in which:

FIG. 1 is a high-level block diagram of one embodiment of one portion of a PON;

FIG. 2A is a functional representation of one embodiment of a multi-level modulated signal receiver front-end;

FIG. 2B is a block diagram of one embodiment of a multi-level modulated signal receiver front-end;

FIG. 3A illustrates an example waveform of an NRZ signal;

FIG. 3B illustrates an example waveform of a duobinary signal;

FIG. 3C illustrates an example waveform of a PAM signal; and

FIG. 4 is a flow diagram of one embodiment of a method of receiving an optical signal.

DETAILED DESCRIPTION

As stated above, multi-level modulation can be used to increase the data rate in a PON, or any other optical or electrical network for that matter. However, because multi-level modulation employs more than two different voltages, a suitable receiver needs to be able to detect and recover clock and data signals in view of the increased number of voltage levels.

Multi-level receivers exist, but they employ single, multi-level CDR circuits. Such circuits are complex and power consumptive. Consequently, the receivers employing

them are expensive. Multi-level CDR circuits are also designed to work with a single modulation technique and are therefore inflexible.

Introduced herein is a receiver architecture in which multiple two-level CDR circuits with or without additional two-level equalization circuitry are employed in concert to detect and recover clock and data signals from multi-level signals. One embodiment employs a plurality of two-level CDR circuits having programmable voltage levels such that the same receiver can be configured for two-level modulation, such as NRZ, three-level modulation, such as duobinary, and four- or higher-level modulation, such as PAM-4.

FIG. 1 is a high-level block diagram of one embodiment of one portion of a PON. In this embodiment, the PON uses an OLT 110 to transmit a multi-level modulated optical signal via an optical transmission medium to a plurality of ONTs 130-1, 130-2, ..., 130-N which are each configured to receive a multi-level modulated optical signal. To facilitate the delivery of the multi-level modulated optical signal to more than one ONT, a passive optical splitter 120 is attached to the optical medium between the OLT 110 and the ONTs 130-1,

130-2, ..., 130-N, thereby distributing the optical signal from the transmitting OLT to each receiving ONT.

FIG. 2A is a functional representation of one embodiment of a multi-level modulated signal receiver front-end. In this embodiment, multi-level modulated signal waveform 210, such as a PAM-4-modulated waveform, is received. A power splitter (not shown) splits the received multi-level signal into n distinct clock and data signal portions 220. In this embodiment, a PAM-4 implementation yields three distinct clock and data signal portions. Logic circuitry 230 is used to process recovered data signals, after which the original multi-level modulated signal 240 can be reliably reconstructed.

FIG. 2B is a block diagram of one embodiment of a multi-level modulated signal receiver front-end. In this embodiment, the multi-level modulated signal receiver front end includes a power splitter configured to split a multi-level modulated signal into a plurality of signal portions 250, a plurality of two-level CDR circuitries 260, and logic circuitry 270, employed to recover a multi-level modulated signal reliably. In the illustrated embodiment, the cardinality, N, of CDR circuitry is dependent upon the implementation of the

multi-level modulated signal: one CDR for NRZ, two for duobinary, and three for PAM-4, etc.

Table 1, below, sets forth an example truth table for the logic circuitry 270. Only one two-level CDR is needed for NRZ; only two two-level CDRs are needed for duobinary; and only three two-level CDRs are needed for PAM-4. In the example of Table 1, the voltage threshold for CDR1 is set at .5V for NRZ, -.5V for duobinary and -.75V for PAM-4. In the example of Table 1, the voltage threshold for CDR2 is set at .5V for duobinary and 0V for PAM-4. In the example of Table 1, the voltage threshold for CDR3 is set at .75V for PAM-4.

Modulation Technique	CDR1	CDR2	CDR3	Result
NRZ	0	--	--	0
	1	--	--	1
Duobinary	0	0	--	-1
	0	1	--	0
	1	1	--	1
PAM-4	0	0	0	-1
	0	0	1	-1/3
	0	1	1	1/3
	1	1	1	1

Table 1 - Truth Table for Logic Circuitry

FIG. 3A illustrates an example waveform of an NRZ signal. NRZ is a simple encoding of a signal in binary, where ones are usually represented as positive voltage, and zeros are represented by negative voltage. There is no rest position. As illustrated by this NRZ waveform

310, the nature of the transition from positive to negative voltage, with no rest or intermediary state, creates distinct "eyes" in the waveform. The redline indicates an exemplary voltage threshold for CDR1 at .5V as described in Table 1.

FIG. 3B illustrates an example waveform of a duobinary signal. An example duobinary signal 320 will consist of three levels of different amplitude voltages (usually 1,0,-1). Compared to a representative NRZ waveform 310, the "eyes" of the duobinary signal are less defined. From Table 1, the uppermost red line in FIG. 3B, indicates an exemplary voltage threshold for CDR2 at 1/3V. The lowermost red line in FIG. 3B, likewise indicates a voltage threshold for CDR1 at -1/3V, in accordance with Table 1.

FIG. 3C illustrates an example waveform of a pulse amplitude modulated (PAM) signal. An example PAM-4 330 will consist of four levels of different amplitude voltages (usually 1,1/3,-1/3,-1). Compared to both the representative NRZ waveform 310, and the duobinary waveform 320, the "eyes" of the PAM signal are much less defined. The uppermost red line in FIG 3C corresponds to the exemplary voltage threshold for CDR3 from Table 1 at .75V. The middle red line in FIG 3C indicates a

voltage threshold for CDR2 at 0V from Table 1. Likewise, in accordance with Table 1, the lowermost red line in FIG 3C indicates a voltage threshold for CDR1 at -.75V.

FIG. 4 is a flow diagram of one embodiment of a method of receiving an optical signal. The method begins in a start step 410. In a step 420, the optical signal is converted into an electrical signal. In a step 430, the electrical signal is split into a plurality of electrical signal portions. In a step 440, distinct clock and data signals are recovered from each of the plurality of electrical signal portions. In a step 450, a recovered electrical signal is generated based on the distinct clock and data signals. The method ends in an end step 460, in which the recovered clock and data signals are employed in various communication functions that may differ depending upon the environment and desired communication.

The operation of one embodiment of the receiver described above has been verified using a 10 Gbps CDR chip (VSC8248) commercially available from Vitesse Semiconductor Corporation of Camarillo, California. The VSC8248 is a quad channel 8.5 Gbps to 11.3 Gbps NRZ CDR device with on-chip adaptive electronic dispersion compensation (EDC) and programmable input equalization

consisting of a nine-tap FFE (feed forward equalizer) and a four-tap DFE (decision feedback equalizer). The input equalization has been optimized to increase the size of ("open") the individual eyes of the PAM-4 signal and duobinary signal. After detecting the individual eyes, the resulting data signals are combined using logic gates, *e.g.*, as described above, to recover the original multi-level signal.

Those skilled in the art to which this application relates will appreciate that other and further additions, deletions, substitutions and modifications may be made to the described embodiments.

WHAT IS CLAIMED IS:

1. A multi-level modulated signal receiver front-end, comprising:

a power splitter configured to split a multi-level modulated signal received by said multi-level modulated signal receiver front-end into a plurality of signal portions;

a plurality of two-level clock-and-data-recovery circuits configured to receive and recover distinct clock and data signals from corresponding ones of said plurality of signal portions; and

logic circuitry configured to generate a recovered signal from said distinct clock and data signals.

2. The receiver front-end as recited in Claim 1 wherein each of said plurality of two-level clock-and-data-recovery circuits is configured to recover clock and data signals represented by voltage transitions across different voltage thresholds.

3. The receiver front-end as recited in Claim 2 wherein said voltage thresholds are programmable.

4. The receiver front-end as recited in Claim 1 wherein said multi-level modulated signal is a non-return-to-zero optical signal, and one of said plurality of two-level clock-and-data-recovery circuits is employed to generate said recovered signal.

5. The receiver front-end as recited in Claim 1 wherein said multi-level modulated signal is a duobinary optical signal, and two of said plurality of two-level clock-and-data-recovery circuits are employed to generate said recovered signal.

6. The receiver front-end as recited in Claim 1 wherein said multi-level modulated signal is a pulse amplitude modulated optical signal, and at least three of said plurality of two-level clock-and-data-recovery circuits are employed to generate said recovered signal.

7. The receiver front-end as recited in Claim 6 wherein said pulse amplitude modulated signal is a PAM-4 modulated optical signal.

8. The receiver front-end as recited in Claim 1 wherein said receiver is a multi-level modulated optical signal receiver.

9. The receiver front-end of Claim 8 further comprising an optical-to-electrical modulator configured to receive and convert an optical signal into an electrical signal.

10. A method of receiving an optical signal, comprising:

converting said optical signal into an electrical signal;

splitting said electrical signal into a plurality of electrical signal portions;

recovering distinct clock and data signals from each of said plurality of electrical signal portions; and

generating a recovered electrical signal based on said distinct clock and data signals.

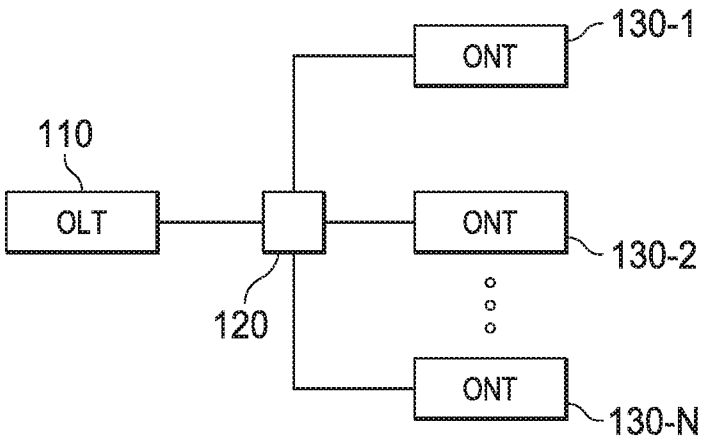

FIG. 1

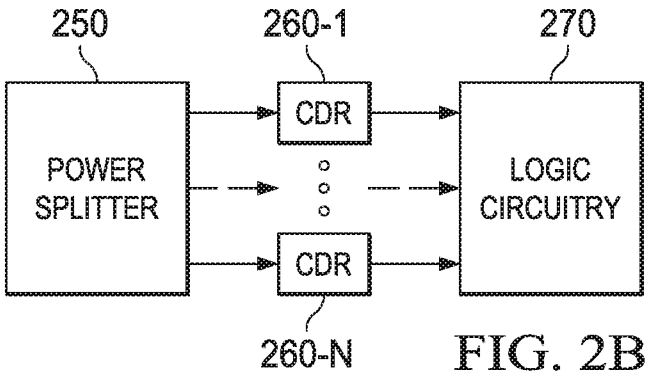

FIG. 2B

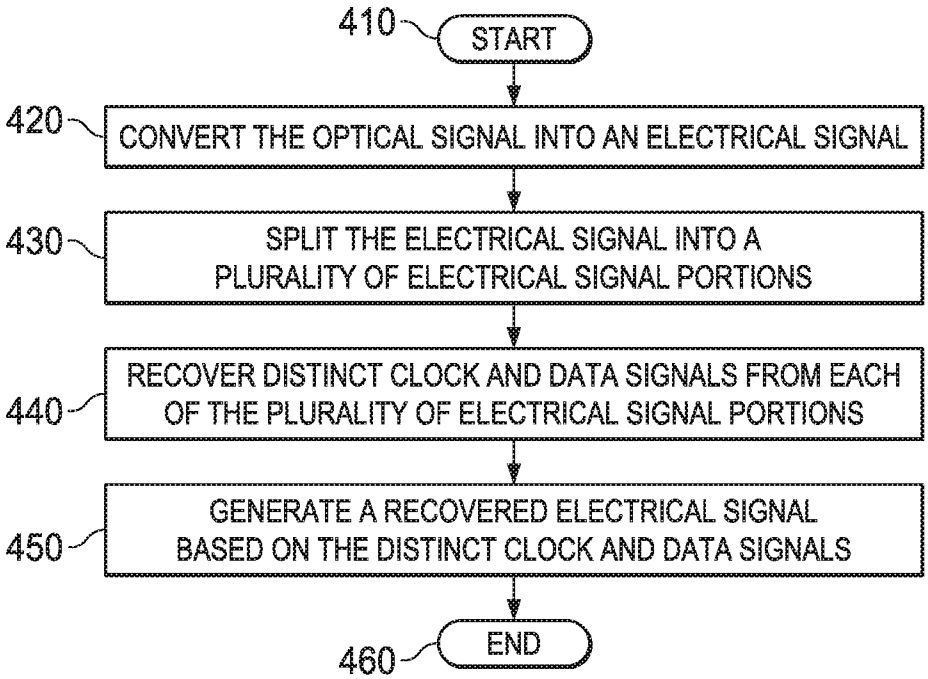

FIG. 4

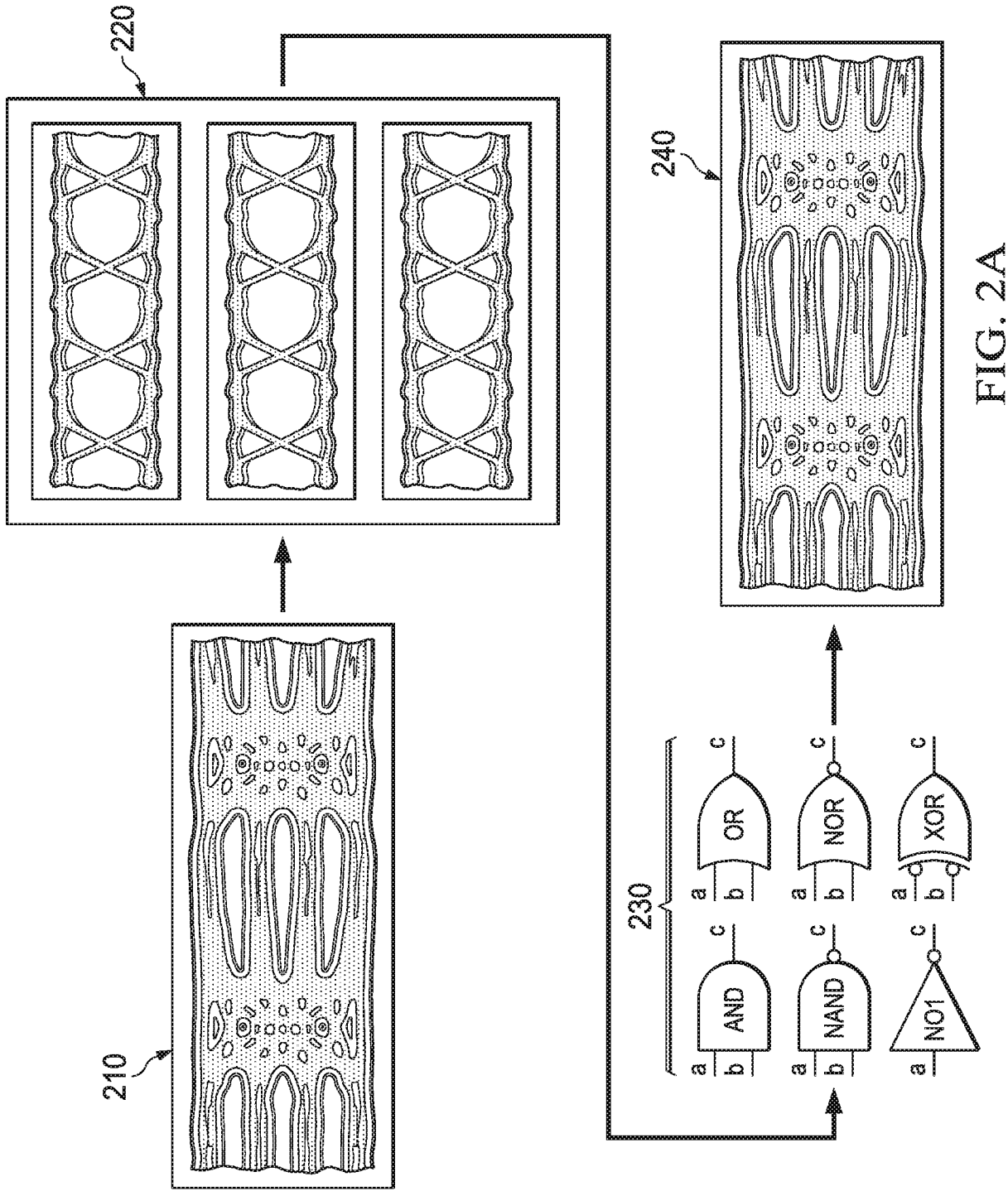

FIG. 2A

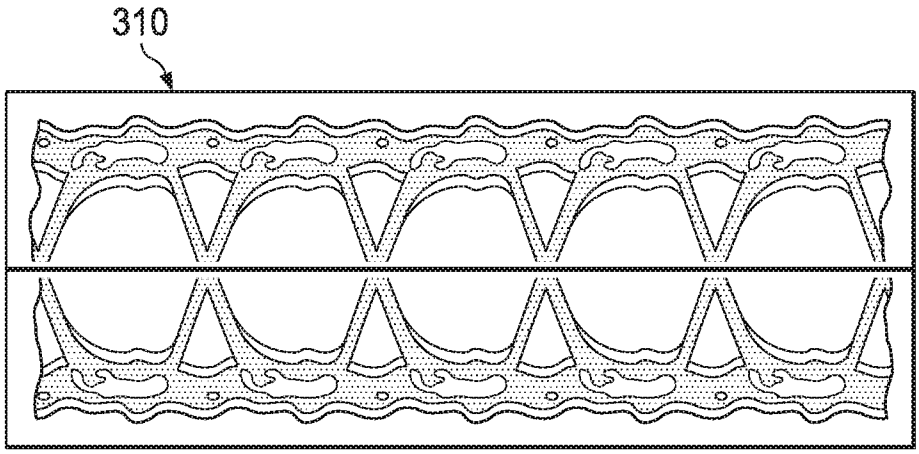

FIG. 3A

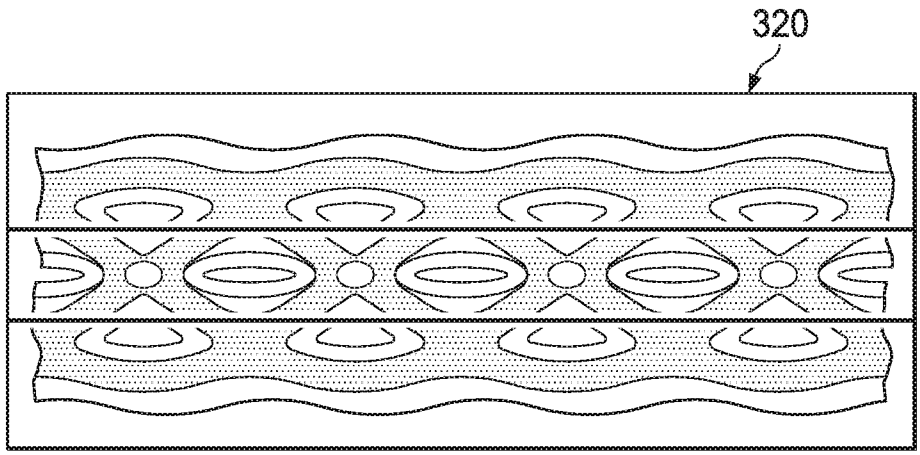

FIG. 3B

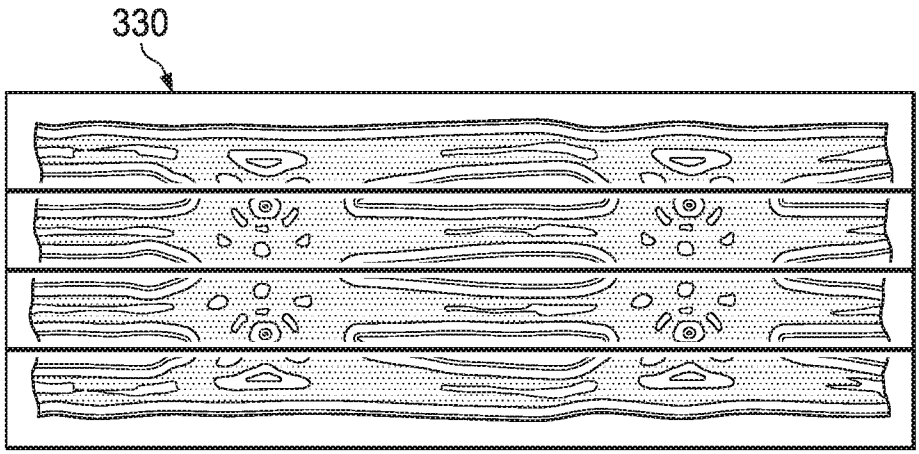

FIG. 3C

INTERNATIONAL SEARCH REPORT

International application No
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A. CLASSIFICATION OF SUBJECT MATTER
INV. H04B10/60 H04L7/00 H04L25/03
ADD.

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H04B H04L H04J

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

EPO-Internal, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

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A	US 2011/255866 A1 (VAN VEEN DOUTJE T [US] ET AL) 20 October 2011 (2011-10-20) paragraphs [0045] - [0049]; figure 5	1-10

☐ Further documents are listed in the continuation of Box C.

☒ See patent family annex.

* Special categories of cited documents :

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Date of the actual completion of the international search	Date of mailing of the international search report
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Name and mailing address of the ISA/	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Fax: (+31-70) 340-3016	De Vries, Jane

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INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No
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