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(54) METHOD AND APPARATUS FOR CIRCUIT BREAKER NODE SOFTWARE ARCHITECTURE

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Publication Classification

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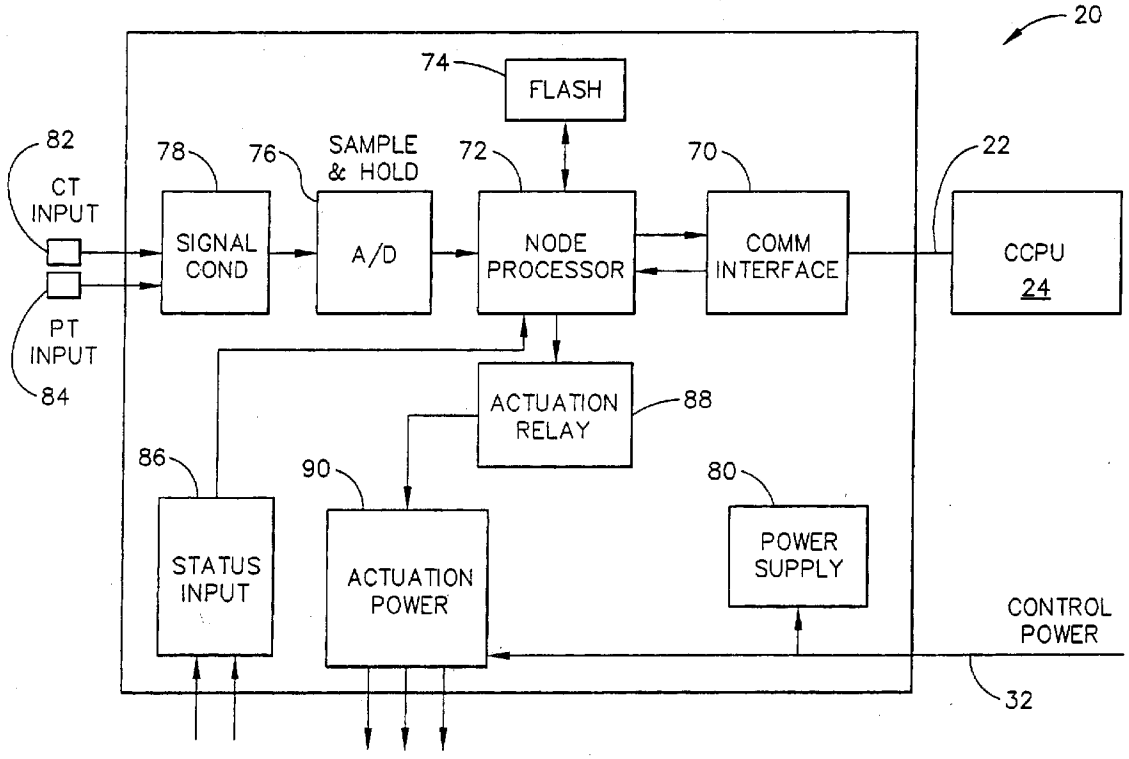
(52) **U.S. Cl.** **700/11**; 700/2

(57) ABSTRACT

A method and apparatus for operating a centrally controlled power distribution system is provided. The power distribution system includes a plurality of circuit breakers, each circuit breaker coupled to a single node electronics unit, the node electronics unit includes a plurality of processors and a memory, and the node electronics unit is communicatively coupled to at least one central control processing unit through an associated network. The method includes triggering a first node electronics unit process with a processor interrupt, and triggering a second node electronics unit process with at least one of a background polling of process execution flags and scheduled processor interrupts. The apparatus includes a software program code segment configured to trigger a first node electronics unit process with a processor interrupt, and trigger a second node electronics unit process with at least one of a background polling of process execution flags and scheduled processor interrupts.



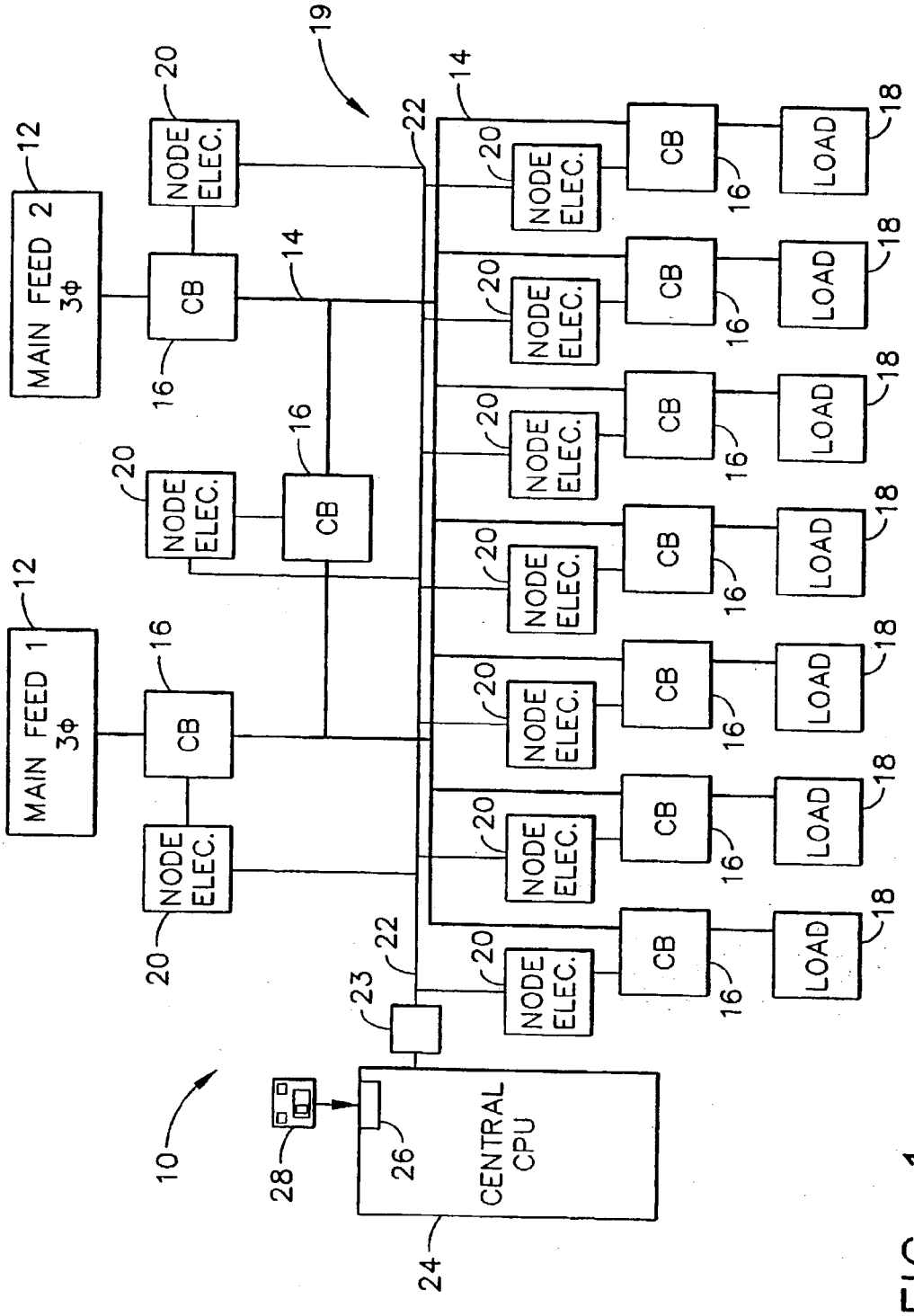

MAIN FEED 1 3φ
MAIN FEED 2 3φ
CB
NODE ELEC.
LOAD
CENTRAL CPU
10
12
14
16
18
19
20
22
23
24
26
28

FIG. 1

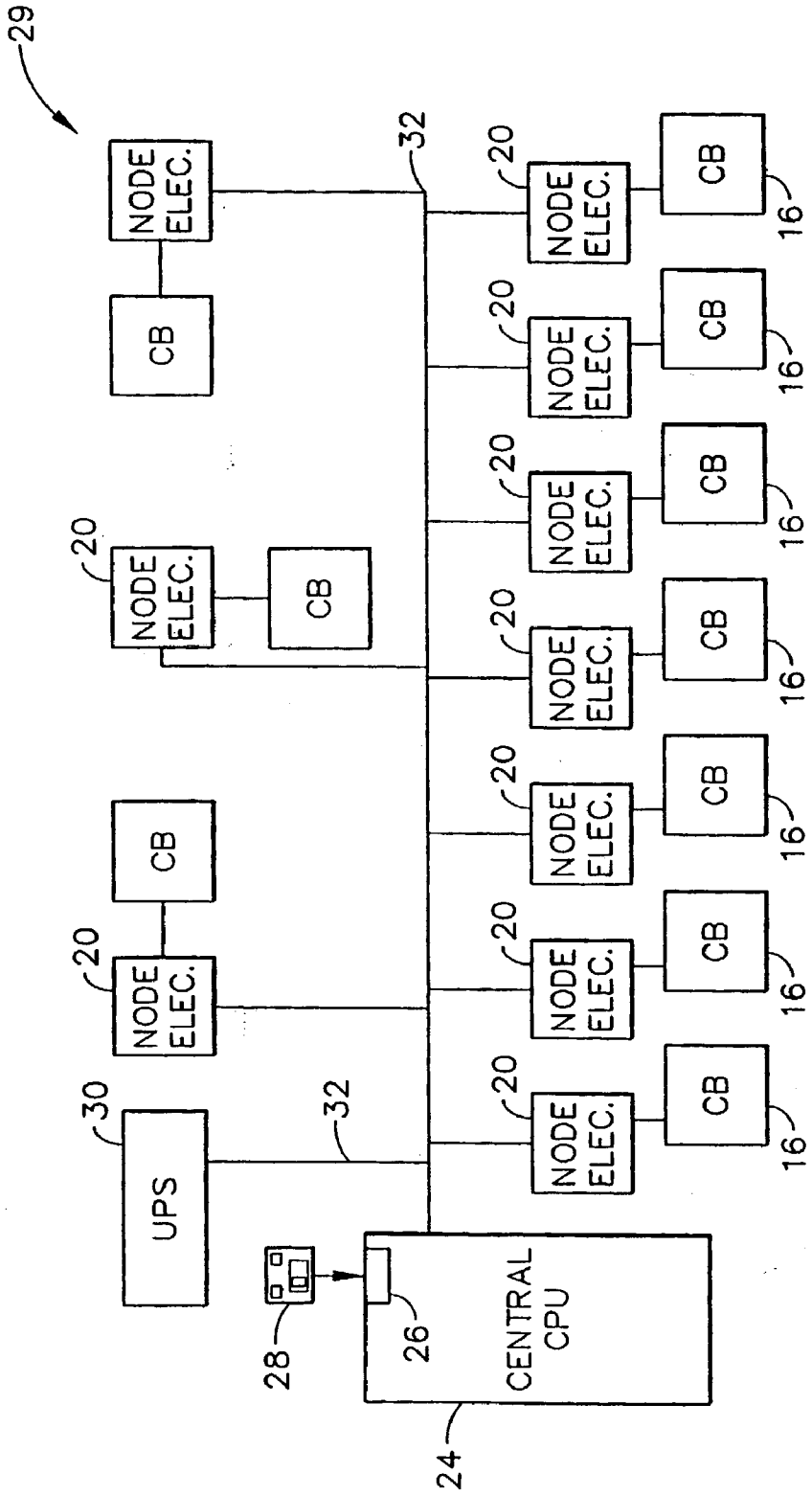


FIG. 2

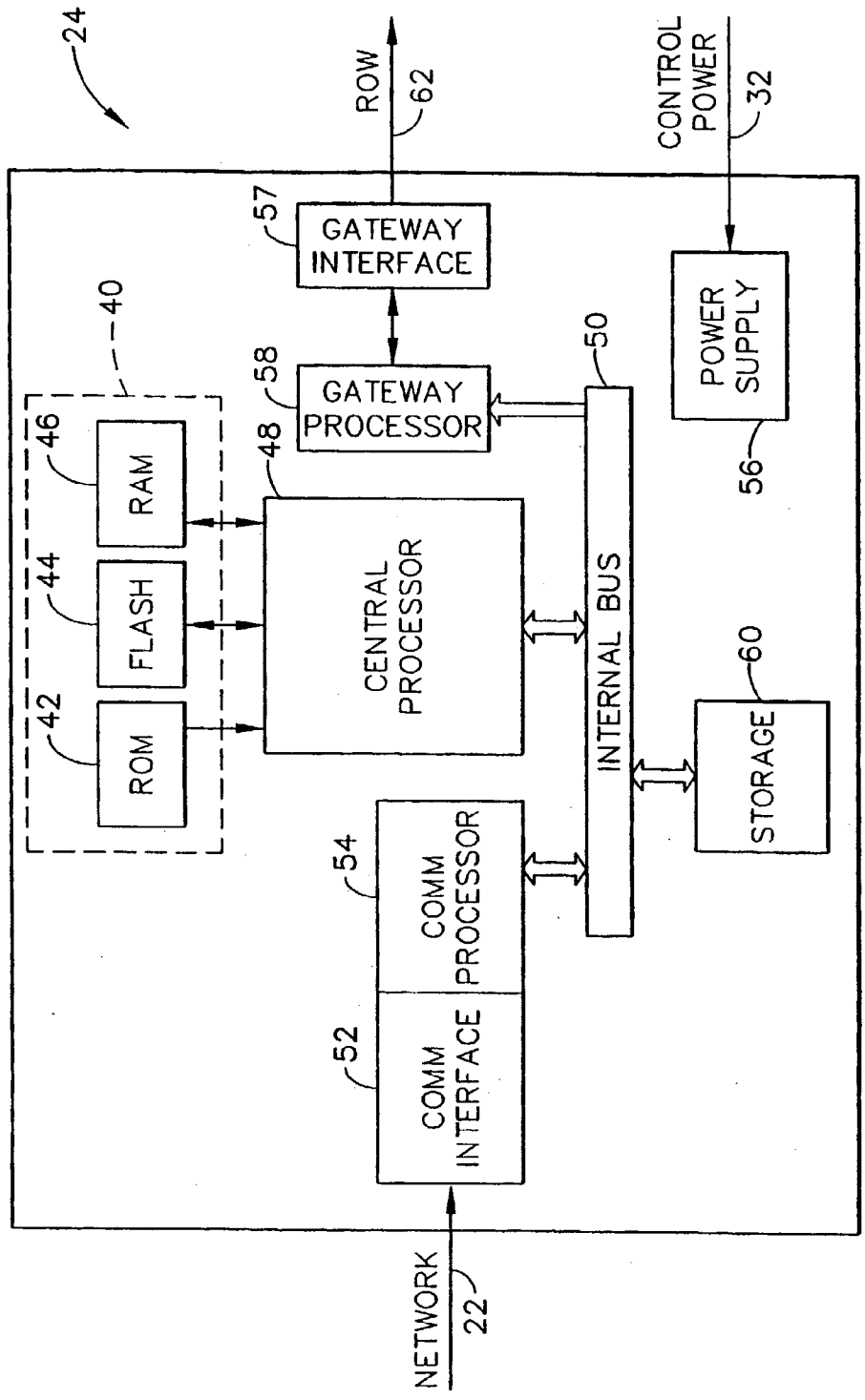

24
ROW
62
CONTROL POWER
32
57
GATEWAY INTERFACE
40
58
GATEWAY PROCESSOR
50
POWER SUPPLY
56
46
RAM
48
CENTRAL PROCESSOR
44
FLASH
INTERNAL BUS
42
ROM
60
STORAGE
54
COMM PROCESSOR
52
COMM INTERFACE
NETWORK
22

FIG. 3

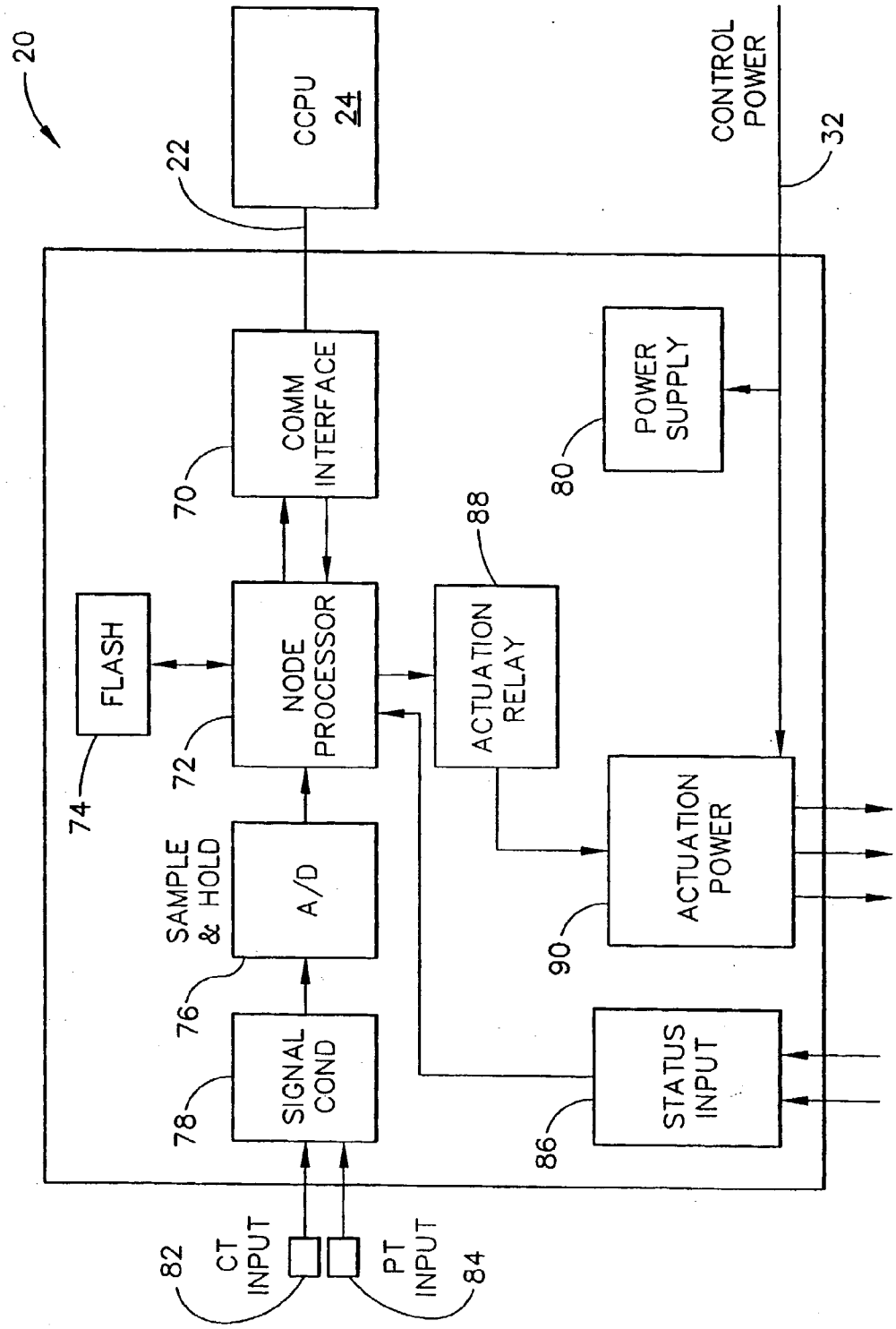

20
CCPU
24
22
CONTROL
POWER
32
COMM
INTERFACE
70
POWER
SUPPLY
80
88
FLASH
74
NODE
PROCESSOR
72
ACTUATION
RELAY
SAMPLE
& HOLD
A/D
76
ACTUATION
POWER
90
SIGNAL
COND
78
STATUS
INPUT
86
82
CT
INPUT
PT
INPUT
84

FIG. 4

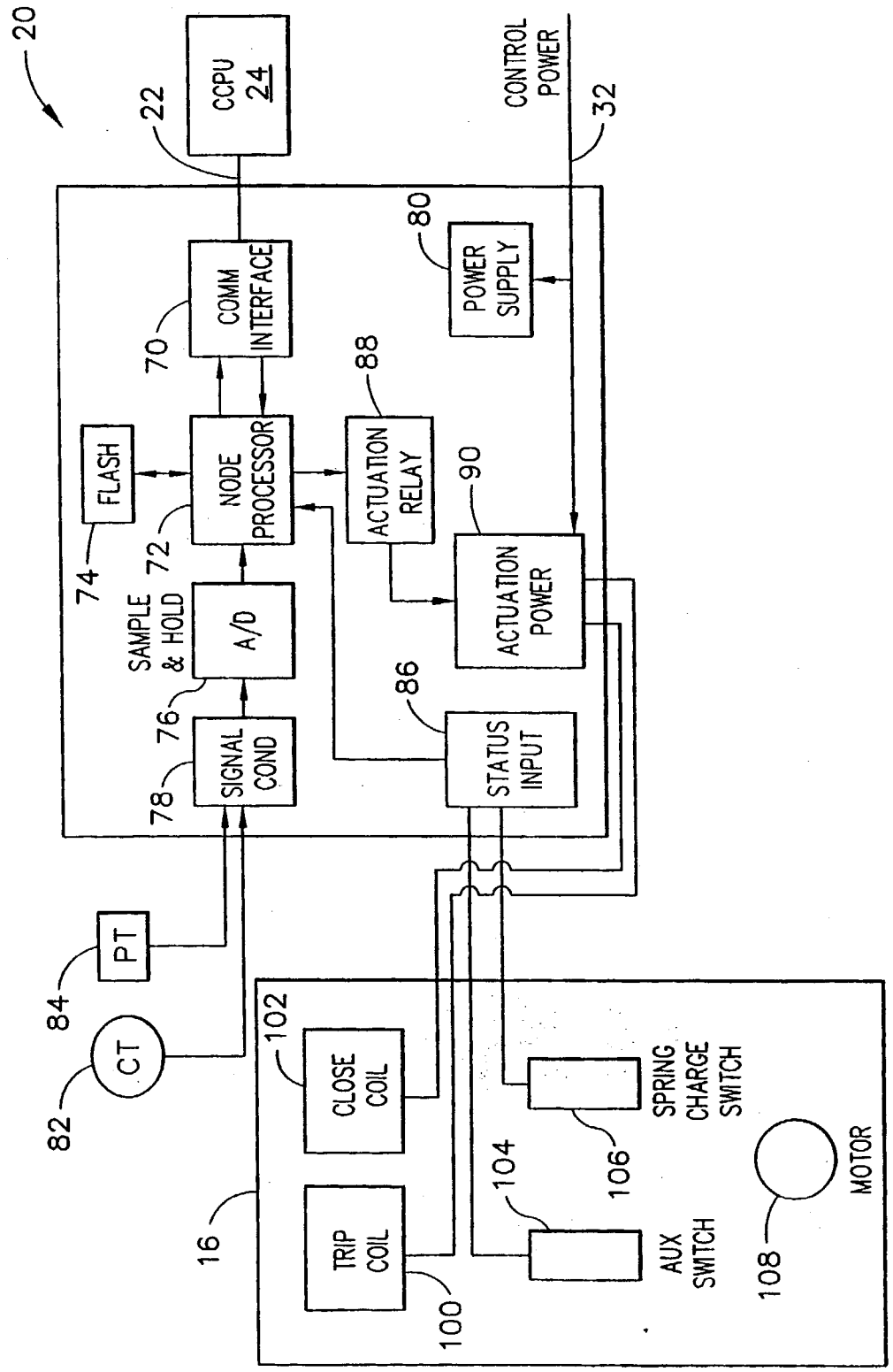

20
22
CCPU 24
CONTROL POWER
32
80
POWER SUPPLY
70
COMM INTERFACE
88
ACTUATION RELAY
90
ACTUATION POWER
FLASH
74
NODE PROCESSOR
72
SAMPLE & HOLD
A/D
76
SIGNAL COND
78
86
STATUS INPUT
PT
84
CT
82
102
CLOSE COIL
SPRING CHARGE SWITCH
106
104
AUX SWITCH
TRIP COIL
100
16
MOTOR
108

FIG. 5

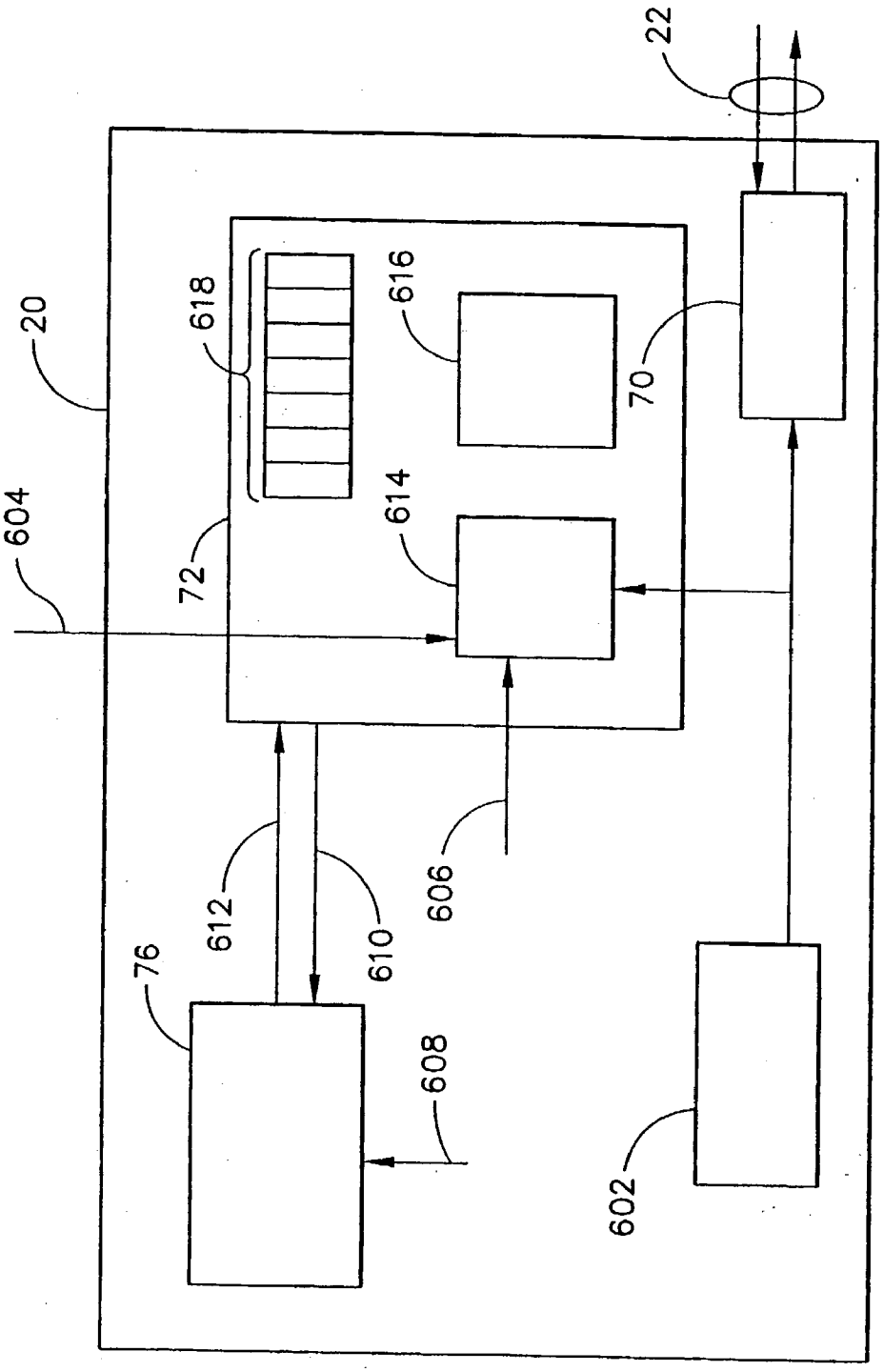


FIG. 6

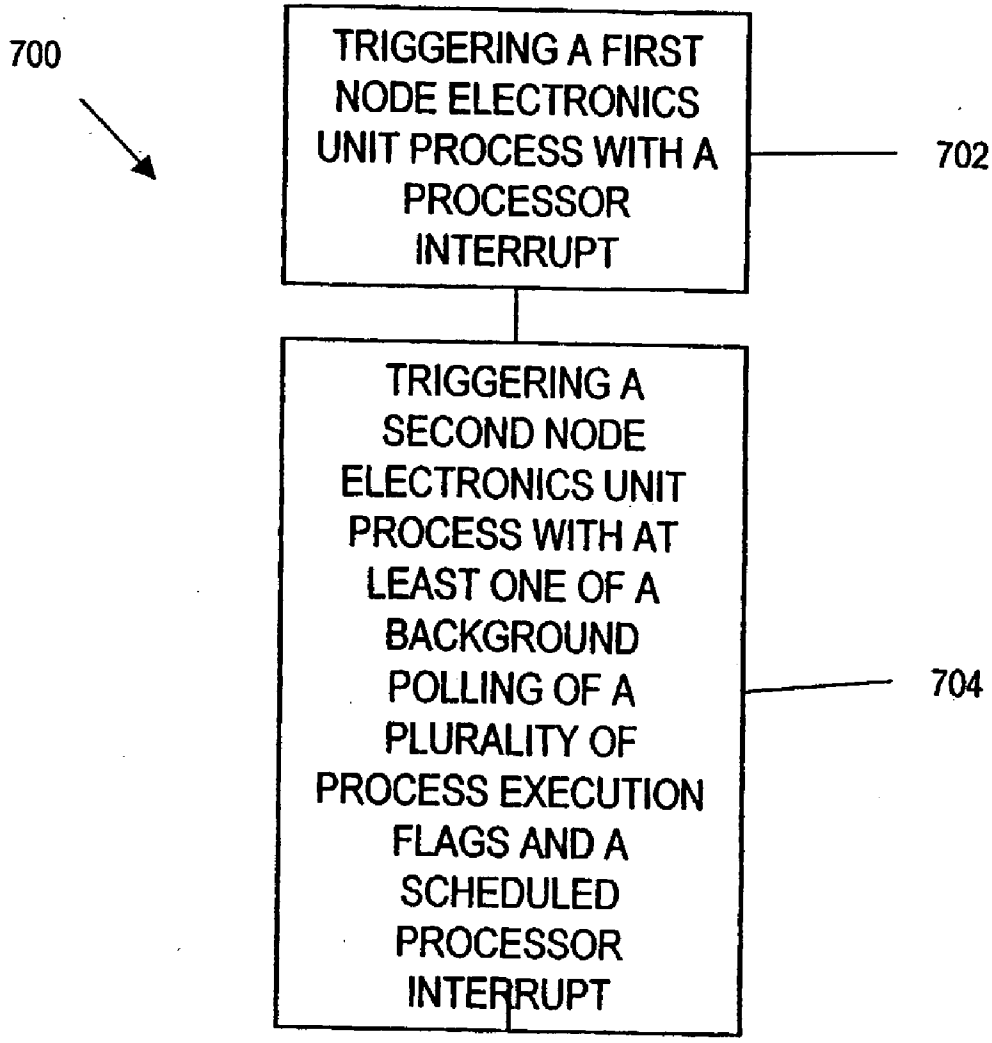

700
TRIGGERING A FIRST NODE ELECTRONICS UNIT PROCESS WITH A PROCESSOR INTERRUPT
702
TRIGGERING A SECOND NODE ELECTRONICS UNIT PROCESS WITH AT LEAST ONE OF A BACKGROUND POLLING OF A PLURALITY OF PROCESS EXECUTION FLAGS AND A SCHEDULED PROCESSOR INTERRUPT
704

FIG. 7

METHOD AND APPARATUS FOR CIRCUIT BREAKER NODE SOFTWARE ARCHITECTURE

CROSS REFERENCE TO RELATED APPLICATIONS

[0001] This application is related to U.S. Patent Application No. 60/359,544 filed on Feb. 25, 2002 for "Integrated Protection, Monitoring, and Control" the content of which is incorporated in its entirety herein by reference. This application is also related to U.S. Patent Application No. 60/438,159 filed on Jan. 6, 2003 for "Single Processor Concept for Protection and Control of Circuit Breakers in Low-Voltage Switchgear" the content of which is incorporated in its entirety herein by reference.

BACKGROUND OF THE INVENTION

[0002] This invention relates generally to electrical switchgear and more particularly, to a method and apparatus for operating a centrally controlled power distribution system circuit breaker node electronics unit.

[0003] In an industrial power distribution system, power generated by a power generation company may be supplied to an industrial or commercial facility wherein the power may be distributed throughout the industrial or commercial facility to various equipment such as, for example, motors, welding machinery, computers, heaters, lighting, and other electrical equipment. At least some known power distribution systems include switchgear which facilitates dividing the power into branch circuits which supply power to various portions of the industrial facility. Circuit breakers are provided in each branch circuit to facilitate protecting equipment within the branch circuit. Additionally, circuit breakers in each branch circuit can facilitate minimizing equipment failures since specific loads may be energized or de-energized without affecting other loads, thus creating increased efficiencies, and reduced operating and manufacturing costs. Similar switchgear may also be used within an electric utility transmission system and a plurality of distribution substations, although the switching operations used may be more complex.

[0004] Switchgear typically include multiple devices, other than the power distribution system components, to facilitate providing protection, monitoring, and control of the power distribution system components. For example, at least some known breakers include a plurality of shunt trip circuits, under-voltage relays, trip units, and a plurality of auxiliary switches that close the breaker in the event of an undesired interruption or fluctuation in the power supplied to the power distribution components. Additionally, at least one known power distribution system also includes a monitor device that monitors a performance of the power distribution system, a control device that controls an operation of the power distribution system, and a protection device that initiates a protective response when the protection device is activated.

[0005] In at least some other known power distribution systems, a monitor and control system operates independently of the protective system. For example, a protective device may de-energize a portion of the power distribution system based on its own predetermined operating limits, without the monitoring devices recording the event. The failure of the monitoring system to record the system shutdown may mislead an operator to believe that an over-current condition has not occurred within the power distribution system, and as such, a proper corrective action may not be initiated by the operator. Additionally, a protective device, i.e. a circuit breaker, may open because of an over-current condition in the power distribution system, but the control system may interpret the over-current condition as a loss of power from the power source, rather than a fault condition. As such, the control logic may undesirably attempt to connect the faulted circuit to an alternate source, thereby restoring the over-current condition. In addition to the potential increase in operational defects which may occur using such devices, the use of multiple devices and interconnecting wiring associated with the devices may cause an increase in equipment size, an increase in the complexity of wiring the devices, and/or an increase in a quantity of devices installed.

BRIEF DESCRIPTION OF THE INVENTION

[0006] In one aspect, method for operating a centrally controlled power distribution system is provided. The power distribution system includes a plurality of circuit breakers, each circuit breaker coupled to a single node electronics unit, the node electronics unit includes a plurality of processors and a memory, and the node electronics unit is communicatively coupled to at least one central control processing unit through an associated network. The method includes triggering a first node electronics unit process with a processor interrupt, and triggering a second node electronics unit process with at least one of a background polling of a plurality of process execution flags and a scheduled processor interrupt.

[0007] In another aspect, apparatus for operating a centrally controlled power distribution system is provided. The power distribution system includes a plurality of circuit breakers, each circuit breaker coupled to a single node electronics unit, said node electronics unit includes a processor and a memory, and the node electronics unit is communicatively coupled to at least one central control processing unit through an associated network. The apparatus includes a software program code segment configured to trigger a first node electronics unit process with a processor interrupt, trigger a second node electronics unit process with at least one of a background polling of a plurality of process execution flags and a scheduled processor interrupt.

BRIEF DESCRIPTION OF THE DRAWINGS

[0008] **FIG. 1** is an exemplary schematic illustration of a power distribution system;

[0009] **FIG. 2** is an exemplary schematic illustration of a node power system;

[0010] **FIG. 3** is an exemplary schematic illustration of a central control processing unit that may used with the power distribution system shown in **FIG. 1**;

[0011] **FIG. 4** is an exemplary schematic illustration of a node electronic unit that may used with the power distribution system shown in **FIG. 1**;

[0012] **FIG. 5** is an exemplary schematic illustration of a circuit breaker that may used with the power distribution system shown in **FIG. 1**; and

[0013] **FIG. 6** is an expanded schematic block diagram of an exemplary node electronics unit shown in **FIG. 4**.

[0014] **FIG. 7** is a flow chart illustrating an exemplary method for operating the node electronics unit shown in **FIG. 6**.

DETAILED DESCRIPTION OF THE INVENTION

[0015] **FIG. 1** illustrates an exemplary schematic illustration of a power distribution system **10**, used by an industrial facility for example. In an exemplary embodiment, system **10** includes at least one main feed system **12**, a power distribution bus **14**, a plurality of power circuit switches or interrupters, also referred to herein as a circuit breakers (CB) **16**, and at least one load **18**, such as, but not limited to, motors, welding machinery, computers, heaters, lighting, and/or other electrical equipment.

[0016] In use, power is supplied to a main feed system **12**, i.e. a switchboard for example, from a source (not shown) such as, an electric generator driven by a prime mover locally, or an electric utility source from an electrical substation. The prime mover may be powered from, for example, but not limited to, a turbine, or an internal combustion engine. Power supplied to main feed system **12** is divided into a plurality of branch circuits by a plurality of busbars configured to route the power from a branch feed breaker and a bus-tie breaker to a plurality of load circuit breakers **16** which supply power to various loads **18** in the industrial facility. In addition, circuit breakers **16** are provided in each branch circuit to facilitate protecting equipment, i.e. loads **18**, connected within the respective branch circuit. Additionally, circuit breakers **16** facilitate minimizing equipment failures since specific loads **18** may be energized or de-energized without affecting other loads **18**, thus creating increased efficiencies, and reduced operating and manufacturing costs.

[0017] Power distribution system **10** includes a circuit breaker control protection system **19** that includes a plurality of node electronics units **20** that are each communicatively coupled to a digital network **22** via a network interface controller switch **23** such as, but not limited to, an Ethernet switch **23**. Circuit breaker control protection system **19** also includes at least one central control processing unit (CCPU) **24** that is communicatively coupled to digital network **22**. In use, each respective node electronic unit **20** is electrically coupled to a respective circuit breaker **16**, such that CCPU **24** is communicatively coupled to each circuit breaker **16** through digital network **22** and through an associated node electronic unit **20**.

[0018] In one embodiment, digital network **22** includes, for example, at least one of a local area network (LAN) or a wide area network (WAN), dial-in-connections, cable modems, and special high-speed ISDN lines. Digital network **22** also includes any device capable of interconnecting to the Internet including a web-based phone, personal digital assistant (PDA), or other web-based connectable equipment.

[0019] In one embodiment, CCPU **24** is a computer and includes a device **26**, for example, a floppy disk drive or CD-ROM drive, to facilitate reading instructions and/or data from a computer-readable medium **28**, such as a floppy disk or CD-ROM. In another embodiment, CCPU **24** executes instructions stored in firmware (not shown). CCPU **24** is programmed to perform functions described herein, but other programmable circuits can likewise be programmed. Accordingly, as used herein, the term computer is not limited to just those integrated circuits referred to in the art as computers, but broadly refers to computers, processors, microcontrollers, microcomputers, programmable logic controllers, application specific integrated circuits, and other programmable circuits. Additionally, although described in a power distribution setting, it is contemplated that the benefits of the invention accrue to all electrical distribution systems including industrial systems such as, for example, but not limited to, an electrical distribution system installed in an office building.

[0020] **FIG. 2** is an exemplary schematic illustration of a node power distribution system **29** that can be used with power distribution system **10** (shown in **FIG. 1**) and more specifically, with circuit breaker control protection system **19** (shown in **FIG. 1**). Node power distribution system **29** includes a power source **30** that is electrically coupled to node electronic units **20** through a node power distribution bus **32**. In an exemplary embodiment, power source **30** is an uninterruptible power supply (UPS). In one embodiment, power source **30** receives power from power system **10** and then distributes this power to node electronic units **20** through node power distribution bus **32**. In an alternative embodiment, power is not supplied to power source **30**, but rather, power source **30** supplies power to node electronic units **20** using an internal power supply, such as, but not limited to, a plurality of batteries (not shown). In another alternate embodiment, node electronic units **20** are powered by secondary current available from current sensor **82** and/or voltage sensor **84**. In this embodiment, circuit breaker control protection system **19** would not include node power distribution system **29**, power source **30**, or node power distribution bus **32**.

[0021] **FIG. 3** is an exemplary schematic illustration of CCPU **24**. CCPU **24** includes at least one memory device **40**, such as, but not limited to, a read only memory (ROM) **42**, a flash memory **44**, and/or a random access memory (RAM) **46**. CCPU **24** also includes a central processor unit (CPU) **48** that is electrically coupled to at least one memory device **40**, as well as an internal bus **50**, a communications interface **52**, and a communications processor **54**. In an exemplary embodiment, CCPU **24** is a printed circuit board and includes a power supply **56** to supply power to a plurality of devices on the printed circuit board.

[0022] Additionally, in an exemplary embodiment, internal bus **50** includes an address bus, a data bus, and a control bus. In use, the address bus is configured to enable CPU **48** to address a plurality of internal memory locations or an input/output port, such as, but not limited to communications interface **52** through communications processor **54**, and a gateway interface **57**, through a gateway processor **58**. The data bus is configured to transmit instructions and/or data between CPU **48** and at least one input/output, and the control bus is configured to transmit signals between the plurality of devices to facilitate ensuring that the devices are operating in synchronization. In the exemplary embodiment, internal bus **50** is a bidirectional bus such that signals can be transmitted in either direction on internal bus **50**. CCPU **24**

also includes at least one storage device **60** configured to store a plurality of information transmitted via internal bus **50**.

[**0023**] In use, gateway interface **57** communicates to a remote workstation (not shown) via an Internet link **62** or an Intranet **62**. In the exemplary embodiment, the remote workstation is a personal computer including a web browser. Although a single workstation is described, such functions as described herein can be performed at one of many personal computers coupled to gateway interface **57**. For example, gateway interface **57** may be communicatively coupled to various individuals, including local operators and to third parties, e.g., remote system operators via an ISP Internet connection. The communication in the example embodiment is illustrated as being performed via the Internet, however, any other wide area network (WAN) type communication can be utilized in other embodiments, i.e., the systems and processes are not limited to being practiced via the Internet. In one embodiment, information is received at gateway interface **57** and transmitted to node electronic unit **20** via CCPU **24** and digital network **22**. In another embodiment, information sent from node electronic unit **20** is received at communication interface **52** and transmitted to Internet **62** via gateway interface **57**.

[**0024**] **FIG. 4** is an exemplary schematic block diagram of single node electronics unit **20**. In the exemplary embodiment, node electronics unit **20** is a unitary device mounted remotely from CCPU **24** and breaker **16**. For example, node electronics unit **20** can be separate from, but proximate to circuit breaker **16**. Node electronics unit **20** includes a communications interface **70** that is coupled to digital network **22**. In the exemplary embodiment, communication interface **70** communicates over network **22** using Fast Ethernet protocol at about 100 Mbps. In another embodiment, node electronics unit **20** includes a plurality of communication interfaces **70** that couple to an equal number of independent networks **22** which, in turn, each couple to independent CCPUs **24**. Such an architecture provides a redundancy that facilitates operation of power distribution system **10**. A number of independent, redundant communications interfaces **70**, networks **22** and CCPUs **24** is determined by a predetermined redundancy requirement of a user. Each communication interface **70** couples electrically to a node processor **72** to transmit data received from a respective CCPU **24** to node processor **72** and to transmit data received from node processor **72** to respective CCPU **24**. In an alternative embodiment, node electronics units **20** include a plurality of node processors **72**. At least one of the plurality of node processors **72** may comprise a self-powered processor. A self-powered processor receives power from a self-power supply circuit **73**. In an embodiment wherein a self-powered processor is used, the self-powered processor is configured to conserve electrical energy when power supply **80** is unable to supply the electrical requirements of the node electronics units **20**. It should be appreciated that, in one embodiment, the self-powered processor conserves energy by being configured to execute only predetermined processes such that the self powered-processor conserves energy. In such a case, self-powered processor is configured for fast wakeup, i.e. an abbreviated initialization process when first powered. It should be further appreciated that, in another embodiment, the fast wakeup configuration allows the self-powered processor to conserve energy by executing only predetermined processes. Self-powered processor is additionally configured to modify its clock speed and processing to coordinate its power usage with power available through self-power supply circuit and power supply **80**. Node processor **72** includes a memory, a communication processor and a command interpreter within. The clocks of each node processor **72** in the plurality of node electronics units **20** in power distribution system **10** are synchronized by a synchronization pulse received from at least one CCPU **24**. Node electronics units **20** determines which synchronization signal received synchronizes the node processors **72**.

[**0025**] Node processor **72** is electrically coupled to a memory device **74**, such as, but not limited to a flash memory device, an analog digital (A/D) converter **76**, and a signal conditioner **78**. Node processor **72** is communicatively coupled to communications interface **70**. Memory device **74** is also communicatively coupled to node processor **72** for exchanging data, and program instructions. In one embodiment, memory device **74** is a single device including a program area and a data area. In an alternative embodiment, memory **74** is a plurality of devices, each including an area for a program, data and configuration constant information. In an embodiment wherein a plurality of node processors **72** are used, memory **74** includes a separate device dedicated to each node processor **72** and a shared memory area accessible and modifiable by each node processor **72**. Node processor **72** is electrically coupled to A/D converter **76** to receive digital signals representing analog signals received from signal conditioner **78**. Analog signals from sensors located remotely from circuit breaker **16** and node electronics unit **20** monitor electrical parameters associated with respective circuit breaker **16**. The analog signals are received by signal conditioner **78** from CT input **82** and PT input **84**. CT input **82** is electrically coupled to an input CT and a burden resistor (not shown). Input current flowing through the burden resistor induces a voltage drop across the burden resistor that is proportional to the input current. The induced voltage is sensed at signal conditioner **78** input. Signal conditioner **78** includes a filtering circuit to improve a signal to noise ratio of the incoming signal, a gain circuit to amplify the incoming signal, a level adjustment circuit to shift the incoming signal to a pre-determined range, and an impedance match circuit to facilitate a signal transfer to A/D converter **76**. In the exemplary embodiment, A/D converter **76** is a sample and hold type of A/D converter. The sample and hold feature facilitates synchronization of electrical parameter measurements in node electronics units **20**. A/D converter **76** samples signal conditioner **78** output when commanded by node processor **72**, which issues synchronization commands as directed by CCPU **24**. In an exemplary embodiment, node electronics unit **20** is a printed circuit board and includes a power supply **80** to power a plurality of devices on the printed circuit board.

[**0026**] In one embodiment, node electronics unit **20** receives signals input from a plurality of devices, such as, but not limited to, a current transformer **82**, and a potential transformer **84**, and/or a circuit breaker **16**. A plurality of inputs from the circuit breaker **16** are provided as status input **86**, and these inputs may include inputs, such as, but not limited to, an auxiliary switch status, and a spring charge switch status. In one embodiment, current transformer **82** includes a plurality of current transformers, each monitoring a different phase of a three phase power system, and at least one current transformer monitoring a neutral phase of the three phase power system. In another embodiment, potential

transformer **84** includes a plurality of potential transformers, each monitoring a different phase of a three-phase power system. An actuation relay module **88** is communicatively coupled to node processor **72** and module **88** is also coupled to an actuation power module **90**. Status input module and actuation power module **90** are electrically coupled to circuit breaker **16** through a standard wiring harness.

[**0027**] In one embodiment, node electronics unit **20** includes a second node processor **72** that executes a program code segment that determines local control and protection actions to be used to determine breaker commands when communications between node electronics unit **20** and CCPU **24** is lost. The second node processor is powered from an electrical source onboard the node electronics unit separate and independent from the control system power supply that supplies the other components of node electronics unit **20**. In this embodiment, first node processor **72** is configured to execute a program code segment that controls all other functions of nod electronics unit **20**, including, but, not limited to, communications functions performed by communications interface **70**, input functions performed by signal conditioner **78**, A/D **76**, and status input **86**, and output functions performed by actuation relay **88** and actuation power module **90**. Second node processor **72** includes a memory separate and independent from memory unit **74**.

[**0028**] In use, the status inputs **86** and signals received from current transformer **82**, and potential transformer **84**, are conditioned by signal conditioner **78** and transmitted to A/D converter **76**, where the analog signals are converted to digital signals for input to node processor **72**. Node processor **72** executes software that is resident on memory **74**. The software instructs node processor **72** to receive digital signals from A/D converter **76** and logical status signals from circuit breaker **16** through status input **86**. Node processor **72** compares the input signals to parameters determined by software executing on node processor **72** and parameters in control and protective actions received from CCPU **24** through network **22** and communications interface **70**. Node processor **72** determines local control and protective actions based on the input signals and the control and protective actions received from CCPU **24**. If node processor **72** and CCPU are communicating properly, a local block signal received from CCPU **24** inhibits node processor **72** from using the local control and protective actions from determining a set of breaker control actions. The breaker control actions are a set of signals that command circuit breaker **16** to operate in a predetermined manner. The presence of the local block signal indicates the communication state between node processor **72** and CCPU **24**. If the local block signal is present in signals received from CCPU **24**, Node processor uses CCPU **24** control and protective actions to determine breaker control actions. If the local block signal is not present, node processor **72** uses local control and protective actions to determine breaker control actions. Node processor **72** transmits breaker control action through actuation relay module **88**, actuation power module **90**, and the standard wiring harness.

[**0029**] Data received from A/D converter **78** and status input **86** by node processor **72** are transmitted to CCPU **24** via node electronics unit **20**, and digital network **22**. The data sent is to CCPU **24** is pre-processed data from node processor **72**, in that, the data sent to CCPU **24** is sent in its raw form, before processing by node processor **72** takes place. The data transmitted to CCPU **24** via node electronics unit **20** is processed by CCPU **24**, which transmits a signal to node electronics unit **20** via digital network **22**. In the exemplary embodiment, node electronics unit **20** actuates circuit breaker **16** in response to the signal received from CCPU **24**. In one embodiment, circuit breaker **16** is actuated in response to commands sent only by CCPU **24**, i.e., circuit breaker **16** is not controlled locally, but rather is operated remotely from CCPU **24** based on inputs received from current transformer **82**, potential transformer **84**, and status inputs **86** received from node electronics unit **20** over network **22**.

[**0030**] **FIG. 5** is an exemplary schematic illustration of circuit breaker **16** that is electrically coupled to node electronics unit **20**. In the exemplary embodiment, circuit breaker **16** includes a switch assembly that includes movable and/or stationary contacts, an arc suppression means, and a tripping and operating mechanism. Circuit breaker **16** auxiliaries include only a trip coil **100**, a close coil **102**, an auxiliary switch **104**, a spring charge switch **106**, and a motor **108**. Circuit breaker **16** does not include a trip unit. Auxiliary switches and sensors are coupled to node electronics unit **20** through a standard wiring harness **110**, which may include both copper wiring and communications conduits. Current sensor **82**, and voltage sensor **84** are coupled to node electronics unit **20** through a cable **112** that may include copper wiring and/or communications conduits. Circuit breaker **16** is a unitary device mounted proximate to CCPU **20**, current sensor **82**, and voltage sensor **84**.

[**0031**] In use, actuation signals from node electronics unit **20** are transmitted to circuit breaker **16** to actuate a plurality of functions in circuit breaker **16**, such as, but not limited to, operating a trip coil **100**, operating a close coil **102**, and affecting a circuit breaker lockout feature. An auxiliary switch **104** and spring charge switch **106** provide a status indication of circuit breaker parameters to node electronics unit **20**. Motor **108** is configured to recharge a close spring (not shown) after circuit breaker **16** closes. To close circuit breaker **16**, a close coil **102** is energized by a close signal from actuation power module **90**. Close coil **102** actuates a closing mechanism (not shown) that couples at least one movable electrical contact (not shown) to a corresponding fixed electrical contact (not shown). The closing mechanism of circuit breaker **16** latches in a closed position such that when close coil **102** is de-energized, circuit breaker **16** remains closed. When breaker **16** closes, an "a" contact of auxiliary switch **104** also closes and a "b" contact of auxiliary switch **104** opens. The position of the "a" and "b" contacts is sensed by node electronics unit **20**. To open circuit breaker **16**, node electronics unit **20** energizes trip coil (TC) **100**. TC **100** acts directly on circuit breaker **16** to release the latching mechanism that holds circuit breaker **16** closed. When the latching mechanism is released, circuit breaker **16** will open, opening the "a" contact and closing the "b" contact of auxiliary switch **104**. Trip coil **100** is then de-energized by node electronics unit **20**. After breaker **16** opens, with the close spring recharged by motor **108**, circuit breaker **16** is prepared for a next operating cycle. In the exemplary embodiment, each node electronics unit **20** is coupled to circuit breaker **16** in a one-to-one correspondence. For example, each node electronics unit **20** communicates directly with only one circuit breaker **16**. In an alternative embodiment, node electronics unit **20** may communicate with a plurality of circuit breakers **16**.

[0032] **FIG. 6** is an expanded schematic block diagram of an exemplary node electronics unit **20** shown in **FIG. 4**. Node electronics unit **20** functions to perform at least the following functions, sample a current flow through circuit breaker **16** and/or a voltage across circuit breaker **16** and synchronized to within about 10 microseconds of the sampling of all other node electronics units **20**, transmit current and/or voltage measurements and node electronics unit **20** and/or circuit breaker **16** state to central control processing unit (CCPU) **24** through network **22**, and receive and decode commands issued by CCPU **24** communicatively coupled through network **22**. These functions need to occur with sufficient temporal speed such that all power distribution system **10** control latency requirements are met. For example, in an instantaneous overcurrent (IOC) event at one of circuit breaker **16**, a TRIP command should be issued for the affected circuit breaker and executed by the associated node electronics unit **20** within **2.6** milliseconds of the onset of IOC.

[0033] Components of node electronics unit **20** that are identical to node electronics unit **20** components shown n **FIG. 4** are shown in **FIG. 6** using the same reference numerals used in **FIG. 4**. Accordingly, node electronics unit **20** includes node processor **72**, sample and hold A/D converter **76**, communication interface **70**, and network **22**. Additionally, node electronics unit **20** includes an execution timer **602**, external interrupt channel **604** and internal interrupt channel **606**. Sample and hold A/D converter **76** includes a data input from signal conditioner **78** (not shown) via an input channel **608**. Sample and hold A/D converter **76** also includes communications paths **610** and **612** to node processor **72** for transmitting a sample command **610** and transmitting digital sampled data **612**

[0034] Node processor **72** includes an interrupt handler **614** which receives interrupt requests from external components via channel **604**, internal components via channel **606**, execution timer **602**, and communications interface **70**. Interrupt handler **614** also services interrupt requests generated onboard processor **72**. Node processor **72** includes a polling subroutine **616** operating in a background environment. Polling subroutine **616** executes when interrupt handler **614** is not servicing interrupts, thus utilizing node processor **72** resources only when the resources are not needed to service higher priority requests. Polling subroutine **616** polls a plurality of process execution flags **618** that are set by other processes executing in processor **72**. A high priority interrupt may start a process that needs lower priority processes to execute, and may set a process execution flag to request service for the process. Likewise, lower priority processes may spawn other processes by setting an execution flag for that process. Processor **72** is programmed to include functions such as an integrator, a differentiator, an amplifier, a comparator, a voltage reference and a current reference for processor operation during periods of power interruption or poor power quality supplied to node electronics unit **20**, when processor **72** may be operating from a self-powered function processing analog input signals.

[0035] In operation, node electronics unit **20** utilizes a software architecture that enables real-time, synchronized monitoring and control of node electronics unit **20** and circuit breaker **16**. In this software architecture, node processes are triggered by external or internal interrupts, or through background polling of process execution flags. High priority process components, for example components that need immediate processing for the system to achieve latency goals, are executed within interrupt handler **614**. If follow-on low priority processes are to occur, a flag **618** is set for the follow-on process. When interrupt handler **616** is not executing, a low priority polling loop is running, checking the status of process flags **618**. If a process's flag is set, its process flag is cleared and the process is executed. As described above, this process may enable the execution of further follow-on processes by setting their process flags.

[0036] In the exemplary embodiment, high priority processes for execution may include recording the local time of an arriving packet, which is triggered by an interrupt from communications interface **70**, initiation of data sampling by sample and hold A/D converter **76**, execution timer reset, which is triggered by a timer expiration interrupt, and enabling data sample collection, which is triggered by a data ready interrupt from A/D converter **76**. Follow-on processes that may be initiated by the high-priority processes may include low priority execution of command message decoding and execution, synchronization processes as needed, for example, when a particular command message is received, low priority evaluation of communication channel health, reading of a set of data samples from the A/D converter, and loading the set of data samples into a data packet. The data packet is transmitted to CCPU **24** when all of the data sample fields of the data packet's have been filled with new data (since the previous packet transmission).

[0037] The software architecture of node electronics unit **20** enables real-time, synchronized monitoring and control of node electronics unit **20**, such as synchronized sampling and transmission of circuit breaker **16** currents and voltages to CCPU **24**, and real-time reception and execution of commands issued by CCPU **24**. The software architecture also provides for division of processes into high priority (i.e. immediate—interrupt driven) and low priority categories, execution of high priority tasks that are important for real-time, synchronized node operation, and use of flags and polling to enable execution of lower priority tasks. High priority tasks, which are triggered by interrupts may include recording the local time of an arriving message packet, initiating A/D converter **76** data acquisition, resetting timer **602**, and enabling data sample collection. Lower priority tasks, which are triggered through the polling of flags set by other processes may include decoding of received, messages and execution of received message commands, evaluation of communication channel health, reading of data samples from A/D converter **76**, and transmission of node electronics unit information to CCPU **24**.

[0038] **FIG. 7** is a flow chart illustrating an exemplary method **700** for operating the node electronics unit shown in **FIG. 6**. In the exemplary embodiment, the node electronics unit is a component of a centrally controlled power distribution system wherein the power distribution system includes a plurality of circuit breakers that are each coupled to a single node electronics unit. Each node electronics unit includes a plurality of processors and a memory, and is communicatively coupled to at least one CCPU through an associated network. Method **700** includes triggering **702** a first node electronics unit process with a processor interrupt. High priority processes may originate internal to the processor and/or external to the processor. An interrupt handler, executing on each processor services each received inter-

rupt. An interrupt may trigger a high priority process such as recording a local time of an arriving message packet, initiation of an A/D converter data sampling and a timer reset, and enabling data sample collection. An interrupt that triggers **702** recording the local time of an arriving message packet is an example of an interrupt from an interrupt source external to processor. Such an interrupt may originate in communications interface. Triggering an initiation of the A/D converter data sampling and the timer reset is an example of an interrupt from an interrupt source internal to processor such as from a timer expiration interrupt. Additionally, a device such as A/D converter may signal a data ready condition to processor using an interrupt. Node electronics unit processor includes a background polling process for processes that are not high priority processes. A lower priority request triggers **704** a second node electronics unit process by background polling of a plurality of process execution flags and/or a scheduled processor interrupt. A device or routine requests servicing of a lower priority process by setting at least one process execution flag, processor polls the process execution flags when processor interrupt handler **614** is not executing, and triggers a low priority process when a process execution flag is set. A first process initiated by a process execution flag may spawn another second process such that a follow-on process execution flag is set by the first process to enable execution of a follow-on process. In the exemplary embodiment, interrupt handler **614** services the processor interrupts. In an alternative embodiment, interrupts are handled using the processor operating system, and processes are scheduled using the processor operating system.

[**0039**] Exemplary processes that may be initiated using a process execution flag include decoding of received messages and executing received message commands, evaluating communication channel health, conducting a node electronics unit self-evaluation, reading data samples from a node electronics unit A/D converter, executing local protection, logging diagnostic history, logging event history, reading circuit breaker status, reading node identification, determining identification of systems units, updating system unit identification, executing a synchronization routine, adaptively modifying node electronics unit parameters and process execution, and transmitting node electronics unit information to the CCPUs.

[**0040**] Node electronics unit parameters may include a local protection function parameter, a communication parameter, a sampling parameter, a diagnostic parameter, and a calibration parameter. Node electronics unit process execution may include a condition for triggering a process, adding a new trigger, replacing an existing trigger, replacing an existing process with an alternate process, adding a new process, removing an existing process. When replacing an existing process with an alternate process, the existing process may be replaced with an alternate process that is resident in the node and the alternate process may be identified by a process description received from a remote source such as a remote processor, a remote controller, a manual entry, an external process server, an external code server, a storage media, and the a process description may include a binary, executable, compilable source code, interpretable source code, or references to resident code blocks.

[**0041**] Node electronics unit parameters and process execution may be adaptively modified based on system resources, a communication network noise level, a data signal-to-noise ratio, a change in a number of network nodes, a communication channel utilization, a change of authorization of parameters, service requested data, and a change command received from at least one of a remote controller and an external processor. The node electronics unit senses parameters associated with potential system problems and routinely performs system troubleshooting and diagnostic self checks to facilitate maintaining optimal system operation during periods of less than optimal system conditions.

[**0042**] Node electronics unit parameters and process execution may be adaptively modified based on service requested data that may include system status data, local status data, local health data, communication network data, data signal-to-noise ratio, event history, and error history.

[**0043**] To facilitate efficient operation during foreseeable operating conditions at least one of the plurality of processors may be configured to operate at a first power consumption, which would be the power consumption level during a normal operating period, and also configured to operate at a second, reduced power consumption, which would occur during periods of a loss of normal power to the node electronics unit as may occur during a fault in the power supply. Additionally, a processor may be programmed to operate as a primary processor and a second processor may be programmed to operate as a secondary processor. The primary processor is operable to perform the functions of a processor in a normal mode and the secondary processor is operable in a sleep mode and may be self powered. The secondary processor may remain in sleep mode until activated by an external signal, such as a loss of power to the node electronics unit or may "wake-up" periodically, based on an internal timer, to determine the status of the node electronics unit and then reenter sleep mode. The secondary processor may be configured to operate with ultra-low power, at very high processor speed, and be capable of a short power-up or initialization time. During periods when the node electronics unit is supplied with normal power, the secondary processor may communicate secondary processor status, secondary processor health, and secondary processor events to the primary processor, and may receive commands, parameters, status information, and health information from the primary processor.

[**0044**] In the exemplary embodiment, at least one processor is programmed to execute a watchdog timer function for monitoring the health of the other processors. Processor generates a first "heartbeat" signal and transmits the heartbeat signal to each other processor or a predetermined number of the other processors. Each processor that receives the first heartbeat signal and is healthy, responds with a second heartbeat signal, which each processor transmits to the sending processor. The sending processor is programmed to determine the health of the other processors based on heartbeat signals received and the watchdog timer.

[**0045**] A processor may be programmed to execute a power supply monitoring function that includes logging power supply events, determining a health of the power supply, and transmitting commands based on the determined health, for example, writing power supply status data to a nonvolatile memory, executing a reduced instruction set to conserve power, and transferring processing control to a

processor operating at reduced power consumption. The processor may further be programmed to execute a backup protection function when operating at reduced power consumption. During reduced power consumption the processor may operate only selected high priority functions using a reduced instruction set and/or reduced clock speed. In the exemplary embodiment, the processor executes the backup protection function using analog signal processing and bypassing the A/D converter to conserve power. As described above, the processor includes functionality that includes an integrator, a differentiator, an amplifier, a comparator, a voltage reference and a current reference for processing the analog input signals. The processor receives analog signals from a source, such as, a current transformer, potential transformer, and/or a status input device, and processes the analog signal using the integrator, the differentiator, the amplifier, the comparator, the voltage reference and the current reference.

[0046] The above-described power distribution system node electronics unit software architecture is cost-effective and highly reliable. The software architecture enables real-time, synchronized monitoring and control of all node electronics units operating on the power distribution system. The software architecture also provides for division of processes into high priority and low priority categories, such that node resources are used efficiently and system latency times may be maintained below predetermined goals. Accordingly, the power distribution system node electronics unit software architecture facilitates protection and monitoring of the power distribution system in a cost-effective and reliable manner.

[0047] Exemplary embodiments of power distribution system node electronics unit components are described above in detail. The components are not limited to the specific embodiments described herein, but rather, components of each system may be utilized independently and separately from other components described herein. Each power distribution system node electronics unit component can also be used in combination with other power distribution system components.

[0048] While the invention has been described in terms of various specific embodiments, those skilled in the art will recognize that the invention can be practiced with modification within the spirit and scope of the claims.

What is claimed is:

1. A method for operating a power distribution system comprising:

interrupting a first process of a node electronics unit with a processor interrupt signal; and

initiating a second process of said node electronics unit with a polling process.

2. A method in accordance with claim 1 wherein interrupting of said first process comprises:

interrupting said first process with at least one signal selected from the group consisting of: an internal processor interrupt signal and an external processor interrupt signal; and

servicing the processor interrupt signal with an interrupt handler executing on the node electronics unit.

3. A method in accordance with claim 2 wherein interrupting said first process comprises triggering at least one of recording a local time of an arriving message packet, initiating an A/D converter data sampling and a timer reset, and enabling data sample collection.

4. A method in accordance with claim 3 wherein recording said local time comprises receiving an arriving message packet from a communication interface interrupt.

5. A method in accordance with claim 3 wherein initiating said A/D converter data sampling and timer reset comprises receiving a timer expiration interrupt.

6. A method in accordance with claim 3 wherein enabling said data sample collection comprises receiving an A/D converter data ready interrupt.

7. A method in accordance with claim 1 wherein initiating said second process comprises:

setting at least one process execution flag;

polling said at least one process execution flag when a processor interrupt handler is not executing; and

triggering a low priority process with said at least one process execution flag.

8. A method in accordance with claim 1 further comprising setting a follow-on process execution flag to enable execution of a follow-on process.

9. A method in accordance with claim 1 further comprising:

handling interrupts using an operating system; and

scheduling processes using the operating system.

10. A method in accordance with claim 1 wherein initiating a second process of said node electronics unit with a polling process further comprises triggering at least one process selected from the group consisting of decoding of received messages and executing received message commands, evaluating communication channel health, conducting a node electronics unit self-evaluation, reading data samples from a node electronics unit A/D converter, executing local protection, logging diagnostic history, logging event history, reading circuit breaker status, reading node identification, determining identification of systems units, updating system unit identification, executing a synchronization routine, adaptively modifying node electronics unit parameters and process execution, and transmitting node electronics unit information to the central control processing unit.

11. A method in accordance with claim 10 wherein said process of adaptively modifying node electronics unit parameters and process execution further comprises adaptively modifying node electronics unit parameters and process execution based on at least one selected from the groups consisting of: system resources, a communication network noise level, a data signal-to-noise ratio, a change in a number of network nodes, a communication channel utilization, a change of authorization of parameters, service requested data, and a change command received from at least one of a remote controller and an external processor.

12. A method in accordance with claim 11 wherein adaptively modifying node electronics unit parameters and process execution based on service requested data further comprises adaptively modifying node electronics unit parameters and process execution based on at least one selected from the group consisting of: system status data,

local status data, local health data, communication network data, a data signal-to-noise ratio, event history, and error history.

13. A method in accordance with claim 10 wherein adaptively modifying node electronics unit parameters further comprises adaptively modifying at least one selected from the group consisting of: a local protection function parameter, a communication parameter, a sampling parameter, a diagnostic parameter, and a calibration parameter.

14. A method in accordance with claim 10 wherein adaptively modifying node electronics unit process execution further comprises at least one selected from the groups consisting of: adaptively modifying a condition for triggering a process, adding a new trigger, replacing an existing trigger, replacing an existing process with an alternate process, adding a new process, removing an existing process.

15. A method in accordance with claim 14 replacing an existing process with an alternate process further comprises replacing an existing process with a process resident in the node and a process description received from a remote source wherein a remote source includes at least one selected from the groups consisting of a remote processor, a remote controller, a manual entry, an external process server, an external code server, a storage media, and wherein a process description includes at least one of binary executable, compilable source code, interpretable source code, and references to resident code blocks.

16. A method in accordance with claim 1 wherein at least one of the plurality of processors is configured to operate at a first power consumption and to operate at a second, reduced power consumption wherein the power consumption of each configured processor operating at the first power consumption is greater than the power consumption of each configured processor operating at the second power consumption, and wherein the method further comprises operating at least one processor at a reduced power consumption.

17. A method in accordance with claim 16 wherein a first processor is programmed to operate as a primary processor and a second processor is programmed to operate as a secondary processor and wherein the method further comprises:

communicating a status of the secondary processor to the primary processor if power to the node electronics unit is available;

receiving at least one of commands, parameters, status information, and health information from the primary processor; and

reporting at least one of secondary processor status, a secondary processor health, and a secondary processor event to the primary processor.

18. A method in accordance with claim 16 wherein at least one processor is programmed to execute a watchdog timer function, the method further comprising:

generating a first signal;

transmitting the first signal to at least one other processor;

receiving a second signal from another processor; and

determining a health of the other processor based on the second signal.

19. A method in accordance with claim 16 wherein at least one processor is programmed to execute a power supply monitoring function and wherein the method further comprises:

logging power supply events;

determining a health of the power supply; and

transmitting commands based on the determined health.

20. A method in accordance with claim 19 further comprising:

writing power supply status data to a nonvolatile memory;

executing a reduced instruction set to conserve power; and

transferring processing control to a processor operating at reduced power consumption.

21. A method in accordance with claim 16 wherein the at least one processor is further programmed to execute a backup protection function when operating at reduced power consumption and wherein the method further comprises executing the backup protection function using analog signal processing.

22. A method in accordance with claim 21 wherein the processor includes an integrator, a differentiator, an amplifier, a comparator, a voltage reference and a current reference for processing analog input signals and wherein the method further comprises:

receiving an analog signal from a source; and

processing the analog signal using at least one of the integrator, the differentiator, the amplifier, the comparator, the voltage reference and the current reference.

23. A system for operating a power distribution system comprising:

means for interrupting a first process of a node electronics unit with a processor interrupt signal; and

means for initiating a second process of said node electronics unit with a polling process.

24. A system in accordance with claim 23 further comprising:

means for interrupting said first process with at least one signal selected from the group consisting of: an internal processor interrupt signal and an external processor interrupt signal; and

means for servicing the processor interrupt signal with an interrupt handler executing on the node electronics unit.

25. A system in accordance with claim 24 wherein means for interrupting said first process comprises means for triggering at least one of recording a local time of an arriving message packet, initiating an A/D converter data sampling and a timer reset, and enabling data sample collection.

26. A system in accordance with claim 25 wherein recording said local time comprises receiving an arriving message packet from a communication interface interrupt.

27. A system in accordance with claim 25 wherein recording said local time comprises receiving an arriving message packet from a communication interface interrupt.

28. A system in accordance with claim 25 wherein initiating said A/D converter data sampling and timer reset comprises receiving a timer expiration interrupt.

29. A system in accordance with claim 23 means for initiating said second process comprises:

means for setting at least one process execution flag;

means for polling said at least one process execution flag when a processor interrupt handler is not executing; and

means for triggering a low priority process with said at least one process execution flag.

30. A system in accordance with claim 29 further comprising means for triggering at least one process selected from the group consisting of: decoding of received messages and execution of received message commands, evaluation of communication channel health, reading of data samples from a node electronics unit A/D converter, and transmission of node electronics unit information to said central control processing unit.

31. A system in accordance with claim 23 further comprising means for setting a follow-on process execution flag to enable execution of a follow-on process.

32. A system for operating power distribution system comprising:

interrupting a first process of a node electronics unit with a processor interrupt signal;

means for servicing the processor interrupt signal with an interrupt handler executing on the node electronics unit and

initiating a second process of said node electronics unit with a polling process.

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