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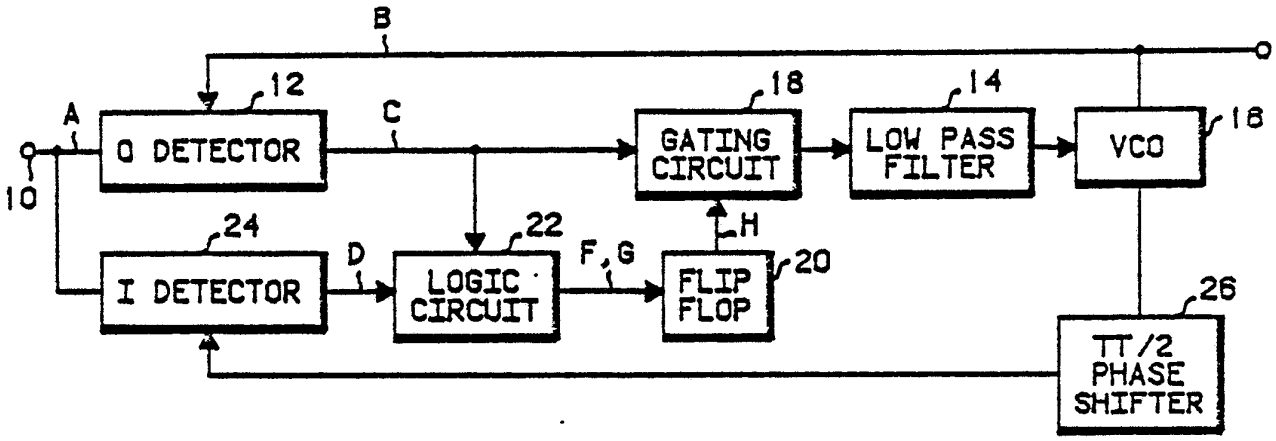
(54) Title: PHASE LOCKED LOOP WITH IMPROVED LOCK-IN



(57) Abstract

The circuit determines whether an incoming frequency is within the normal 'lock-in' range of a phase locked loop VCO (16) or not, and whether it is higher or lower than the VCO frequency. If not within normal range, the beats are rectified and gated (18) to provide a DC control voltage of the proper value and polarity for locking the oscillator on the incoming frequency. Rectification may be half (18) or full (38) wave as needed, and the circuit may include filter bandwidth control (46) as well. This circuit is suitable for signals of any waveform, quadrature signals, and AM stereophonic signals.

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PHASE LOCKED LOOP WITH IMPROVED LOCK-IN

Background of the Invention

This invention relates to the field of phase locked loops and, more particularly, to means of providing fast "pull-in" even when locking signal and VCO reference frequency differ by a frequency substantially higher than the bandwidth of the control filter.

A conventional phase locked loop may have a relatively narrow "lock-in" range, determined largely by the band-width of the filter. Considerations of stability and pull-in time also limit the range of a PLL. There have been many modifications made to PLL circuits over the years since they were first developed. One of these was the "quadricorrelator" which was developed for use with the NTSC color television signals to provide automatic color synchronization. The quadricorrelator included a beat detector and means for changing the bandwidth of the filter when the oscillator was not locked to the frequency of the incoming signal. In another improvement circuit, a plurality of NAND gates was utilized to detect the trailing edges of the two input signals and provide a DC signal to the VCO. While partially successful, this circuit provides a small "dead spot" in the close-in range, and thus will not provide the phase accuracy necessary for cases where the phase relationship between the VCO and the locking signal must be accurately maintained.

Summary of the Invention

It is therefore an object of the present invention to provide fast lock-in of a PLL together with a wide pull-in range.

It is a particular object to provide these in a receiver for AM stereo signals.

These objects and others are provided in a circuit in accordance with the present invention wherein the PLL includes an in-phase detector, a quadrature detector, a filter coupled to the quadrature detector output and an oscillator controlled by the filter output. One oscillator output is coupled to the quadrature detector and a phase shifted output is coupled to the in-phase detector. A logic circuit is coupled to the detector outputs and detects beats between the two. The logic circuit also determines whether the VCO is too high or too low and provides a control signal to a gating circuit coupled between the quadrature detector and the filter. If the received frequency is out of the lock-in range of the VCO, the detector signals are rectified via the gating circuit to provide a DC signal of the proper polarity to pull the VCO frequency to the proper frequency.

Brief Description of the Drawing

Fig. 1 is a block diagram of a PLL including the invention.

Fig. 2 is a timing chart of the signals for the diagram of Fig. 1.

Fig. 3 is a circuit diagram of one embodiment of the logic circuit of Fig. 1.

Fig. 4 is a variation of the block diagram of Fig. 1.

Fig. 5 is similar to Fig. 1, with added features.

Fig. 6 is a block diagram of an AM stereo receiver including the invention.

Detailed Description of a Preferred Embodiment

The block diagram of Fig. 1 shows a phase locked loop including the invention. At an input terminal 10, a signal is received as from the IF stage of a radio receiver (see Fig. 6) and is coupled to a PLL consisting of a phase detector 12, a low-pass filter 14, and a voltage controlled oscillator 16. These elements of the PLL operate as in the usual PLL, but inserted between the phase detector 12 and the filter 14 is a gating circuit 18. The gating circuit is coupled to a flip-flop 20, a logic circuit 22 and a second phase detector 24. The output of the VCO is coupled back to the phase detector 12 and, through a 90° phase shifter 26, to a phase detector 24. Phase detector 12 is termed the "Q" detector (quadrature), and phase detector 24, the "I" detector (in-phase), for reasons which will become apparent hereinafter.

The circuit functions as a phase detector when the PLL is locked to the frequency of the incoming signal, but functions as a frequency detector when there is a significant difference between the frequencies. The gating circuit 18 allows the phase detector 12 output to be coupled directly to the filter 14 for controlling the VCO 16 during "lock". When the radio receiver is not tuned closely enough to the VCO frequency for fast lock-in to occur, the circuit determines whether the VCO frequency is too high or too low and couples a modified control signal to the filter which will provide fast lock-in.

Fig. 2 is a timing chart of signals which relate to the block diagram of Fig. 1 and which represent the out-of-lock condition. Signal A represents the incoming carrier (f_A) at the terminal 10. This carrier signal may be wave-shaped or not, but for simplicity of drawing

it is shown here as sinusoidal. Signal B represents the output of the VCO at two-thirds the incoming frequency ($2f_A/3$). Signal C is the beat ($f_A/3$) produced by multiplying the incoming signal A by signal B. Signal D represents the beat produced by multiplying signal A by the phase-shifted signal B. It should be noted here that signal D will lead or lag signal C depending on whether the VCO frequency is higher or lower than the incoming signal, as indicated by the solid and dashed lines, respectively. The pulses of signal E represent the zero crossings of signal C (see Fig. 3). Signals F and G are the two separate output signals of the logic circuit 22 which are coupled to the Set and Reset inputs of the F/F 20. Signal H is the output of the F/F 20 and is the control signal for the gating circuit 18.

Fig. 3 is a circuit diagram of the preferred embodiment of the logic circuit 22. The output signal C of the Q detector 12 (Fig. 1) is coupled to inputs 28, 30 of a zero crossing detector 32. Transistors Q1, Q2 and Q3 are coupled to a current source 34. Two resistors R1, R2 form a divider across the terminals 28, 30 and the bases of the transistors are coupled to the ends and the center of the divider.

When signal C (from detector 12) is positive, the current from the current source 34 is steered through Q1 to B+; when C is negative, the current is steered through Q3. When C is approximately 0 (at the zero crossings) current passes through all three transistors and the Q2 current is coupled to a steering gate 36. The output of Q2 is signal E of Fig. 2. The gate 36, comprised of Q4, Q5 is controlled by the output (signal D) of the I detector 24. If D is positive when the zero crossing occurs, signal E is steered through Q4 (as signal F) to the "Set" input of the F/F 20. If D is negative when the zero crossing occurs, signal E is steered through Q5 as signal G to the "Reset" input of the F/F. In signals F,

G, the solid line pulses represent the "above frequency" condition, while the dashed line pulses represent "below frequency". The output of the F/F (signal H) is represented by the solid line when the incoming signal is high, and by the dashed line when the incoming signal is low. With the signal H controlling the gating circuit 18, the signals from the Q detector 12 are rectified before being coupled to the filter 14. The polarity of the gate output signals is determined by whether the incoming signal leads or lags the VCO frequency. While the output signals from the Q detector 12 would be of too high a frequency to pass through the low-pass filter 14 (when the incoming signal is out of lock-in range), the rectified signals will provide the proper filter output to lock the VCO at the proper frequency. When the VCO reaches the locked-in condition, the beats (signal C) will go to zero and the gating circuit 18 will remain in the closed position. No signals are shown for the "locked" condition, since the PLL will function as it normally would when locked.

Fig. 4 is a block diagram as in Fig. 1, wherein the outputs of the detectors 12, 24, instead of being half wave rectified, are full wave rectified, since the simple gating circuit 18 is now replaced by a phase reversing gate 38, also controlled by the signal H. In some environments, this embodiment may be preferred since it provides a higher control voltage for the VCO, thus even faster lock-in.

Fig. 5 is a block diagram similar to that of Fig. 1, but with the addition of a control for the filter bandwidth. A filter control circuit 46 is coupled to the output of the detector 24 and is used to control the bandwidth of the filter. While the output of the detector 12 can be used for activating the change of bandwidth in response to the locked or unlocked condition of the PLL, the output signal of the detector 24 is

preferred. Such bandwidth control is known and is discussed in the Background of the Invention herein above. In the present circuit, bandwidth would likely be changed from "normal" to "narrower", rather than from "wider" to "normal", thus providing faster lock-in rather than wider pull-in range.

Fig. 6 is a block diagram of an AM stereo receiver such as is shown in a co-pending U.S. patent application S.N. 133,189, assigned to the assignee of the present invention, integrated with the present invention.

The receiver shown is designed to receive a compatible AM stereo signal of the form $(1 + L + R) \cos (w_c t + \phi)$ where ϕ is arc $\tan[(L - R)/(1 + L + R)]$. In the receiver, an antenna 50 receives the compatible AM stereo signal as given above, and this signal is processed in the usual fashion in RF stage 52 and IF stage 54. The monophonic or sum signal L + R is obtained by coupling the output of the IF stage to an envelope detector 56. The L + R signal is then coupled to a matrix 58. The output of the IF stage 54 is also coupled through a variable gain amplifier 60 to the I detector 24 and to the Q phase detector 12. An output of the VCO 16 ($\cos w_c t$) is coupled to the I detector 24 and to the 90^o phase shifter 26. The phase shifter output ($\sin w_c t$) is coupled to the Q detector 12.

The output of the envelope detector 56 is coupled to a high gain operational amplifier 62. The inverting input of the amplifier 62 is coupled from the output of the I detector 24 which is also coupled to the logic circuit 22. The output of the amplifier 62 is coupled to the variable gain amplifier 60, and this feedback loop forces the output signal of the amplifier 62 to become 1 + L + R. This amounts to a multiplication of the amplifier 60 output by a correction factor of $1/\cos \phi$. Since the output signal of the Q detector 12 would be $(L - R) \cos \phi$ without the correction, the corrected

output signal is L - R. This L - R signal is coupled to the matrix 58 which then provides separated L and R output signals.

As described above with respect to Fig. 1, the outputs of the I detector 24 and the Q detector 12 are coupled to the logic circuit 22. The output of the logic circuit (signals F, G) are coupled to the set and reset of the F/F 20, and the output (signal H) of the F/F controls the gating circuit 18. The output of the gating circuit is, again, the signal which, coupled through the low-pass filter 14, controls the VCO 16.

It will be apparent that the "full-wave rectification" of the circuit of Fig. 4 could also be employed in the receiver of Fig. 6. In either case, the two detectors, in-phase and quadrature, used for determining the sum L + R and difference L - R signals of the AM stereophonic receiver can also supply the signals necessary for providing wide pull-in range and fast lock up of the PLL. This improved PLL is also applicable to other AM stereo receivers as well.

In the context of an AM stereo receiver, it is particularly desirable to have a PLL which locks up quickly on the incoming frequency, even when the receiver is poorly tuned. (With pushbutton radios, tuning errors of 2 kHz are not unusual.) A PLL with a wide pull-in range and fast lock-in has many other applications in such fields as FM stereo, television and frequency synthesizers.

Thus there has been shown and described a circuit for improving the operation of a phase locked loop in almost any environment, and an AM stereo receiver wherein the in-phase and quadrature detectors serve the dual purpose described above. Other variations and modifications are possible, particularly in the logic elements, and it is intended to cover all such as fall within the spirit and scope of the appended claims.

What is claimed is:

Claims

1. A phase locked loop comprising:

input means;

first, in-phase detector means coupled to the input means for providing a first detector output signal;

second, quadrature detector means coupled to the input means for providing a second detector output signal, said second output signal being in quadrature with the first output signal;

filter means coupled to the second detector means output;

oscillator means coupled to be controlled by the filter means output, for providing at least one signal to the first and second detector means;

logic means coupled to the outputs of the first and second detector means for detecting beats between said output signals, for detecting the relative phase of said signals, and for providing a control signal in response to said detection; and

gating means coupled to control the connection between the second detector means and the filter means in response to the control signal from the logic means.

2. A phase locked loop in accordance with claim 1 and wherein the filter means is a low-pass filter.

3. A phase locked loop in accordance with claim 1 and wherein the logic means includes third detector means for detecting the zero crossings of the second detector means output signal, steering means and bistable means, the steering means coupled to steer the third detector means output signal to the respective inputs of the bistable means in response to the output signal of the first detector means.

4. A phase locked loop in accordance with claim 1 wherein the gating means includes means for providing half-wave rectification of the signals from the second, quadrature detector in response to the control signal from the logic means.

Fig. 1

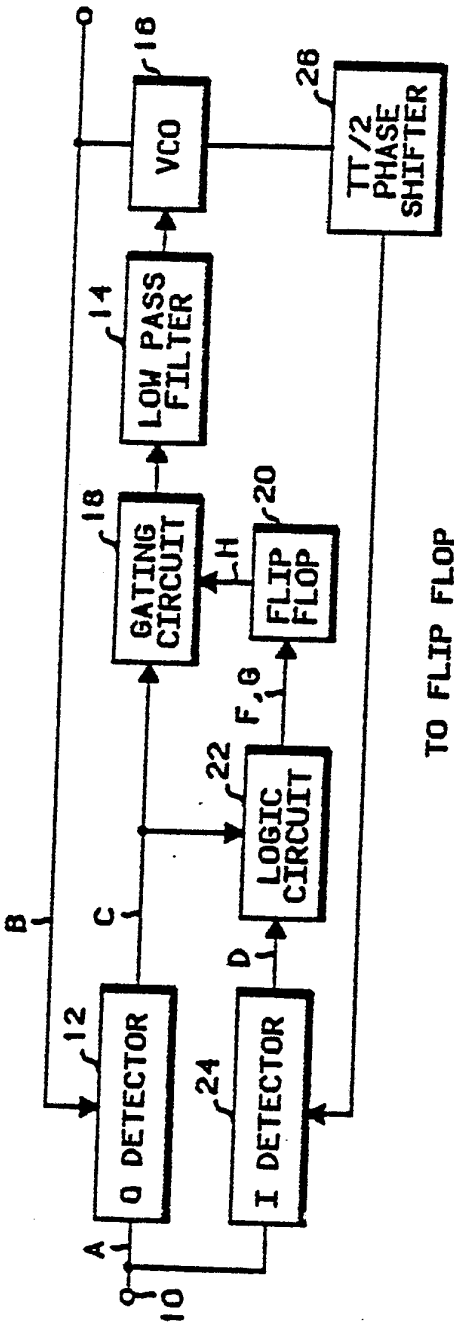


Fig. 2

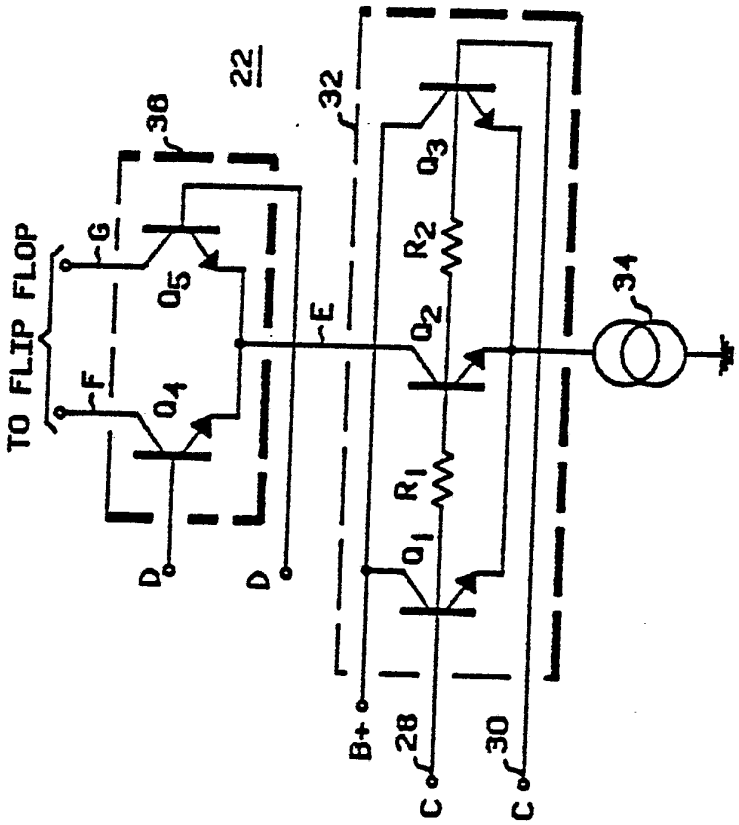


FIG. 2

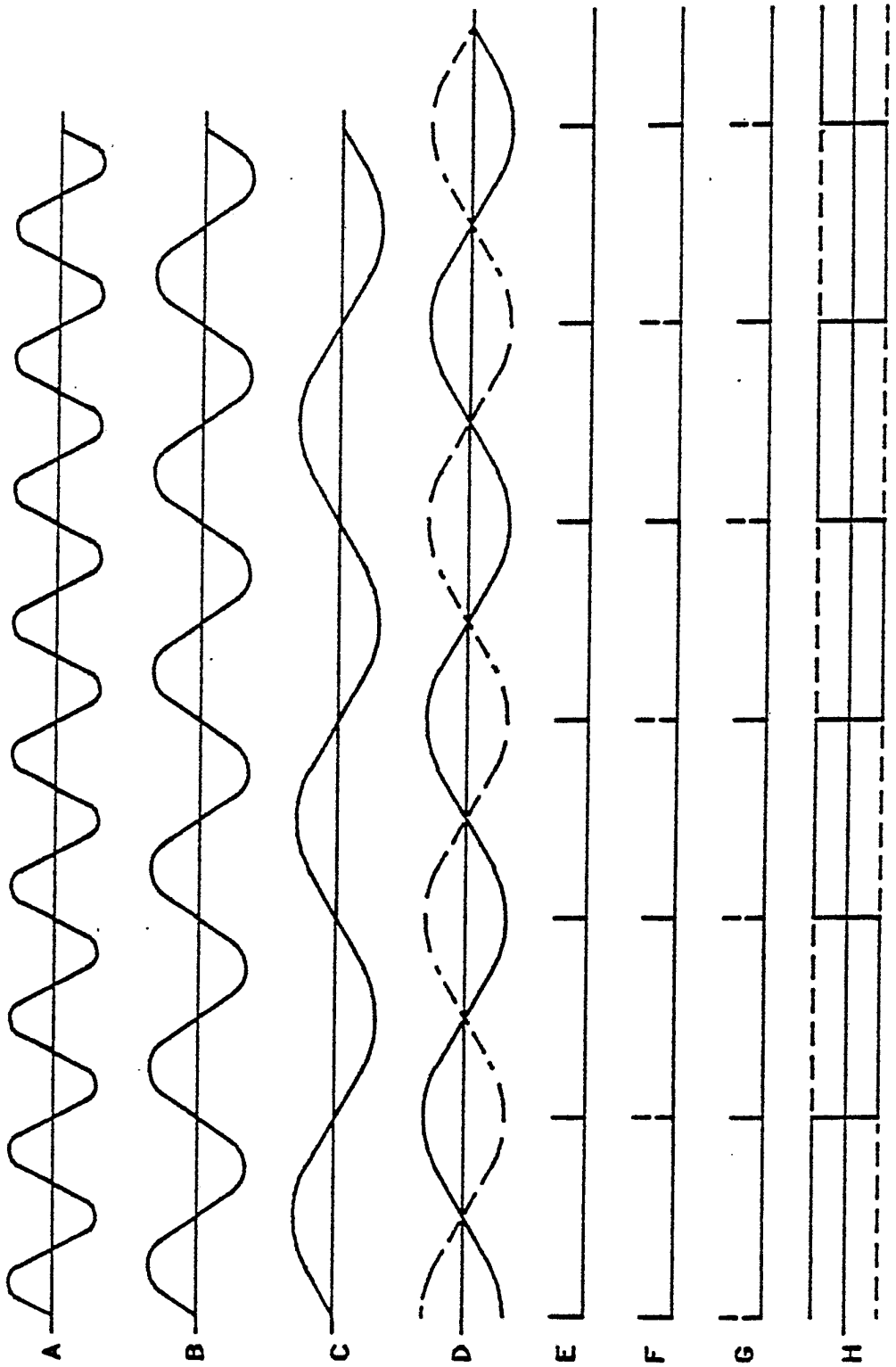


FIG. 4

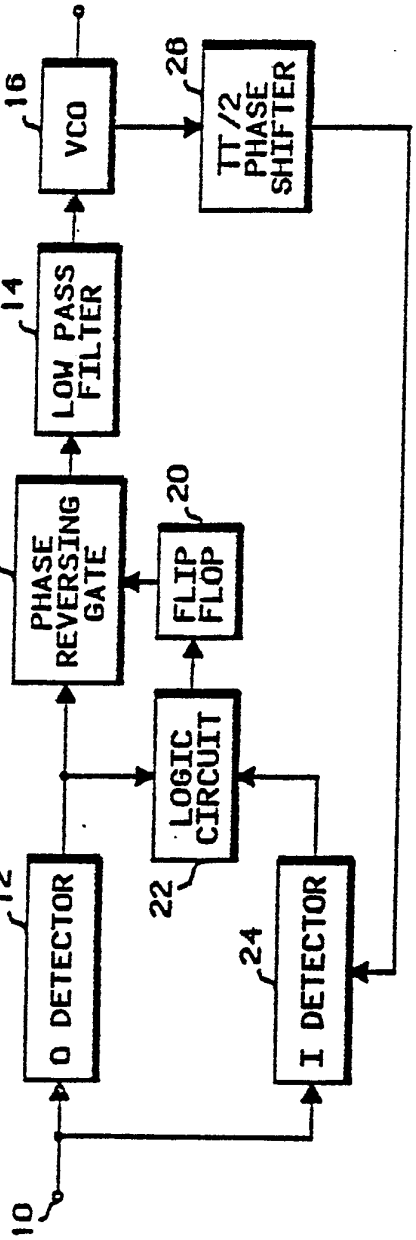
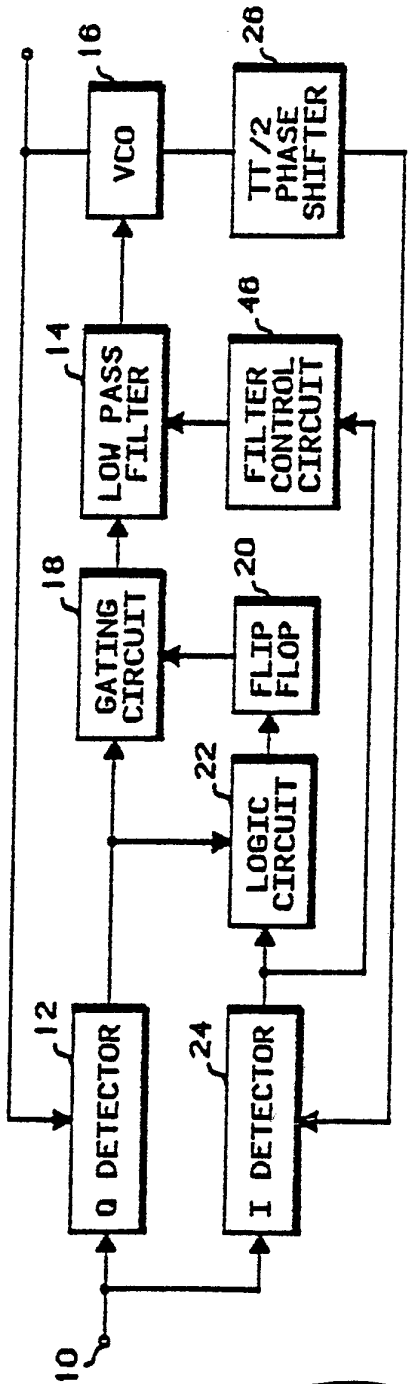


FIG. 5



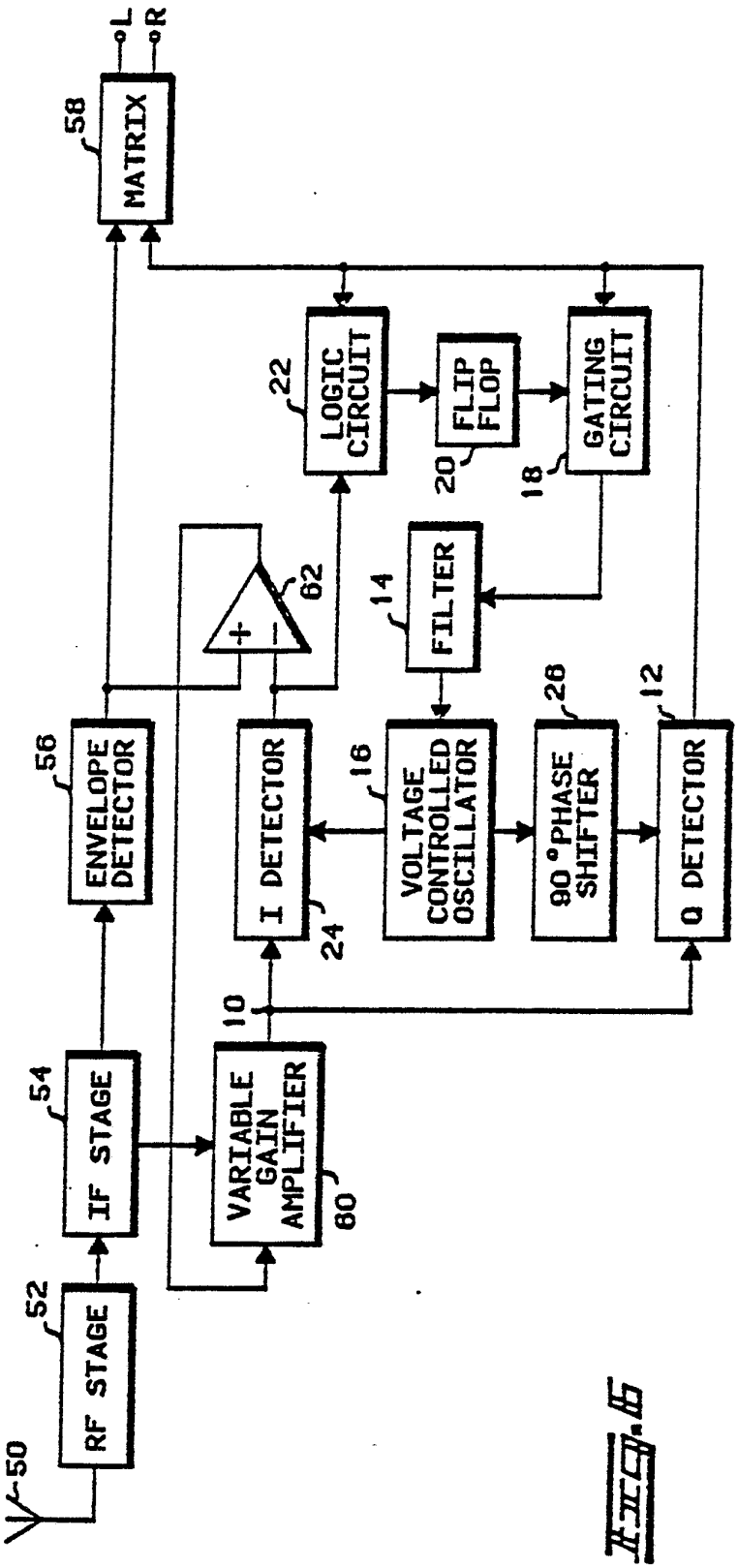


FIG. 5

INTERNATIONAL SEARCH REPORT

International Application No PCT/US 82/00051

I. CLASSIFICATION OF SUBJECT MATTER (if several classification symbols apply, indicate all) [3]

According to International Patent Classification (IPC) or to both National Classification and IPC

INT. CL.[3] H03D 3/18; H04B 1/16
U.S. CL. 329/112,124; 455/209,260

II. FIELDS SEARCHED

Minimum Documentation Searched [4]

Classification System	Classification Symbols
U.S.	179/1GS 329/112,122,123,124,125 455/208,209,260,264

Documentation Searched other than Minimum Documentation to the Extent that such Documents are Included in the Fields Searched [5]

III. DOCUMENTS CONSIDERED TO BE RELEVANT [14]

Category *	Citation of Document, [16] with indication, where appropriate, of the relevant passages [17]	Relevant to Claim No. [18]
A	US, A, 3,909,735, Published 30 September 1975 Anderson et al.	1-4
A	US, A, 4,117,410, Published 26 September 1978 Bender.	1-4
A	US, A, 4,213,096, Published 15 July 1980 Daniel.	1-4
A,P	US, A, 4,270,221, Published 26 May 1981 Daniel	1-4

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IV. CERTIFICATION

Date of the Actual Completion of the International Search [2]	Date of Mailing of this International Search Report [2]
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ISA/US	Douglas W. Olms