Dec. 23, 1969 J. G. WARREN 3,486,018

ELECTRICAL SIGNAL FUNCTION GENERATORS

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Fig. 1.

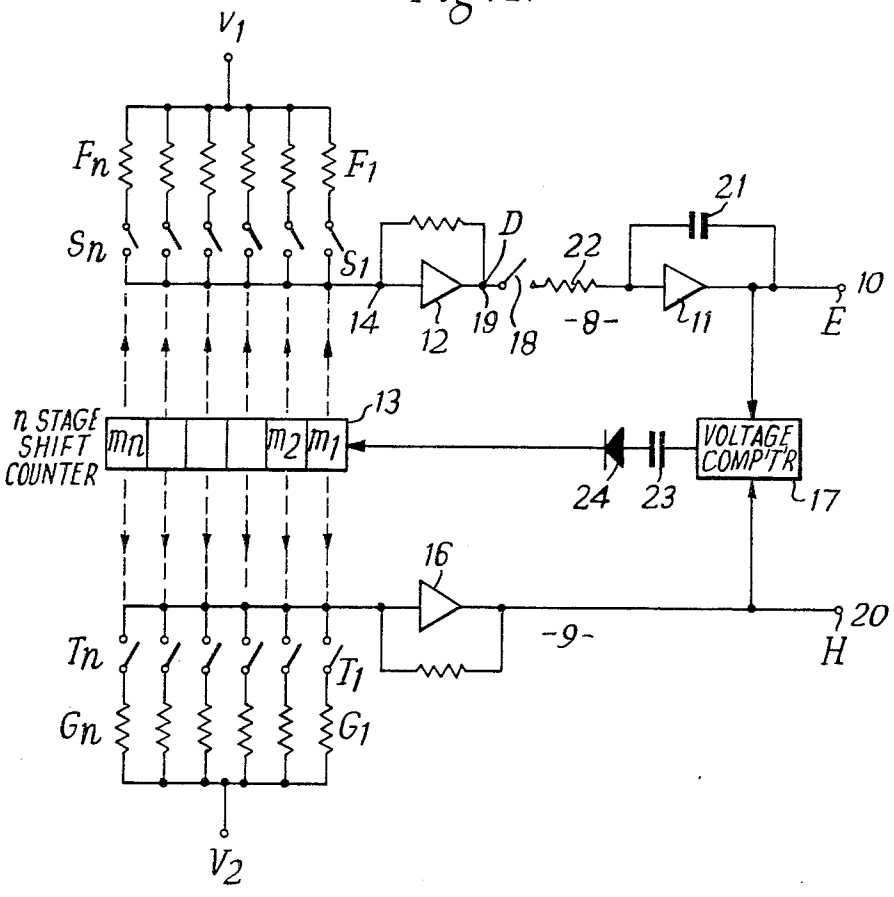
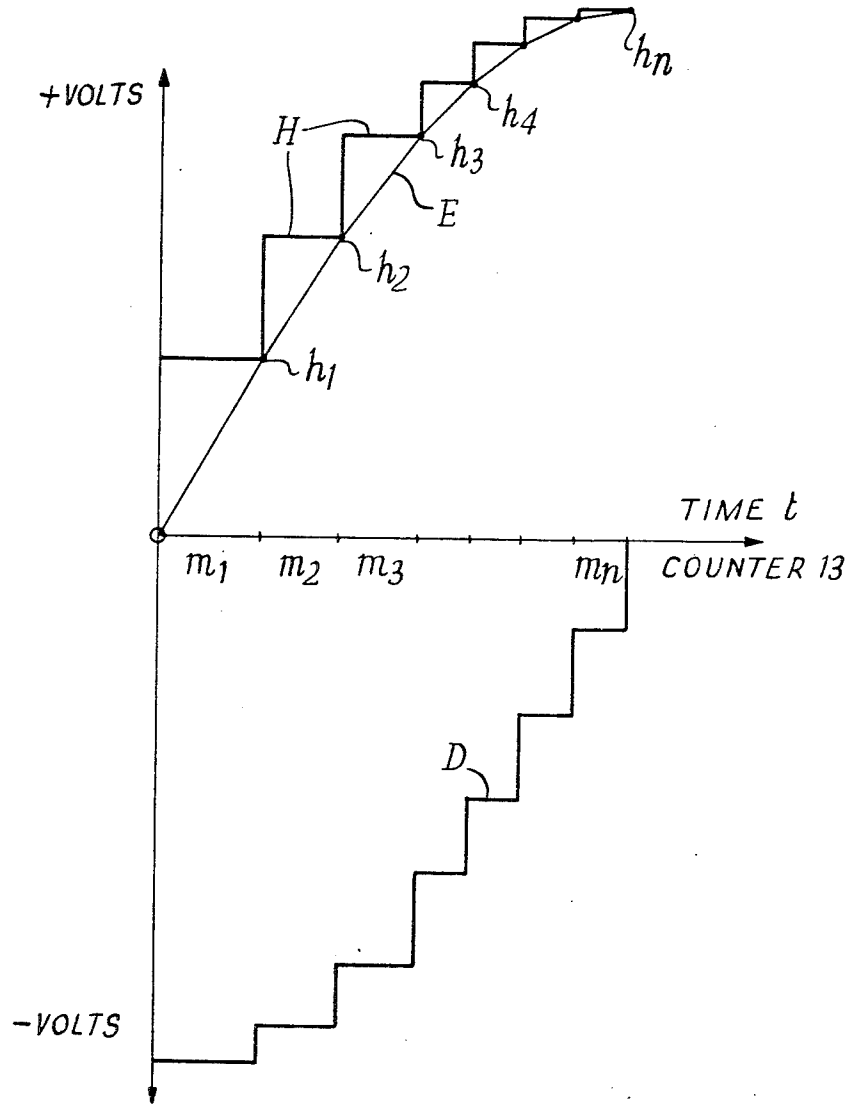


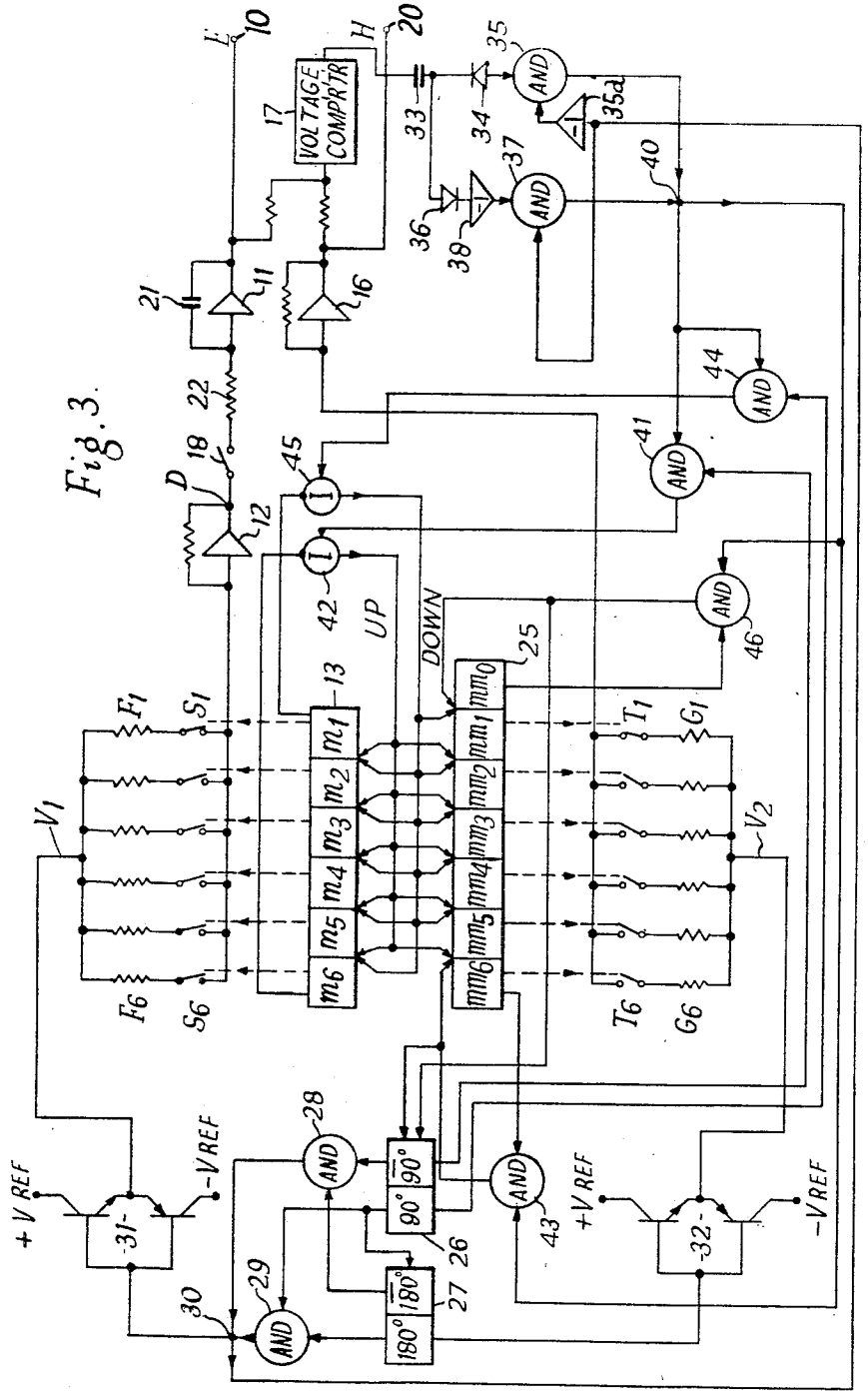
Fig. 2.



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Fig. 3.



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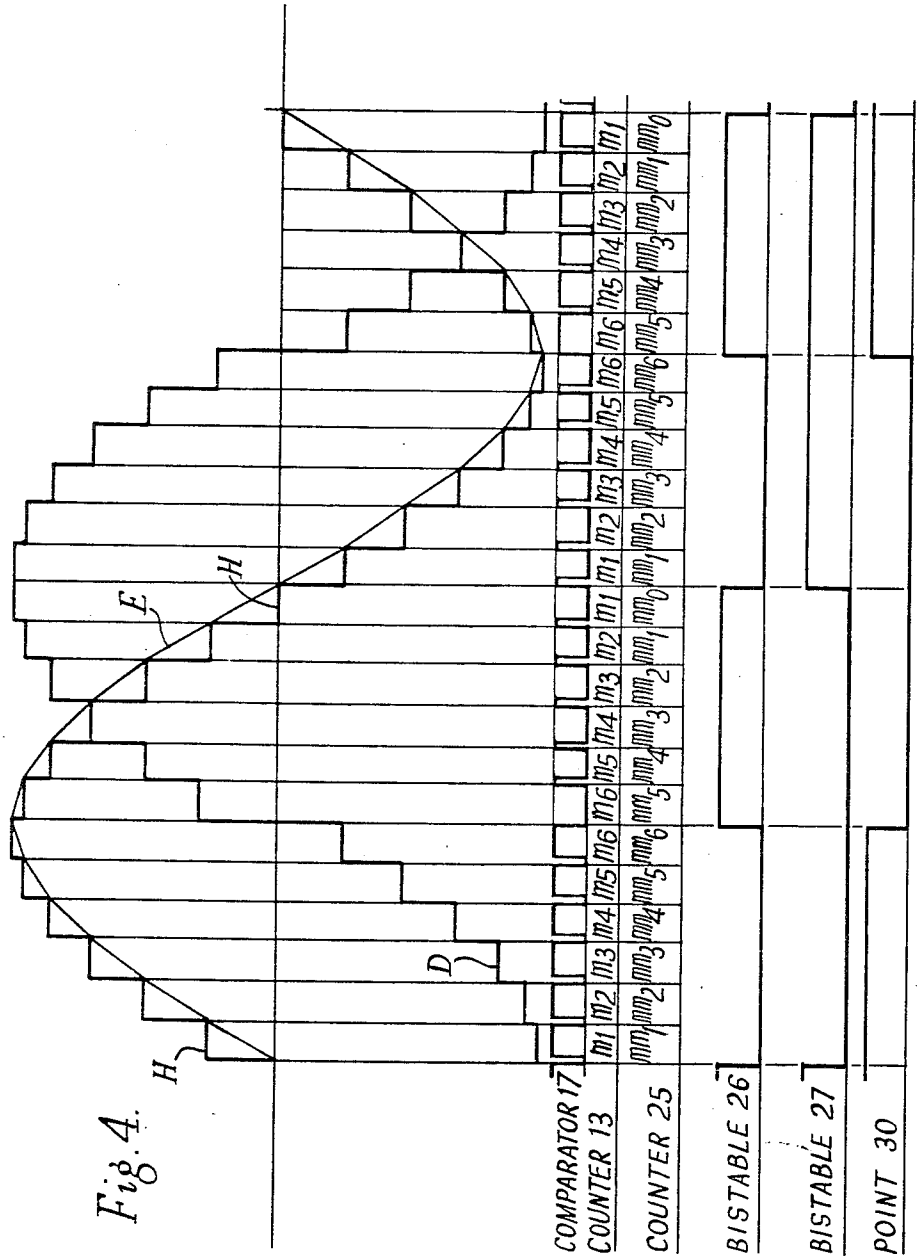


Fig. 4.

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Fig. 5.

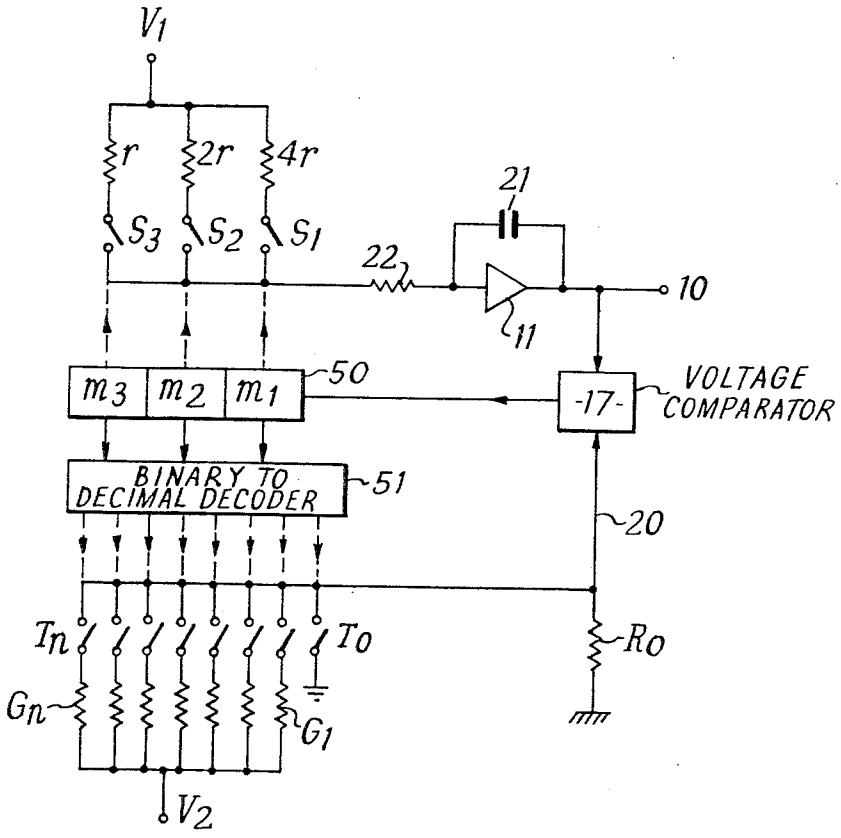


Fig. 6.

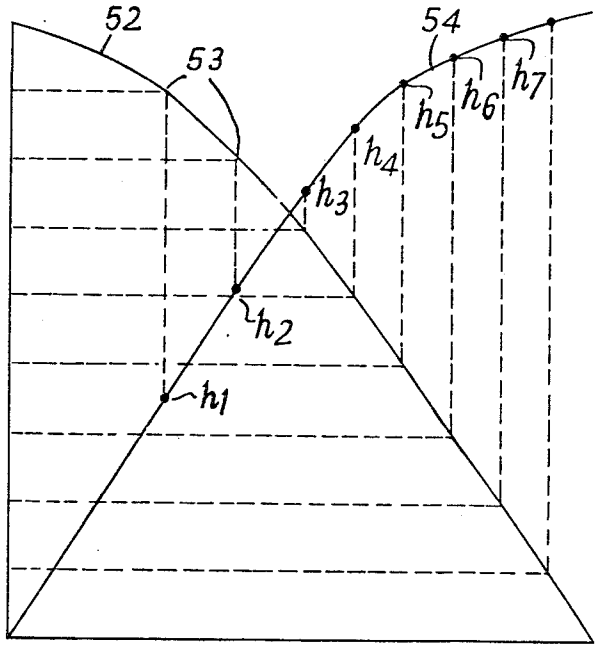
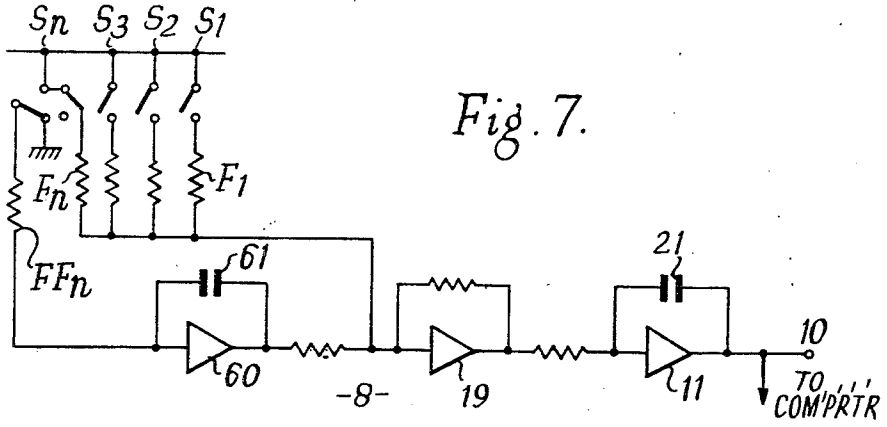

52
53
54
h1
h2
h3
h4
h5
h6
h7

Fig. 7.


Sn S3 S2 S1
Fn
F1
FFn
61
60
21
11
10
TO COMPTR
19

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3,486,018

ELECTRICAL SIGNAL FUNCTION GENERATORS

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Int. Cl. G06g 7/26, 7/28; G06f 15/34
U.S. Cl. 235—197 10 Claims

ABSTRACT OF THE DISCLOSURE

An electrical signal function generator in which two sets of signal sources provide selectable inputs to two circuits having different transfer functions, one nonlinear and one constant. The outputs of the two circuits are compared. When they are equal (or bear any predetermined relationship), a pulse is provided to a pulse register. The pulse register provides outputs to switching means which change the selection of signal sources. The sources selected determine the slope of the signals produced by the two circuits, thereby generating any desired functions. Monotonic or periodic functions can be generated over a wide frequency range. Logic circuits are used to switch signal source polarities to produce alternating functions.

This invention relates to electrical signal function generators, that is to say devices which provide a voltage or current signal which approximates a specified function of time in an analogue manner. The invention is concerned with generators of the type in which the function is constructed of a plurality of segments spanning defined break points at which there is generally a second order discontinuity, i.e. a discontinuity in slope.

The object of this invention is to provide an improved function generator which can be designed to provide a variety of functions with relatively simple components and which can, if required, determine derivatives beyond the first of each signal segment. Moreover periodic functions can be generated over a wide range of frequencies.

The invention comprises a pulse register, first and second sets of constant signal sources and corresponding first and second quadripole networks, the pulse register being arranged as it passes through successive states to couple to the input of each quadripole network a succession of different signal sources or combinations thereof from the set of sources corresponding to the network, and means for comparing the outputs of the two networks and for supplying a pulse to the register when the outputs attain a predetermined relationship, the networks having different transfer functions conforming with the constraints set out below.

The principle upon which the above-defined function generator operates is that, each time a pulse is supplied to the register and it changes to its next state, the change in the signal sources upsets the balance between the two outputs of the quadripole networks. Because of the different transfer functions of the two networks the outputs progress once again towards the condition of balance detected by the comparing means and when this is reached a further pulse is supplied to the register. The condition of balance, i.e. the said predetermined relationship, may be equality between the outputs of the network though this is not essential.

By a pulse register is meant any device or circuit which passes through a series of successive states in response to successive pulses applied thereto and may thus be (inter alia) a binary or other counter, a ring counter, or a shift register.

The above-mentioned constraints can be defined by considering the networks to have their transfer functions expressed in the form:

$$a_0+a_1p+a_2p^2+\ldots+\frac{b_1}{p+c_1}+\frac{b_2}{(p+c_2)^2}+\cdots$$

wherein p is the differential operator (d/dt) and the a's, b's and c's are constants.

The constraints are that all a_1, a_2, etc. for both networks must be zero whilst a_0 for one network must be finite but must be zero for the other network unless first order discontinuities are required at the break points. Within these constraints the networks may be either active (as hereinafter described) or passive. They conveniently have together common (grounded) input and output terminals.

In order to generate a periodic function of time it is necessary either to use a comparator which responds to the attainment of the predetermined relationship irrespective of the sense of approach thereto (i.e. in the case of the relationship being equality, irrespective of whether equality was approached from the situation with the first quadripole network output greater than the second quadripole network output or vice versa) or to switch the sense of the comparison when the slope of the function changes sign.

A development of the invention consists in not only changing the signal sources as the register changes state but in changing the characteristics of at least one quadripole network at least on the occasion of certain changes of state of the register. This may be done by substitution of different networks, by switching different networks in cascade with each other and in other ways. A simple example of this will be described subsequently.

The invention has particular utility in the generation of sinusoids of widely variable frequency (e.g. 0.001 c./s. to 100 kc./s.) for use, for example, in measuring the transfer functions of servo systems.

The invention will be further described by way of example with reference to the accompanying drawings, in which:

FIG. 1 is a schematic diagram of a simple embodiment for generating a continuous monotonic function of time,

FIG. 2 shows waveforms used in explaining the operation of FIG. 1 when the function is a sinewave in the quadrant 0 to $\pi/2$.

FIG. 3 shows the circuit of FIG. 1 developed to generate a continuous sinewave, and

FIG. 4 shows explanatory waveforms relating to FIG. 3.

FIG. 5 shows a modification of FIG. 1,

FIG. 6 shows an explanatory graph relating to FIG. 3, and

FIG. 7 shows another modification.

In FIG. 1 an n stage shift counter **13** has stages m_1 to m_n all but one of which are in the "0" state. As the counter is pulsed a "1" is shifted through the stages m_1, m_2, etc. For the purposes of explanation each stage may be considered to consist of a bistable circuit including a relay which is energised when the "1" is in the stage. The relay, when energised, closes the corresponding pair of switches in two sets of switches (relay contacts) S_1 to S_n and T_1 to T_n. (In practice transistor switches and controlling logic would be used in known manner to obtain the necessary speed of operation.) The switches S_1 to S_n control a set of current sources comprising resistors F_1 to F_n and a common voltage source V_1, connecting these sources one by one to the input terminal **14** of a first quadripole network **8**. Similarly the switches T_1 to T_n control a set of current sources comprising resistors G_1 to G_n and a common voltage source V_2. These feed a second network **9**.

Both networks have common grounded terminals which are not shown. The network **8** consists of an operational amplifier **12** with resistive feedback followed by another operational amplifier **11** having capacitive feedback **21**, thus forming an integrator which has an input resistor **22**. The transfer function of this network is positive and of the form b/p, the magnitude of b being determined by the values R and C of the resistor **22** and capacitor **21**. The network **9** consists simply of an operational amplifier **16** with resistive feedback and has a constant, negative transfer function. To allow for the difference between the signs of the transfer functions, the voltages V_1 and V_2 are of opposite sign, for example $+V_{ref}$ and $-V_{ref}$, so providing voltages of the same sign on the output terminals **10** and **20** of the networks **8** and **9** respectively. The voltages may be designated E and H respectively.

The voltages E and H are applied to the two sides of a voltage comparator **17** which pulses the counter **13** each time E attains the magnitude of H. The comparator can thus be a conventional trigger circuit having E and H fed to its two sides, with a capacitor **23** for differentiating the output voltage level changes of the comparator and a diode **23** for passing the pulses thus produced only when the trigger circuit changes state upon E attaining H and for suppressing the pulses produced when the trigger circuit changes state in the other direction.

The operation of the circuit can be considered from an initial condition in which the counter **13** is in the state m_1 so that switches S_1 and T_1 are closed. If a switch **18** between the amplifiers **12** and **11** is open, steady potentials D and H (FIG. 2 at time 0) are developed at the outputs **19** and **20** of the amplifiers **12** and **16** respectively, the magnitudes of D and H being determined by F_1 and G_1 respectively.

When the switch **18** is closed the potential E commences to rise until, at the break point h_1, it reaches H whereupon the trigger circuit **17** changes state, a pulse is fed to the counter **13** which assumes the state m_2, opens the switches S_1 and T_1 and closes the switches S_2 and T_2. The newly assumed potentials D, E and H immediately cause the circuit **17** to switch back to its original state and E now rises with a new slope determined by F_2, so producing the segment h_1 to h_2. This process continues until the whole curve (to h_n) has been produced.

The break points may be positioned as required to give whatever shape of curve is desired. When the positions of the break points have been decided the values of the F and G resistors are readily determined, the resistors F_1 to F_n in accordance with the slopes of the line segments respectively and the resistors G_1 to G_n in accordance with the break point values h_1 to h_n respectively. The conductances of G_1 to G_n thus increase progressively whilst the conductances of F_1 to F_n decrease progressively and, if E is a sinewave, it will be seen that D and H are respectively staircase opproximations to $-\cos t$ and $\sin t$ respectively in the first quadrant. The integrator **11**, **21** sees to it that, at the break points, the relationship is preserved:

$$\sin t = -\int -\cos t$$

FIG. 3 shows the complete circuit for generating a continuous sine wave using six break points in each quadrant. Separate shift counters **13** and **25** are now provided for the switches S_1 to S_6 and the switches T_1 to T_6 respectively. The counter **13** has stages m_1 to m_6 and the counter **25** has stages mm_0 to mm_6, none of the switches T_1 to T_6 being closed in the state mm_0. The operations in the four quadrants are controlled by two bistables **26** and **27**, the former of which is caused, in a manner to be described subsequently, to change state at the end of every quadrant. The two halves of this bistable are designated 90° and $\overline{90°}$ and the output waveform for the 90° half is shown in FIG. 4. The bistable **27** is driven from one half of the bistable **26** and therefore changes state at intervals of $\pi/2$. Its two haves are designated 180° and $\overline{180°}$ and the output waveform for the 180° half is shown in FIG. 4.

Two AND gates **28** and **29** are used to derive another waveform which switches at intervals of $\pi/2$ but in quadrature with the bistable **27**. Thus the gate **28** produces an output when the $\overline{90°}$ half of bistable **26** is on and when the $\overline{180°}$ half of bistable **27** is on. The gate **29** produces an output when the 90° and 180° halves are both on. The outputs of the two gates combine at point **30** to produce the waveform shown for this point in FIG. 4.

FIG. 4 also shows the waveforms for the points E, D and H which correspond to the waveforms shown in FIG. 2 for one quadrant only. It is readily seen that the following polarities for V_1 and V_2 are required:

	V_1	V_2
Quadrant 1	$+V_{ref}$	$-V_{ref}$
Quadrant 2	$-V_{ref}$	$-V_{ref}$
Quadrant 3	$-V_{ref}$	$+V_{ref}$
Quadrant 4	$+V_{ref}$	$+V_{ref}$

These polarities are readily achieved using two conventional emitter switches **31** and **32** driven respectively by the waveform at the point **30** and the waveform on the 180° half of the bistable **27**, as shown in FIG. 3. The output of the comparator **17** assumes a lower level when E is more positive than H and an upper level when H is more positive than E. The output waveform of the comparator **17** is therefore as shown in FIG. 4, the narrow pulses in the waveform representing the brief intervals during which the waveforms E and H cross at the break points. It is the leading edges of these pulses which are required to define the instant of each break point and it will be seen that the leading edge is negative-going in quadrants **1** and **4** and positive going in quadrants **2** and **3**. The transitions in the comparator waveform are differentiated by a capacitor **33**. The negative spikes in quadrants **1** and **4** are selected by a diode **34** and a gate **35** opened by the waveform at point **30** inverted by an inverter **35***a*. The positive spikes in quadrants **2** and **3** are selected by a diode **36**, inverted by an inverter **38** and a gate **37** opened by the inverted spikes and the waveform at point **30**. The positive spikes at the output of the gate **37** are combined with the output of the gate **35** to provide a train of negative pulses, one at every break point, appearing at point **40**.

These pulses are used to operate the counters **13** and **25** and also the bistable **26**. In the first and third quadrants the counters **13** and **25** are required to count up and pulses from the point **40** are applied to count up inputs of the counters through an AND gate **41** opened by the output of the 90° half of the bistable **26**. However, the counter **13** is not required to count at the end of the said two quadrants and accordingly a further gate **42**, an inhibit gate, is placed in series with the gate **41**, the inhibit input being taken from the counter stage m_6. The counter **25** on the other hand is required to count down to the stage mm_5 at the ends of these two quadrants and a pulse for performing this function is derived from the point **40** through an AND gate **43** opened when the counter **25** is in the mm_6 state. The output of the gate **43** is also used to pulse the bistable **26** at the ends of the first and third quadrants.

For counting down in the second and third quadrants, pulses are derived from the point **40** through an AND gate **44** opened by the 90° waveform of the bistable **26**. Again a series inhibit gate **45** is used with its inhibit input connected to the m_1 stage of the counter **13**. The counter **25** is pulsed from the stage mm_0 to the stage mm_1 by the output of an AND gate **46** responsive to the stage mm_0. This gate **46** provides the pulses for switching the bistable **26** at the ends of the second and third quadrants.

Detailed description of the operation of this embodiment is unnecessary since the principle is the same as in FIG. 1 and the logical functions involved in switching the

voltages V_1 and V_2 and the counters **13** and **25** will be fully apparent from the preceding description.

The waveform E has of course relatively sharp peaks at its maxima and minima as the waveform always has a finite slope. The peaks can be smoothed by means of a simple "soft" clipping diode network. Alternatively, the circuit to be described with reference to FIG. 7 can be used.

The current switches S_1 to S_6 and T_1 to T_6 may be field effect transistors with their gate terminals biased beyond the cut off point of the drain source current. Such transistors are not fully bipolar when used as switches but they remain cut off provided the drain gate and source gate depletion layers are reverse biased by making the gate drive voltage (the output of the bistable **27** or the voltage on point **30**) greater than the signal voltage ($\pm V_{ref}$).

The use of two parallel shift counters **13** and **25** is a convenient way of achieving the different requirements for operating the switches S_1 to S_6 and T_1 to T_6. A single counter could be used with suitable logic interposed between the counter stages and the switches, the logic being controlled by the bistables **26** and **27**. This solution is however unlikely to be any cheaper than the use of two shift counters. If a single counter plus logic is used, the counter may be a binary or binary coded decimal counter. The advantages of a generator such as has been described with reference to FIG. 3 are the wide frequency range which can be obtained. The frequency can be varied by varying the value of the resistor **22** and it may be arranged that control of this resistor is digital. Analogue variation of frequency may be achieved by varying the magnitude of either V_1 or V_2. There is a constant phase difference between the waveforms E and H on the terminals **10** and **20** and the shape of the waveforms is fully determined by the values of the resistors F_1 to F_n and G_1 to G_n. The amplitude of the function is determined by V_2. A six stage device has been described for simplicity. An eight stage device has an accuracy of about 0.1%. The upper frequency limit is determined by the speed of the counters **13** and **14**. A disadvantage is that the resistors F_1 to F_n have to be accurately matched to the resistors G_1 to G_n respectively.

The basic features of a modification designed to overcome this difficulty are shown in FIG. 5. A high speed, three-stage binary counter **50** with stages M_1 to M_3 controls switches S_1 to S_3 which in turn control three resistors $4r$, $2r$ and r replacing the resistors F_1 to F_n. The values of these resistors are in the ratio 4:2:1. Switches T_0 to T_n are controlled through a binary to decimal decoder **51**. The rest of the circuit remains as before, except that the amplifiers **12** and **16** have been omitted in this embodiment and the terminal **20** is connected to earth through a resistor R_0.

FIG. 6 shows how the values of G_1 to G_n can be calculated graphically. Horizontals are drawn to a cosine curve **52** from points equally spaced along the ordinate axis. Verticals are then dropped from the points of intersection **53** with the cosine curve to a sine curve **54** and the points of intersection are the break points h_1 etc. The resistors R_1 etc. are in the ratio $R_1=R_0/h_1$; $R_2=R_0/h_2$ etc.

Finally FIG. 7 shows how the maxima and minima of a curve may be approximated by a parabola. This is done by arranging that the switch S_n switches in, in addition to the resistor F_n, a further resistor FF_n in series with an integrating amplifier **60** (with a feedback capacitor **61**) the effect of which is to make the transfer function of the network **8** in the interval h_{n-1} to h_{n+1} of the form

$$\frac{b_1}{p}+\frac{b_2}{p^2}$$

There is accordingly no actual break point at h_n; H (FIG. 2) is left at the same value from h_{n-2} to h_{n+1} and h_{n+1} is detected when E falls back to H after following a parabola from h_{n-1}.

I claim:

1. An electrical signal function generator comprising the combination of a pulse register; a first set of constant signal sources; first circuit means having a predetermined transfer function for accepting a first electrical signal and for producing an output signal in accordance with said transfer function; a second set of constant signal sources; second circuit means for accepting a second electrical signal and for producing an output signal in accordance with a constant transfer function; first switching means responsive to accumulated pulse counts in said pulse register for selectively connecting at least one signal source of said first set of sources to said first circuit means to provide said first electrical signal; second switching means responsive to accumulated pulse counts in said pulse register for selectively connecting at least one signal source of said second set of sources to said second circuit means to provide said second electrical signal; and comparator circuit means for comparing the outputs of said first and second circuit means and for supplying a pulse to said pulse register when the magnitudes of said outputs attain a predetermined relationship, said pulse register being responsive to each such pulse to cause said switching means to change the signal sources connected to said first and second circuit means.

2. A function generator according to claim **1**, wherein said first circuit means has a transfer function of the form b/p, where b is a preselected constant and p is the differential operator.

3. A function generator according to claim **2**, wherein said second circuit means has a constant transfer function.

4. A function generator according to claim **1**, wherein one of said switching means includes third switching means responsive to the pulse register to change the transfer function of at least one of said first and second circuit means when said register attains a preselected accumulated count.

5. A function generator according to claim **4**, wherein said third switching means is constructed to switch said at least one circuit means between two states, in one of which the circuit means has a transfer function of the form b/p and in the other of which the circuit means has a transfer function of the form

$$\frac{b_1}{p}+\frac{b_2}{p}$$

wherein b, b_1 and b_2 are constants and p is the differential operator.

6. A function generator according to claim **1**, wherein each of said first and second sets of signal sources comprises a set of resistors and each of said first and second switching means is operative to connect selected ones of said resistors, in turn, in series circuit relationship between a reference voltage and the input to the corresponding one of said first and second circuit means.

7. A function generator according to claim **6**, wherein said resistors in said first set of signal sources are arranged in order of increasing conductance and said resistors in said second set of signal sources are arranged in order of decreasing conductance.

8. A function generator according to claim **1**, wherein one of said first and second set of signal sources comprises a set of binary weighted resistors and said switching means is operative to connect combinations of resistors corresponding to successive numbers in the binary scale in turn between a reference voltage and the input to the corresponding one of said first and second circuit means.

9. A function generator according to claim **8**, wherein the other set of signal sources comprises a set of resistors and the switching means is operative to connect the resistors in turn between a reference voltage and the input to the corresponding one of said first and second circuit means.

10. An electrical signal function generator comprising the combination of a pulse register; a first set of constant signal sources; a second set of constant signal sources; first circuit means for accepting an electrical signal and for producing an output signal in accordance with a predetermined transfer function; second circuit means for accepting an electrical signal and for producing an output signal in accordance with a predetermined transfer function; first switching means responsive to accumulated pulse counts in said pulse register for selectively connecting at least one signal source of said first set of sources to said first circuit means; second switching means responsive to accumulated pulse counts in said pulse register for selectively connecting at least one signal source of said second set of sources to said second circuit means; comparator circuit means for comparing the outputs of said first and second circuit means and for supplying a pulse to said pulse register when the magnitudes of said outputs attain a predetermined relationship, said pulse register being responsive to each such pulse to cause said switching means to change the selection of signal sources connected to said first and second circuit means; each of said first and second set of signal sources comprising a plurality of resistors, one end of each of said resistors being connectable to a source of DC voltage and the other end of each of said resistors being selectively connectable by one of said switching means to one of said circuit means; and logic circuit means connected to said comparator circuit means and to said signal sources for connecting one of said sets of signal sources to a positive DC voltage source and the other to a negative DC voltage in response to a first state of said pulse register, and for reversing the polarities of said connections in response to a second state of said register.

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