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Declarations under Rule 4.17:

— *as to applicant's entitlement to apply for and be granted a patent (Rule 4.17(ii))*

(54) Title: APPARATUS AND METHOD FOR TESTING ALL TEST CIRCUITS ON A WAFER FROM A SINGLE TEST SITE

(57) Abstract: An apparatus has a semiconductor wafer hosting rows and columns of chips, where the rows and columns of chips are separated by scribe lines. Vertical and horizontal routing lines are in the scribe lines interconnecting the rows and columns of chips. Test circuit sites are in the scribe lines, each test circuit site including contact pads for simultaneous connection to probe card needles, sensor circuit select and control circuitry, and a sensor circuit bank.

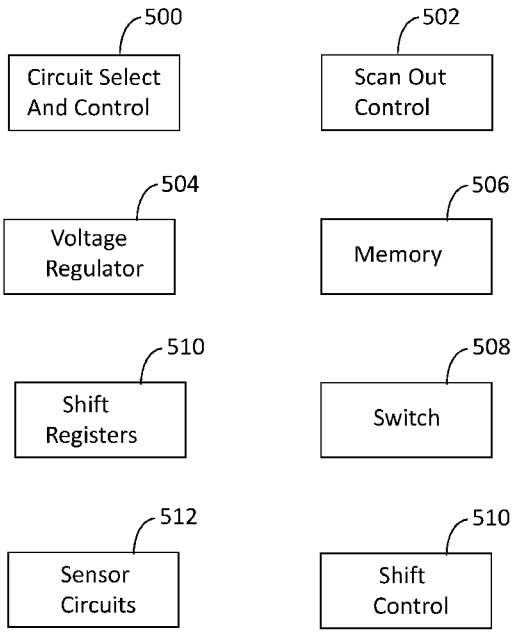

FIG. 5

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[Continued on next page]

Published:
— *with international search report (Art. 21(3))*

APPARATUS AND METHOD FOR TESTING ALL TEST CIRCUITS ON A WAFER FROM A SINGLE TEST SITE

CROSS-REFERENCE TO RELATED INVENTION

[0001] This application claims priority to U.S. Provisional Patent Application Serial Number 63/215,074, filed June 25, 2021, the contents of which are incorporated herein by reference.

FIELD OF THE INVENTION

[0002] This invention relates generally to testing semiconductor wafers. More particularly, this invention relates to techniques for testing all test circuits on a wafer from a single test site.

BACKGROUND OF THE INVENTION

[0003] Figure 1 illustrates a known semiconductor wafer testing system including test equipment 100 connected to a probe card 102, which makes connections with pads on a wafer 104. Figure 2 illustrates a semiconductor wafer 104 with individual chips 200. The individual chips 200 form rows and columns of chips which are separated by scribe lines 202. Within scribe line 202 there are test circuits 204. The test circuits 204 are used during wafer level testing. When testing is completed, a saw is used in the scribe lines to divide the individual chips for subsequent packaging. This cutting process destroys the test circuits 204 in the scribe lines. Figure 3 illustrates a simple test circuit with a gate pad 300, a source pad 302 and a drain pad 304. A probe card needle 306 is connected to the drain pad 304. Figure 4 illustrates multiple probe card needles 306 connected to multiple pads 400 of a semiconductor. Placement of probe card needles on different sites on a wafer is time consuming.

[0004] Thus, there is a need for improved wafer testing techniques.

SUMMARY OF THE INVENTION

[0005] An apparatus has a semiconductor wafer hosting rows and columns of chips, where the rows and columns of chips are separated by scribe lines. Vertical and horizontal routing lines are in the scribe lines interconnecting the rows and columns of chips. Test circuit sites are in the scribe lines, each test circuit site including contact pads for

simultaneous connection to probe card needles, sensor circuit select and control circuitry, and a sensor circuit bank.

BRIEF DESCRIPTION OF THE FIGURES

[0006] The invention is more fully appreciated in connection with the following detailed description taken in conjunction with the accompanying drawings, in which:

[0007] FIGURE 1 illustrates a semiconductor wafer testing system known in the prior art.

[0008] FIGURE 2 illustrates a prior art semiconductor wafer with a scribe line hosting test circuits.

[0009] FIGURE 3 illustrates a prior art test circuit and associated probe card needle.

[0010] FIGURE 4 illustrates prior art probe card needles connected to test circuit pads.

[0011] FIGURE 5 illustrates components associated with embodiments of the invention.

[0012] FIGURE 6 illustrates probe card needles engaging test circuit pads on a single test site that is used to access different test sites on a wafer, with each test site including a voltage regulator.

[0013] FIGURE 7 illustrates probe card needles engaging test circuit pads on a single test site that is used to access different test sites on a wafer, with each test site including power gated linear regulator.

[0014] FIGURE 8 illustrates probe card needles engaging test circuit pads on a single test site that is used to access different test sites on a wafer, with each test site including a power gated header switch.

[0015] FIGURE 9 illustrates an existing metal mask and stitching metal mask utilized in accordance with an embodiment of the invention.

[0016] FIGURE 10 illustrates the stitching metal mask aligned with the existing metal mask in accordance with an embodiment of the invention.

[0017] FIGURE 11 illustrates four adjacent die linked by metal extensions from the stitching metal mask.

[0018] Like reference numerals refer to corresponding parts throughout the several views of the drawings.

DETAILED DESCRIPTION OF THE INVENTION

[0019] Figure 5 illustrates components of the invention formed in scribe lines of a wafer. The components include circuit select and control circuitry 500, scan out control circuitry 502, one or more voltage regulators 504, one or more memory banks 506, one or more

switches 508, one or more shift registers 510, shift control circuitry 510 and sensor circuits 512.

[0020] Figure 6 illustrates vertical routing lines 600 and horizontal routing lines 602 used to interconnect all test sites on different die of a wafer. In this way, all of the test sites on all of the die can be accessed from the probe contacts from any single die. By way of example, Die 1 has a test site with pads 400 to engage probe card needles 306. Die 1 has a circuit select and control circuit 500 responsive to a global circuit select and control signal from test equipment 100. A voltage or linear regulator 504 receives a global Vdd/Vss power signal and a global Vdd/Vss reference voltage, which is used to regulate the global Vdd/Vss power signal to accommodate process variations and inconsistent resistive networks. Power is supplied via Vdd and Vss power pads and is distributed to all die on the wafer. Since there is current flowing through the power distribution network, the resistance on each path produces an "IR" voltage drop wherein the Vdd and Vss voltages that are measured at the sensor circuit are different from the Vdd and Vss voltages that are applied at the test equipment 100. The magnitude of the IR voltage drop varies significantly for each die since each die has a different amount of resistance in the power distribution path. In one implementation, a separate reference voltage for Vdd and/or Vss is routed to each die through a network that is fully separate and independent from the power distribution path. In the case of the reference voltage network, the terminal resistances at the equipment side and on each die is very high so that only a negligible amount of current is flowing through the reference path and there is negligible IR voltage drop. In or near the sensor circuit bank 604, voltage regulator 504 is used to adjust the Vdd and/or Vss of the sensor circuit bank so that the reference voltages are achieved directly at the sensor circuit bank 604. The linear regulator 504 has an additional feature wherein it isolates and suppresses any switching noise or voltage changes from the test circuits that might be injected back on the global power distribution network. This is a key feature when running multiple test circuits at the same time (on different sensor circuit banks) in that the switching noise from one test circuit does not interfere and corrupt the measurement on other test circuits that are running at the same time.

[0021] The sensor circuit bank 512 is a circuit block that contains an array of test circuits, such as ring oscillators, that may contain a number anywhere from a few test circuits to perhaps tens of thousands of test circuits. A pad or pads on the pad array module are allocated for driving the sensor circuit select and control 500, which is used to select and run a single circuit in the sensor circuit bank 512 for a period of time. In one implementation, the same test circuit at the same digital address in the sensor circuit bank 512 is run on all die

simultaneously. The measurement results, which are digitized values from each sensor circuit in the sensor circuit bank 512, are output to a memory 506. The memory 506 can be built to store the results from the entire set of sensor circuits in the sensor circuit bank 512 or for just one sensor circuit.

[0022] The measurement data stored in memory can be output to the probe pad module via a network of shift registers located on each die. Data is first copied from the memory 506 to the shift registers 510. Using the shift control 510, which is controlled from a pad or pads on the probe pad module, the network of shift registers are directed to move the data between die in any of four directions (up, down, left, right). All die on the wafer receive the same shift command. If the data stored in registers on die on the edge of the wafer are shifted to a location that is off of the die edge, the data is deleted. The original set of measurements can be restored by pushing the measurement data from the memory bank to the shift registers again. In this manner, all measurement data can be scanned out through a pad or pads on the pad array module.

[0023] A sensor circuit bank 512 executes wafer testing operations with measurement results being loaded into memory 506. The measurement results are read from memory to shift registers 510 operative with shift control circuit 510. The shift control circuit 510 receives a die-to-die sift control signal, which results in the shift registers supplying a global data scan-out signal that is routed to the test equipment.

[0024] Figure 7 illustrates an embodiment where only one die or test site is measured at a time. Data shift control uses to shift a "One-Hot" selection scheme (i.e., only 1 die or test site contains data in the shift registers across the die in the horizontal and vertical directions). The One-Hot bit selection connects or disconnects the sensor circuit select and control circuit 500 from the global circuit select and control.

[0025] Figure 8 is another embodiment where the regulator 504 is replaced with a power gated head switch and the Vdd/Vss reference voltages are replaced with Vdd/Vss voltage sense signals. This circuit senses the voltages at Vdd and Vss and reads out the values to the external test equipment 100. In this scheme, each test circuit in the sensor circuit bank 512 on each die or test site must be run sequentially. The power gated head switch connects the Vdd and Vss rails of the one-hot selected die or test site to the global Vdd/Vss sense connection. Now the external test equipment can measure and record the Vdd and Vss voltages at the Vdd and Vss rails of the sensor circuit bank 512. As an optional implementation, the global Vdd/Vss sense voltage measurement can be used to correct the global Vdd/Vss power values (i.e., correct for the IR voltage drop between the global

Vdd/Vss power pads and the sensor circuit bank so that the intended supply voltages are applied to the sensor circuit bank 512).

[0026] It should be appreciated that the vertical routing lines 600, the horizontal routing lines 602 and the various test circuits in the scribe lines may be implemented on multiple metal layers connected by vias.

[0027] Figure 9 illustrates an existing metal mask 900 used to form a metal layer associated with a die 200. The metal mask 900 includes metal traces 902 that extend to the end of a die. An embodiment of the invention uses a stitching metal mask 904 to extend the metal traces 902 of a die into scribe lines for connections to other components. The stitching metal mask 904 includes metal extensions 906. Mask alignment marks 908 exist on both the existing metal mask 900 and the stitching metal mask 904.

[0028] Figure 10 illustrates the existing metal mask 900 aligned with the stitching metal mask 904. This allows for four adjacent die 200_1, 200_2, 200_3 and 200_4 to be interconnected on a metal layer, as shown in Figure 11.

[0029] The foregoing description, for purposes of explanation, used specific nomenclature to provide a thorough understanding of the invention. However, it will be apparent to one skilled in the art that specific details are not required in order to practice the invention. Thus, the foregoing descriptions of specific embodiments of the invention are presented for purposes of illustration and description. They are not intended to be exhaustive or to limit the invention to the precise forms disclosed; obviously, many modifications and variations are possible in view of the above teachings. The embodiments were chosen and described in order to best explain the principles of the invention and its practical applications, they thereby enable others skilled in the art to best utilize the invention and various embodiments with various modifications as are suited to the particular use contemplated. It is intended that the following claims and their equivalents define the scope of the invention.

In the claims:

1. An apparatus, comprising:

a semiconductor wafer hosting rows and columns of chips, where the rows and columns of chips are separated by scribe lines;

vertical and horizontal routing lines in the scribe lines interconnecting the rows and columns of chips; and

a plurality of test circuit sites in the scribe lines, each test circuit site including

a plurality of contact pads for simultaneous connection to probe card needles,

sensor circuit select and control circuitry, and

a sensor circuit bank.

2. The apparatus of claim 1 wherein each test circuit site further includes a voltage regulator.

3. The apparatus of claim 1 wherein each test circuit site further includes a memory.

4. The apparatus of claim 1 wherein each test circuit site further includes shift registers.

5. The apparatus of claim 1 wherein each test circuit further includes a one-hot shift register.

6. The apparatus of claim 1 wherein each test circuit further includes shift control circuitry.

7. The apparatus of claim 1 wherein each test circuit site further includes a header switch.

8. The apparatus of claim 1 wherein the contact pads include contact pads for Vdd and Vss global power signals.

9. The apparatus of claim 1 wherein the contact pads include contact pads for Vdd and Vss reference signals.

10. The apparatus of claim 1 wherein the contact pads include contact pads for Vdd and Vss sense signals.

11. The apparatus of claim 1 wherein the contact pads include a contact pad for global sensor circuit control signals.

12. The apparatus of claim 1 wherein the contact pads include a contact pad for scan out control signals.

13. The apparatus of claim 1 wherein the contact pads include a contact pad for measurement scan out signals.

14. The apparatus of claim 1 wherein the rows and columns of chips are selectively connected in the scribe lines by metal extensions from a stitching metal mask.

15. The apparatus of claim 14 wherein the stitching metal mask has mask alignment marks.

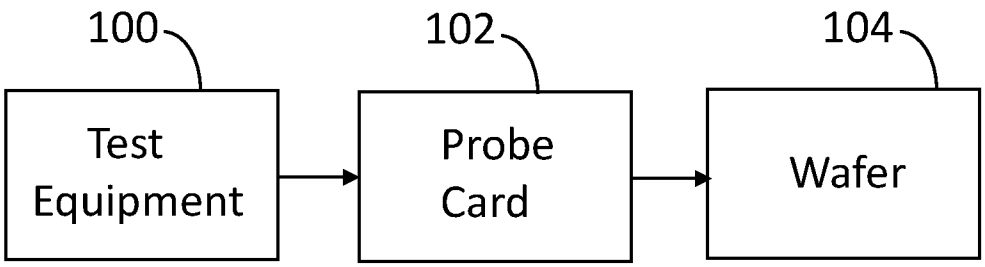

FIG. 1
(Prior Art)

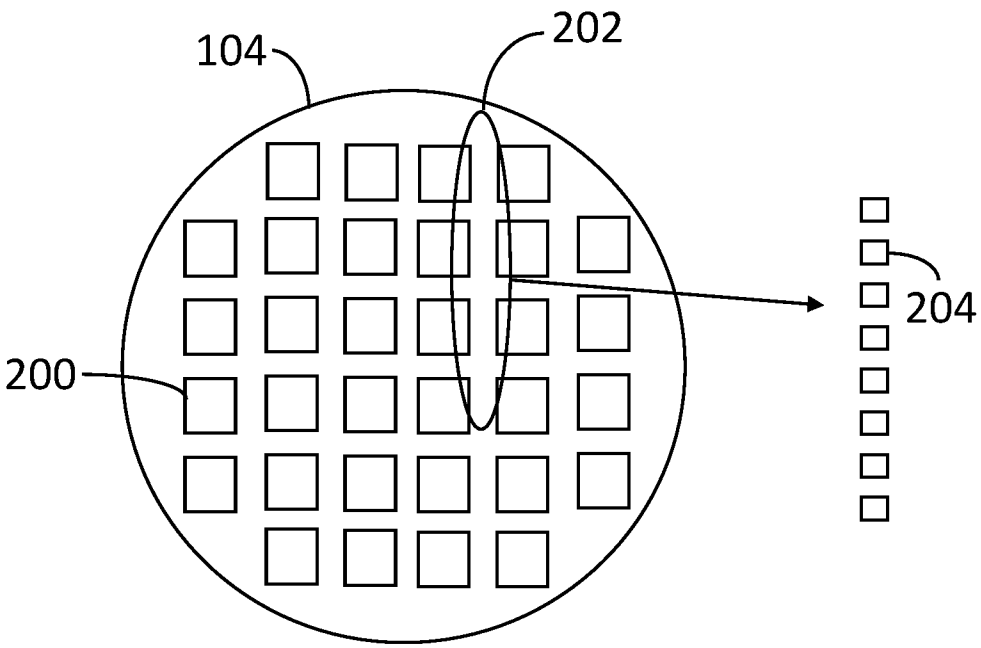

FIG. 2
(Prior Art)

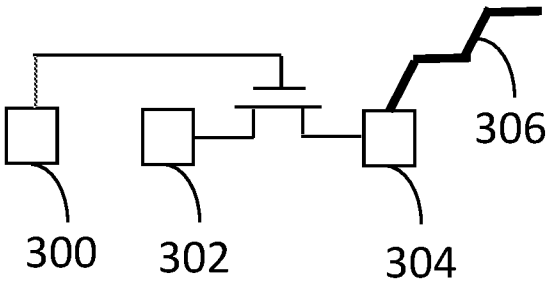

FIG. 3
(Prior Art)

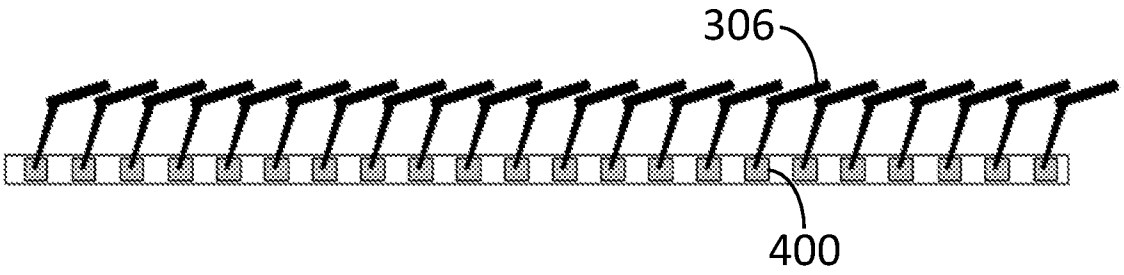

FIG. 4
(Prior Art)

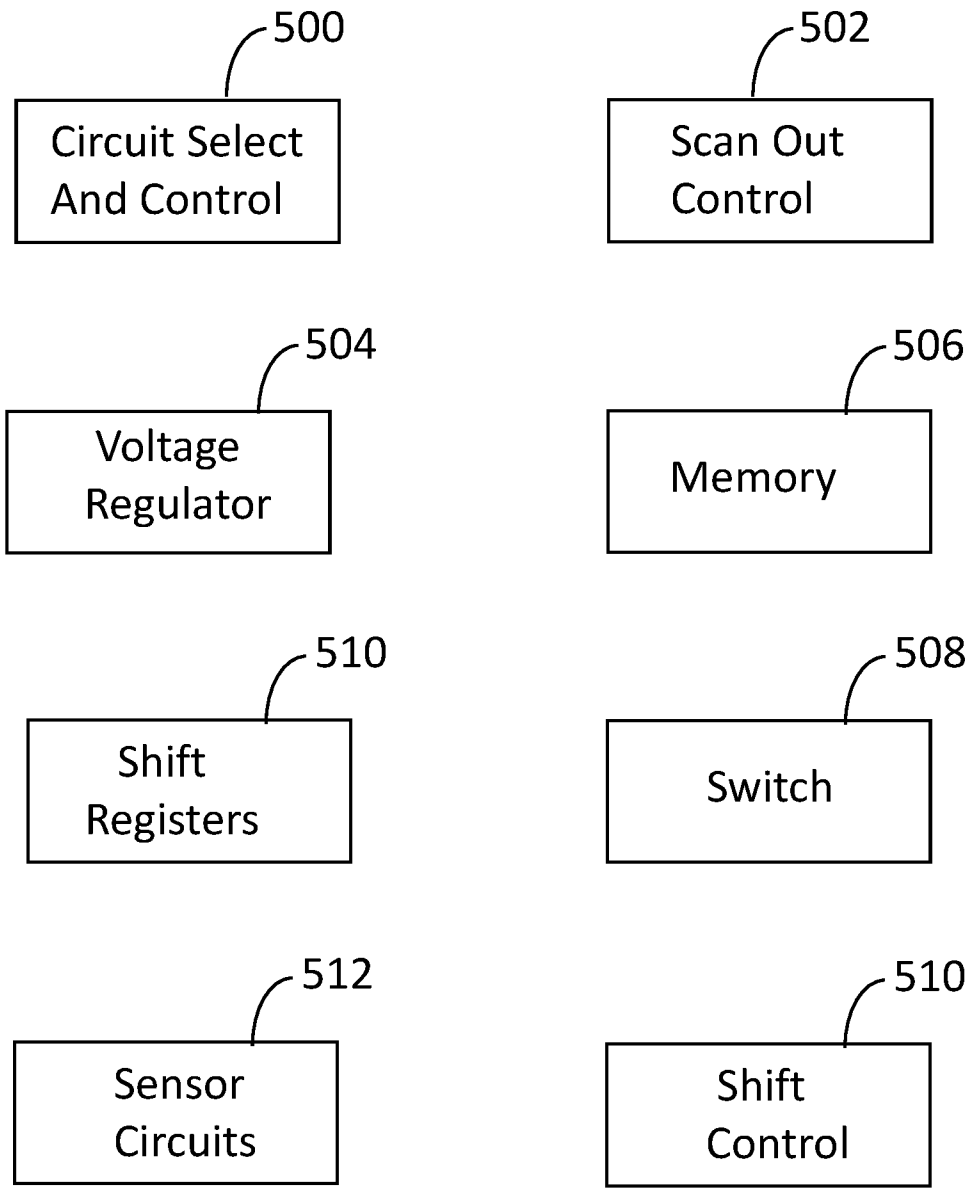
500
Circuit Select And Control
502
Scan Out Control
504
Voltage Regulator
506
Memory
510
Shift Registers
508
Switch
512
Sensor Circuits
510
Shift Control

FIG. 5

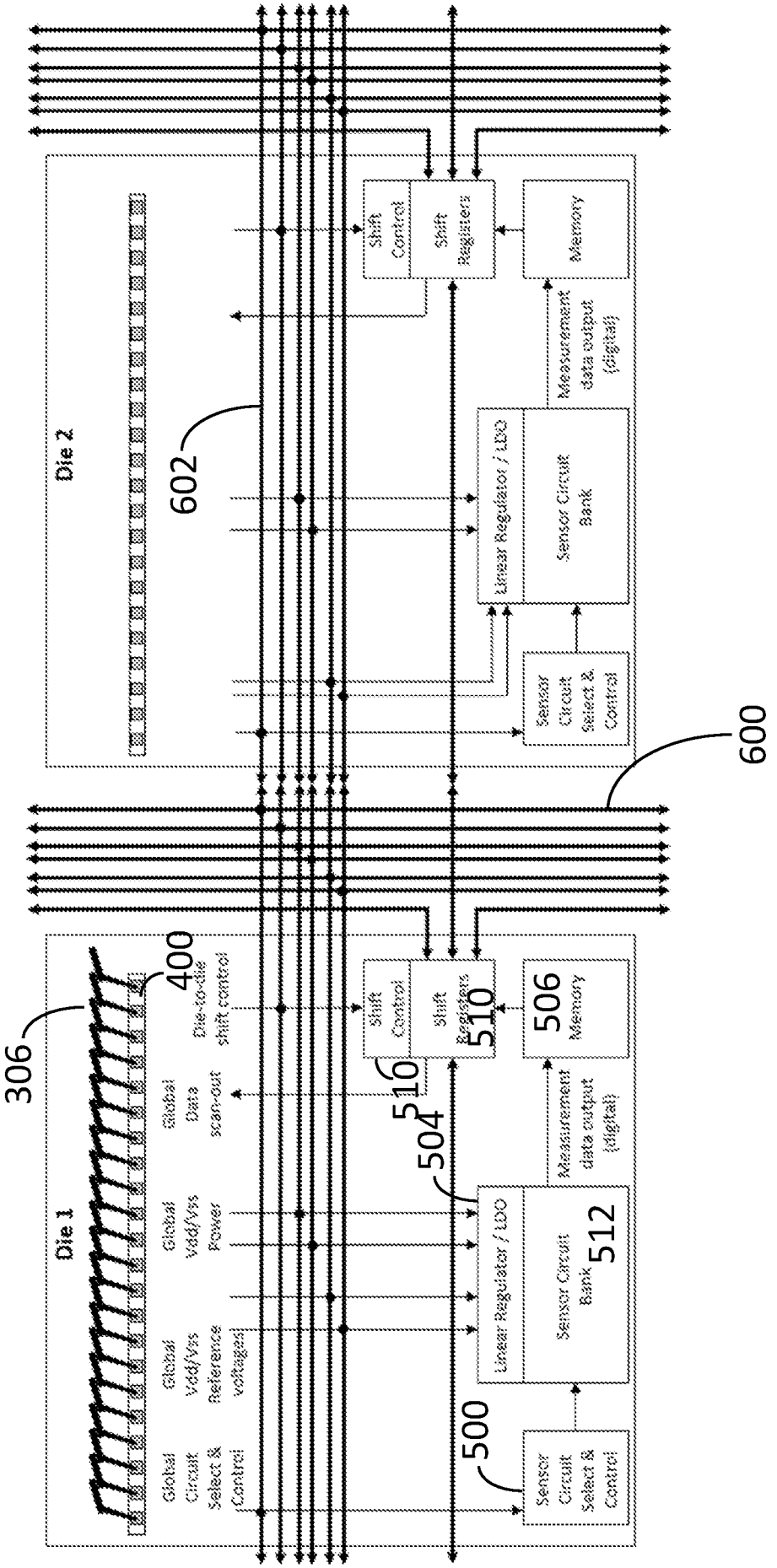
Die 2
602
Shift Control
Shift Registers
Memory
Measurement data output (digital)
Linear Regulator / LDO
Sensor Circuit Bank
Sensor Circuit Select & Control
600
306
400
Die 1
Global Circuit Select & Control
Global Vdd/Vss reference voltages
Global Vdd/Vss Power
Global Data scan-out
Die-to-die shift control
510
504
506
512
500

FIG. 6

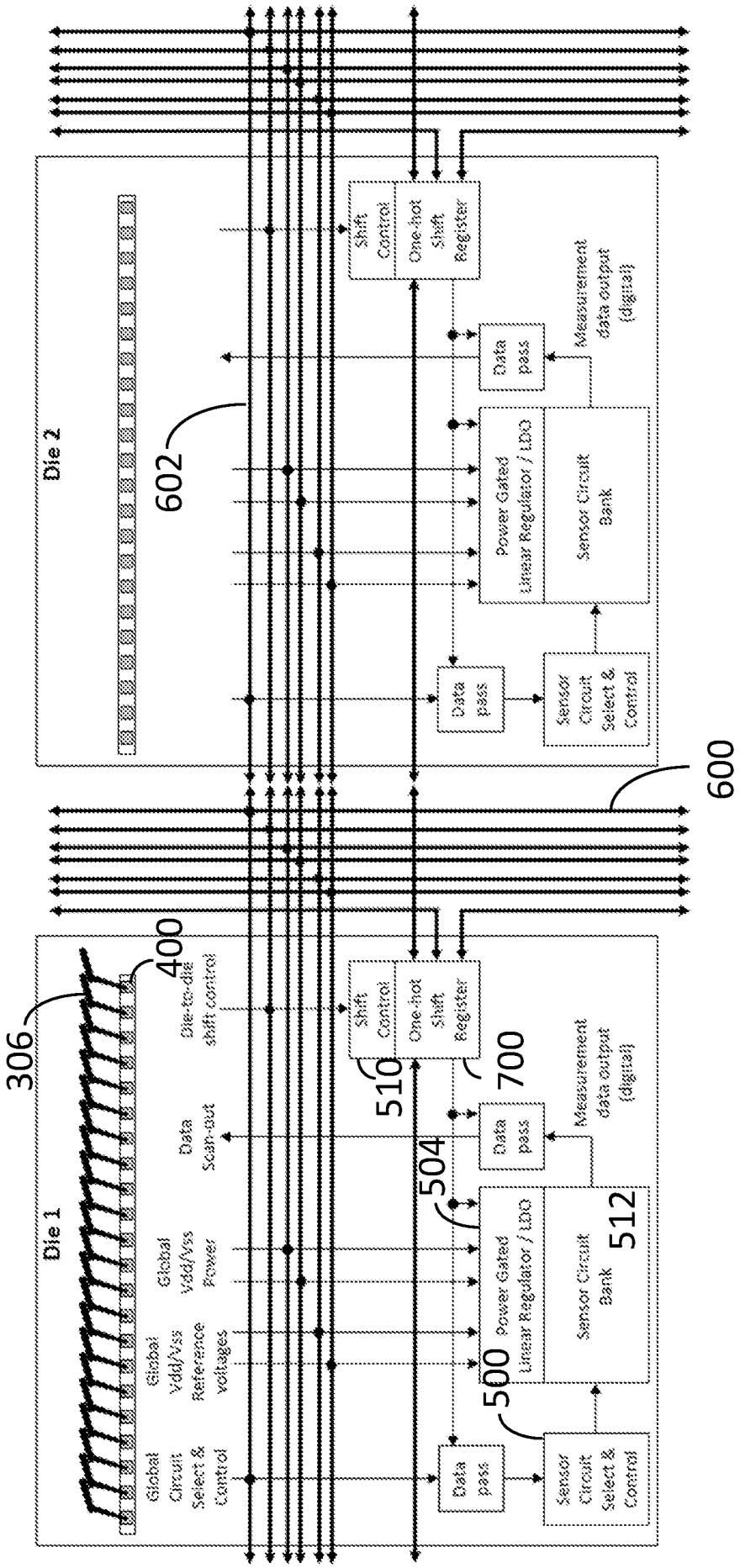
Die 1
Die 2
306
400
602
600
500
504
510
512
700
Global Circuit Select & Control
Global Vdd/Vss Reference voltages
Global Vdd/Vss Power
Data Scan-out
Die-to-die shift control
Shift Control
One-hot Shift Register
Data pass
Power Gated Linear Regulator / LDO
Sensor Circuit Bank
Sensor Circuit Select & Control
Measurement data output (digital)

FIG. 7

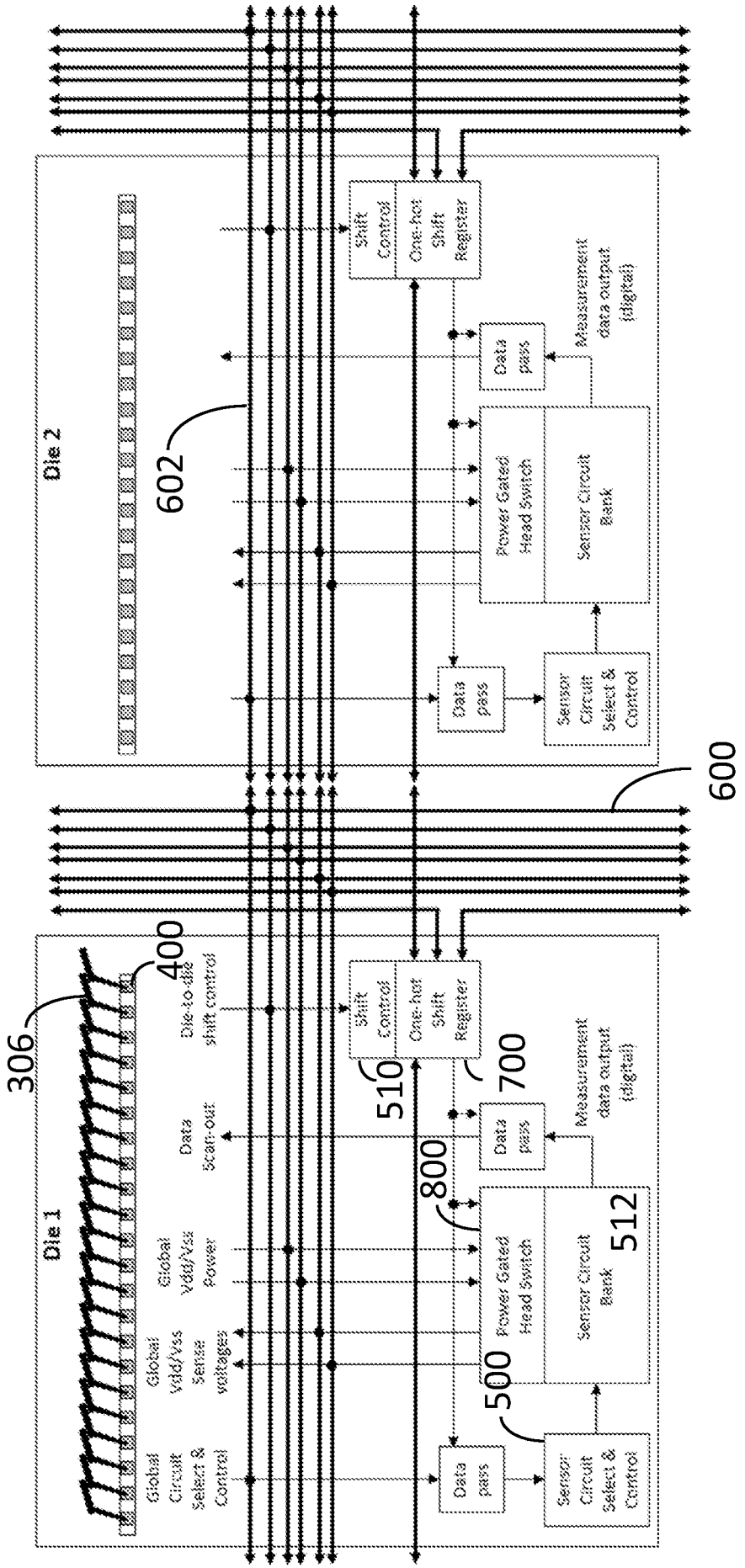
Die 2
602
Shift Control
One-hot Shift Register
Data pass
Measurement data output (digital)
Power Gated Head Switch
Sensor Circuit Bank
Sensor Circuit Select & Control
600
Die 1
306
400
Die-to-die shift control
Data Scan-out
Global Vdd/Vss Power
Global Vdd/Vss Sense voltages
Global Circuit Select & Control
510
700
800
512
500

FIG. 8

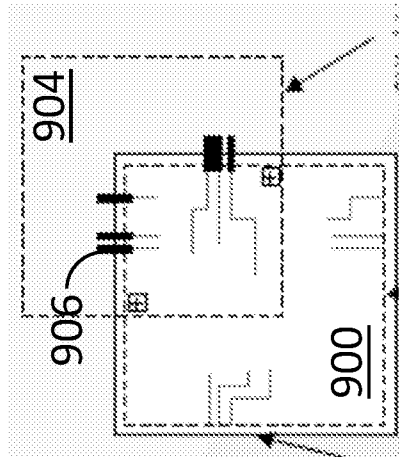

FIG. 10

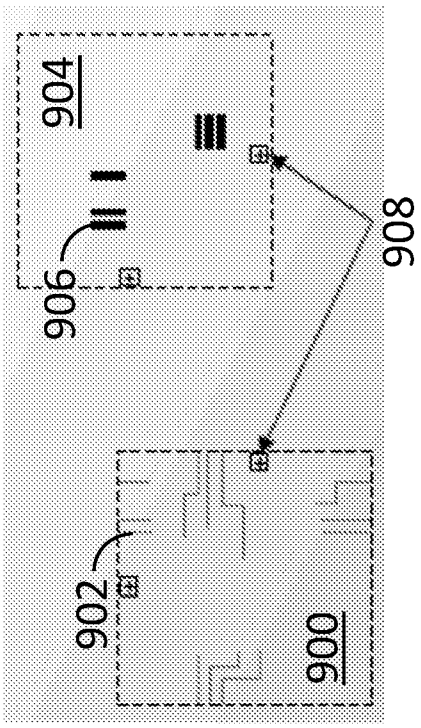

FIG. 9

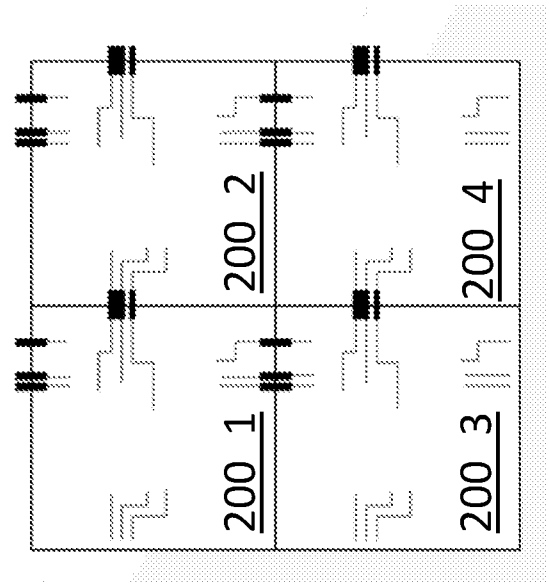

FIG. 11

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US22/34857

A. CLASSIFICATION OF SUBJECT MATTER

IPC - INV. G01R 31/3187; G01R 31/3185 (2022.01)

ADD.

CPC - INV. H01L 22/32; G01R 31/318505; G01R 31/318511; G01R 31/3187; H01L 22/34

ADD.

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

See Search History document

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

See Search History document

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

See Search History document

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X --- Y	US 2010/0237891 A1 (LIN, K. ET AL.) 23 September 2010; figures 5, 10, 11, 13A-13B, 23, 27; paragraphs [0027-0032, 0034, 0046, 0058, 0059, 0091, 0092, 0167, 0178, 0185-0186, 0215]	1-4, 6 and 8 --- 5, 7, 9-15
Y	US 2019/0157243 A1 (CEREBRAS SYSTEMS INC) 23 May 2019; figures 1, 2 and 4E-4F; paragraphs [0037, 0045, 0048, 0049 0082, 0083].	14-15
Y	US 2002/0047724 A1 (MARSHALL, A. ET AL.) 25 April 2002; figures 1 and 5A; paragraphs [0036, 0079, 0061].	5, 11
Y	US 2016/0070277 A1 (QUALCOMM INCORPORATED) 10 March 2016; figures 6 and 7A; paragraphs [0041, 0046].	7
Y	US 2020/0132757 A1 (TAIWAN SEMICONDUCTOR MANUFACTURING COMPANY, LTD) 30 April 2020; figures 6-7, 10, 11A, 11B 12-13; paragraphs [0040, 0049, 0056, 0057, 0059, 0060 0067-0069, 0071, 0072]	9-10 and 12-13
A	US 2007/0244593 A1 (EITA KINOSHITA) 18 October 2007; entire document.	1-15

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"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
31 August 2022 (31.08.2022)	SEP 21 2022
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