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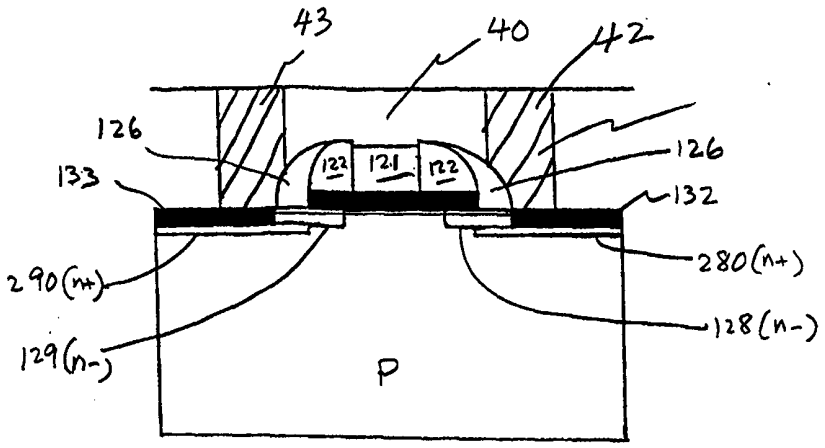
(54) Title: ULSI MOS WITH HIGH DIELECTRIC CONSTANT GATE INSULATOR



(57) Abstract

MOS transistor formed on a semiconductor substrate of a first conductivity type and method of fabrication are provided. The device includes (a) an interfacial layer formed on the substrate; (b) a high dielectric constant layer covering the interfacial layer that comprises a material that is selected from the group consisting of Ta_2O_5, $Ta_2(O_{1-x}N_x)_5$ wherein x ranges from greater than 0 to 0.6, a solid solution of $(Ta_2O_5)_r$–$(TiO_2)_{1-r}$ wherein r ranges from about 0.9 to 1, a solid solution $(Ta_2O_5)_s$–$(Al_2O_3)_{1-s}$ wherein s ranges from 0.9 to 1, a solid solution of $(Ta_2O_5)_t$–$(ZrO_2)_{1-t}$ wherein t ranges from about 0.9 to 1, a solid solution of $(Ta_2O_5)_u$–$(HfO_2)_{1-u}$ wherein u ranges from about 0.9 to 1, and mixtures thereof wherein the interfacial layer separates the high dielectric constant layer from the substrate; (c) a gate electrode having a width of less than 0.3 micron covering the high dielectric constant layer; (d) first and second lightly doped regions of a second conductivity type disposed on respective areas of the substrate surface; (e) a source and drain regions of the second conductivity type; and (f) a pair of spacers formed adjacent to the gate electrode and formed on the high dielectric constant layer. The high dielectric layer can be subject to densification. The gate oxide material will significantly improve the performance of an MOS device by reducing or eliminating the current leakage associated with prior art devices.

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ULSI MOS WITH HIGH DIELECTRIC CONSTANT GATE INSULATOR

Field of the Invention

The present invention relates generally to methods for fabricating integrated circuits using metal oxide semiconductor (MOS) technology. More particularly, the present invention relates to MOS devices with a gate width of less than 0.3 micron.

Background of the Invention

Metal oxide semiconductors are well known in the art. With the rapid integration of elements in the device, the thickness of the silicon oxide gate dielectric layer has approached the 2 nm thickness level. Such thin gate oxide layers require stringent protocols during fabrication especially in the gate etching process. In addition, concomitant with this reduction in the thickness of the gate oxide layer is the device's high leakage current caused by direct tunneling effects.

Shinriki et. al., U.S. Patent 5,292,673 describes a MOSFET that contains a tantalum pentoxide gate insulating film. Although the patent asserts that the device exhibits improved electrical characteristics, nevertheless, it is believed that the device suffers from, among other things, high leakage currents because of the silicon oxide layer, which is formed by reoxidation between the tantalum pentoxide gate insulating film and the silicon substrate, has defects including non-uniformity.

Summary of the Invention

The present invention is based in part on the recognition that employing a gate dielectric layer formed at least in part from a high dielectric constant material comprising Ta_2O_5 will significantly improve the performance of the MOS device by, among other things, reducing or eliminating the current leakage associated with prior art devices.

Accordingly, in one aspect the invention is directed to a method for fabricating an MOS device having a gate width of less than 0.3 micron that includes the steps of:

(a) forming an interfacial layer on a semiconductor substrate of a first conductive type wherein the interfacial is preferably sufficiently thin to limit parasitic capacitance of the device;

(b) forming a high dielectric constant layer on the interfacial layer that comprises a material that is selected from the group consisting of Ta_2O_5, $Ta_2(O_{1-x}N_x)_5$ wherein x ranges from greater than 0 to 0.6, a solid solution of $(Ta_2O_5)_r$-$(TiO_2)_{1-r}$ wherein r ranges from about 0.9 to 1, a solid solution $(Ta_2O_5)_s$-$(Al_2O_3)_{1-s}$ wherein s ranges from 0.9 to 1, a solid solution of $(Ta_2O_5)_t$-$(ZrO_2)_{1-t}$ wherein t ranges from about 0.9 to 1, a solid solution of $(Ta_2O_5)_u$-$(HfO_2)_{1-u}$ wherein u ranges from about 0.9 to 1, and mixtures thereof wherein the interfacial layer separates the high dielectric constant layer from the substrate;

(c) depositing a layer of electrically conductive material on the high dielectric constant layer;

(d) selectively removing portions of the layer of electrically conductive material to form a gate electrode and to expose portions of the high dielectric constant layer;

(e) implanting impurity ions through the exposed portions of the high dielectric constant layer into the substrate to form source and drain regions of a second conductive type;

(f) forming first spacers that are adjacent the gate electrode and cover portions of the source and drain regions of the second conductive type;

(g) removing the exposed portions of the high dielectric constant layer;

(h) implanting a second dose of impurity ions into the source and drain regions;

(i) depositing a layer of insulator material over the surface of the device, wherein the layer of insulator material may have an irregular surface;

(j) optionally, planarizing the surface of the insulator material;

(k) removing portions of the insulator material to form contact holes in the insulator material that are in communication with the source and drain regions; and

(l) filling the contact holes with contact material.

In preferred embodiments, the electrically conductive material comprises metal that is selected from the group consisting of TiN, W, Ta, Mo and mixtures thereof. Alternatively, the electrically conductive material comprises doped polysilicon.

In another embodiment the method includes the step of forming second spacers that are adjacent the first spacers and cover portions of the source and drain regions

following step (g) and before step (h) and/or the step of forming a silicide layer on the source and drain regions following step (h).

In another aspect, the invention is directed to an MOS transistor formed on a semiconductor substrate of a first conductivity type that includes:

(a) an interfacial layer formed on the substrate;

(b) a high dielectric constant layer covering the interfacial layer that comprises a material that is selected from the group consisting of Ta_2O_5, $Ta_2(O_{1-x}N_x)_5$ wherein x ranges from greater than 0 to 0.6, a solid solution of $(Ta_2O_5)_r$-$(TiO_2)_{1-r}$ wherein r ranges from about 0.9 to 1, a solid solution $(Ta_2O_5)_s$-$(Al_2O_3)_{1-s}$ wherein s ranges from 0.9 to 1, a solid solution of $(Ta_2O_5)_t$-$(ZrO_2)_{1-t}$ wherein t ranges from about 0.9 to 1, a solid solution of $(Ta_2O_5)_u$-$(HfO_2)_{1-u}$ wherein u ranges from about 0.9 to 1, and mixtures thereof wherein the interfacial layer separates the high dielectric constant layer from the substrate;

(c) a gate electrode having a width of less than 0.3 micron covering the high dielectric constant layer;

(d) first and second lightly doped regions of a second conductivity type disposed on respective areas of the substrate surface;

(e) a source and drain regions of the second conductivity type; and

(f) a pair of spacers formed adjacent to the gate electrode and formed on the high dielectric constant layer.

In a preferred embodiment, the MOS transistor also includes an insulator layer covering the device and defining a first contact hole that is filled with a first contact material and a second contact hole that are filled with a second contact material, wherein the insulator layer has a substantially planar surface.

Brief Description of the Drawings

Figures 1A through 1H illustrate the steps in fabricating an MOS device according to the present invention.

Detailed Description of the Preferred Embodiments

It is to be noted that "n+" and "n-" are used throughout the present disclosure. The short hand notation specifies the electron concentration of various regions of a metal-oxide-semiconductor device. For instance, "n-" specifies a region of light

electron concentration (on the order of $1x10^{18}cm^{-3}$) while "n+" specifies a region of high electron concentration (on the order of $1x10^{20}cm^{-3}$).

Figures 1A-1H illustrate an exemplary method for fabricating an integrated circuit device with the inventive process. A p type semiconductor substrate will be employed for illustrative purposes. Therefore, n- source and n- drain regions and n+source and n+ drain regions are formed in the substrate. Referring to Figure 1A, silicon substrate 100 has an interfacial layer 105 preferably comprising SiO_2, Si_3N_4, or silicon oxynitride formed on an upper surface of the substrate. The interfacial layer is formed by conventional processes, such as, for example, rapid thermal processing (RTP), thermal annealing, CVD, plasma nitridation or oxidation, or wet chemical treatment, such as immersion into boiling nitric acid. A preferred method of forming the interfacial layer comprises exposing the silicon substrate in an RF or microwave plasma in an atmosphere containing ozone, oxygen, N_2O, nitrogen, or mixtures thereof. The interfacial layer serves to prevent reaction of Ta_2O_5 in layer 110 with the silicon substrate. The interfacial layer will have a thickness that is sufficient to prevent reaction between the high dielectric constant layer and the silicon substrate and the thickness typically ranges from about 1 nm to 5 nm and preferably about 1 nm to 2 nm.

Subsequently, high dielectric constant layer 110 and electrically conductive layer 120 are formed on interfacial layer 105. The high dielectric constant layer 110 preferably comprises material that is selected from Ta_2O_5, $Ta_2(O_{1-x}N_x)_5$ wherein x preferably ranges from greater than 0 to 0.6, a solid solution of $(Ta_2O_5)_r$-$(TiO_2)_{1-r}$ wherein r preferably ranges from about 0.9 to 1, a solid solution of $(Ta_2O_5)_s$-$(Al_2O_3)_{1-s}$ wherein s preferably ranges from 0.9 to 1, a solid solution of $(Ta_2O_5)_t$-$(ZrO_2)_{1-t}$ wherein t preferably ranges from about 0.9 to 1, a solid solution of $(Ta_2O_5)_u$-$(HfO_2)_{1-u}$ wherein u ranges from about 0.9 to 1, and mixtures thereof. Typically, the high dielectric constant layer will have a thickness that ranges from about 4 nm to 12 nm and preferably from about 5 nm to 10 nm. The high dielectric constant layer will form the gate oxide layer. The particular high dielectric constant materials employed with the present invention allows for a thicker gate oxide layer to be formed, resulting in less stringent requirements on gate etching selectivity during the fabrication process. In addition, it is believed that during operation of the MOS transistors, the devices will exhibit a higher transconductance parameter. Further, since Ta has already been used in MOS fabrication, Ta_2O_5 containing gate oxides are expected to be compatible with

the materials in the other MOS materials. The high dielectric constant film can be fabricated by conventional means including, for example, LPCVD, PECVD, ECR CVD, UVCVD, and reactive sputtering.

In particular Ta_2O_5 films can be prepared by chemical vapor deposition (CVD) and physical vapor deposition (PVD) as described in Alers et al., "Nitrogen Plasma Annealing for Low Temperature Ta_2O_5 Films", Appl. Phys. Lett., Vol. 72, (11), March 1998, pages 1308-1310. $Ta_2(O_{1-x}N_x)_5$ films can be prepared by thermal CVD or plasma-assisted CVD as described in U.S. Patent 5,677,015. $(Ta_2O_5)_r$-$(TiO_2)_{1-r}$ films can be prepared by RF magnetron sputtering deposition as described in Gan et al. "Dielectric property of $(TiO_2)_x$ - $(Ta_2O_5)_{1-x}$ Thin Films", Appl. Phys. Lett. Vol. 72, (3), January 1998, pages 332-334 or by chemical CVD as described in U.S. Patent 4,734,340. $(Ta_2O_5)_s$-$(Al_2O_3)_{1-s}$ films can be prepared by metalorganic solution deposition as described in Joshi et al., "Structural and electrical properties of crystalline $(1-x)Ta_2O_5$-xAl_2O_3 thin films fabricated by metalorganic solution deposition technique", Appl. Phys. Lett. Vol. 71, (10), September 1997. Each of the above cited references is incorporated herein. Finally, the $(Ta_2O_5)_t$-$(ZrO_2)_{1-t}$ and $(Ta_2O_5)_u$-$(HfO_2)_{1-u}$ thin films can be fabricated by techniques used in fabricating the other solid solution materials. Prior to formation of the electrically conductive layer 120, the high dielectric constant material is preferably subjected to a densification process comprising, for example, exposing the silicon substrate to a RTP or an RF or microwave plasma in an atmosphere containing ozone, oxygen, N_2O, nitrogen, or mixtures thereof. Densification is further described in Alers et. al. cited above. Densification improves the high dielectric constant material with respect to the leakage current of the MOS device made.

Electrically conductive layer 120 preferably comprises one or more layers of a high melting metal such as, for example, TiN, W, Ta, Mo which can be deposited by sputtering. This layer typically has a thickness that ranges from about 100 nm to 300 nm, and preferably from about 150 nm to 250 nm. As will be described herein, this electrically conductive layer will form the gate electrode in this embodiment.

An optional oxide layer can be deposited and patterned over the electrically conductive layer 120. Subsequently, a layer of photoresist material 160 is applied onto electrically conductive layer 120 before the photoresist is masked and patterned using conventional photoresist techniques to form a gate pattern. After etching, the line width (L) of the gate 121 is typically less than 0.3 micron, and preferably equal to or less than

about 0.18 micron. Etching down to the top high dielectric constant layer 110 removes the exposed electrically conductive material as shown in Figure 1B. Source 190 and drain 180 regions are formed by self aligned ion implantation before the remaining photoresist material 160A is removed to form the device shown in Figure 1C. As is apparent, interfacial layer 105 shown in Figures 1A and 1B is not shown in Figure 1C or subsequent figures although the layer is present in the structures illustrated.

Referring to Figure 1D, spacers 122 are formed by depositing a phosphosilicate glass (PSG) film 124 over the entire surface of the device of Figure 1C and then anisotropic etching the glass. The spacers can also be made from oxides or nitrides. Subsequently, the exposed high dielectric constant material is removed by plasma etching using fluorine or chlorine containing etchant gases to yield the structure of Figure 1E. The remaining layer of high dielectric material 115 serves as the gate oxide. Second spacers 126 are formed by the same procedure as for spacers 122. Lightly doped source (n-) 129 and drain (n-) 128 regions are then formed by ion implantation as shown in Figure 1F with the concomitant formation of source (n+) 290 and drain (n+) 280 regions.

Silicide layers 133 and 132 are then formed on the source and drain regions. One method comprises the steps of (1) depositing a layer of suitable metal preferably titanium, cobalt, or multiple layers of these metals, over the surface of the device of Figure 1F, (2) allowing the metal and silicon in the substrate to react, and thereafter (3) removing unreacted metal. Another method comprises depositing silicide, e.g., $metal_xSi_y$, directly onto source and drain regions using conventional selective deposition techniques, e.g., CVD.

Following formation of the silicide regions, a conformal layer of PSG film 40 is deposited on the structure of Figure 1G, thereafter, the top surface of the PSG film is planarized by conventional techniques such as chemical-mechanical polishing (CMP). CMP is particularly advantageous when small contact holes (less than 0.3 micron) are required. Subsequently, contact holes are etched in the PSG and they then filled with an electrically conductive, e.g., metal, material 42 and 43 as shown in Fig. 1H.

As is apparent, the above structure has a metal gate electrode 121. In an alternative embodiment, instead of a metal gate electrode, a doped polysilicon gate electrode can be employed. In this case, a doped polysilicon layer would be deposited in place of the electrically conductive 120 layer as shown in Figure 1A. Optionally, a

diffusion barrier layer made from a suitable material such as, for example, TiN, WN, and TaN, can be deposited between layers 110 and 120. This barrier layer, which is typically 5 nm to 15 nm thick, prevents polysilicon gate material from reacting with the tantalum pentoxide in the gate dielectric. In this scenario, the rest of the process would be essentially the same as above, however, the preferred silicidation procedure entails depositing a metal film over the structure so that a polycide layer on the surface of the doped polysilicon layer is formed as well.

It is to be emphasized that although n channel transistors have been described in detail herein, the present invention may also be practiced as a p channel transistor. In fabricating the p channel device, the doping conductives of the p channel device are simply opposite to those of the n channel device.

Although only preferred embodiments of the invention are specifically disclosed and described above, it will be appreciated that many modifications and variations of the present invention are possible in light of the above teachings and within the purview of the appended claims without departing from the spirit and intended scope of the invention.

CLAIMS:

1. A method for fabricating a MOS device having a gate width of less than 0.3 micron that comprises the steps of:

(a) forming an interfacial layer on a semiconductor substrate of a first conductivity type;

(b) forming a high dielectric constant layer on the interfacial layer that comprises a material that is selected from the group consisting of Ta_2O_5, $Ta_2(O_{1-x}N_x)_5$ wherein x ranges from greater 0 to 0.6, a solid solution of $(Ta_2O_5)_r$-$(TiO_2)_{1-r}$ wherein r ranges from about 0.9 to 1, a solid solution $(Ta_2O_5)_s$-$(Al_2O_3)_{1-s}$ wherein s ranges from 0.9 to 1, a solid solution of $(Ta_2O_5)_t$-$(ZrO_2)_{1-t}$ wherein t ranges from about 0.9 to 1, a solid solution of $(Ta_2O_5)_u$-$(HfO_2)_{1-u}$ wherein u ranges from about 0.9 to 1, and mixtures thereof wherein the interfacial layer separates the high dielectric constant layer from the substrate;

(c) depositing a layer of electrically conductive material on the high dielectric constant layer;

(d) selectively removing portions of the layer of electrically conductive material to form a gate electrode and to expose portions of the high dielectric constant layer;

(e) implanting impurity ions through the exposed portions of the high dielectric constant layer into the substrate to form source and drain regions of a second conductivity type;

(f) forming first spacers that are adjacent the gate electrode and cover portions of the source and drain regions of the second conductivity type;

(g) removing the exposed portions of the high dielectric constant layer;

(h) implanting a second dose of impurity ions into the source and drain regions;

(i) depositing a layer of insulator material over the surface of the device;

(j) optionally, planarizing the surface of the insulator material;

(k) removing portions of the insulator material to form contact holes in the insulator material that are in communication with the source and drain regions; and

(l) filling the contact holes with contact material.

2. The method of claim 1 comprising the step of densifying the high dielectric constant layer.

3. The method of claim 1 wherein the electrically conductive material comprises metal that is selected from the group consisting of TiN, W, Ta, Mo and multilayers thereof.

4. The method of claim 1 wherein the electrically conductive material comprises doped polysilicon.

5. The method of claim 4 further comprising the step of forming a barrier layer between the electrically conductive material and the high dielectric constant layer.

6. The method of claim 1 further comprising the step of forming second spacers that are adjacent the first spacers and cover portions of the source and drain regions following step (g) and before step (h).

7. The method of claim 1 further comprising the step of forming a silicide layer on the source and drain regions following step (h).

8. The method of claim 7 wherein forming the silicide layer comprises the steps of:

depositing a layer of metal over the at least the source and drain regions;

heating the layer of metal to cause the metal to react with the silicon on the surface of the source and drain regions to form metal silicide layers in the source and drain regions; and

removing unreacted metal from the layer of metal.

9. The method of claim 7 wherein forming the silicide layer comprises selectively depositing silicide over the source and drain regions.

10. The method of claim 1 wherein the high dielectric constant material layer has a thickness that ranges from about 4 nm to 12 nm.

11. The method of claim 1 wherein the interfacial layer comprises silicon oxide, silicon nitride, or silicon oxynitride.

12. The method of claim 1 wherein step (h) comprises introducing a light dosage of impurities to form lightly doped source and drain regions.

13. The method of claim 1 wherein the high dielectric constant material is Ta_2O_5.

14. The method of claim 1 wherein the high dielectric constant material is $Ta_2(O_{1-x}N_x)_5$ wherein x ranges from greater than 0 to 0.6.

15. The method of claim 1 wherein the high dielectric constant material is a solid solution $(Ta_2O_5)_r$-$(TiO_2)_{1-r}$ wherein r preferably ranges from about 0.9 to 1.

16. The method of claim 1 wherein the high dielectric constant material is a solid solution $(Ta_2O_5)_s$-$(Al_2O_3)_{1-s}$ wherein s ranges from 0.9 to 1.

17. The method of claim 1 wherein the high dielectric constant material is a solid solution $(Ta_2O_5)_t$-$(ZrO_2)_{1-t}$ wherein t ranges from about 0.9 to 1.

18. The method of claim 1 wherein the high dielectric constant material is a solid solution of $(Ta_2O_5)_u$-$(HfO_2)_{1-u}$ wherein u ranges from about 0.9 to 1.

19. The method of claim 1 wherein the substrate comprises silicon.

20. The method of claim 1 wherein the first spacers comprise an oxide or nitride material.

21. The method of claim 1 wherein step (i) comprises depositing a conformal layer of insulator material and (j) planarizes the surface of the insulator material by chemical mechanical planarization.

22. An MOS transistor formed on a semiconductor substrate of a first conductivity type comprising:

(a) an interfacial layer formed on the substrate;

(b) a high dielectric constant layer covering the interfacial layer that comprises a material that is selected from the group consisting of Ta_2O_5, $Ta_2(O_{1-x}N_x)_5$ wherein x ranges from greater than 0 to 0.6, a solid solution of $(Ta_2O_5)_r$-$(TiO_2)_{1-r}$ wherein r ranges from about 0.9 to 1, a solid solution $(Ta_2O_5)_s$-$(Al_2O_3)_{1-s}$ wherein s ranges from 0.9 to 1, a solid solution of $(Ta_2O_5)_t$-$(ZrO_2)_{1-t}$ wherein t ranges from about 0.9 to 1, a solid solution of $(Ta_2O_5)_u$-$(HfO_2)_{1-u}$ wherein u ranges from about 0.9 to 1, and mixtures thereof wherein the interfacial layer separates the high dielectric constant layer from the substrate;

(c) a gate electrode having a width of less than 0.3 micron covering the high dielectric constant layer;

(d) first and second lightly doped regions of a second conductivity type disposed on respective areas of the substrate surface;

(e) a source and drain regions of a second conductivity type; and

(f) a pair of spacers formed adjacent to the gate electrode and formed on the high dielectric constant layer.

23. The MOS transistor of claim 22 comprising:

(g) an insulator layer covering the device and defining a first contact hole that is filled with a first contact material and a second contact hole that are filled with a second contact material, wherein the insulator layer has a substantially planar surface.

24. The MOS transistor of claim 22 wherein the gate electrode is formed from a metal that is selected from the group consisting of TiN, W, Ta, MO and multilayers thereof.

25. The MOS transistor claim 22 wherein the gate electrode comprises doped polysilicon.

26. The MOS transistor of claim 25 comprising a barrier layer between the gate electrode and the high dielectric constant layer.

27. The MOS transistor of claim 22 comprising a pair of second spacers that are adjacent to the first spacers and formed on the lightly doped regions.

28. The MOS transistor of claim 22 comprising a silicide layer on the source and drain regions.

29. The MOS transistor of claim 22 wherein the high dielectric constant material layer has a thickness that ranges from about 4 nm to 12 nm.

30. The MOS transistor of claim 22 wherein the high dielectric constant material is Ta_2O_5.

31. The MOS transistor of claim 22 wherein the high dielectric constant material is $Ta_2(O_{1-x}N_x)_5$ wherein x ranges from 0 to 0.6.

32. The MOS transistor of claim 22 herein the high dielectric constant material is a solid solution of $(Ta_2O_5)_r$-$(TiO_2)_{1-r}$ wherein r preferably ranges from about 0.9 to 1.

33. The MOS transistor of claim 22 wherein the high dielectric constant material is a solid solution $(Ta_2O_5)_s$-$(Al_2O_3)_{1-s}$ wherein s ranges from 0.9 to 1.

34. The MOS transistor of claim 22 wherein the high dielectric constant material is a solid solution $(Ta_2O_5)_t$-$(ZrO_2)_{1-t}$ wherein t ranges from about 0.9 to 1.

35. The MOS transistor of claim 22 wherein the high dielectric constant material is a solid solution of $(Ta_2O_5)_u$-$(HfO_2)_{1-u}$ wherein u ranges from about 0.9 to 1.

36. The MOS transistor of claim 22 wherein the substrate comprises silicon.

37. The MOS transistor of claim 22 wherein the first spacers comprise an oxide or nitride material.

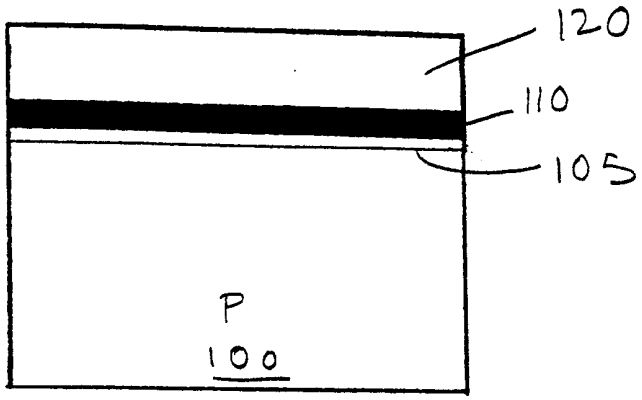

FIG. 1A

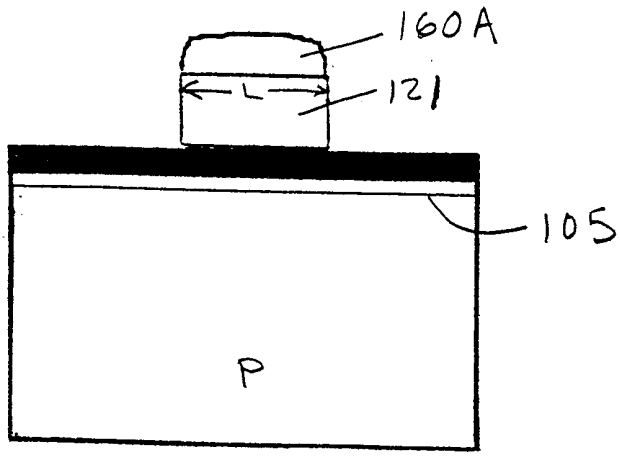

FIG. 1B

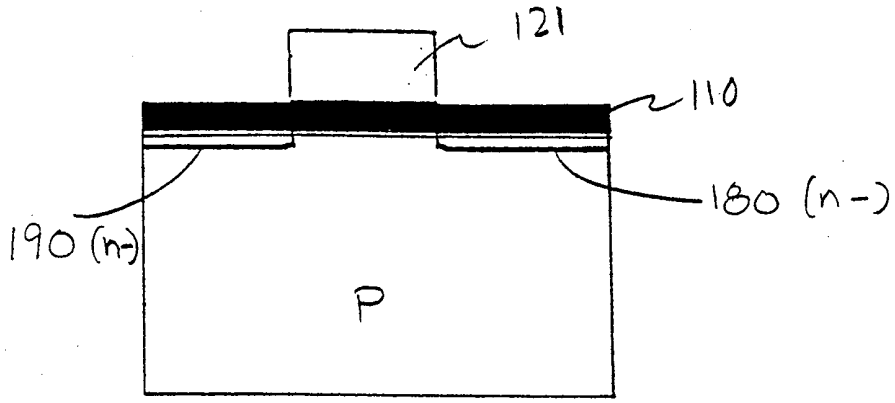

FIG. 1C

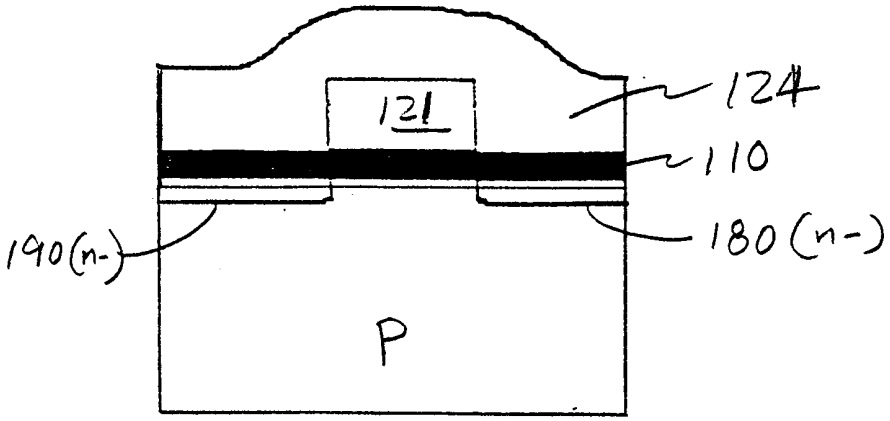

FIG. 1D

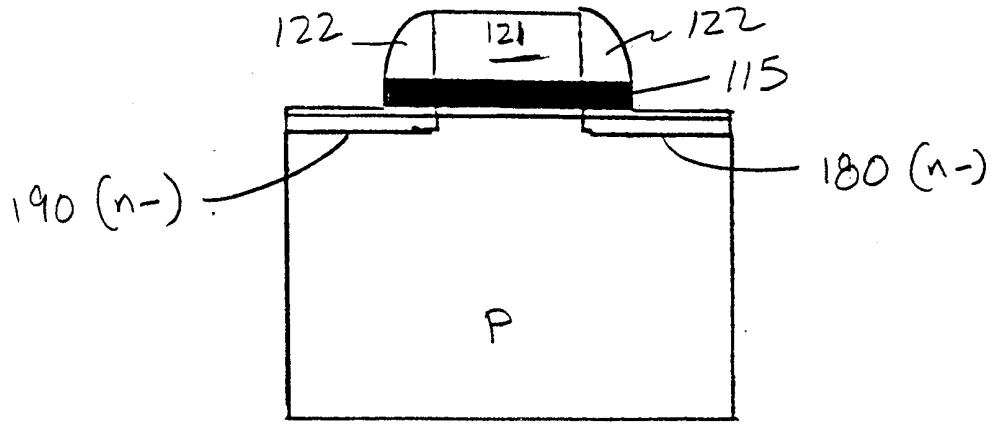
122
121
122
115
190 (n-)
180 (n-)
P

FIG. 1E

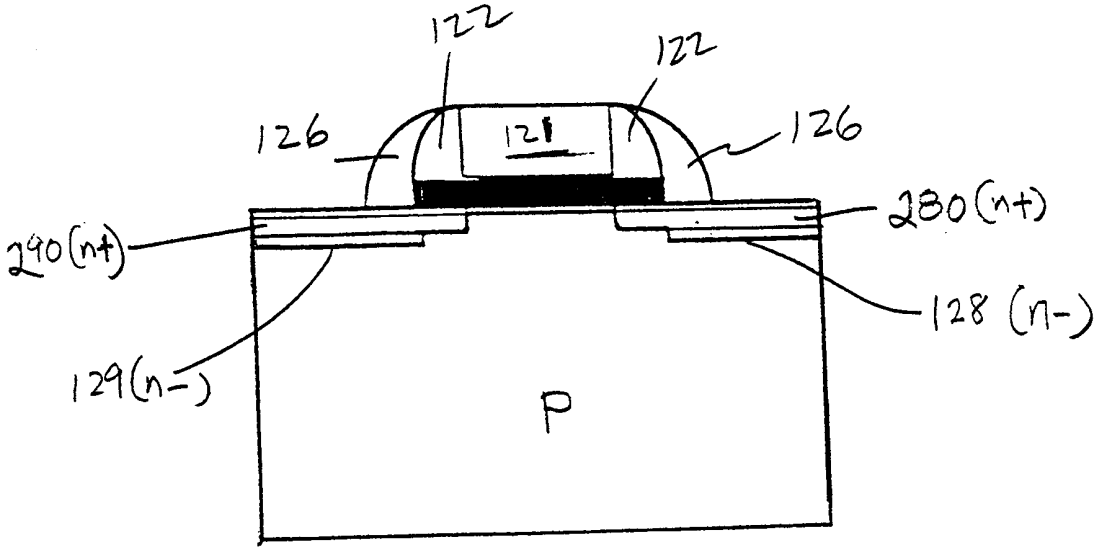
122
122
126
121
126
280(n+)
290(n+)
128 (n-)
129(n-)
P

FIG. 1F

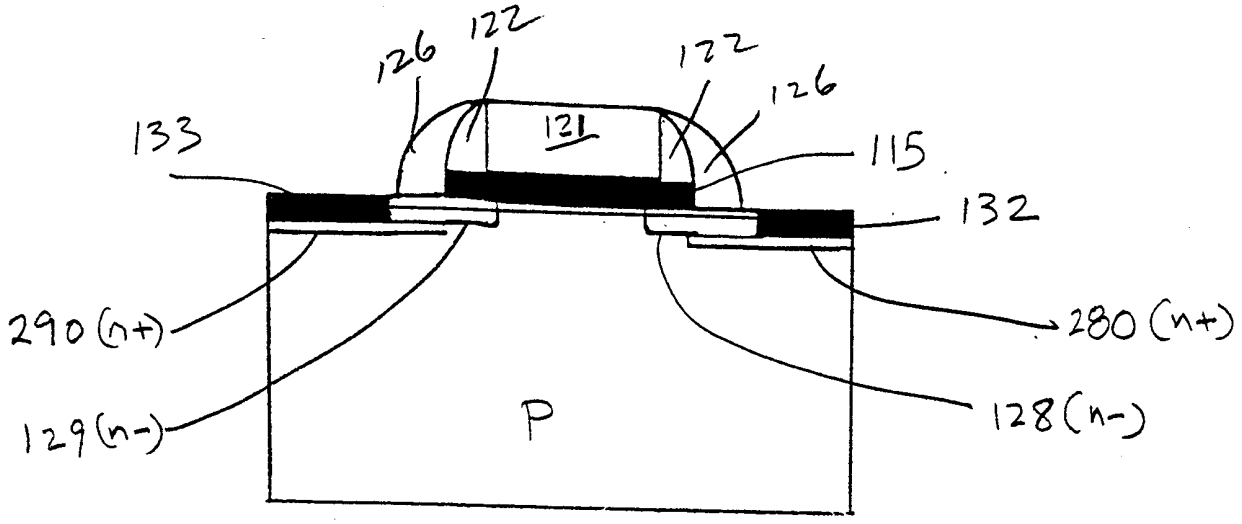
126
122
122
126
133
121
115
132
290 (n+)
280 (n+)
129 (n-)
128 (n-)
P

FIG. 1G

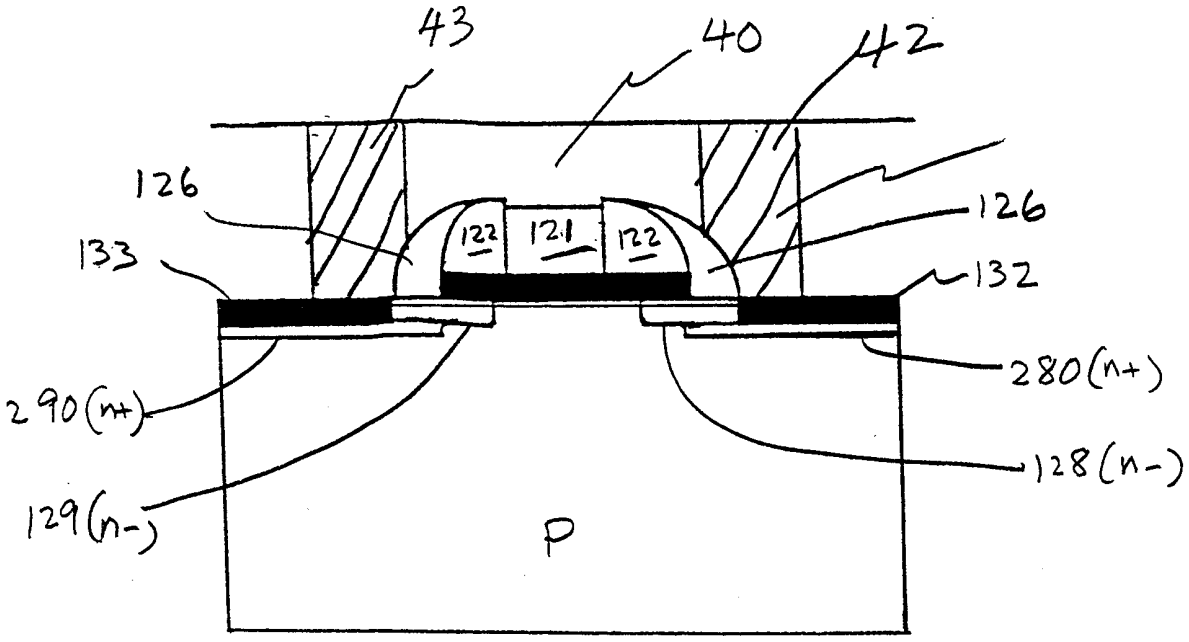
43
40
42
126
126
133
122
121
122
132
290 (n+)
280 (n+)
128 (n-)
129 (n-)
P

FIG. 1H

INTERNATIONAL SEARCH REPORT

International Application No
PCT/US 99/13787

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 H01L21/336 H01L29/51 H01L29/78

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 5 292 673 A (SHINRIKI HIROSHI ET AL) 8 March 1994 (1994-03-08) cited in the application figures 6-9 column 2, line 3 - line 9 column 3, line 41 -column 4, line 5 column 4, line 25 - line 65 column 5, line 9 - line 11 column 5, line 22 -column 7, line 19	22, 24-27, 29,30, 36,37
A		1,3-6, 10,11, 13,19,20

-/--

[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

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"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

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"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

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"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
30 September 1999	15/10/1999

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax: (+31-70) 340-3016	Polesello, P

1

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C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
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P,A	abstract; figures 1-6	1,11,13, 19

A	EP 0 844 647 A (TEXAS INSTRUMENTS INC) 27 May 1998 (1998-05-27) figure 2 column 2, line 7 - line 12 column 2, line 50 -column 3, line 54	1,4,5, 10-12, 19,20, 22,25, 26,36,37

A	US 5 596 214 A (ENDO NOBUHIRO) 21 January 1997 (1997-01-21) figures 3,5,7,9 column 14, line 48 -column 15, line 27 column 16, line 63 -column 17, line 11 column 18, line 45 -column 19, line 12	1,3,11, 13,19, 22-24, 30,36

A	US 3 731 163 A (SHUSKUS A) 1 May 1973 (1973-05-01) figure 1 column 3, line 61 -column 4, line 30	1-4,11, 13-19, 22,24, 25,30-36

A	US 5 702 972 A (HSU SHUN-LIANG ET AL) 30 December 1997 (1997-12-30) figures 2-7,9 column 2, line 35 -column 4, line 4	1,4,6-9, 11,12, 19-23, 25,27, 28,36,37

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A	PRATT I H: "Thin-film dielectric properties of r.f. sputtered oxides" SOLID STATE TECHNOLOGY, DEC. 1969, USA, vol. 12, no. 12, pages 49-57, XP002117110 ISSN: 0038-111X page 53, column 2, line 5 -page 55, column 2, line 28 tables II-III figure 10	1,13,16, 18,22, 30,33,35

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C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	REDDY P K ET AL: "Dielectric properties of tantalum oxynitride films. (Thin film capacitors for hybrid integrated circuits)" PHYSICA STATUS SOLIDI A, 16 JULY 1979, EAST GERMANY, vol. 54, no. 1, pages K63-K66, XP002117111 ISSN: 0031-8965 page K63, line 23 -page K65, line 16 figure 2 ---	1,14,22, 31
A	GAN J -Y ET AL: "Dielectric property of (TiO/sub 2/)/sub x/-(Ta/sub 2/O/sub 5/)/sub 1-x/ thin films" APPLIED PHYSICS LETTERS, 19 JAN. 1998, AIP, USA, vol. 72, no. 3, pages 332-334, XP002116551 ISSN: 0003-6951 cited in the application * the whole document * ---	1,2,15, 22,31
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International Application No
PCT/US 99/13787

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document, with indication,where appropriate, of the relevant passages	Relevant to claim No.
A	ALERS G B ET AL: "Nitrogen plasma annealing for low temperature Ta/sub 2/O/sub 5/ films" APPLIED PHYSICS LETTERS, 16 MARCH 1998, AIP, USA, vol. 72, no. 11, pages 1308-1310, XP002116553 ISSN: 0003-6951 cited in the application page 1308, column 1, line 13 - line 29	2

1

INTERNATIONAL SEARCH REPORT

Information on patent family members

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PCT/US 99/13787

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		JP 3074878 A	29-03-1991
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