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(54) **PRINTED CIRCUIT BOARD AND MANUFACTURING METHOD THEREFOR**

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(52) **U.S. Cl.** **361/748**

(57) **ABSTRACT**

A printed circuit board of a card edge connector type includes interconnections formed on a surface of a substrate to be electrically coupled to respective connecting terminals formed by electrolytic plating on an edge of the substrate, and connecting terminal-forming wirings being respectively in connection with the interconnections, when the connecting terminals are formed by the electrolytic plating. The interconnections are electrically isolated from the connecting terminal-forming wirings by process openings formed in the substrate.

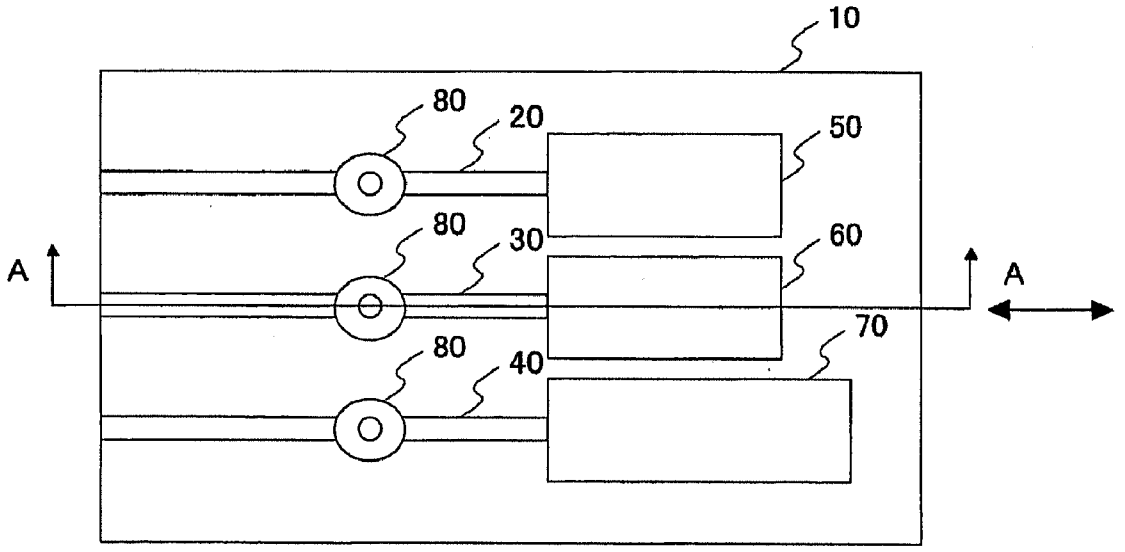


FIG. 1A

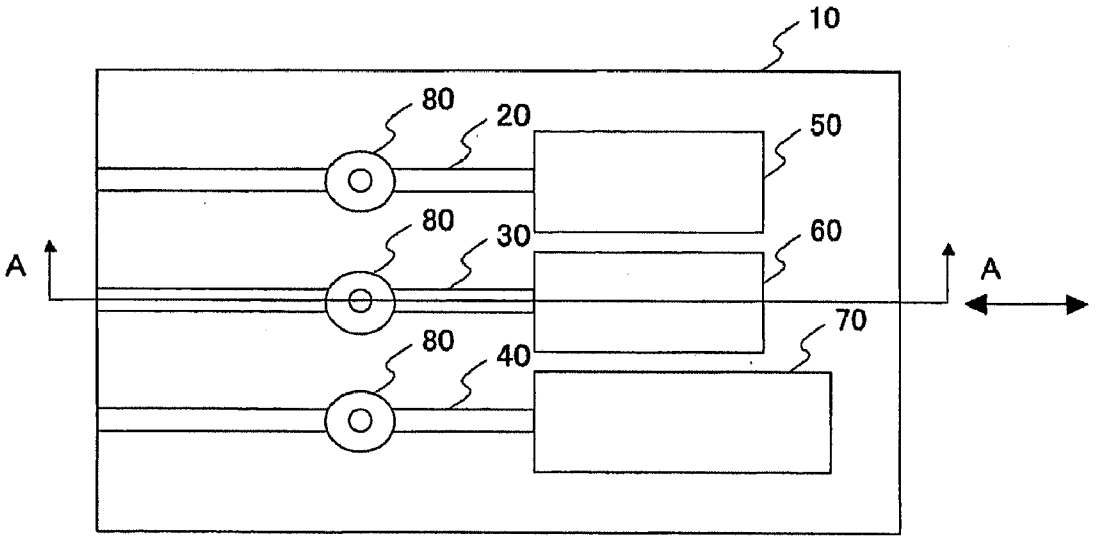


FIG. 1B

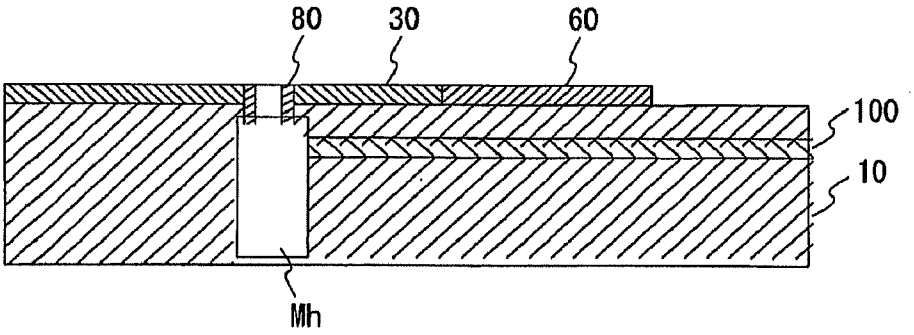


FIG. 2

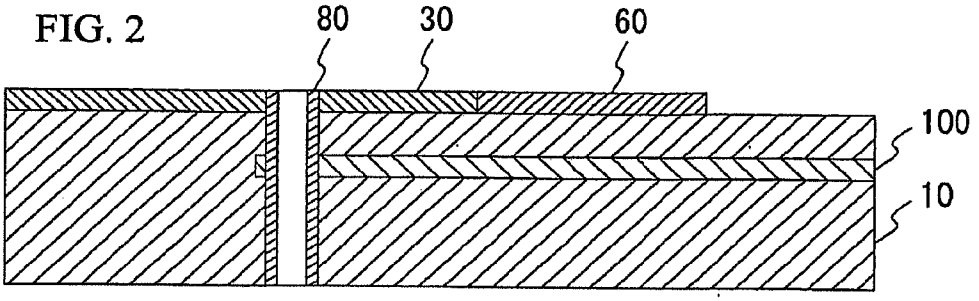


FIG. 3A

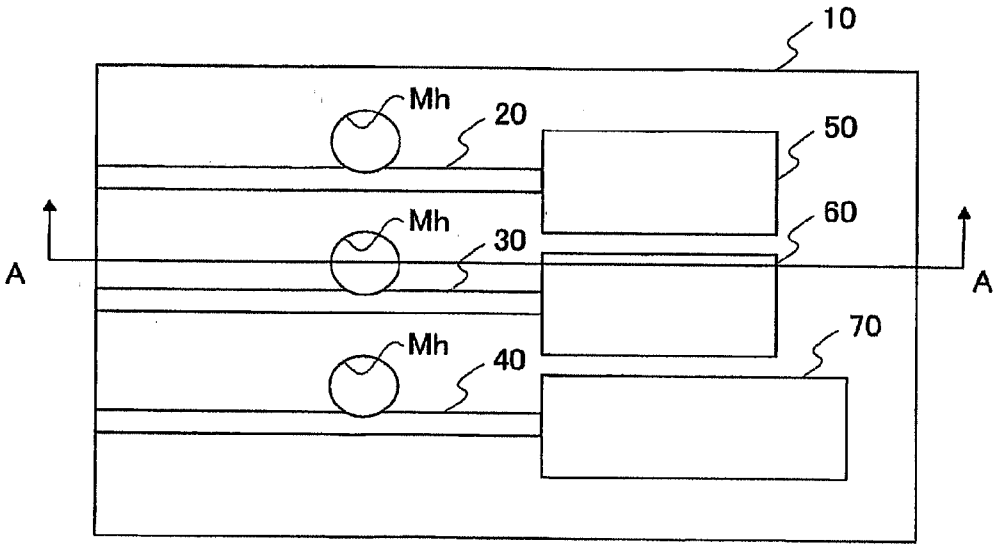


FIG. 3B

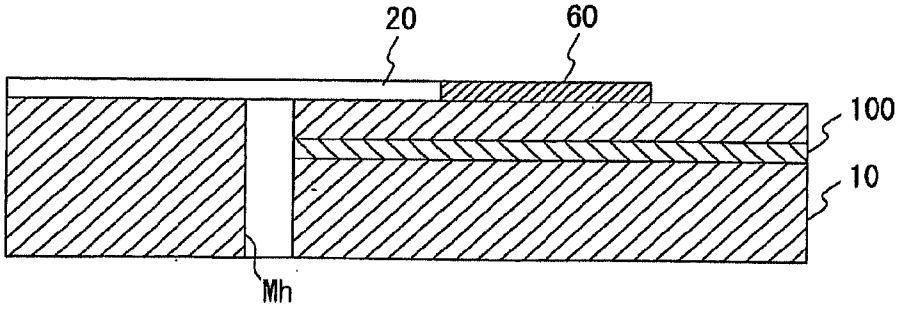


FIG. 4A

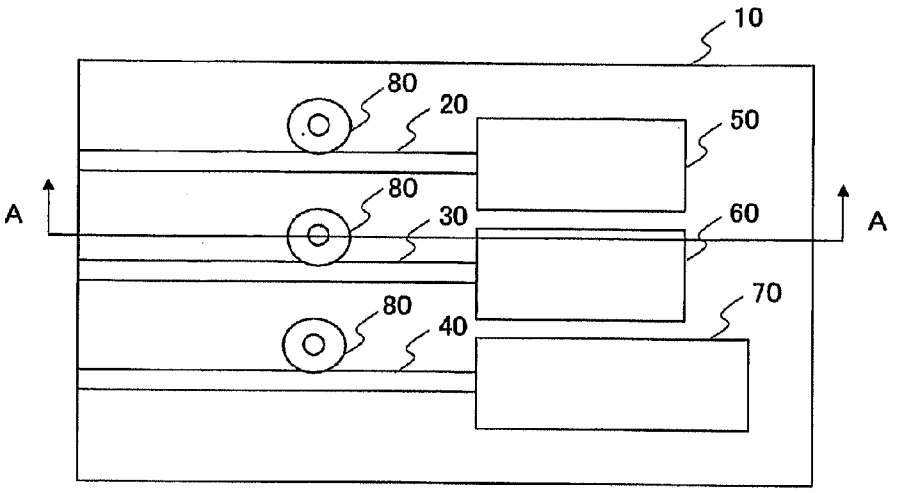


FIG. 4B

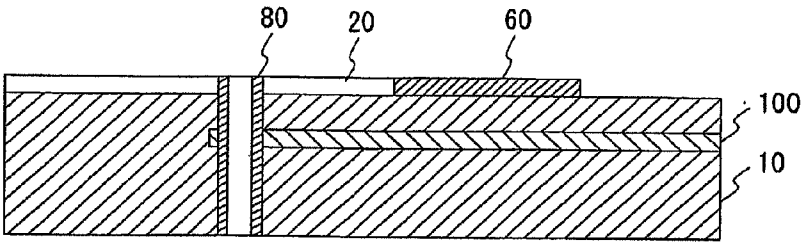


FIG. 5A

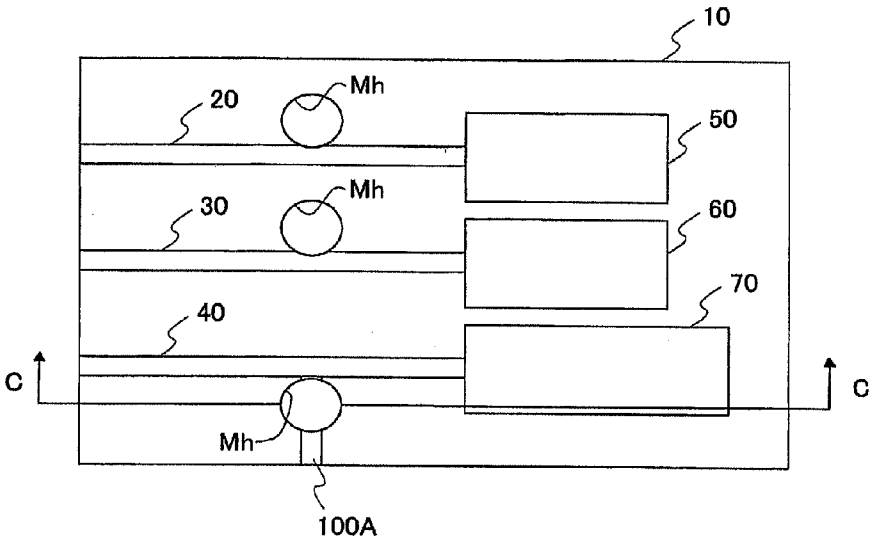


FIG. 5B

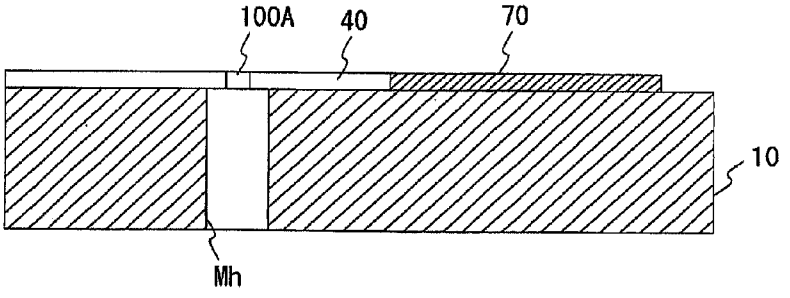


FIG. 6

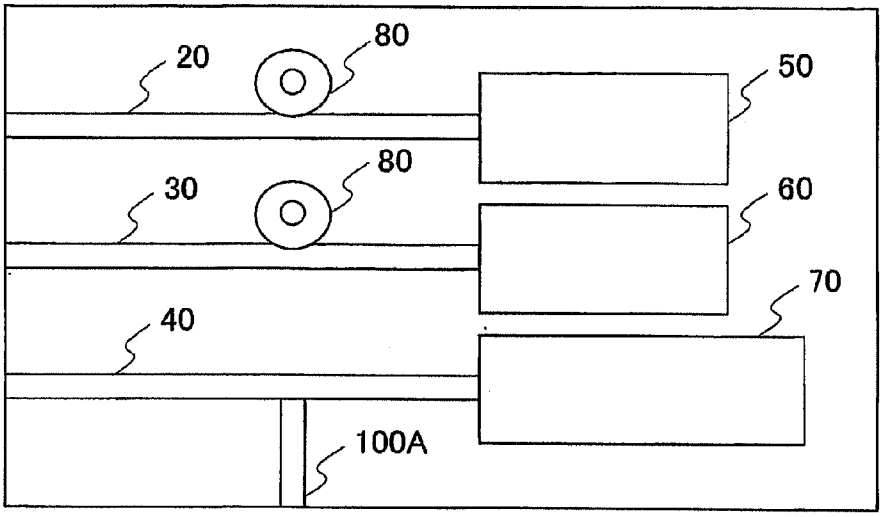


FIG. 7

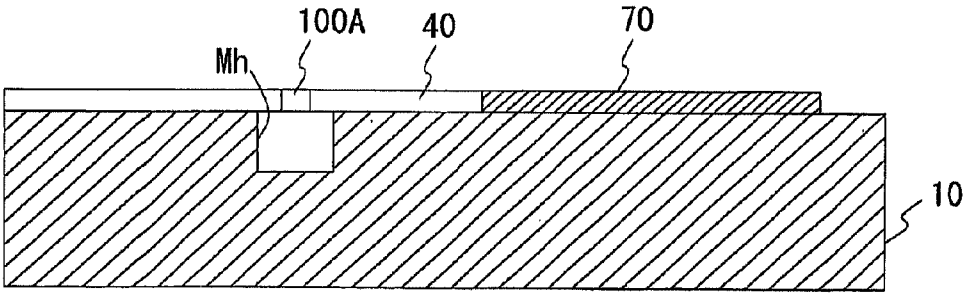


FIG. 8A

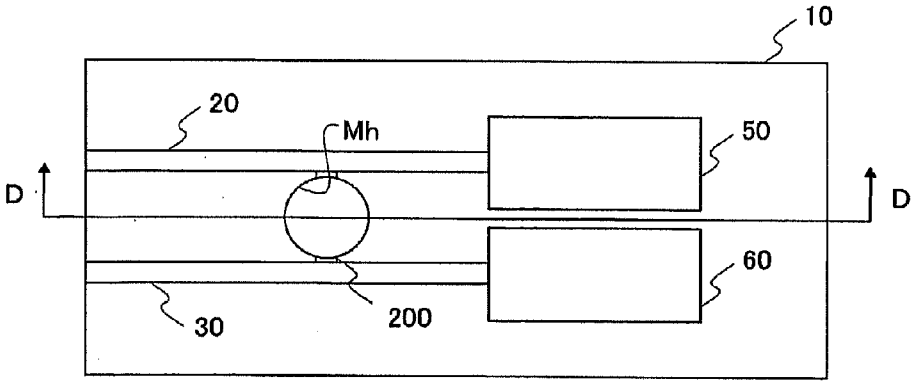


FIG. 8B

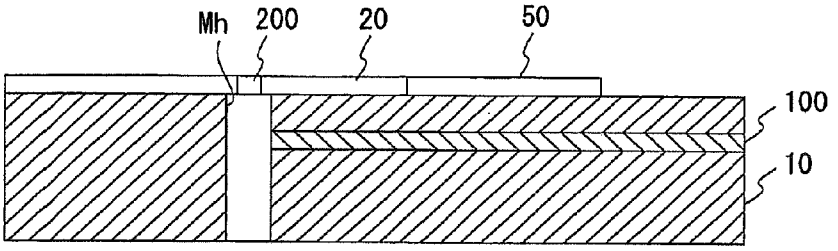


FIG. 9A

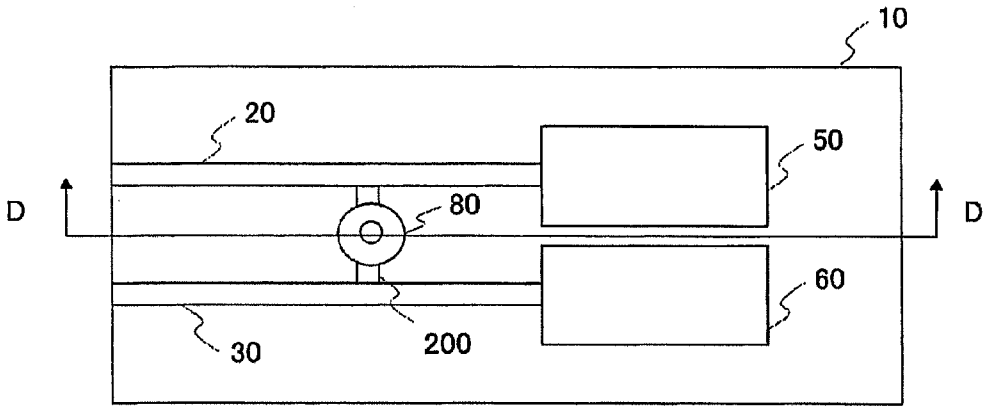


FIG. 9B

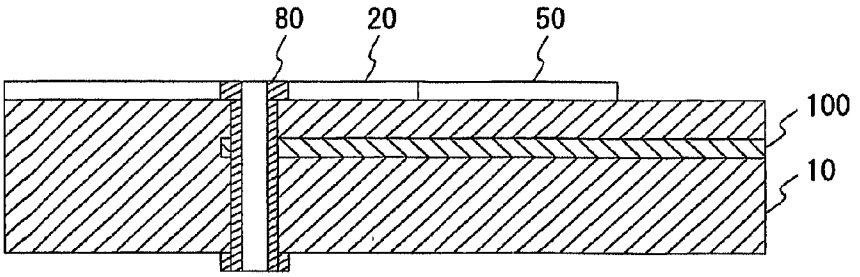


FIG. 10A

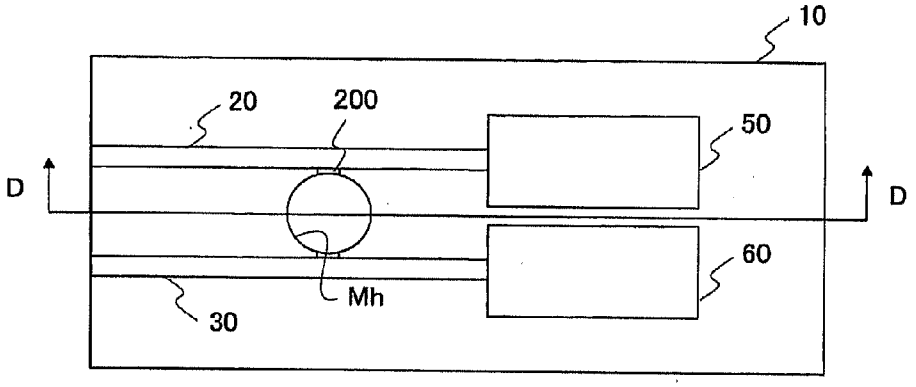


FIG. 10B

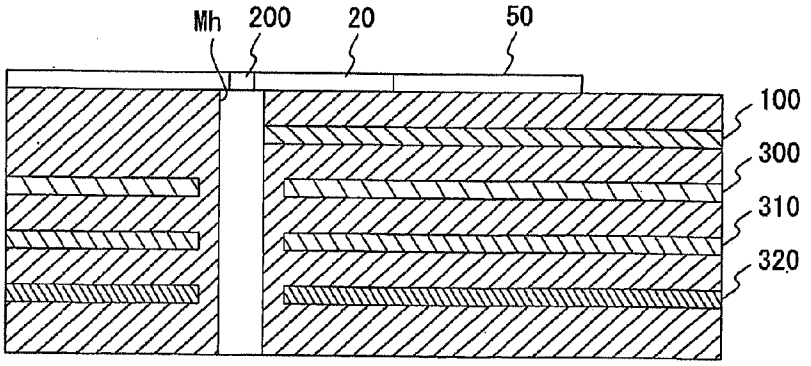


FIG. 11A

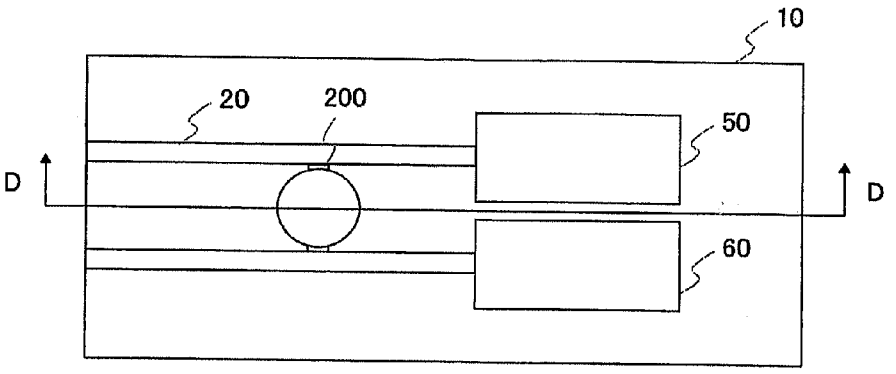
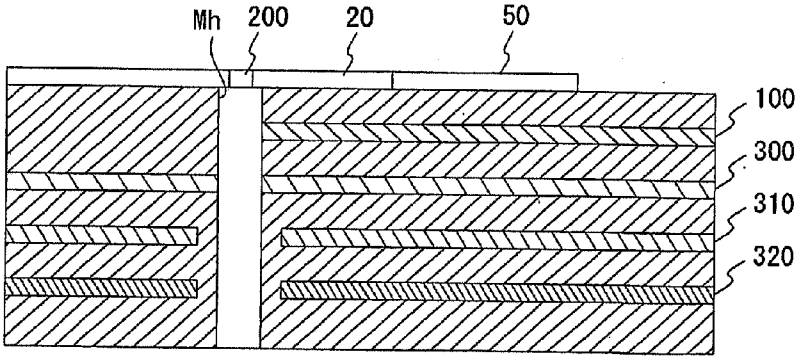


FIG. 11B



PRINTED CIRCUIT BOARD AND MANUFACTURING METHOD THEREFOR

CROSS REFERENCE TO RELATED APPLICATIONS

[0001] This application is a divisional of and claims priority to U.S. patent application Ser. No. 12/617,171, filed on Nov. 12, 2009, now pending, which is a divisional of U.S. patent application Ser. No. 11/487,979, filed on Jul. 18, 2006, now U.S. Pat. No. 7,638,715, the contents of both of which are hereby incorporated by reference.

BACKGROUND OF THE INVENTION

[0002] 1. Field of the Invention

[0003] This invention generally relates to a printed circuit board of a card edge connector type and a manufacturing method therefor.

[0004] 2. Description of the Related Art

[0005] A card edge connector type of printed circuit board is known, as disclosed, for example, in Japanese Patent application Publication No. 2005-26020. This printed circuit board of the card edge connector type includes multiple connecting terminals formed on one end of the printed circuit board, and is inserted into or pulled out of a corresponding connector. The above-described card edge connector type of printed circuit board is configured in such a manner that distances from a card edge to the connecting terminals are selectively varied in order to adjust touch timings between the respective connecting terminals and corresponding contacts on the connector, when a card edge portion is inserted into the connector.

[0006] In a case where the above-described connecting terminals that can adjust the touch timings with the connector are formed by electrolytic gold plating, connecting terminal-forming wirings are needed for forming the connecting terminals. However, when the connecting terminal-forming wirings are arranged between the card edge and the connecting terminals, there is the possibility that the function of adjusting the touch timings cannot be assured. Accordingly, the connecting terminal-forming wirings have to be coupled respectively to the connecting terminals through signal lines connected to the connecting terminals.

[0007] Meanwhile, if the circuit is operated with the connecting terminal-forming wirings respectively coupled to the signal lines, this causes impedance mismatching or signal transmission loss. In particular, in a case where the connecting terminal-forming wirings are connected to the signal lines that transmits high-speed signals of as high as GHz band.

SUMMARY OF THE INVENTION

[0008] The present invention has been made in view of the above circumstances and provides a printed circuit board and a manufacturing method therefor, in which it is possible to eliminate the influence on the circuit characteristics of connecting terminal-forming wirings respectively connected to signal lines or the like so as to form connecting terminals by electrolytic plating on a printed circuit board of a card edge connector type.

[0009] According to one aspect of the present invention, there is provided a printed circuit board of a card edge connector type including: interconnections formed on a surface of a substrate to be electrically coupled to respective connecting terminals formed by electrolytic plating on an edge of the substrate; and connecting terminal-forming wirings being respectively in connection with the interconnections, when the connecting terminals are formed by the electrolytic plating. The interconnections are electrically isolated from the connecting terminal-forming wirings by process openings formed in the substrate. With the above-described configuration, the process openings are formed after the interconnections and the connecting-terminal forming wirings are respectively coupled. Thus, the interconnections and the connecting-terminal forming wirings can be isolated electrically, thereby eliminating the influence on the circuit characteristics of the connecting terminal-forming wirings with ease.

[0010] According to another aspect of the present invention, there is provided a printed circuit board of a card edge connector type including: two interconnections formed in parallel on a surface of a substrate to be electrically coupled to respective connecting terminals formed by electrolytic plating on an edge of the substrate; and a connecting terminal-forming wiring being commonly in connection with the two interconnections, when the connecting terminals are formed by the electrolytic plating. The two interconnections are electrically isolated from the connecting terminal-forming wiring by a process opening formed in the substrate, the process opening being commonly connected to the two interconnections. With the above-described configuration, the connecting terminal-forming wiring can be commonly provided to the two interconnections.

[0011] According to still another aspect of the present invention, there is provided a manufacturing method of a printed circuit board of a card edge connector type including: forming interconnections and connecting terminal-forming wirings by electrolytic plating before connecting terminals are formed by electrolytic plating on an edge of a substrate, so that the interconnections are respectively connected to connecting terminals and the connecting terminal-forming wirings are respectively connected to the interconnections; and forming process openings in the substrate to electrically isolate the interconnections from the connecting terminal-forming wirings.

BRIEF DESCRIPTION OF THE DRAWINGS

[0012] Preferred embodiments of the present invention will be described in detail with reference to the following drawings, wherein:

[0013] FIG. **1**A is a top view illustrating a configuration of a printer circuit board in accordance with an exemplary embodiment of the present invention;

[0014] FIG. **1**B is a cross-sectional view taken along a line A-A shown in FIG. **1**A;

[0015] FIG. **2** is a cross-sectional view showing a state before process openings are formed on the printed circuit board;

[0016] FIG. **3**A is a top view illustrating a configuration of the printed circuit board in accordance with another exemplary embodiment of the present invention;

[0017] FIG. **3**B is a cross-sectional view taken along a line A-A shown in FIG. **3**A;

[0018] FIG. **4**A is a top view showing a state before process openings are formed on the printed circuit board;

[0019] FIG. **4**B is a cross-sectional view taken along a line A-A shown in FIG. **4**A;

[0020] FIG. **5**A is a top view illustrating a configuration of the printed circuit board in accordance with yet another exemplary embodiment of the present invention;

[0021] FIG. **5**B is a cross-sectional view taken along a line C-C shown in FIG. **5**A;

[0022] FIG. **6** is a top view showing a state before process openings are formed on the printed circuit board;

[0023] FIG. **7** is a variation example of the configuration of the printed circuit board shown in FIG. **5**A and FIG. **5**B;

[0024] FIG. **8**A is a top view illustrating a configuration of the printed circuit board in accordance with yet another exemplary embodiment of the present invention;

[0025] FIG. **8**B is a cross-sectional view taken along a line D-D shown in FIG. **8**A;

[0026] FIG. **9**A is a top view showing a state before process openings are formed on the printed circuit board;

[0027] FIG. **9**B is a cross-sectional view taken along a line D-D shown in FIG. **9**A;

[0028] FIG. **10**A and FIG. **10**B show yet another exemplary embodiment in accordance with the present invention; and

[0029] FIG. **11**A and FIG. **11**B show yet another exemplary embodiment in accordance with the present invention.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

[0030] A description will now be given, with reference to the accompanying drawings, of embodiments of the present invention.

[0031] FIG. **1**A, FIG. **1**B, and FIG. **2** illustrate an exemplary embodiment of the present invention. FIG. **1**A is a top view illustrating a configuration of a printed circuit board. FIG. **1**B is a cross-sectional view taken along a line A-A shown in FIG. **1**A. FIG. **2** is a cross-sectional view showing a state before process openings are formed on the printed circuit board. Referring to FIG. **1**A and FIG. **1**B, the printed circuit board is of a card edge connector type having multiple connecting terminals **50**, **60**, and **70** are formed on a surface of one edge of a multilayer substrate **10** (hereinafter, simply referred to as substrate **10**), by electrolytic gold plating. The substrate **10** is made of a dielectric material such as an epoxy resin or the like. The printed circuit board is inserted into or pulled out of a connector, not shown, in directions of two-headed arrows shown in FIG. **1**A. At this time, the connecting terminals **50**, **60**, and **70** and the edge of the substrate **10** are provided in such a manner that the distance between the connecting terminals **50** and the edge is almost identical to that between the connecting terminal **60** and the edge, and the distance between the connecting terminal **70** and the edge is selectively longer than those between the terminal **50** or **60** and the edge.

[0032] Also, interconnections **20**, **30**, and **40** electrically coupled to the connecting terminals **50**, **60**, and **70** are formed of a conductive material such as copper or the like on a surface of the substrate **10** by a known technique. The interconnections **20**, and **30** are lines provided for high-speed signals that transmit, for example, high-speed signals of as high as GHz band. The interconnection **40** is provided for a power supply, ground, or low-speed signals. Via hole platings **80** made of copper or the like are respectively formed to serve as via hole conductors and extend to given depths of the interconnections **20**, **30**, and **40**, and are respectively connected to the interconnections **20**, **30**, and **40**.

[0033] Connecting terminal-forming wirings **100** are provided as an inner layer of the substrate **10**, as shown in FIG. **1**B. The connecting terminal-forming wirings **100** are used with being connected to the interconnections **20**, **30**, and **40** respectively, while the connecting terminals **50**, **60**, and **70** are being formed by the electrolytic gold plating. The connecting terminal-forming wirings **100** are patterned, for example, by a conductive material such as copper or the like, and are respectively formed to correspond to the connecting terminals **50**, **60**, and **70**. Process openings Mh are formed in positions that correspond to those for forming the via hole platings **80** so as to extend to given depths in the substrate **10** (in other words, so as not to pierce through the substrate **10**) and electrically isolate the corresponding interconnections **20**, **30**, and **40** from the connecting terminal-forming wirings **100**.

[0034] On the printer circuit board before the process openings Mh are formed, the via hole plating **80** is electrically coupled with the connecting terminal-forming wiring **100**, as shown in FIG. **2**. The printer circuit board of FIG. **2** is formed by a known technique. The connecting terminal-forming wirings **100**, the interconnections **20**, **30**, and **40**, and the via hole platings **80** are formed, and the connecting terminals **50**, **60**, and **70** are then formed by the electrolytic gold plating with the use of the connecting terminal-forming wirings **100**. Here, the connecting terminal-forming wirings **100**, the interconnections **20**, **30**, and **40**, and the via hole platings **80** are electrically coupled to respectively establish electrical connection paths so as to provide the connecting terminals **50**, **60**, and **70**.

[0035] Then, the connecting terminals **50**, **60**, and **70** are formed by a known technique of the electrolytic gold plating. Subsequently, the process opening Mh is processed to a given depth of the substrate **10** in the position that corresponds to the position where the via hole plating **80** is formed, from the backside of the substrate **10** by use of a process machine equipped with a drill, so the via hole plating **80** and the connecting terminal-forming wiring **100** are disconnected. As described heretofore, as shown in FIG. **1**A and FIG. **1**B, the connecting terminal-forming wirings **100** are electrically isolated from the interconnections **20**, **30**, and **40**, thereby making it possible to prevent the impedance mismatching and signal transmission loss caused by unnecessary connections between the connecting terminal-forming wirings **100** and the interconnections **20**, **30**, and **40**.

[0036] FIG. **3**A through FIG. **4**B show another exemplary embodiment in accordance with the present invention. FIG. **3**A is a top view illustrating a configuration of the printed circuit board in accordance with another exemplary embodiment of the present invention. FIG. **3**B is a cross-sectional view taken along a line A-A shown in FIG. **3**A. FIG. **4**A is a top view showing a state before process openings are formed on the printed circuit board. FIG. **4**B is a cross-sectional view taken along a line A-A shown in FIG. **4**A. Hereinafter, in FIG. **3**A through FIG. **4**B, the same components and configurations as those of the above-described exemplary embodiment have the same reference numerals.

[0037] The points of difference between the present embodiment and the above-described embodiment are now described. The via hole platings **80** are formed adjacently to the interconnections **20**, **30**, and **40**, as shown in FIG. **4**A and FIG. **4**B, and then the connecting terminal-forming wirings **100** are respectively connected to the corresponding interconnections **20**, **30**, and **40**, in accordance with the present embodiment. Subsequently, the process openings Mh that piece through the substrate **10** are formed in the positions that correspond to those for forming the via hole platings **80**, so the connecting terminal-forming wirings **100** are electrically isolated from the interconnections **20**, **30**, and **40**. Here, the

positions and sizes for forming the via hole platings **80** and those of the process openings Mh are determined in consideration of the interconnections **20**, **30**, and **40**, so that the interconnections **20**, **30**, and **40** have designed widths. According to the configuration employed in the present embodiment, the process openings Mh pierce through the substrate **10**, thereby facilitating the process.

[0038] FIG. **5**A, FIG. **5**B, and FIG. **6** show yet another exemplary embodiment in accordance with the present invention. FIG. **5**A is a top view illustrating a configuration of the printed circuit board in accordance with yet another exemplary embodiment of the present invention. FIG. **5**B is a cross-sectional view taken along a line C-C shown in FIG. **5**A. FIG. **6** is a top view showing a state before process openings are formed on the printed circuit board. Hereinafter, in FIG. **5**A through FIG. **6**, the same components and configurations as those of the above-described exemplary embodiments have the same reference numerals.

[0039] In the present embodiment, the via hole plating **80** is not provided on the interconnection **40**. Instead, as shown in FIG. **6**, the interconnections **20**, **30**, and **40** are formed on the surface of the substrate **10**, and a connecting terminal-forming wiring **100**A is provided to be connected to the interconnection **40** on the surface of the substrate **10**. In addition, as shown in FIG. **5**A and FIG. **5**B, the process openings Mh that extends through the substrate **10** are formed for the interconnections **20** and **30** in the positions that correspond to those for forming the via hole platings **80**. The process opening Mh that extends through the substrate **10** is formed for the interconnection **40** in the position that corresponds to that for forming the via hole plating **80** to cut across the connecting terminal-forming wiring **100**A. The positions and sizes of the process openings Mh are determined in consideration of the interconnections **20**, **30**, and **40**, so that the interconnections **20**, **30**, and **40** may have designed widths. As stated, it is possible form the connecting terminal-forming wiring **100**A at the same time in the process of forming the interconnections **20**, **30**, and **40**, by arranging the connecting terminal-forming wiring **100**A on the surface of the substrate **10**. Also, the connecting terminal-forming wiring may be formed for the interconnection **20** or **30** on the surface of the substrate **10**. In FIG. **6**, the process opening Mh for the interconnection **40** is a through hole. However, referring now to FIG. **7**, for example, the process opening Mh may be a blind hole that extends to a given depth in the substrate **10**. This enables a lower layer of the process opening Mh to be utilized efficiently.

[0040] FIG. **8**A through FIG. **9**B show yet another exemplary embodiment in accordance with the present invention. FIG. **8**A is a top view illustrating a configuration of the printed circuit board in accordance with another exemplary embodiment of the present invention. FIG. **8**B is a cross-sectional view taken along a line D-D shown in FIG. **8**A. FIG. **9**A is a top view showing a state before process openings are formed on the printed circuit board. FIG. **9**B is a cross-sectional view taken along a line D-D shown in FIG. **9**A. Hereinafter, in FIG. **8**A through FIG. **9**B, the same components and configurations as those of the above-described exemplary embodiments have the same reference numerals.

[0041] On the surface of the substrate **10** employed in the present embodiment, referring to FIG. **9**A and FIG. **9**B, two interconnections **20** and **30** are arranged in parallel and the process opening Mh that pierces through the substrate **10** is arranged between the two interconnections **20** and **30**. Referring to FIG. **8**B, a connecting terminal-forming wiring **100** is provided as an inner layer of the substrate **10**. The connecting terminal-forming wiring **100** is commonly provided to the two interconnections **20** and **30**.

[0042] As shown in FIG. **9**A and FIG. **9**B, before the process opening Mh is formed on the printed circuit board, the connecting terminal-forming wiring **100** is formed as an inner layer of the substrate **10**, the interconnections **20** and **30** are formed on the surface of the substrate **10**, an interconnection **200** is formed on the surface of the substrate **10** to connect the interconnections **20** and **30**, and the via hole plating **80** is formed between the interconnections **20** and **30** to connect the interconnection **200** and the connecting terminal-forming wiring **100**. Subsequently, the via hole plating is formed in the position that corresponds to that for forming the via hole plating **80**. The via hole plating **80** and the interconnection **200** are wholly or partially removed to electrically isolate the two interconnections **20** and **30** from the connecting terminal-forming wiring **100**. Here, the position and size for forming the via hole plating **80** and those of the process openings Mh are determined in consideration of the interconnections **20** and **30**, so that the interconnections **20** and **30** have designed widths.

[0043] It is thus possible to reduce the number of processed necessary for the process of the process opening Mh, by forming the via hole plating **80** and the connecting terminal-forming wiring **100** commonly provided for the interconnections **20** and **30** that transmit high-speed signals.

[0044] FIG. **10**A and FIG. **10**B show yet another exemplary embodiment in accordance with the present invention. Hereinafter, in FIG. **10**A through FIG. **10**B, the same components and configurations as those of the above-described exemplary embodiments have the same reference numerals. In this printed circuit board, the process opening Mh that pierces through the substrate is isolated from conductive layers composed of a wiring layer for ground **300**, a wiring layer for power supply **310**, and a wiring layer for signal **320**. In other words, in accordance with the present embodiment, the conductive layers composed of the wiring layer for ground **300**, the wiring layer for power supply **310**, and the wiring layer for signal **320** are formed in the forming process so as to save regions where the process opening Mh pierces through. With the afore-described configuration, when the process opening Mh is processed with a drill, no drilled residue particles are generated from the respective conductive layers, thereby preventing the respective conductive layers being short-circuited. Referring now to FIG. **11**A and FIG. **11**B, for example, it may be configured such that only the wiring layer for ground **300** is in contact with the process opening Mh (which pierces through the substrate **10**). There is no possibility of short-circuiting, if only one layer is in contact with the process opening Mh.

[0045] In the above-described embodiments, a description has been given of a case where a conductive via hole is formed by plating. However, the present invention is not limited to this case. The via hole may be formed by another method. In the above-described embodiments, the connecting terminals are formed by electrolytic gold plating. However, another type of electrolytic plating may be employed for forming the connecting terminals.

[0046] In the above-described embodiments, a description has been given of a case where the process openings are processed to electrically isolate all the interconnections **20**, **30**, and **40** from the connecting terminal-forming wirings

100. However, it may be configured such that the process openings are processed only for the interconnections **20** and **30** that transmit high-speed signals so as to electrically isolate from the connecting terminal-forming wiring.

[0047] According to one aspect of the present invention, there is provided a printed circuit board of a card edge connector type including: interconnections formed on a surface of a substrate to be electrically coupled to respective connecting terminals formed by electrolytic plating on an edge of the substrate; and connecting terminal-forming wirings being respectively in connection with the interconnections, when the connecting terminals are formed by the electrolytic plating. The interconnections are electrically isolated from the connecting terminal-forming wirings by process openings formed in the substrate.

[0048] In the above-described printed circuit board, the connecting terminal-forming wirings may be formed as inner layers of the substrate, and may be isolated from the interconnections by the process openings that extend to a given depth in the substrate. The above-described configuration eliminates the necessity of providing a through hole in the substrate, thereby making it possible to prevent the process opening formed in the substrate from affecting the conductive layers formed as inner layers in the substrate.

[0049] In the above-described printed circuit board, the connecting terminal-forming wirings may be formed apart from a card edge connector portion on the surface of the substrate, and may be electrically isolated from the interconnections by the process openings that pierce through the substrate. With the above-described configuration, it is possible to form the interconnections and the connecting terminal-forming wirings at the same time, thereby facilitating the formation of the connecting terminal-forming wirings.

[0050] In the above-described printed circuit board, the interconnections may include interconnections that transmit high-speed signals; and the process openings electrically isolate at least the interconnections that transmit the high-speed signals from the connecting terminal-forming wirings. With the above-described configuration, it is only necessary to form the process openings to isolate the connecting terminal-forming wirings from the signal lines that transmit high-speed signals that affect the circuit characteristics.

[0051] In the above-described printed circuit board, the process openings may be isolated from a conductive layer formed as an inner layer of the substrate. With the above-described configuration, it is possible to prevent the problem such as short-circuiting caused by the drilled residue particles.

[0052] In the above-described printed circuit board, the process openings may be in contact with only one layer out of multiple conductive layers formed as inner layers. With the above-described configuration, it is possible to process a layer having a large area such as a ground layer and to prevent the problem such as the short-circuiting caused by the drilled residue particles, when only one layer is in contact with the process opening.

[0053] In the above-described printed circuit board, via holes may be formed to respectively connect the interconnections and the connecting terminal-forming wirings. With the above-described configuration, it is possible to connect the interconnections formed on the surface of the substrate and the connecting terminal-forming wirings formed as inner layers by the via holes, and the processing can be facilitated by forming the process openings in the position that correspond to those for forming the via holes.

[0054] In the above-described printed circuit board, the electrolytic plating may include electrolytic gold plating. With the above-described configuration, it is possible to form the connecting terminals with the use of highly conductive gold plating and to retain the thickness of the connecting terminals sufficiently as compared to those with the use of nonelectrolytic plating.

[0055] According to an exemplary embodiment of the present invention, it is possible to eliminate the influence on the circuit characteristics of the connecting terminal-forming wiring connected to the signal line or the like so as to form the connecting terminals on the printer circuit board of the card edge connector type by electrolytic plating.

[0056] The present invention is not limited to the above-mentioned embodiments, and other embodiments, variations and modifications may be made without departing from the scope of the present invention.

[0057] The present invention is based on Japanese Patent Application No. 2005-212427 filed on Jul. 22, 2005, the entire disclosure of which is hereby incorporated by reference.

1. A printed circuit board of a card edge connector type comprising:

two interconnections formed in parallel on a surface of a substrate to be electrically coupled to respective connecting terminals formed by electrolytic plating on an edge of the substrate; and

a connecting terminal-forming wiring being commonly in connection with the two interconnections, when the connecting terminals are formed by the electrolytic plating,

wherein the two interconnections are electrically isolated from the connecting terminal-forming wiring by a process opening formed in the substrate, the process opening being commonly connected to the two interconnections.

2. The printed circuit board as claimed in claim **1**, wherein the connecting terminal-forming wirings are formed as inner layers of the substrate, and are isolated from the interconnections by the process opening that extends to a given depth in the substrate.

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