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(54) **MICROELECTRONIC ASSEMBLIES INCLUDING SOLDER AND NON-SOLDER INTERCONNECTS**

(57) Microelectronic assemblies, related devices and methods, are disclosed herein. In some embodiments, a microelectronic assembly may include a first die, having a first surface and an opposing second surface, in a first layer; a redistribution layer (RDL) on the

first layer, wherein the RDL is electrically coupled to the second surface of the first die by solder interconnects, and a second die in a second layer on the RDL, wherein the second die is electrically coupled to the RDL by non-solder interconnects.

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Description

Background

[0001] Integrated circuit (IC) devices (e.g., dies) are typically coupled together in a multi-die IC package to integrate features or functionality and to facilitate connections to other components, such as package substrates. In a conventional package, dies may be coupled together by solder. Such a package may be limited in the achievable interconnect density by the solder interconnects between the dies.

Brief Description of the Drawings

[0002] Embodiments will be readily understood by the following detailed description in conjunction with the accompanying drawings. To facilitate this description, like reference numerals designate like structural elements. Embodiments are illustrated by way of example, not by way of limitation, in the figures of the accompanying drawings.

FIG. 1 is a side, cross-sectional view of an example microelectronic assembly, in accordance with various embodiments.

FIG. 2 is a side, cross-sectional view of an example microelectronic assembly, in accordance with various embodiments.

FIGS. 3A-3G are side, cross-sectional views of various stages in an example process for manufacturing the microelectronic assembly of FIG. 1, in accordance with various embodiments.

FIGS. 4A-4G are side, cross-sectional views of various stages in an example process for manufacturing the microelectronic assembly of FIG. 2, in accordance with various embodiments.

FIG. 5 is a flow diagram of an example method of fabricating an example microelectronic assembly, in accordance with various embodiments.

FIG. 6 is a top view of a wafer and dies that may be included in a microelectronic assembly, in accordance with any of the embodiments disclosed herein.

FIG. 7 is a cross-sectional side view of an IC device that may be included in a microelectronic assembly, in accordance with any of the embodiments disclosed herein.

FIG. 8 is a cross-sectional side view of an IC device assembly that may include a microelectronic assembly, in accordance with any of the embodiments disclosed herein.

FIG. 9 is a block diagram of an example electrical device that may include a microelectronic assembly, in accordance with any of the embodiments disclosed herein.

Detailed Description

[0003] Microelectronic assemblies, related devices and methods, are disclosed herein. For example, in some embodiments, a microelectronic assembly may include a first die, having a first surface and an opposing second surface, in a first layer; a redistribution layer (RDL) on the first layer, wherein the RDL is electrically coupled to the second surface of the first die by solder interconnects, and a second die in a second layer on the RDL, wherein the second die is electrically coupled to the RDL by non-solder interconnects.

[0004] Communicating large numbers of signals between two or more dies in a multi-die IC package is challenging due to the increasingly small size of such dies and increased use of stacking dies. To achieve high interconnect density in a multi-die IC package, some conventional approaches require additional assembly operations, which increases the cost and complexity of manufacturing. The microelectronic structures and assemblies disclosed herein may achieve interconnect densities as high or higher than conventional approaches without the expense of conventional costly manufacturing operations. Further, the microelectronic structures and assemblies disclosed herein offer new flexibility to electronics designers and manufacturers, allowing them to select an architecture that achieves their device goals without excess cost or manufacturing complexity.

[0005] In the following detailed description, reference is made to the accompanying drawings that form a part hereof wherein like numerals designate like parts throughout, and in which is shown, by way of illustration, embodiments that may be practiced. It is to be understood that other embodiments may be utilized, and structural or logical changes may be made without departing from the scope of the present disclosure. Therefore, the following detailed description is not to be taken in a limiting sense.

[0006] Various operations may be described as multiple discrete actions or operations in turn, in a manner that is most helpful in understanding the claimed subject matter. However, the order of description should not be construed as to imply that these operations are necessarily order dependent. In particular, these operations may not be performed in the order of presentation. Operations described may be performed in a different order from the described embodiment. Various additional operations may be performed, and/or described operations may be omitted in additional embodiments.

[0007] For the purposes of the present disclosure, the phrase "A and/or B" means (A), (B), or (A and B). For the purposes of the present disclosure, the phrase "A, B, and/or C" means (A), (B), (C), (A and B), (A and C), (B and C), or (A, B, and C). The drawings are not necessarily to scale. Although many of the drawings illustrate rectilinear structures with flat walls and right-angle corners, this is simply for ease of illustration, and actual devices made using these techniques will exhibit rounded cor-

ners, surface roughness, and other features.

[0008] The description uses the phrases "in an embodiment" or "in embodiments," which may each refer to one or more of the same or different embodiments. Furthermore, the terms "comprising," "including," "having," and the like, as used with respect to embodiments of the present disclosure, are synonymous. As used herein, a "package" and an "IC package" are synonymous, as are a "die" and an "IC die." The terms "top" and "bottom" may be used herein to explain various features of the drawings, but these terms are simply for ease of discussion, and do not imply a desired or required orientation. As used herein, the term "insulating" means "electrically insulating," unless otherwise specified. Throughout the specification, and in the claims, the term "coupled" means a direct or indirect connection, such as a direct electrical, mechanical, or magnetic connection between the things that are connected or an indirect connection, through one or more passive or active intermediary devices. The meaning of "a," "an," and "the" include plural references. The meaning of "in" includes "in" and "on." Unless otherwise specified the use of the ordinal adjectives "first," "second," and "third," etc., to describe a common object, merely indicate that different instances of like objects are being referred to, and are not intended to imply that the objects so described must be in a given sequence, either temporally, spatially, in ranking or in any other manner.

[0009] When used to describe a range of dimensions, the phrase "between X and Y" represents a range that includes X and Y. For convenience, the phrase "FIG. 3" may be used to refer to the collection of drawings of FIGS. 3A-3G, the phrase "FIG. 4" may be used to refer to the collection of drawings of FIGS. 4A-4G, etc. Although certain elements may be referred to in the singular herein, such elements may include multiple sub-elements. For example, "an insulating material" may include one or more insulating materials.

[0010] FIG. 1 is a side, cross-sectional view of an example microelectronic assembly, in accordance with various embodiments. The microelectronic assembly 100 may include a multi-layer die subassembly 104 having a first layer die 114-1 coupled by solder interconnects 130 and a second layer die 114-2 electrically coupled by non-solder interconnects 132. As used herein, the term a "multi-layer die subassembly" 104 may refer to a composite die having two or more stacked dielectric layers with one or more dies in each layer, and conductive interconnects and/or conductive pathways connecting the one or more dies, including dies in non-adjacent layers. As used herein, the terms a "multi-layer die subassembly" and a "composite die" may be used interchangeably. As shown in FIG. 1, the multi-layer die subassembly 104 may include a first layer 104-1 having a die 114-1 and a conductive pillar 152, a second layer 104-2 having a die 114-2 and a die 114-3, and an RDL 148 between the first and second layers 104-1, 104-2 where the die 114-1 is electrically coupled to the RDL 148 via solder interconnects 130 and the dies 114-2, 114-3 are electrically cou-

pled to the RDL 148 via non-solder interconnects 132. The multi-layer die subassembly 104 may further include a die 114-4 in the first layer 104-1 within a footprint of the die 114-2, having through silicon vias (TSVs) 117, and electrically coupled to the RDL 148 by solder interconnects 130. The multi-layer die subassembly 104 may include a first surface 170-1 and an opposing second surface 170-2. In particular, the dies 114-1, 114-4 may include a bottom surface (e.g., the surface facing towards the first surface 170-1) with first conductive contacts 122, and an opposing top surface (e.g., the surface facing towards the second surface 170-2) with second conductive contacts 124. The dies 114-2, 114-3 may include conductive contacts 122 on the bottom surface of the die (e.g., the surface facing towards the first surface 170-1). The RDL 148 may include first conductive contacts 172 on a bottom surface and second conductive contacts 174 on a top surface of the RDL. As used herein, a "conductive contact" may refer to a portion of conductive material (e.g., metal) serving as an electrical interface between different components (e.g., part of a conductive interconnect); conductive contacts may be recessed in, flush with (e.g., as shown in FIG. 2), or extending away from a surface of a component (e.g., as shown in FIG. 1), and may take any suitable form (e.g., a conductive pad or socket, or portion of a conductive line or via). Any of the conductive contacts disclosed herein (e.g., the conductive contacts 122, 124, 144, 146, 172, and/or 174) may include bond pads, solder bumps, conductive posts, or any other suitable conductive contact, for example. As shown in FIG. 1, the dies 114-1, 114-2, 114-3, and 114-4 are depicted as having conductive contacts extending away from a surface of the die, and may be referred to herein as "a bumped die" or "a micro-bumped die." As shown in FIG. 2, the dies 114-2, 114-3 are depicted as having conductive contacts flush with a surface of the die, and may be referred to herein as "a bumpless die." The die 114 may include other conductive pathways (e.g., including lines and vias) and/or to other circuitry (not shown) coupled to the respective conductive contacts (e.g., conductive contacts 122, 124) on the surface of the die 114.

[0011] The dies 114-1, 114-4 in the first layer 104-1 may be coupled to the package substrate 102 by die-to-package substrate (DTPS) interconnects 150, and may be coupled to the dies 114-2, 114-3 in the second layer 104-2 by solder interconnects 130, conductive pathways 196 in the RDL 148, and non-solder interconnects 132. The dies 114-2, 114-3 in the second layer 104-2 may be coupled to the package substrate 102 via non-solder interconnects 132, conductive pathways 196 in the RDL 148, the conductive pillars 152, and the DTPS interconnects 150 to form multi-level (ML) interconnects. The ML interconnects may be power delivery interconnects or high speed signal interconnects. As used herein, the term "ML interconnect" may refer to an interconnect that includes a conductive pillar between a first component and a second component where the first component and the second component are not in adjacent layers, or may

refer to an interconnect that spans one or more layers (e.g., an interconnect between a first die in a first layer and a second die in a third layer, or an interconnect between a package substrate and a die in a second layer). In particular, as shown in FIG. 1, the DTPS interconnects 150 may include conductive contacts 146 on the top surface of the package substrate 102, solder 134, and conductive contacts 144 on a bottom surface of the multi-layer die subassembly 104.

[0012] An RDL 148 may include an insulating material (e.g., a dielectric material formed in multiple layers, as known in the art) and one or more conductive pathways 196 through the dielectric material (e.g., including conductive traces and/or conductive vias, as shown). The conductive pathways 196 may electrically couple the first conductive contacts 172 and the second conductive contacts 174 on the RDL 148. In some embodiments, the insulating material of the RDL 148 may be composed of dielectric materials, bismaleimide triazine (BT) resin, polyimide materials, epoxy materials (e.g., glass reinforced epoxy matrix materials, epoxy build-up films, or the like), mold materials, oxide-based materials (e.g., silicon dioxide or spin on oxide), or low-k and ultra low-k dielectric (e.g., carbon-doped dielectrics, fluorine-doped dielectrics, porous dielectrics, and organic polymeric dielectrics). In some embodiments, the multi-layer die subassembly 104 may include one or more RDLs 148. In some embodiments, the one or more RDLs 148 may be at the first surface 170-1 of the first layer 104-1.

[0013] The conductive pillars 152 may be formed of any suitable conductive material, such as copper, silver, nickel, gold, aluminum, or other metals or alloys, for example. The conductive pillars 152 may be formed using any suitable process, including, for example, a lithographic process or an additive process, such as cold spray or 3-dimensional printing. In some embodiments, the conductive pillars 152 disclosed herein may have a pitch between 75 microns and 200 microns. As used herein, pitch is measured center-to-center (e.g., from a center of a conductive pillar to a center of an adjacent conductive pillar). The conductive pillars 152 may have any suitable size and shape. In some embodiments, the conductive pillars 152 may have a circular, rectangular, or other shaped cross-section.

[0014] The die 114 disclosed herein may include an insulating material (e.g., a dielectric material formed in multiple layers, as known in the art) and multiple conductive pathways formed through the insulating material. In some embodiments, the insulating material of a die 114 may include a dielectric material, such as silicon dioxide, silicon nitride, oxynitride, polyimide materials, glass reinforced epoxy matrix materials, or a low-k or ultra low-k dielectric (e.g., carbon-doped dielectrics, fluorine-doped dielectrics, porous dielectrics, organic polymeric dielectrics, photo-imageable dielectrics, and/or benzocyclobutene-based polymers). In some embodiments, the insulating material of a die 114 may include a semiconductor material, such as silicon, germanium, or a III-V

material (e.g., gallium nitride), and one or more additional materials. For example, an insulating material may include silicon oxide or silicon nitride. The conductive pathways in a die 114 may include conductive traces and/or conductive vias, and may connect any of the conductive contacts in the die 114 in any suitable manner (e.g., connecting multiple conductive contacts on a same surface or on different surfaces of the die 114). Example structures that may be included in the dies 114 disclosed herein are discussed below with reference to FIG. 7. The conductive pathways in the dies 114 may be bordered by liner materials, such as adhesion liners and/or barrier liners, as suitable. In some embodiments, the die 114 is a wafer. In some embodiments, the die 114 is a monolithic silicon, a fan-out or fan-in package die, or a die stack (e.g., wafer stacked, die stacked, or multi-layer die stacked).

[0015] In some embodiments, the die 114 may include conductive pathways to route power, ground, and/or signals to/from other dies 114 included in the microelectronic assembly 100. For example, the die 114-1 may include TSVs (not shown), including a conductive material via, such as a metal via, isolated from the surrounding silicon or other semiconductor material by a barrier oxide), or other conductive pathways through which power, ground, and/or signals may be transmitted between the package substrate 102 and one or more dies 114 "on top" of the dies 114-1, 114-4 (e.g., in the embodiment of FIG. 1, the dies 114-2 and/or 114-3). In some embodiments, the die 114-1 may not route power and/or ground to the dies 114-2 and 114-3; instead, the dies 114-2, 114-3 may couple directly to power and/or ground lines in the package substrate 102 by ML interconnects (e.g., via conductive pillars 152). In some embodiments, the die 114-1 in the first layer 104-1, also referred to herein as "base die," "interposer die," or bridge die," may be thicker than the dies 114-2, 114-3 in the second layer 104-2. In some embodiments, a die 114 may span multiple layers of the multi-layer die subassembly 104. In some embodiments, the die 114-1 may be a memory device (e.g., as described below with reference to the die 1502 of FIG. 6), a high frequency serializer and deserializer (SerDes), such as a Peripheral Component Interconnect (PCI) express. In some embodiments, the die 114-1 may be a processing die, a radio frequency chip, a power converter, a network processor, a workload accelerator, a security encryptor, or a passive/active bridge die to provide high Bandwidth Die-to-Die interconnections between the die 114-2 and 114-3 at low power. In some embodiments, the die 114-2 and/or the die 114-3 may be a processing die.

[0016] The multi-layer die subassembly 104 may include an insulating material 133 (e.g., a dielectric material formed in multiple layers, as known in the art) to form the multiple layers and to embed one or more dies in a layer. In particular, the first dies 114-1, 114-4 and conductive pillars 152 may be embedded in the insulating material 133 in the first layer 104-1 and the second and third dies

114-2, 114-3 may be embedded in the insulating material 133 in the second layer 104-2. In some embodiments, the insulating material 133 of the multi-layer die subassembly 104 may be a dielectric material, such as an organic dielectric material, a fire retardant grade 4 material (FR-4), bismaleimide triazine (BT) resin, polyimide materials, glass reinforced epoxy matrix materials, or low-k and ultra low-k dielectric (e.g., carbon-doped dielectrics, fluorine-doped dielectrics, porous dielectrics, and organic polymeric dielectrics). In some embodiments, the die 114 may be embedded in an inhomogeneous dielectric, such as stacked dielectric layers (e.g., alternating layers of different inorganic dielectrics). In some embodiments, the insulating material 133 of the multi-layer die subassembly 104 may be a mold material, such as an organic polymer with inorganic silica particles. The multi-layer die subassembly 104 may include one or more ML interconnects through the dielectric material (e.g., including conductive vias and/or conductive pillars, as shown). The multi-layer die subassembly 104 may have any suitable dimensions. For example, in some embodiments, a thickness of the multi-layer die subassembly 104 may be between 100 μm and 2000 μm . In some embodiments, the multi-layer die subassembly 104 may include a composite die, such as stacked dies. The multi-layer die subassembly 104 may have any suitable number of layers, any suitable number of dies, and any suitable die arrangement. For example, in some embodiments, the multi-layer die subassembly 104 may have between 3 and 20 layers of dies. In some embodiments, the multi-layer die subassembly 104 may include a layer having between 2 and 50 dies.

[0017] The package substrate 102 may include an insulating material (e.g., a dielectric material formed in multiple layers, as known in the art) and one or more conductive pathways to route power, ground, and signals through the dielectric material (e.g., including conductive traces and/or conductive vias, as shown). In some embodiments, the insulating material of the package substrate 102 may be a dielectric material, such as an organic dielectric material, a fire retardant grade 4 material (FR-4), BT resin, polyimide materials, glass reinforced epoxy matrix materials, organic dielectrics with inorganic fillers or low-k and ultra low-k dielectric (e.g., carbon-doped dielectrics, fluorine-doped dielectrics, porous dielectrics, and organic polymeric dielectrics). In particular, when the package substrate 102 is formed using standard printed circuit board (PCB) processes, the package substrate 102 may include FR-4, and the conductive pathways in the package substrate 102 may be formed by patterned sheets of copper separated by build-up layers of the FR-4. The conductive pathways in the package substrate 102 may be bordered by liner materials, such as adhesion liners and/or barrier liners, as suitable. In some embodiments, the package substrate 102 may be formed using a lithographically defined via packaging process. In some embodiments, the package substrate 102 may be manufactured using standard organic pack-

age manufacturing processes, and thus the package substrate 102 may take the form of an organic package. In some embodiments, the package substrate 102 may be a set of redistribution layers formed on a panel carrier by laminating or spinning on a dielectric material, and creating conductive vias and lines by laser drilling and plating. In some embodiments, the package substrate 102 may be formed on a removable carrier using any suitable technique, such as a redistribution layer technique. Any method known in the art for fabrication of the package substrate 102 may be used, and for the sake of brevity, such methods will not be discussed in further detail herein.

[0018] In some embodiments, the package substrate 102 may be a lower density medium and the die 114 may be a higher density medium or have an area with a higher density medium. As used herein, the term "lower density" and "higher density" are relative terms indicating that the conductive pathways (e.g., including conductive interconnects, conductive lines, and conductive vias) in a lower density medium are larger and/or have a greater pitch than the conductive pathways in a higher density medium. In some embodiments, a higher density medium may be manufactured using a modified semi-additive process or a semi-additive build-up process with advanced lithography (with small vertical interconnect features formed by advanced laser or lithography processes), while a lower density medium may be a PCB manufactured using a standard PCB process (e.g., a standard subtractive process using etch chemistry to remove areas of unwanted copper, and with coarse vertical interconnect features formed by a standard laser process). In other embodiments, the higher density medium may be manufactured using semiconductor fabrication process, such as a single damascene process or a dual damascene process. In some embodiments, additional dies may be disposed on the top surface of the dies 114-2, 114-3. In some embodiments, additional components may be disposed on the top surface of the dies 114-2, 114-3. Additional passive components, such as surface-mount resistors, capacitors, and/or inductors, may be disposed on the top surface or the bottom surface of the package substrate 102, or embedded in the package substrate 102.

[0019] The microelectronic assembly 100 of FIG. 1 may also include an underfill material 127. In some embodiments, the underfill material 127 may extend between the multi-layer die subassembly 104 and the package substrate 102 around the associated DTPS interconnects 150. In some embodiments, the underfill material 127 may extend around the associated solder interconnects 130. The underfill material 127 may be an insulating material, such as an appropriate epoxy material. In some embodiments, the underfill material 127 may include a capillary underfill, non-conductive film (NCF), or molded underfill. In some embodiments, the underfill material 127 may include an epoxy flux that assists with soldering the multi-layer die subassembly 104 to the package substrate 102 when forming the DTPS interconnects 150,

and then polymerizes and encapsulates the DTPS interconnects 150. The underfill material 127 may be selected to have a coefficient of thermal expansion (CTE) that may mitigate or minimize the stress between the dies 114 and the package substrate 102 arising from uneven thermal expansion in the microelectronic assembly 100. In some embodiments, the CTE of the underfill material 127 may have a value that is intermediate to the CTE of the package substrate 102 (e.g., the CTE of the dielectric material of the package substrate 102) and a CTE of the dies 114 and/or insulating material 133 of the multi-layer die sub-assembly 104.

[0020] The DTPS interconnects 150 disclosed herein may take any suitable form. In some embodiments, a set of DTPS interconnects 150 may include solder (e.g., solder bumps or balls that are subject to a thermal reflow to form the DTPS interconnects 150). In some embodiments, a set of DTPS interconnects 150 may include an anisotropic conductive material, such as an anisotropic conductive film or an anisotropic conductive paste. An anisotropic conductive material may include conductive materials dispersed in a non-conductive material.

[0021] The solder interconnects 130 disclosed herein may take any suitable form. The solder interconnects 130 may have a finer pitch than the DTPS interconnects 150 in a microelectronic assembly. In some embodiments, the solder interconnects 130 may include small conductive bumps (e.g., copper bumps) attached to the conductive contacts 124 by solder. In some embodiments, the solder interconnects 130 disclosed herein may have a pitch between 10 microns and 100 microns. In some embodiments, a diameter of the solder is equal to approximately half a minimum pitch. The solder interconnects 130 may have too fine a pitch to couple to the package substrate 102 directly (e.g., too fine to serve as DTPS interconnects 150). In some embodiments, the solder interconnects 130 may be used as data transfer lanes, while the DTPS interconnects 150 may be used for power and ground lines, among others. In some embodiments, the solder interconnects 130 in a microelectronic assembly 100 may be solder interconnects that include a solder with a higher melting point than a solder included in some or all of the DTPS interconnects 150. For example, when the solder interconnects 130 in a microelectronic assembly 100 are formed before the DTPS interconnects 150 are formed, solder interconnects 130 may use a higher-temperature solder (e.g., with a melting point above 200 degrees Celsius), while the DTPS interconnects 150 may use a lower-temperature solder (e.g., with a melting point below 200 degrees Celsius). In some embodiments, a higher-temperature solder may include tin; tin and gold; or tin, silver, and copper (e.g., 96.5 % tin, 3% silver, and 0.5% copper). In some embodiments, a lower-temperature solder may include tin and bismuth (e.g., eutectic tin bismuth) or tin, silver, and bismuth. In some embodiments, a lower-temperature solder may include indium, indium and tin, or gallium.

[0022] The non-solder interconnects 132 disclosed

herein may take any suitable form. The non-solder interconnects 132 may have a finer pitch than the DTPS interconnects 150 in a microelectronic assembly. In some embodiments, some or all of the non-solder interconnects 132 in a microelectronic assembly 100 may be metal-to-metal interconnects (e.g., copper-to-copper interconnects, or plated interconnects). In some embodiments, the non-solder interconnects 132 disclosed herein may have a pitch between 50 microns and 150 microns.

[0023] In the microelectronic assemblies 100 disclosed herein, some or all of the DTPS interconnects 150 may have a larger pitch than some or all of the solder interconnects 130. Solder interconnects 130 may have a smaller pitch than DTPS interconnects 150 due to the greater similarity of materials between the dies 114 and the RDL 148 than between the die 114 and the package substrate 102 on either side of a set of DTPS interconnects 150. In particular, the differences in the material composition of a die 114 and a package substrate 102 may result in differential expansion and contraction of the die 114 and the package substrate 102 due to heat generated during operation (as well as the heat applied during various manufacturing operations). To mitigate damage caused by this differential expansion and contraction (e.g., cracking, solder bridging, etc.), the DTPS interconnects 150 may be formed larger and farther apart than the solder interconnects 130, which may experience less thermal stress due to the greater material similarity of the dies 114 and the RDL 148. In some embodiments, the DTPS interconnects 150 disclosed herein may have a pitch between 100 microns and 350 microns.

[0024] The microelectronic assembly 100 of FIG. 1 may also include a circuit board (not shown). The package substrate 102 may be coupled to the circuit board by second-level interconnects at the bottom surface of the package substrate 102. The second-level interconnects may be any suitable second-level interconnects, including solder balls for a ball grid array arrangement, pins in a pin grid array arrangement or lands in a land grid array arrangement. The circuit board may be a motherboard, for example, and may have other components attached to it. The circuit board may include conductive pathways and other conductive contacts for routing power, ground, and signals through the circuit board, as known in the art. In some embodiments, the second-level interconnects may not couple the package substrate 102 to a circuit board, but may instead couple the package substrate 102 to another IC package, an interposer, or any other suitable component. In some embodiments, the multi-layer die subassembly 104 may not be coupled to a package substrate 102, but may instead be coupled to a circuit board, such as a PCB.

[0025] Although FIG. 1 depicts a multi-layer die subassembly 104 having a particular number of dies 114 coupled to the package substrate 102 and to other dies 114, this number and arrangement are simply illustrative, and a multi-layer die subassembly 104 may include any desired number and arrangement of dies 114 coupled to

a package substrate 102. Although FIG. 1 shows the dies 114-1, 114-4 as a double-sided die and the dies 114-2, 114-3 as single-sided dies, the dies 114 may be a single-sided or a double-sided die and may be a single-pitch die or a mixed-pitch die. In some embodiments, additional components may be disposed on the top surface of the dies 114-2 and/or 114-3. In this context, a double-sided die refers to a die that has connections on both surfaces. In some embodiments, a double-sided die may include TSVs (e.g., the TSVs 117 in die 114-4) to form connections on both surfaces. The active surface of a double-sided die, which is the surface containing one or more active devices and a majority of interconnects, may face either direction depending on the design and electrical requirements.

[0026] Many of the elements of the microelectronic assembly 100 of FIG. 1 are included in other ones of the accompanying drawings; the discussion of these elements is not repeated when discussing these drawings, and any of these elements may take any of the forms disclosed herein. Further, a number of elements are illustrated in FIG. 1 as included in the microelectronic assembly 100, but a number of these elements may not be present in a microelectronic assembly 100. For example, in various embodiments, the die 114-4, the underfill material 127, and the package substrate 102 may not be included. In some embodiments, individual ones of the microelectronic assemblies 100 disclosed herein may serve as a system-in-package (SiP) in which multiple dies 114 having different functionality are included. In such embodiments, the microelectronic assembly 100 may be referred to as an SiP.

[0027] FIG. 2 is a side, cross-sectional view of an example microelectronic assembly, in accordance with various embodiments. The microelectronic assembly 100 may include a multi-layer die subassembly 104 having a first layer die 114-1 coupled by solder interconnects 130 and a second layer die 114-2 electrically coupled by non-solder interconnects 132. As shown in FIG. 2, the multi-layer die subassembly 104 may include a first layer 104-1 having a die 114-1 and a conductive pillar 152, a second layer 104-2 having dies 114-2, 114-3 that are bumpless dies, and an RDL 148 between the first and second layers 104-1, 104-2 where the die 114-1 is electrically coupled to the RDL 148 via solder interconnects 130 and the dies 114-2, 114-3 are electrically coupled to the RDL 148 via non-solder interconnects 132. In particular, the dies 114-2, 114-3 may include conductive contacts 122 on a bottom surface that are recessed or flush with the bottom surface, such that the dies 114-2, 114-3 are bumpless dies. The die 114-1 in the first layer 104-1 may be coupled to the package substrate 102 by die-to-package substrate (DTPS) interconnects 150, and may be coupled to the dies 114-2, 114-3 in the second layer 104-2 by solder interconnects 130, conductive pathways 196 in the RDL 148, and non-solder interconnects 132. The dies 114-2, 114-3 in the second layer 104-2 may be coupled to the package substrate 102 via non-solder interconnects 132,

conductive pathways 196 in the RDL 148, the conductive pillars 152, and the DTPS interconnects 150.

[0028] Any suitable techniques may be used to manufacture the microelectronic assemblies 100 disclosed herein. For example, FIGS. 3A-3G are side, cross-sectional views of various stages in an example process for manufacturing the microelectronic assembly 100 of FIG. 1, in accordance with various embodiments. Although the operations discussed below with reference to FIGS. 3A-3G (and others of the accompanying drawings representing manufacturing processes) are illustrated in a particular order, these operations may be performed in any suitable order. Further, additional operations which are not illustrated may also be performed without departing from the scope of the present disclosure. Also, various ones of the operations discussed herein with respect to FIGS. 3A-3G may be modified in accordance with the present disclosure to fabricate others of microelectronic assembly 100 disclosed herein.

[0029] FIG. 3A illustrates an assembly subsequent to mounting dies 114-2, 114-3 on a carrier 105 with a surface having conductive contacts 122 facing away from the carrier 105. Any suitable method may be used to place the dies 114-2, 114-3 for example, automated pick-and-place. A carrier 105 may include any suitable material for providing mechanical stability during manufacturing operations, and in some embodiments, may include a semiconductor wafer (e.g., a silicon wafer) or glass (e.g., a glass panel). The dies 114-2, 114-3 may have a die-to-die gap 119 between 1 micron and 100 microns.

[0030] FIG. 3B illustrates an assembly subsequent to depositing an insulating material 133 on and around the dies 114-2, 114-3, and planarizing the top surface of the assembly to decrease a thickness (e.g., z-height) of the conductive contacts 122 and/or the insulating material 133 to form the second layer 104-2. The insulating material 133 may be a mold material, such as an organic polymer with inorganic silica particles, an epoxy material, or a silicon and nitrogen material (e.g., in the form of silicon nitride). In some embodiments, the insulating material 133 is a dielectric material. In some embodiments, the dielectric material may include an organic dielectric material, a fire retardant grade 4 material (FR-4), BT resin, polyimide materials, glass reinforced epoxy matrix materials, or low-k and ultra low-k dielectric (e.g., carbon-doped dielectrics, fluorine-doped dielectrics, porous dielectrics, and organic polymeric dielectrics). The insulating material 133 may be formed using any suitable process, including lamination, or slit coating and curing. In some embodiments, the insulating material 133 may be dispensed in liquid form to flow around and conform to various shapes of components and metallization, and, subsequently, may be subjected to a process, for example, curing, that solidifies the insulating material 133. In some embodiments, the insulating material 133 may be initially deposited on and over the top surface of the dies 114-2, 114-3, then polished back to expose the top surface of the conductive contacts 122 on the dies 114-2,

114-3. The insulating material 133 may be removed using any suitable technique, including grinding, or etching, such as a wet etch, a dry etch (e.g., a plasma etch), a wet blast, or a laser ablation (e.g., using excimer laser). In some embodiments, the thickness of the insulating material 133 may be minimized to reduce the etching time required. In some embodiments, the top surface of the insulating material 133 may be planarized using any suitable process, such as chemical mechanical polishing (CMP).

[0031] FIG. 3C illustrates an assembly subsequent to forming an RDL 148 on a top surface of the assembly of FIG. 3B and forming non-solder interconnects 132. The RDL 148 may include conductive pathways 196 between first conductive contacts 172 and second conductive contacts 174 on the RDL 148. The RDL 148 may be manufactured using any suitable technique, such as a PCB technique or a redistribution layer technique.

[0032] FIG. 3D illustrates an assembly subsequent to depositing a conductive material, such as copper, on a top surface of the assembly of FIG. 3C to generate conductive pillars 152. The conductive pillars 152 may be formed on and electrically coupled to the conductive contacts 174 on the RDL 148. The conductive pillars 152 may be formed using any suitable technique, for example, a lithographic process or an additive process, such as cold spray or 3-dimensional printing. The conductive pillars 152 may have any suitable dimensions. In some embodiments, the conductive pillars 152 may span one or more layers. For example, in some embodiments, an individual conductive pillar 152 may have an aspect ratio (height:diameter) between 1:1 and 4:1 (e.g., between 1:1 and 3:1). In some embodiments, an individual conductive pillar 152 may have a diameter (e.g., cross-section) between 10 microns and 150 microns. For example, an individual conductive pillar 152 may have a diameter between 50 microns and 100 microns. In some embodiments, an individual conductive pillar 152 may have a height (e.g., z-height or thickness) between 50 and 150 microns. The conductive pillars 152 may have any suitable cross-sectional shape, for example, square, triangular, and oval, among others.

[0033] FIG. 3E illustrates an assembly subsequent to placing dies 114-1, 114-4 on a top surface of the assembly of FIG. 3D and forming solder interconnects 130 between the dies 114-1, 114-4 and the conductive contacts 172 on the RDL 148. Any suitable method may be used to place the dies 114-1, 114-4, for example, automated pick-and-place. The dies 114-1, 114-4 may include first conductive contacts 122 and second conductive contacts 124. The die 114-4 may further include TSVs 117. In some embodiments, the first conductive contacts 122 may be formed on the dies 114-1, 114-2 subsequent to placing them on the assembly. In some embodiments, the first conductive contacts 122 may be formed on the dies 114-1, 114-4 prior to placing them on the assembly. The assembly of FIG. 3E may be subjected to a solder reflow process during which solder components of the

solder interconnects 130 melt and bond to mechanically and electrically couple the dies 114-1, 114-4 to the RDL 148.

[0034] FIG. 3F illustrates an assembly subsequent to depositing an insulating material 133 on and around the dies 114-1, 114-4 and the conductive pillars 152 to form the first layer 104-1. The insulating material 133 may include any suitable material and may be formed and removed using any suitable process, including as described above with reference to FIG. 3B. In some embodiments, the insulating material 133 in the first layer 104-1 (e.g., deposited in FIG. 3F) is different material than the insulating material 133 in the second layer 104-2 (e.g., deposited in FIG. 3B). In some embodiments, the insulating material 133 in the first layer 104-1 (e.g., deposited in FIG. 3F) is a same material as the insulating material 133 in the second layer 104-2 (e.g., deposited in FIG. 3B). In some embodiments, underfill 127 may be dispensed around the solder interconnects 130 prior to depositing the insulating material 133. In some embodiments, underfill 127 around the solder interconnects 130 may be omitted. In some embodiments, the insulating material 133 may be initially deposited on and over the top surface of the dies 114-1, 114-4 and the conductive pillars 152, then polished back to expose the top surface of the first conductive contacts 122 on the dies 114-1, 114-4 and the conductive pillars 152. If the insulating material 133 is formed to completely cover the dies 114-1, 114-4 and the conductive pillars 152, the insulating material 133 may be removed using any suitable technique, including grinding, or etching, such as a wet etch, a dry etch (e.g., a plasma etch), a wet blast, or a laser ablation (e.g., using excimer laser). In some embodiments, the thickness of the insulating material 133 may be minimized to reduce the etching time required. In some embodiments, the top surface of the insulating material 133 may be planarized using any suitable process, such as CMP. In some embodiments, an other RDL (not shown) may be formed on a top surface of the assembly of FIG. 3F. The other RDL may be formed using any suitable process, such as the process described above with reference to FIG. 3C.

[0035] FIG. 3G illustrates an assembly subsequent to inverting the assembly of FIG. 3F, removing the carrier 105, and performing finishing operations on the bottom surface of the assembly of FIG. 3G, such as forming conductive contacts 144, depositing solder resist (not shown), and depositing solder 134 on a bottom surface (e.g., at the first surface 170-1). If multiple assemblies are manufactured together, the assemblies may be singulated after removal of the carrier 105. The assembly of FIG. 3G may itself be a microelectronic assembly 100, as shown. Further manufacturing operations may be performed on the microelectronic assembly 100 of FIG. 3G to form other microelectronic assembly 100; for example, the solder 134 may be used to couple the microelectronic assembly 100 of FIG. 3G to a package substrate 102 via DTPS interconnects 150, similar to the microelectronic

assembly 100 of FIG. 1.

[0036] FIGS. 4A-4G are side, cross-sectional views of various stages in an example process for manufacturing the microelectronic assembly 100 of FIG. 2, in accordance with various embodiments. FIG. 4A illustrates an assembly subsequent to mounting dies 114-2, 114-3 on a first carrier 105-1 with a surface having conductive contacts 122 facing towards the first carrier 105-1. Any suitable method may be used to place the dies 114-2, 114-3 for example, automated pick-and-place. A carrier 105 may include any suitable material for providing mechanical stability during manufacturing operations, and in some embodiments, may include a semiconductor wafer (e.g., a silicon wafer) or glass (e.g., a glass panel). The dies 114-2, 114-3 may have a die-to-die gap 119 between 1 micron and 100 microns.

[0037] FIG. 4B illustrates an assembly subsequent to depositing an insulating material 133 on and around the dies 114-2, 114-3, and planarizing the top surface of the insulating material 133 and dies 114-2, 114-3 to form the second layer 104-2. The insulating material 133 may include any suitable material and may be formed and removed using any suitable process, including as described above with reference to FIG. 3.

[0038] FIG. 4C illustrates an assembly subsequent to mounting a second carrier 105-2 to the top surface of the assembly of FIG. 3B, removing the first carrier 105-1, and inverting the assembly.

[0039] FIG. 4D illustrates an assembly subsequent to forming an RDL 148 on a top surface of the assembly of FIG. 4C and forming non-solder interconnects 132. In some embodiments, the top surface of the assembly FIG. 4C may be cleaned and planarized using any suitable processes, for example, a dry or wet process to remove adhesive residue, followed by a mechanical grind and CMP to create an ultra smooth, planar die surface for forming RDL 148. The RDL 148 may include conductive pathways 196 between first conductive contacts 172 and second conductive contacts 174 on the RDL 148. The RDL 148 may be manufactured using any suitable technique, such as a PCB technique or a redistribution layer technique.

[0040] FIG. 4E illustrates an assembly subsequent to depositing a conductive material, such as copper, on a top surface of the assembly of FIG. 4D to generate conductive pillars 152, placing die 114-1, and forming solder interconnects 130 between the die 114-1 and the RDL 148. In particular, conductive contacts 124 on the die 114-1 may be coupled to conductive contacts 172 on the RDL 148 by solder to form solder interconnects 130. The die 114-1 may further include conductive contacts 122. In some embodiments, the conductive contacts 122 may be formed on the die 114-1 subsequent to placing the die on the assembly. In some embodiments, the first conductive contacts 122 may be formed on the die 114-1 prior to placing the die on the assembly. The assembly of FIG. 4E may be subjected to a solder reflow process during which solder components of the solder intercon-

nects 130 melt and bond to mechanically and electrically couple the die 114-1 to the RDL 148. The conductive pillars 152 may be formed using any suitable technique, for example, a lithographic process or an additive process, such as cold spray or 3-dimensional printing. The conductive pillars 152 may have any suitable dimensions. Any suitable method may be used to place the die 114-1, for example, automated pick-and-place. Any suitable method may be used to form the conductive pillars, for example, as described above with reference to FIG. 3.

[0041] FIG. 4F illustrates an assembly subsequent to depositing an insulating material 133 on and around the die 114-1 and the conductive pillars 152 to form the first layer 104-1. The insulating material 133 may include any suitable material and may be formed and removed using any suitable process, including as described above with reference to FIG. 3. In some embodiments, the insulating material 133 in the first layer 104-1 (e.g., deposited in FIG. 4F) is different material than the insulating material 133 in the second layer 104-2 (e.g., deposited in FIG. 4B). In some embodiments, the insulating material 133 in the first layer 104-1 (e.g., deposited in FIG. 4F) is a same material as the insulating material 133 in the second layer 104-2 (e.g., deposited in FIG. 4B). In some embodiments, underfill 127 may be dispensed around the solder interconnects 130 prior to depositing the insulating material 133. In some embodiments, underfill 127 around the solder interconnects 130 may be omitted. In some embodiments, an other RDL (not shown) may be formed on a top surface of the assembly of FIG. 4F. The other RDL may be formed using any suitable process, such as the process described above with reference to FIG. 4D.

[0042] FIG. 4G illustrates an assembly subsequent to inverting the assembly of FIG. 4F, removing the second carrier 105-2, and performing finishing operations on the bottom surface of the assembly of FIG. 4G, such as forming conductive contacts 144, depositing solder resist (not shown), and depositing solder 134 on a bottom surface (e.g., at the first surface 170-1). If multiple assemblies are manufactured together, the assemblies may be singulated after removal of the second carrier 105-2. The assembly of FIG. 4G may itself be a microelectronic assembly 100, as shown. Further manufacturing operations may be performed on the microelectronic assembly 100 of FIG. 4G to form other microelectronic assembly 100; for example, the solder 134 may be used to couple the microelectronic assembly 100 of FIG. 4G to a package substrate 102 via DTPS interconnects 150, similar to the microelectronic assembly 100 of FIG. 2.

[0043] FIG. 5 is a flow diagram of an example method of fabricating an example microelectronic assembly, in accordance with various embodiments. At 502, second layer dies 114-2, 114-3 may be attached to a carrier 105 with conductive contacts 122 facing away from the carrier 105. The second layer dies 114-2, 114-3 may be encapsulated with an insulating material 133 and planarized prior to being attached to the carrier 105 (e.g., as shown

in FIGS. 4A-4C) or may be encapsulated and planarized subsequent to being attached to the carrier 105 (e.g., as shown in FIGS. 3A and 3B).

[0044] At 504, an RDL 148 is formed on the top surface of the second layer dies 114-2, 114-3 and conductive contacts 174 on the RDL 148 are electrically coupled to conductive contacts 122 on the second layer dies 114-2, 114-3 by non-solder interconnects 132.

[0045] At 506, conductive pillars 152 are formed on a top surface of the RDL 148 and the conductive pillars 152 are electrically coupled to conductive contacts 172 on the RDL 148 by non-solder interconnects.

[0046] At 508, a first layer die 114-1 is attached to a top surface of the RDL 148 and conductive contacts 172 on the RDL 148 are electrically coupled to conductive contacts 124 on the first layer die 114-1 by solder interconnects 130. Underfill 127 may be disposed around the solder interconnects 130. The underfill process may include dispensing underfill material in liquid form, allowing the material to flow and fill interstitial gaps around the solder interconnects 130, and subjecting the assembly to a curing process, such as baking, to solidify the material.

[0047] At 510, an insulating material 133 may be disposed over the first layer die and conductive pillars 152 using any suitable method such that the insulating material 133 encapsulates the first layer die 114-1 and the conductive pillars 152. A top surface of the insulating material 133 may be planarized using CMP or any other suitable process. A grinding (also called grind back) process may substantially planarize and/or smooth a top surface of the assembly, for example, to enable attaching a heat sink or other component as appropriate. In some embodiments, an other RDL may be formed on a top surface of the insulating material encapsulating the first layer die.

[0048] At 512, carrier 105 may be detached using any suitable process and surface finishing operations may be performed. In some embodiments, surface finishing operations may be performed prior to removal of the carrier 105. Surface finishing operations may include, for example, forming conductive contacts 144, dispensing solder resist, and attaching solder balls 134 at a bottom surface of the multi-layer die assembly (e.g., at first surface 170-1).

[0049] The microelectronic assemblies 100 disclosed herein may be used for any suitable application. For example, in some embodiments, a microelectronic assembly 100 may be used to enable very small form factor voltage regulation for field programmable gate array (FPGA) or processing units (e.g., a central processing unit, a graphics processing unit, a FPGA, a modem, an applications processor, etc.) especially in mobile devices and small form factor devices. In another example, the die 114 in a microelectronic assembly 100 may be a processing device (e.g., a central processing unit, a graphics processing unit, a FPGA, a modem, an applications processor, a server processor, etc.).

[0050] The microelectronic assemblies 100 disclosed herein may be included in any suitable electronic component. FIGS. 6-9 illustrate various examples of apparatuses that may include, or be included in, any of the microelectronic assemblies 100 disclosed herein.

[0051] FIG. 6 is a top view of a wafer 1500 and dies 1502 that may be included in any of the microelectronic assemblies 100 disclosed herein (e.g., as any suitable ones of the dies 114). The wafer 1500 may be composed of semiconductor material and may include one or more dies 1502 having IC structures formed on a surface of the wafer 1500. Each of the dies 1502 may be a repeating unit of a semiconductor product that includes any suitable IC. After the fabrication of the semiconductor product is complete, the wafer 1500 may undergo a singulation process in which the dies 1502 are separated from one another to provide discrete "chips" of the semiconductor product. The die 1502 may be any of the dies 114 disclosed herein. The die 1502 may include one or more transistors (e.g., some of the transistors 1640 of FIG. 7, discussed below), supporting circuitry to route electrical signals to the transistors, passive components (e.g., signal traces, resistors, capacitors, or inductors), and/or any other IC components. In some embodiments, the wafer 1500 or the die 1502 may include a memory device (e.g., a random access memory (RAM) device, such as a static RAM (SRAM) device, a magnetic RAM (MRAM) device, a resistive RAM (RRAM) device, a conductive-bridging RAM (CBRAM) device, etc.), a logic device (e.g., an AND, OR, NAND, or NOR gate), or any other suitable circuit element. Multiple ones of these devices may be combined on a single die 1502. For example, a memory array formed by multiple memory devices may be formed on a same die 1502 as a processing device (e.g., the processing device 1802 of FIG. 9) or other logic that is configured to store information in the memory devices or execute instructions stored in the memory array. In some embodiments, a die 1502 (e.g., a die 114) may be a central processing unit, a radio frequency chip, a power converter, or a network processor. Various ones of the microelectronic assemblies 100 disclosed herein may be manufactured using a die-to-wafer assembly technique in which some dies 114 are attached to a wafer 1500 that include others of the dies 114, and the wafer 1500 is subsequently singulated.

[0052] FIG. 7 is a cross-sectional side view of an IC device 1600 that may be included in any of the microelectronic assemblies 100 disclosed herein (e.g., in any of the dies 114). One or more of the IC devices 1600 may be included in one or more dies 1502 (FIG. 6). The IC device 1600 may be formed on a die substrate 1602 (e.g., the wafer 1500 of FIG. 6) and may be included in a die (e.g., the die 1502 of FIG. 6). The die substrate 1602 may be a semiconductor substrate composed of semiconductor material systems including, for example, n-type or p-type materials systems (or a combination of both). The die substrate 1602 may include, for example, a crystalline substrate formed using a bulk silicon or a silicon-on-in-

ulator (SOI) substructure. In some embodiments, the die substrate 1602 may be formed using alternative materials, which may or may not be combined with silicon, that include, but are not limited to, germanium, indium antimonide, lead telluride, indium arsenide, indium phosphide, gallium arsenide, or gallium antimonide. Further materials classified as group II-VI, III-V, or IV may also be used to form the die substrate 1602. Although a few examples of materials from which the die substrate 1602 may be formed are described here, any material that may serve as a foundation for an IC device 1600 may be used. The die substrate 1602 may be part of a singulated die (e.g., the dies 1502 of FIG. 6) or a wafer (e.g., the wafer 1500 of FIG. 6).

[0053] The IC device 1600 may include one or more device layers 1604 disposed on the die substrate 1602. The device layer 1604 may include features of one or more transistors 1640 (e.g., metal oxide semiconductor field-effect transistors (MOSFETs)) formed on the die substrate 1602. The device layer 1604 may include, for example, one or more source and/or drain (S/D) regions 1620, a gate 1622 to control current flow in the transistors 1640 between the S/D regions 1620, and one or more S/D contacts 1624 to route electrical signals to/from the S/D regions 1620. The transistors 1640 may include additional features not depicted for the sake of clarity, such as device isolation regions, gate contacts, and the like. The transistors 1640 are not limited to the type and configuration depicted in FIG. 7 and may include a wide variety of other types and configurations such as, for example, planar transistors, non-planar transistors, or a combination of both. Non-planar transistors may include FinFET transistors, such as double-gate transistors or tri-gate transistors, and wrap-around or all-around gate transistors, such as nanoribbon and nanowire transistors.

[0054] Each transistor 1640 may include a gate 1622 formed of at least two layers, a gate dielectric and a gate electrode. The gate dielectric may include one layer or a stack of layers. The one or more layers may include silicon oxide, silicon dioxide, silicon carbide, and/or a high-k dielectric material. The high-k dielectric material may include elements such as hafnium, silicon, oxygen, titanium, tantalum, lanthanum, aluminum, zirconium, barium, strontium, yttrium, lead, scandium, niobium, and zinc. Examples of high-k materials that may be used in the gate dielectric include, but are not limited to, hafnium oxide, hafnium silicon oxide, lanthanum oxide, lanthanum aluminum oxide, zirconium oxide, zirconium silicon oxide, tantalum oxide, titanium oxide, barium strontium titanium oxide, barium titanium oxide, strontium titanium oxide, yttrium oxide, aluminum oxide, lead scandium tantalum oxide, and lead zinc niobate. In some embodiments, an annealing process may be carried out on the gate dielectric to improve its quality when a high-k material is used.

[0055] The gate electrode may be formed on the gate dielectric and may include at least one p-type work func-

tion metal or n-type work function metal, depending on whether the transistor 1640 is to be a PMOS or a NMOS transistor. In some implementations, the gate electrode may consist of a stack of two or more metal layers, where one or more metal layers are work function metal layers and at least one metal layer is a fill metal layer. Further metal layers may be included for other purposes, such as a barrier layer. For a PMOS transistor, metals that may be used for the gate electrode include, but are not limited to, ruthenium, palladium, platinum, cobalt, nickel, conductive metal oxides (e.g., ruthenium oxide), and any of the metals discussed below with reference to an NMOS transistor (e.g., for work function tuning). For an NMOS transistor, metals that may be used for the gate electrode include, but are not limited to, hafnium, zirconium, titanium, tantalum, aluminum, alloys of these metals, carbides of these metals (e.g., hafnium carbide, zirconium carbide, titanium carbide, tantalum carbide, and aluminum carbide), and any of the metals discussed above with reference to a PMOS transistor (e.g., for work function tuning).

[0056] In some embodiments, when viewed as a cross-section of the transistor 1640 along the source-channel-drain direction, the gate electrode may consist of a U-shaped structure that includes a bottom portion substantially parallel to the surface of the die substrate 1602 and two sidewall portions that are substantially perpendicular to the top surface of the die substrate 1602. In other embodiments, at least one of the metal layers that form the gate electrode may simply be a planar layer that is substantially parallel to the top surface of the die substrate 1602 and does not include sidewall portions substantially perpendicular to the top surface of the die substrate 1602. In other embodiments, the gate electrode may consist of a combination of U-shaped structures and planar, non-U-shaped structures. For example, the gate electrode may consist of one or more U-shaped metal layers formed atop one or more planar, non-U-shaped layers.

[0057] In some embodiments, a pair of sidewall spacers may be formed on opposing sides of the gate stack to bracket the gate stack. The sidewall spacers may be formed from materials such as silicon nitride, silicon oxide, silicon carbide, silicon nitride doped with carbon, and silicon oxynitride. Processes for forming sidewall spacers are well known in the art and generally include deposition and etching process steps. In some embodiments, a plurality of spacer pairs may be used; for instance, two pairs, three pairs, or four pairs of sidewall spacers may be formed on opposing sides of the gate stack.

[0058] The S/D regions 1620 may be formed within the die substrate 1602 adjacent to the gate 1622 of each transistor 1640. The S/D regions 1620 may be formed using an implantation/diffusion process or an etching/deposition process, for example. In the former process, dopants such as boron, aluminum, antimony, phosphorous, or arsenic may be ion-implanted into the die substrate 1602 to form the S/D regions 1620. An annealing process that activates the dopants and causes them to diffuse farther into the die substrate 1602 may follow

the ion-implantation process. In the latter process, the die substrate 1602 may first be etched to form recesses at the locations of the S/D regions 1620. An epitaxial deposition process may then be carried out to fill the recesses with material that is used to fabricate the S/D regions 1620. In some implementations, the S/D regions 1620 may be fabricated using a silicon alloy such as silicon germanium or silicon carbide. In some embodiments, the epitaxially deposited silicon alloy may be doped in situ with dopants such as boron, arsenic, or phosphorous. In some embodiments, the S/D regions 1620 may be formed using one or more alternate semiconductor materials such as germanium or a group III-V material or alloy. In further embodiments, one or more layers of metal and/or metal alloys may be used to form the S/D regions 1620.

[0059] Electrical signals, such as power and/or input/output (I/O) signals, may be routed to and/or from the devices (e.g., transistors 1640) of the device layer 1604 through one or more interconnect layers disposed on the device layer 1604 (illustrated in FIG. 7 as interconnect layers 1606-1610). For example, electrically conductive features of the device layer 1604 (e.g., the gate 1622 and the S/D contacts 1624) may be electrically coupled with the interconnect structures 1628 of the interconnect layers 1606-1610. The one or more interconnect layers 1606-1610 may form a metallization stack (also referred to as an "ILD stack") 1619 of the IC device 1600.

[0060] The interconnect structures 1628 may be arranged within the interconnect layers 1606-1610 to route electrical signals according to a wide variety of designs; in particular, the arrangement is not limited to the particular configuration of interconnect structures 1628 depicted in FIG. 7. Although a particular number of interconnect layers 1606-1610 is depicted in FIG. 7, embodiments of the present disclosure include IC devices having more or fewer interconnect layers than depicted.

[0061] In some embodiments, the interconnect structures 1628 may include lines 1628a and/or vias 1628b filled with an electrically conductive material such as a metal. The lines 1628a may be arranged to route electrical signals in a direction of a plane that is substantially parallel with a surface of the die substrate 1602 upon which the device layer 1604 is formed. For example, the lines 1628a may route electrical signals in a direction in and out of the page from the perspective of FIG. 7. The vias 1628b may be arranged to route electrical signals in a direction of a plane that is substantially perpendicular to the surface of the die substrate 1602 upon which the device layer 1604 is formed. In some embodiments, the vias 1628b may electrically couple lines 1628a of different interconnect layers 1606-1610 together.

[0062] The interconnect layers 1606-1610 may include a dielectric material 1626 disposed between the interconnect structures 1628, as shown in FIG. 7. In some embodiments, the dielectric material 1626 disposed between the interconnect structures 1628 in different ones of the interconnect layers 1606-1610 may have different

compositions; in other embodiments, the composition of the dielectric material 1626 between different interconnect layers 1606-1610 may be the same.

[0063] A first interconnect layer 1606 (referred to as Metal 1 or "M1") may be formed directly on the device layer 1604. In some embodiments, the first interconnect layer 1606 may include lines 1628a and/or vias 1628b, as shown. The lines 1628a of the first interconnect layer 1606 may be coupled with contacts (e.g., the S/D contacts 1624) of the device layer 1604.

[0064] A second interconnect layer 1608 (referred to as Metal 2 or "M2") may be formed directly on the first interconnect layer 1606. In some embodiments, the second interconnect layer 1608 may include vias 1628b to couple the lines 1628a of the second interconnect layer 1608 with the lines 1628a of the first interconnect layer 1606. Although the lines 1628a and the vias 1628b are structurally delineated with a line within each interconnect layer (e.g., within the second interconnect layer 1608) for the sake of clarity, the lines 1628a and the vias 1628b may be structurally and/or materially contiguous (e.g., simultaneously filled during a dual damascene process) in some embodiments.

[0065] A third interconnect layer 1610 (referred to as Metal 3 or "M3") (and additional interconnect layers, as desired) may be formed in succession on the second interconnect layer 1608 according to similar techniques and configurations described in connection with the second interconnect layer 1608 or the first interconnect layer 1606. In some embodiments, the interconnect layers that are "higher up" in the metallization stack 1619 in the IC device 1600 (i.e., farther away from the device layer 1604) may be thicker.

[0066] The IC device 1600 may include a solder resist material 1634 (e.g., polyimide or similar material) and one or more conductive contacts 1636 formed on the interconnect layers 1606-1610. In FIG. 7, the conductive contacts 1636 are illustrated as taking the form of bond pads. The conductive contacts 1636 may be electrically coupled with the interconnect structures 1628 and configured to route the electrical signals of the transistor(s) 1640 to other external devices. For example, solder bonds may be formed on the one or more conductive contacts 1636 to mechanically and/or electrically couple a chip including the IC device 1600 with another component (e.g., a circuit board). The IC device 1600 may include additional or alternate structures to route the electrical signals from the interconnect layers 1606-1610; for example, the conductive contacts 1636 may include other analogous features (e.g., posts) that route the electrical signals to external components.

[0067] In some embodiments in which the IC device 1600 is a double-sided die (e.g., like the die 114-1), the IC device 1600 may include another metallization stack (not shown) on the opposite side of the device layer(s) 1604. This metallization stack may include multiple interconnect layers as discussed above with reference to the interconnect layers 1606-1610, to provide conductive

pathways (e.g., including conductive lines and vias) between the device layer(s) 1604 and additional conductive contacts (not shown) on the opposite side of the IC device 1600 from the conductive contacts 1636.

[0068] In other embodiments in which the IC device 1600 is a double-sided die (e.g., like the die 114-1), the IC device 1600 may include one or more TSVs through the die substrate 1602; these TSVs may make contact with the device layer(s) 1604, and may provide conductive pathways between the device layer(s) 1604 and additional conductive contacts (not shown) on the opposite side of the IC device 1600 from the conductive contacts 1636.

[0069] FIG. 8 is a cross-sectional side view of an IC device assembly 1700 that may include any of the microelectronic assemblies 100 disclosed herein. In some embodiments, the IC device assembly 1700 may be a microelectronic assembly 100. The IC device assembly 1700 includes a number of components disposed on a circuit board 1702 (which may be, e.g., a motherboard). The IC device assembly 1700 includes components disposed on a first face 1740 of the circuit board 1702 and an opposing second face 1742 of the circuit board 1702; generally, components may be disposed on one or both faces 1740 and 1742. Any of the IC packages discussed below with reference to the IC device assembly 1700 may take the form of any suitable ones of the embodiments of the microelectronic assemblies 100 disclosed herein.

[0070] In some embodiments, the circuit board 1702 may be a PCB including multiple metal layers separated from one another by layers of dielectric material and interconnected by electrically conductive vias. Any one or more of the metal layers may be formed in a desired circuit pattern to route electrical signals (optionally in conjunction with other metal layers) between the components coupled to the circuit board 1702. In other embodiments, the circuit board 1702 may be a non-PCB substrate. In some embodiments the circuit board 1702 may be, for example, a circuit board.

[0071] The IC device assembly 1700 illustrated in FIG. 8 includes a package-on-interposer structure 1736 coupled to the first face 1740 of the circuit board 1702 by coupling components 1716. The coupling components 1716 may electrically and mechanically couple the package-on-interposer structure 1736 to the circuit board 1702, and may include solder balls (as shown in FIG. 8), male and female portions of a socket, an adhesive, an underfill material, and/or any other suitable electrical and/or mechanical coupling structure.

[0072] The package-on-interposer structure 1736 may include an IC package 1720 coupled to an interposer 1704 by coupling components 1718. The coupling components 1718 may take any suitable form for the application, such as the forms discussed above with reference to the coupling components 1716. Although a single IC package 1720 is shown in FIG. 8, multiple IC packages may be coupled to the interposer 1704; indeed, additional

interposers may be coupled to the interposer 1704. The interposer 1704 may provide an intervening substrate used to bridge the circuit board 1702 and the IC package 1720. The IC package 1720 may be or include, for example, a die (the die 1502 of FIG. 6), an IC device (e.g., the IC device 1600 of FIG. 7), or any other suitable component. Generally, the interposer 1704 may spread a connection to a wider pitch or reroute a connection to a different connection. For example, the interposer 1704 may couple the IC package 1720 (e.g., a die) to a set of ball grid array (BGA) conductive contacts of the coupling components 1716 for coupling to the circuit board 1702. In the embodiment illustrated in FIG. 8, the IC package 1720 and the circuit board 1702 are attached to opposing sides of the interposer 1704; in other embodiments, the IC package 1720 and the circuit board 1702 may be attached to a same side of the interposer 1704. In some embodiments, three or more components may be interconnected by way of the interposer 1704.

[0073] In some embodiments, the interposer 1704 may be formed as a PCB, including multiple metal layers separated from one another by layers of dielectric material and interconnected by electrically conductive vias. In some embodiments, the interposer 1704 may be formed of an epoxy resin, a fiberglass-reinforced epoxy resin, an epoxy resin with inorganic fillers, a ceramic material, or a polymer material such as polyimide. In some embodiments, the interposer 1704 may be formed of alternate rigid or flexible materials that may include the same materials described above for use in a semiconductor substrate, such as silicon, germanium, and other group III-V and group IV materials. The interposer 1704 may include metal interconnects 1708 and vias 1710, including but not limited to TSVs 1706. The interposer 1704 may further include embedded devices 1714, including both passive and active devices. Such devices may include, but are not limited to, capacitors, decoupling capacitors, resistors, inductors, fuses, diodes, transformers, sensors, electrostatic discharge (ESD) devices, and memory devices. More complex devices such as radio frequency devices, power amplifiers, power management devices, antennas, arrays, sensors, and microelectromechanical systems (MEMS) devices may also be formed on the interposer 1704. The package-on-interposer structure 1736 may take the form of any of the package-on-interposer structures known in the art.

[0074] The IC device assembly 1700 may include an IC package 1724 coupled to the first face 1740 of the circuit board 1702 by coupling components 1722. The coupling components 1722 may take the form of any of the embodiments discussed above with reference to the coupling components 1716, and the IC package 1724 may take the form of any of the embodiments discussed above with reference to the IC package 1720.

[0075] The IC device assembly 1700 illustrated in FIG. 8 includes a package-on-package structure 1734 coupled to the second face 1742 of the circuit board 1702 by coupling components 1728. The package-on-pack-

age structure 1734 may include an IC package 1726 and an IC package 1732 coupled together by coupling components 1730 such that the IC package 1726 is disposed between the circuit board 1702 and the IC package 1732. The coupling components 1728 and 1730 may take the form of any of the embodiments of the coupling components 1716 discussed above, and the IC packages 1726 and 1732 may take the form of any of the embodiments of the IC package 1720 discussed above. The package-on-package structure 1734 may be configured in accordance with any of the package-on-package structures known in the art.

[0076] FIG. 9 is a block diagram of an example electrical device 1800 that may include one or more of the microelectronic assemblies 100 disclosed herein. For example, any suitable ones of the components of the electrical device 1800 may include one or more of the IC device assemblies 1700, IC devices 1600, or dies 1502 disclosed herein, and may be arranged in any of the microelectronic assemblies 100 disclosed herein. A number of components are illustrated in FIG. 9 as included in the electrical device 1800, but any one or more of these components may be omitted or duplicated, as suitable for the application. In some embodiments, some or all of the components included in the electrical device 1800 may be attached to one or more motherboards. In some embodiments, some or all of these components are fabricated onto a single system-on-a-chip (SoC) die.

[0077] Additionally, in various embodiments, the electrical device 1800 may not include one or more of the components illustrated in FIG. 9, but the electrical device 1800 may include interface circuitry for coupling to the one or more components. For example, the electrical device 1800 may not include a display device 1806, but may include display device interface circuitry (e.g., a connector and driver circuitry) to which a display device 1806 may be coupled. In another set of examples, the electrical device 1800 may not include an audio input device 1824 or an audio output device 1808, but may include audio input or output device interface circuitry (e.g., connectors and supporting circuitry) to which an audio input device 1824 or audio output device 1808 may be coupled.

[0078] The electrical device 1800 may include a processing device 1802 (e.g., one or more processing devices). As used herein, the term "processing device" or "processor" may refer to any device or portion of a device that processes electronic data from registers and/or memory to transform that electronic data into other electronic data that may be stored in registers and/or memory. The processing device 1802 may include one or more digital signal processors (DSPs), application-specific ICs (ASICs), central processing units (CPUs), graphics processing units (GPUs), cryptoprocessors (specialized processors that execute cryptographic algorithms within hardware), server processors, or any other suitable processing devices. The electrical device 1800 may include a memory 1804, which may itself include one or more memory devices such as volatile memory

(e.g., dynamic random access memory (DRAM)), non-volatile memory (e.g., read-only memory (ROM)), flash memory, solid state memory, and/or a hard drive. In some embodiments, the memory 1804 may include memory that shares a die with the processing device 1802. This memory may be used as cache memory and may include embedded dynamic random access memory (eDRAM) or spin transfer torque magnetic random access memory (STT-MRAM).

[0079] In some embodiments, the electrical device 1800 may include a communication chip 1812 (e.g., one or more communication chips). For example, the communication chip 1812 may be configured for managing wireless communications for the transfer of data to and from the electrical device 1800. The term "wireless" and its derivatives may be used to describe circuits, devices, systems, methods, techniques, communications channels, etc., that may communicate data through the use of modulated electromagnetic radiation through a non-solid medium. The term does not imply that the associated devices do not contain any wires, although in some embodiments they might not.

[0080] The communication chip 1812 may implement any of a number of wireless standards or protocols, including but not limited to Institute for Electrical and Electronic Engineers (IEEE) standards including Wi-Fi (IEEE 802.11 family), IEEE 802.16 standards (e.g., IEEE 802.16-2005 Amendment), Long-Term Evolution (LTE) project along with any amendments, updates, and/or revisions (e.g., advanced LTE project, ultra mobile broadband (UMB) project (also referred to as "3GPP2"), etc.). IEEE 802.16 compatible Broadband Wireless Access (BWA) networks are generally referred to as WiMAX networks, an acronym that stands for Worldwide Interoperability for Microwave Access, which is a certification mark for products that pass conformity and interoperability tests for the IEEE 802.16 standards. The communication chip 1812 may operate in accordance with a Global System for Mobile Communication (GSM), General Packet Radio Service (GPRS), Universal Mobile Telecommunications System (UMTS), High Speed Packet Access (HSPA), Evolved HSPA (E-HSPA), or LTE network. The communication chip 1812 may operate in accordance with Enhanced Data for GSM Evolution (EDGE), GSM EDGE Radio Access Network (GERAN), Universal Terrestrial Radio Access Network (UTRAN), or Evolved UTRAN (E-UTRAN). The communication chip 1812 may operate in accordance with Code Division Multiple Access (CDMA), Time Division Multiple Access (TDMA), Digital Enhanced Cordless Telecommunications (DECT), Evolution-Data Optimized (EV-DO), and derivatives thereof, as well as any other wireless protocols that are designated as 3G, 4G, 5G, and beyond. The communication chip 1812 may operate in accordance with other wireless protocols in other embodiments. The electrical device 1800 may include an antenna 1822 to facilitate wireless communications and/or to receive other wireless communications (such as AM or FM radio

transmissions).

[0081] In some embodiments, the communication chip 1812 may manage wired communications, such as electrical, optical, or any other suitable communication protocols (e.g., the Ethernet). As noted above, the communication chip 1812 may include multiple communication chips. For instance, a first communication chip 1812 may be dedicated to shorter-range wireless communications such as Wi-Fi or Bluetooth, and a second communication chip 1812 may be dedicated to longer-range wireless communications such as global positioning system (GPS), EDGE, GPRS, CDMA, WiMAX, LTE, EV-DO, or others. In some embodiments, a first communication chip 1812 may be dedicated to wireless communications, and a second communication chip 1812 may be dedicated to wired communications.

[0082] The electrical device 1800 may include battery/power circuitry 1814. The battery/power circuitry 1814 may include one or more energy storage devices (e.g., batteries or capacitors) and/or circuitry for coupling components of the electrical device 1800 to an energy source separate from the electrical device 1800 (e.g., AC line power).

[0083] The electrical device 1800 may include a display device 1806 (or corresponding interface circuitry, as discussed above). The display device 1806 may include any visual indicators, such as a heads-up display, a computer monitor, a projector, a touchscreen display, a liquid crystal display (LCD), a light-emitting diode display, or a flat panel display.

[0084] The electrical device 1800 may include an audio output device 1808 (or corresponding interface circuitry, as discussed above). The audio output device 1808 may include any device that generates an audible indicator, such as speakers, headsets, or earbuds.

[0085] The electrical device 1800 may include an audio input device 1824 (or corresponding interface circuitry, as discussed above). The audio input device 1824 may include any device that generates a signal representative of a sound, such as microphones, microphone arrays, or digital instruments (e.g., instruments having a musical instrument digital interface (MIDI) output).

[0086] The electrical device 1800 may include a GPS device 1818 (or corresponding interface circuitry, as discussed above). The GPS device 1818 may be in communication with a satellite-based system and may receive a location of the electrical device 1800, as known in the art.

[0087] The electrical device 1800 may include an other output device 1810 (or corresponding interface circuitry, as discussed above). Examples of the other output device 1810 may include an audio codec, a video codec, a printer, a wired or wireless transmitter for providing information to other devices, or an additional storage device.

[0088] The electrical device 1800 may include an other input device 1820 (or corresponding interface circuitry, as discussed above). Examples of the other input device 1820 may include an accelerometer, a gyroscope, a com-

pass, an image capture device, a keyboard, a cursor control device such as a mouse, a stylus, a touchpad, a bar code reader, a Quick Response (QR) code reader, any sensor, or a radio frequency identification (RFID) reader.

[0089] The electrical device 1800 may have any desired form factor, such as a computing device or a handheld, portable or mobile computing device (e.g., a cell phone, a smart phone, a mobile internet device, a music player, a tablet computer, a laptop computer, a netbook computer, an ultrabook computer, a personal digital assistant (PDA), an ultra mobile personal computer, etc.), a desktop electrical device, a server, or other networked computing component, a printer, a scanner, a monitor, a set-top box, an entertainment control unit, a vehicle control unit, a digital camera, a digital video recorder, or a wearable computing device. In some embodiments, the electrical device 1800 may be any other electronic device that processes data.

[0090] The following paragraphs provide various examples of the embodiments disclosed herein.

[0091] Example 1 is a microelectronic assembly, including a first die, having a first surface and an opposing second surface, in a first layer; a redistribution layer (RDL) on the first layer, wherein the RDL is electrically coupled to the second surface of the first die by solder interconnects, and a second die in a second layer on the RDL, wherein the second die is electrically coupled to the RDL by non-solder interconnects.

[0092] Example 2 may include the subject matter of Example 1, and may further specify that the first die is electrically coupled to the second die by the solder interconnects, conductive pathways in the RDL, and the non-solder interconnects.

[0093] Example 3 may include the subject matter of Example 1 or 2, and may further specify that the non-solder interconnects include metal-to-metal interconnects.

[0094] Example 4 may include the subject matter of any of Examples 1-3, and may further specify that a pitch of the solder interconnects is between 10 and 100 microns.

[0095] Example 5 may include the subject matter of any of Examples 1-4, and may further specify that a pitch of the non-solder interconnects is between 50 and 150 microns.

[0096] Example 6 may include the subject matter of any of Examples 1-5, and may further specify that the first layer and the second layer include one or more insulating materials.

[0097] Example 7 may include the subject matter of any of Examples 1-6, and may further specify that the solder interconnects are first solder interconnects, and the microelectronic assembly and may further include a package substrate electrically coupled to the first surface of the first die by second solder interconnects.

[0098] Example 8 may include the subject matter of any of Examples 1-7, and may further specify that the non-solder interconnects are first non-solder intercon-

nects, and the microelectronic assembly and may further include a conductive pillar in the first layer, wherein the conductive pillar is coupled to the RDL by second non-solder interconnects.

[0099] Example 9 may include the subject matter of any of Examples 1-8, and may further include a third die, having a first surface, an opposing second surface, and through-substrate vias (TSVs) between the first and second surfaces, in the first layer within a footprint of the second die, wherein the third die is electrically coupled to the RDL by solder interconnects.

[0100] Example 10 is a microelectronic assembly, including a first die, having a first surface with first conductive contacts and an opposing second surface with second conductive contacts, in a first layer; a redistribution layer (RDL), having a first surface with third conductive contacts and an opposing second surface with fourth conductive contacts, on the first layer, wherein the third conductive contacts on the RDL are electrically coupled to the second conductive contacts on the first die by solder interconnects, and a second die, having a surface with fifth conductive contacts, in a second layer on the second surface of the RDL, wherein the fifth conductive contacts on the second die are electrically coupled to the fourth conductive contacts on the RDL by non-solder interconnects.

[0101] Example 11 may include the subject matter of Example 10, and may further specify that the fifth conductive contacts are recessed or flush with the surface of the second die.

[0102] Example 12 may include the subject matter of Example 10 or 11, and may further specify that the fifth conductive contacts extend away from the surface of the second die.

[0103] Example 13 may include the subject matter of any of Examples 10-12, and may further specify that the first die is electrically coupled to the second die by the solder interconnects, conductive pathways in the RDL, and the non-solder interconnects.

[0104] Example 14 may include the subject matter of any of Examples 10-13, and may further specify that the non-solder interconnects include metal-to-metal interconnects.

[0105] Example 15 may include the subject matter of any of Examples 10-14, and may further specify that a pitch of the solder interconnects is between 10 and 100 microns.

[0106] Example 16 may include the subject matter of any of Examples 10-15, and may further specify that a pitch of the non-solder interconnects is between 50 and 150 microns.

[0107] Example 17 may include the subject matter of any of Examples 10-16, and may further specify that the solder interconnects are first solder interconnects, and the microelectronic assembly and may further include a package substrate electrically coupled to the first conductive contacts of the first die by second solder interconnects.

[0108] Example 18 may include the subject matter of any of Examples 10-17, and may further include a conductive pillar in the first layer, wherein the conductive pillar is coupled to a respective one of the third conductive contacts on the RDL by a non-solder interconnect.

[0109] Example 19 may include the subject matter of any of Examples 10-18, and may further specify that the non-solder interconnects are first non-solder interconnects, and the microelectronic assembly and may further include a third die, having a surface with sixth conductive contacts, in the second layer, wherein the sixth conductive contacts on the third die are electrically coupled to the fourth conductive contacts on the RDL by second non-solder interconnects.

[0110] Example 20 may include the subject matter of Example 19, and may further specify that the first die is electrically coupled to the third die by the solder interconnects, conductive pathways in the RDL, and the second non-solder interconnects.

[0111] Example 21 is a method of manufacturing a microelectronic assembly, including encapsulating a first die having first conductive contacts and a second die having second conductive contacts with an insulating material and exposing the first and second conductive contacts; forming a redistribution layer (RDL) on the first and second dies and electrically coupling the RDL to the first and second conductive contacts by non-solder interconnects; attaching a third die having third conductive contacts to the RDL and electrically coupling the third conductive contacts on the third die to the RDL by solder interconnects; and forming an insulating material around the third die.

[0112] Example 22 may include the subject matter of Example 21, and may further specify that the first conductive contacts are recessed or flush with a surface of the first die.

[0113] Example 23 may include the subject matter of Example 21 or 22, and may further specify that the first conductive contacts extend from a surface of the first die.

[0114] Example 24 may include the subject matter of any of Examples 21-23, and may further include forming a conductive pillar on the RDL prior to forming the insulating material around the third die; and forming an insulating material around the conductive pillar and the third die.

Claims

1. A microelectronic assembly, comprising:

a first die, having a first surface and an opposing second surface, in a first layer;
a redistribution layer (RDL) on the first layer, wherein the RDL is electrically coupled to the second surface of the first die by solder interconnects, and
a second die in a second layer on the RDL,

wherein the second die is electrically coupled to the RDL by non-solder interconnects.

2. The microelectronic assembly of claim 1, wherein the first die is electrically coupled to the second die by the solder interconnects, conductive pathways in the RDL, and the non-solder interconnects. 5
3. The microelectronic assembly of claim 1 or 2, wherein the non-solder interconnects include metal-to-metal interconnects. 10
4. The microelectronic assembly of any one of claims 1-3, wherein a pitch of the solder interconnects is between 10 and 100 microns. 15
5. The microelectronic assembly of any one of claims 1-4, wherein a pitch of the non-solder interconnects is between 50 and 150 microns. 20
6. The microelectronic assembly of any one of claims 1-5, wherein the first layer and the second layer include one or more insulating materials. 25
7. The microelectronic assembly of any one of claims 1-6, wherein the solder interconnects are first solder interconnects, and the microelectronic assembly further comprising:
a package substrate electrically coupled to the first surface of the first die by second solder interconnects. 30
8. The microelectronic assembly of any one of claims 1-7, wherein the non-solder interconnects are first non-solder interconnects, and the microelectronic assembly further comprising:
a conductive pillar in the first layer, wherein the conductive pillar is coupled to the RDL by second non-solder interconnects. 35
40
9. The microelectronic assembly of any one of claims 1-8, further comprising:
a third die, having a first surface, an opposing second surface, and through-substrate vias (TSVs) between the first and second surfaces, in the first layer within a footprint of the second die, wherein the third die is electrically coupled to the RDL by solder interconnects. 45
10. The microelectronic assembly of any one of claims 1-9, wherein the second die includes conductive contacts electrically coupled to the RDL by the non-solder interconnects and the conductive contacts are recessed or flush with the surface of the second die. 50
55
11. The microelectronic assembly of any one of claims 1-9, wherein the second die includes conductive contacts electrically coupled to the RDL by the non-sol-

der interconnects and the conductive contacts extend away from the surface of the second die.

12. A method of manufacturing a microelectronic assembly, comprising:

encapsulating a first die having first conductive contacts and a second die having second conductive contacts with an insulating material and exposing the first and second conductive contacts;
forming a redistribution layer (RDL) on the first and second dies and electrically coupling the RDL to the first and second conductive contacts by non-solder interconnects;
attaching a third die having third conductive contacts to the RDL and electrically coupling the third conductive contacts on the third die to the RDL by solder interconnects; and
forming an insulating material around the third die.
13. The method of claim 12, wherein the first conductive contacts are recessed or flush with a surface of the first die.
14. The method of claim 12, wherein the first conductive contacts extend from a surface of the first die.
15. The method of any one of claims 12-14, further comprising:

forming a conductive pillar on the RDL prior to forming the insulating material around the third die; and
forming an insulating material around the conductive pillar and the third die.

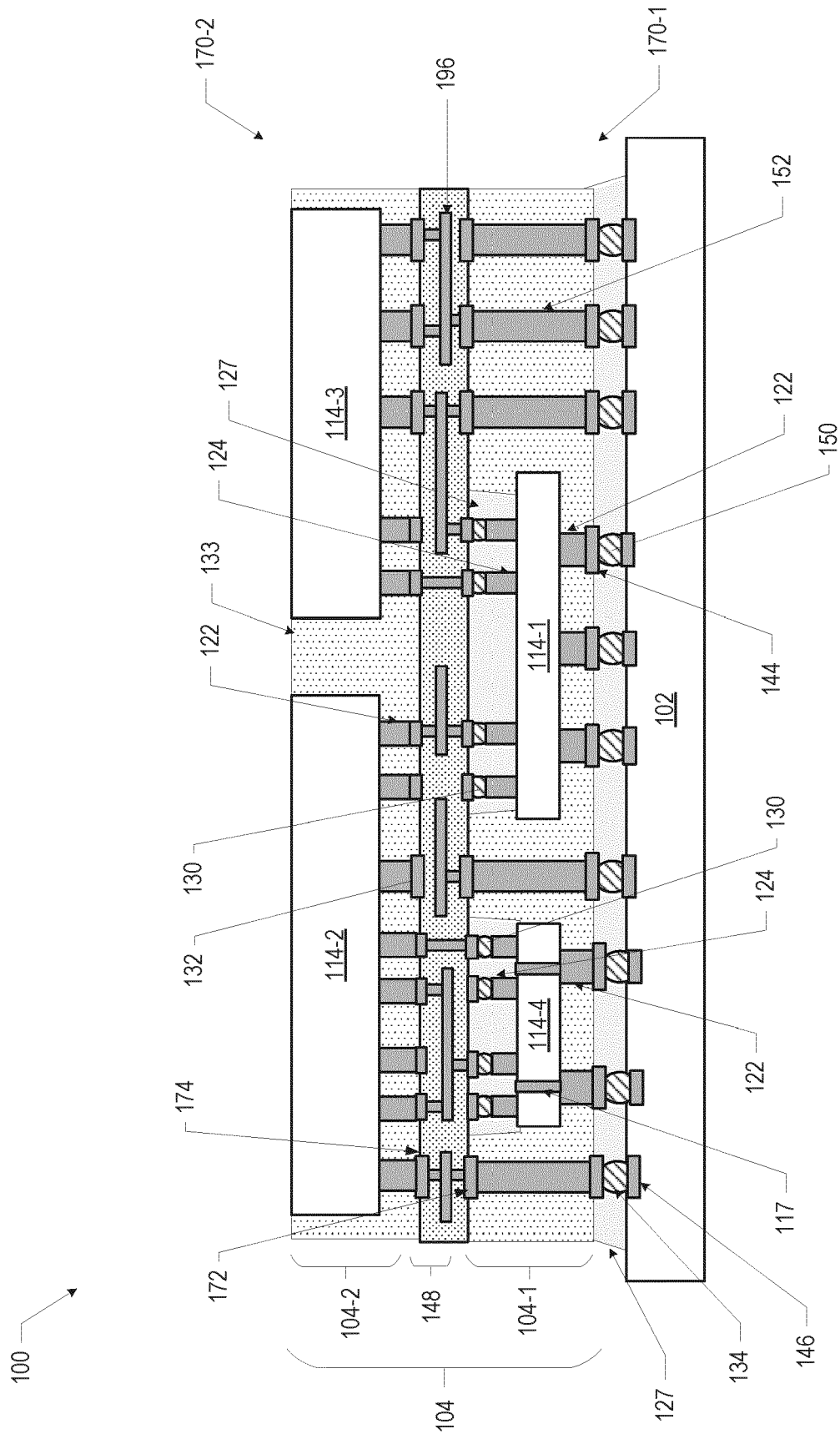


FIG. 1

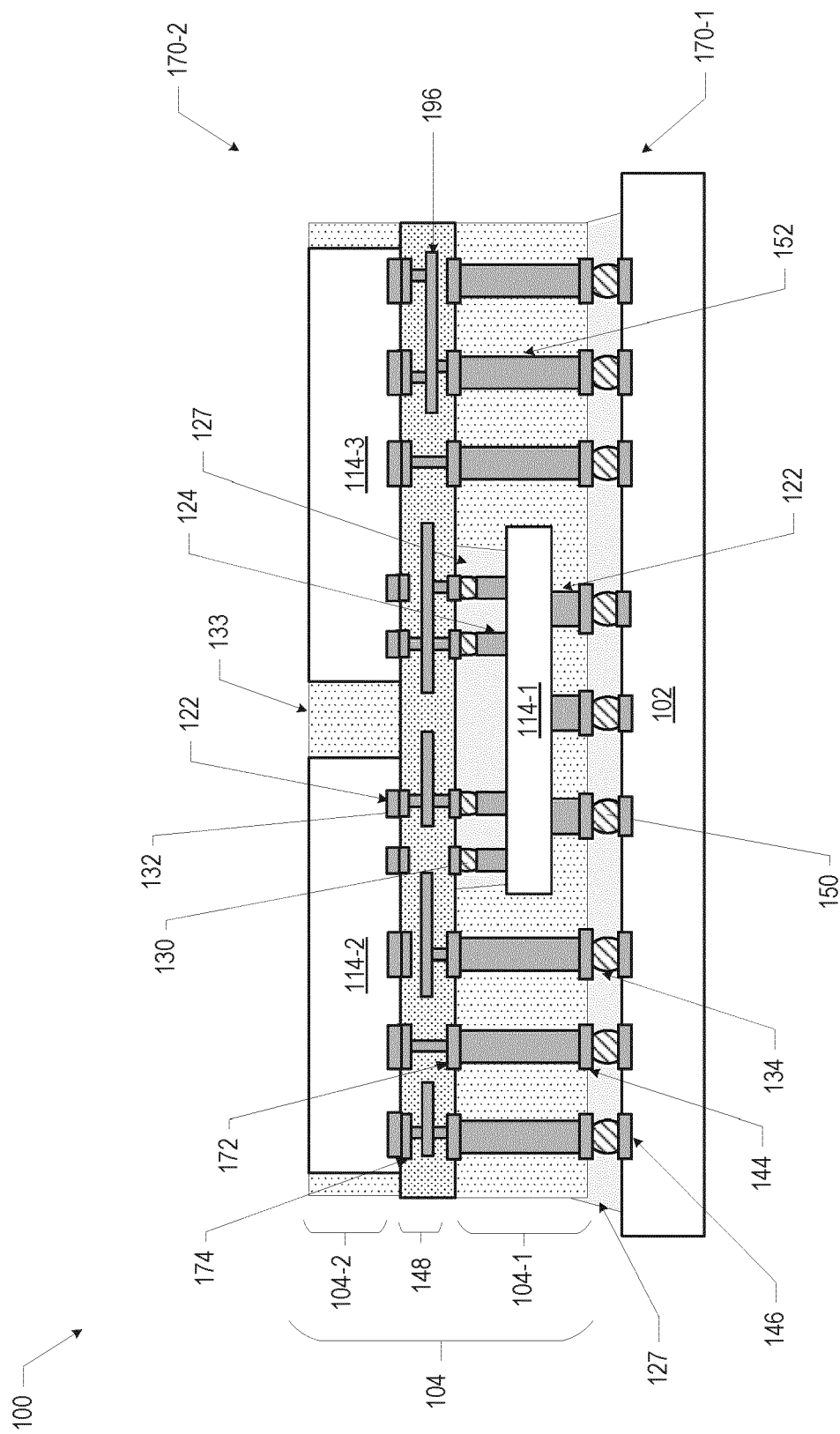


FIG. 2

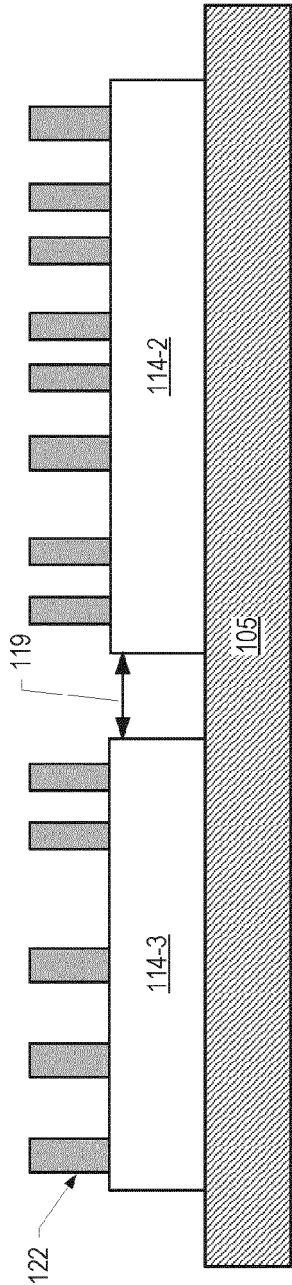


FIG. 3A

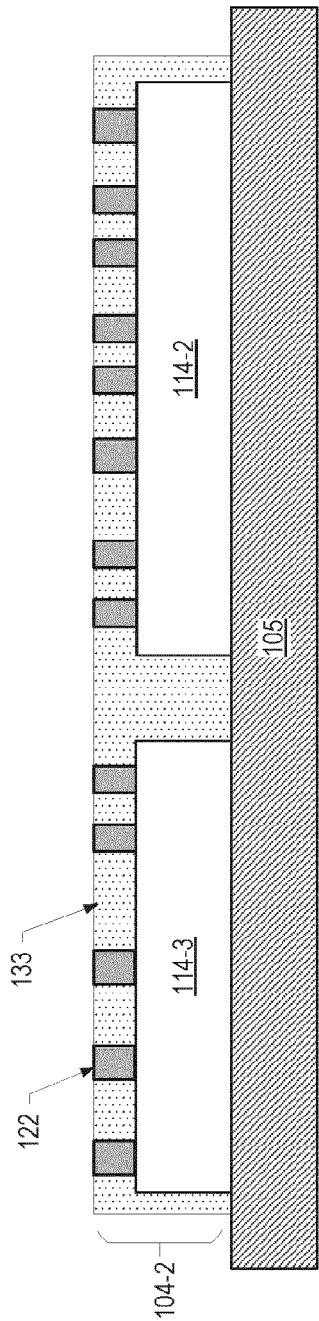


FIG. 3B

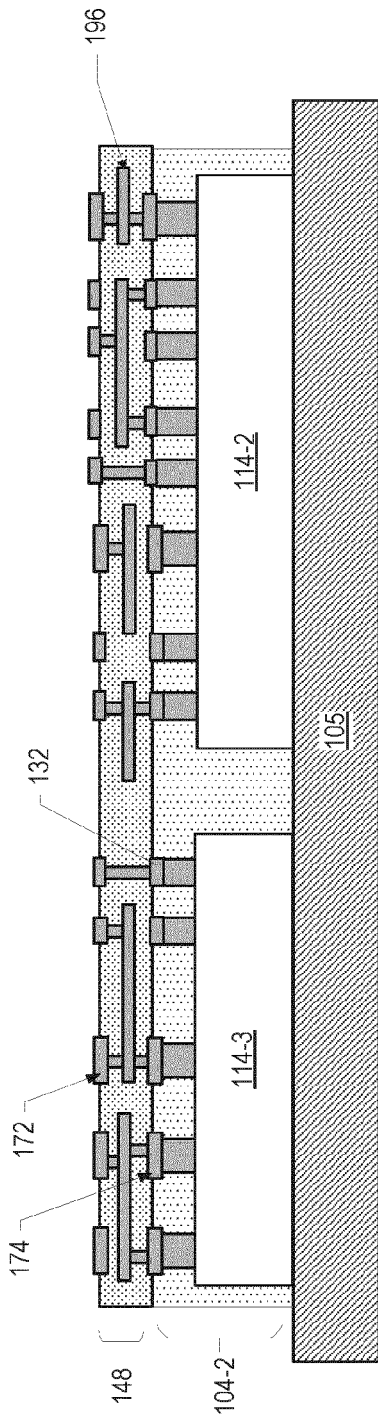


FIG. 3C

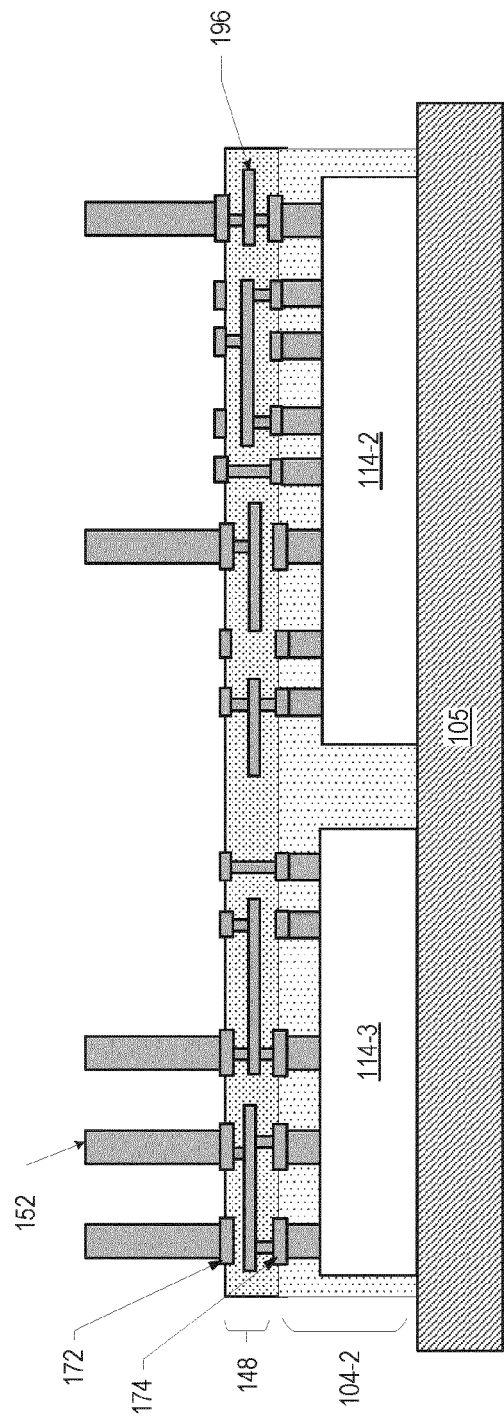


FIG. 3D

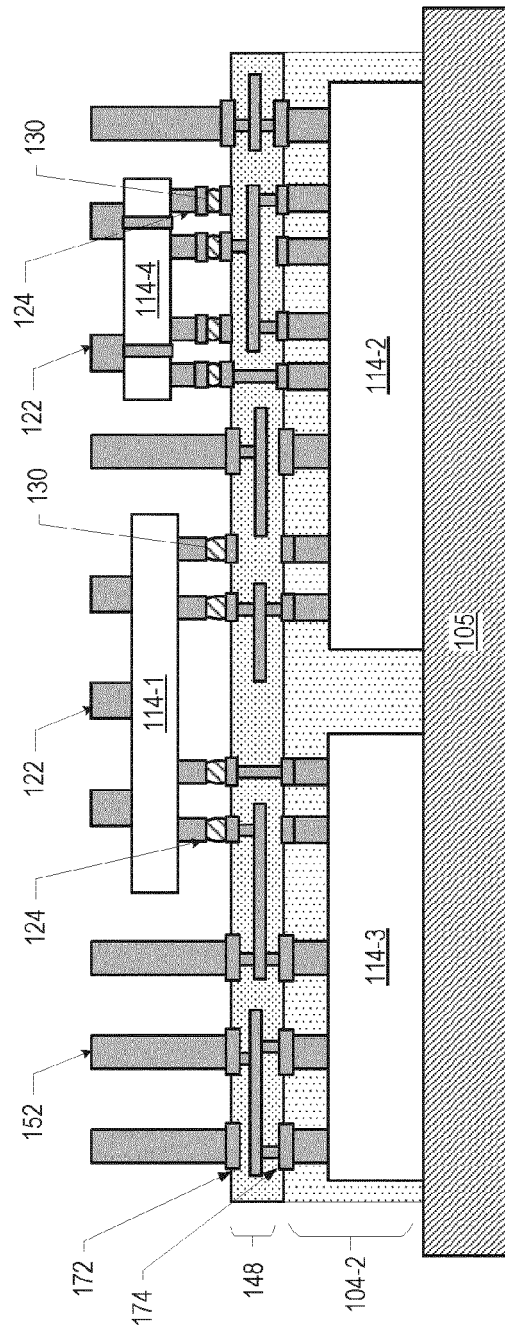


FIG. 3E

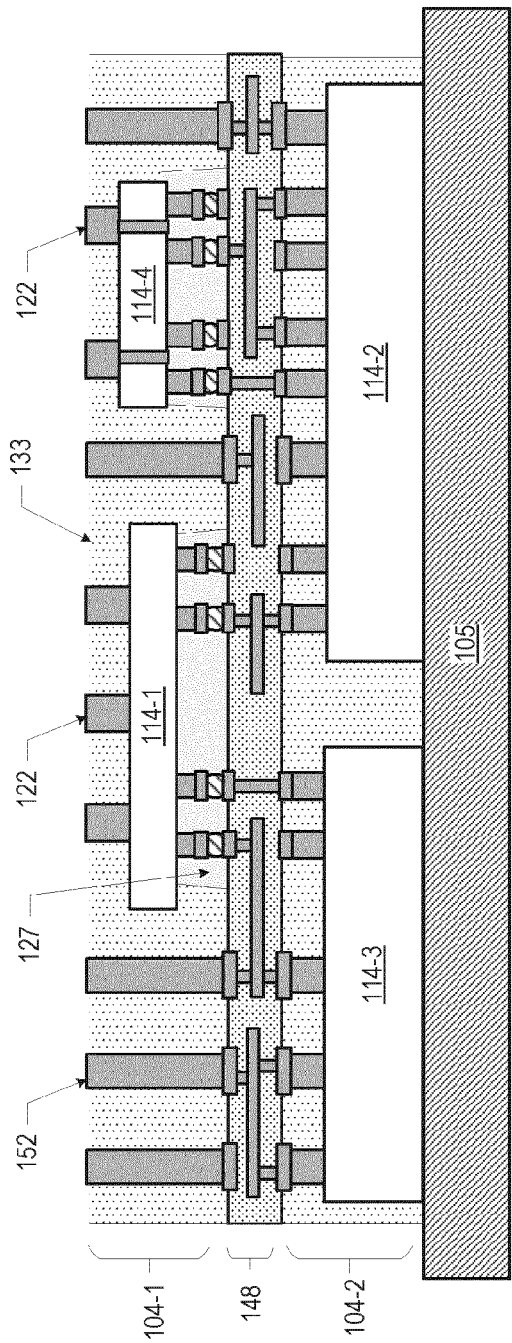


FIG. 3F

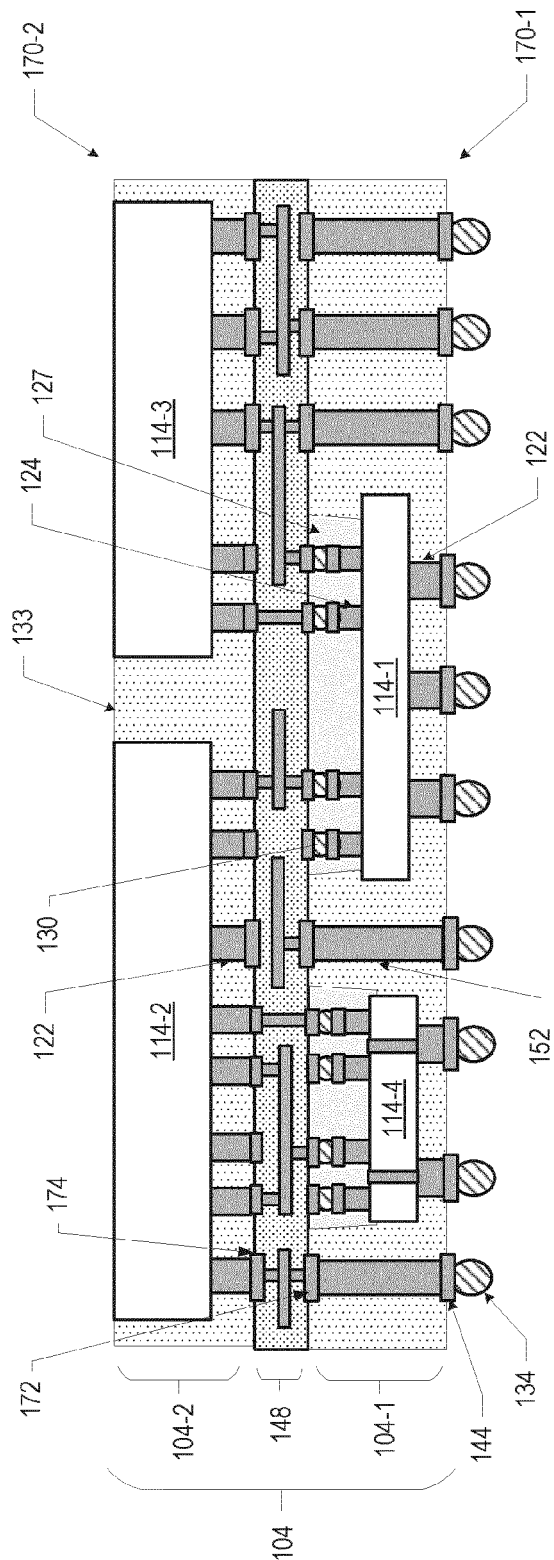


FIG. 3G

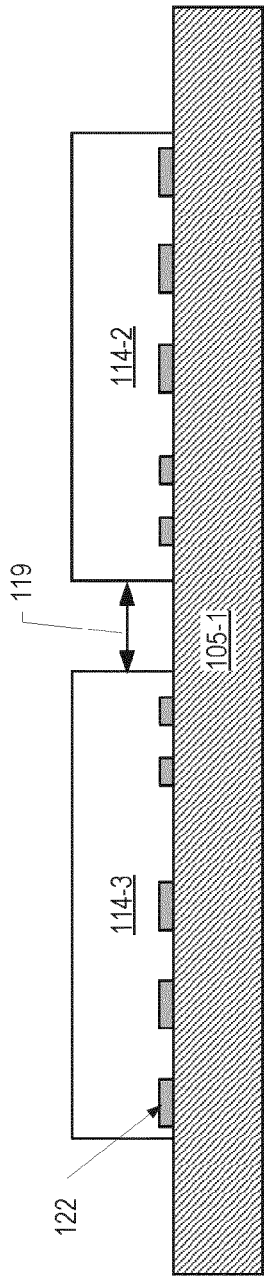


FIG. 4A

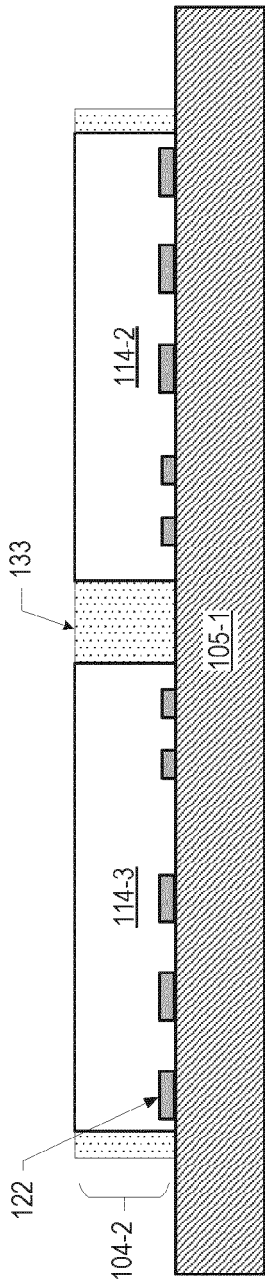


FIG. 4B

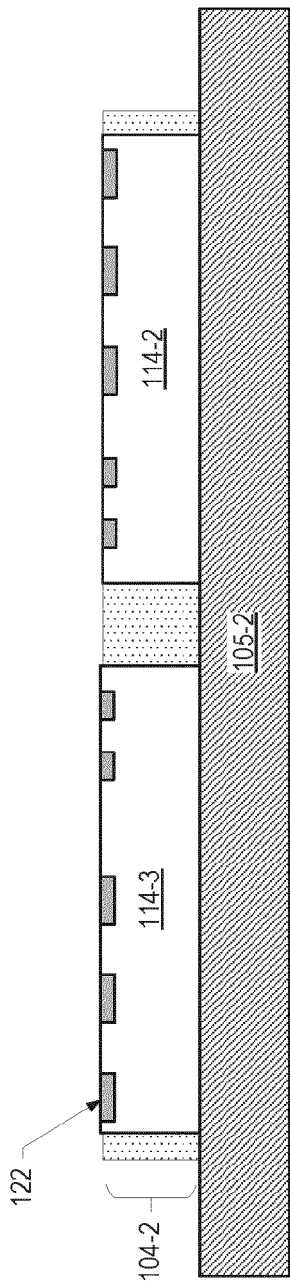


FIG. 4C

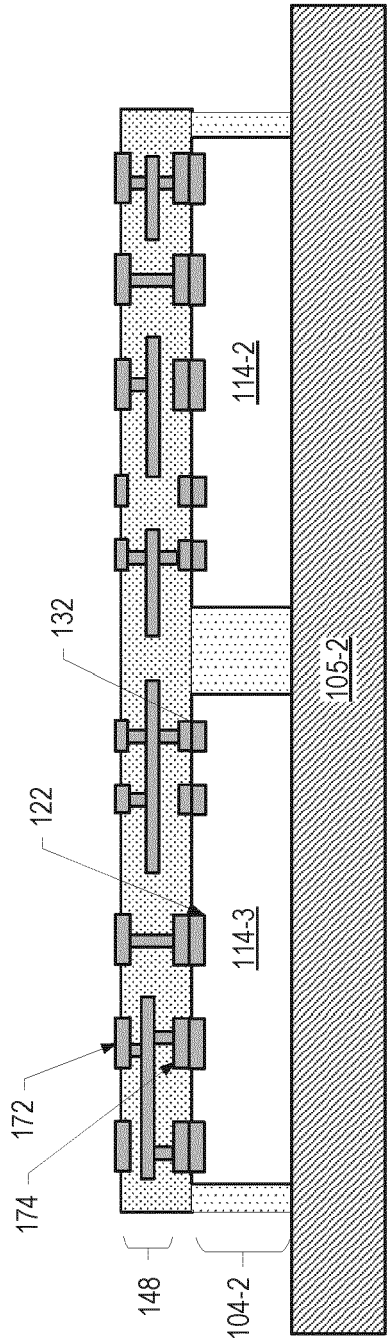


FIG. 4D

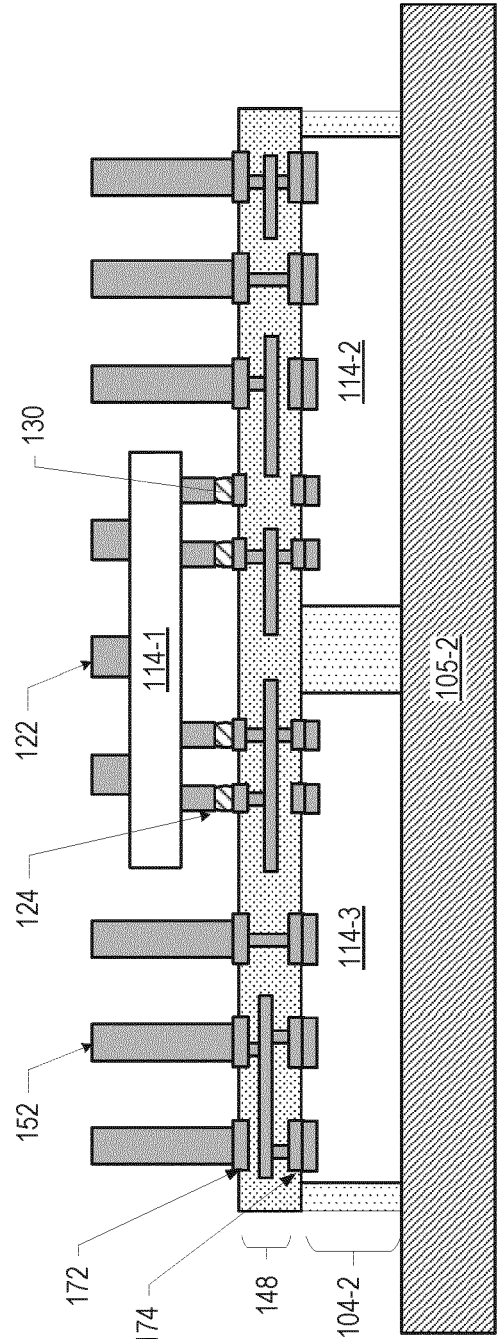


FIG. 4E

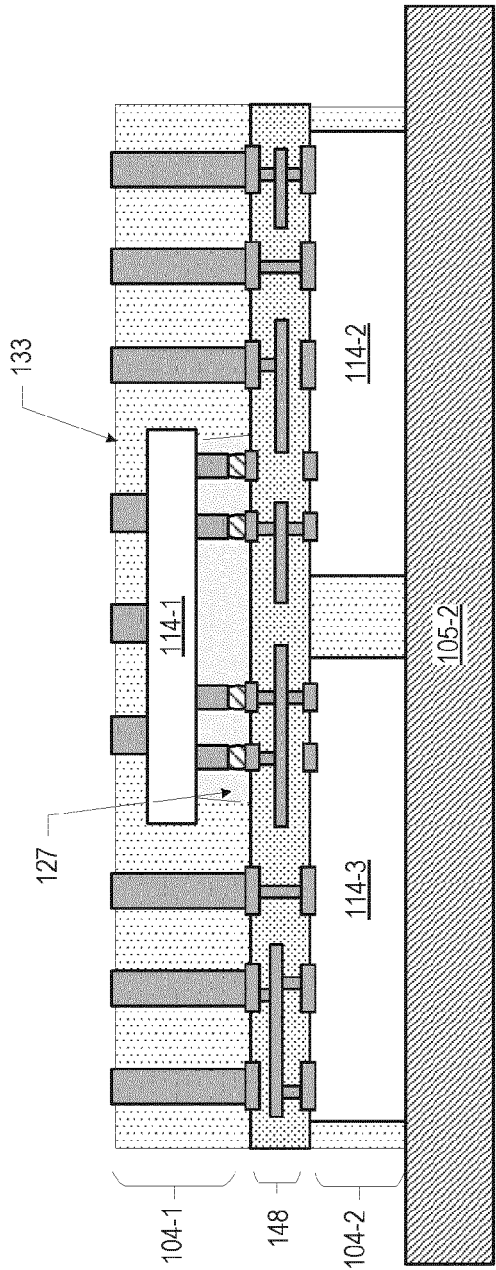


FIG. 4F

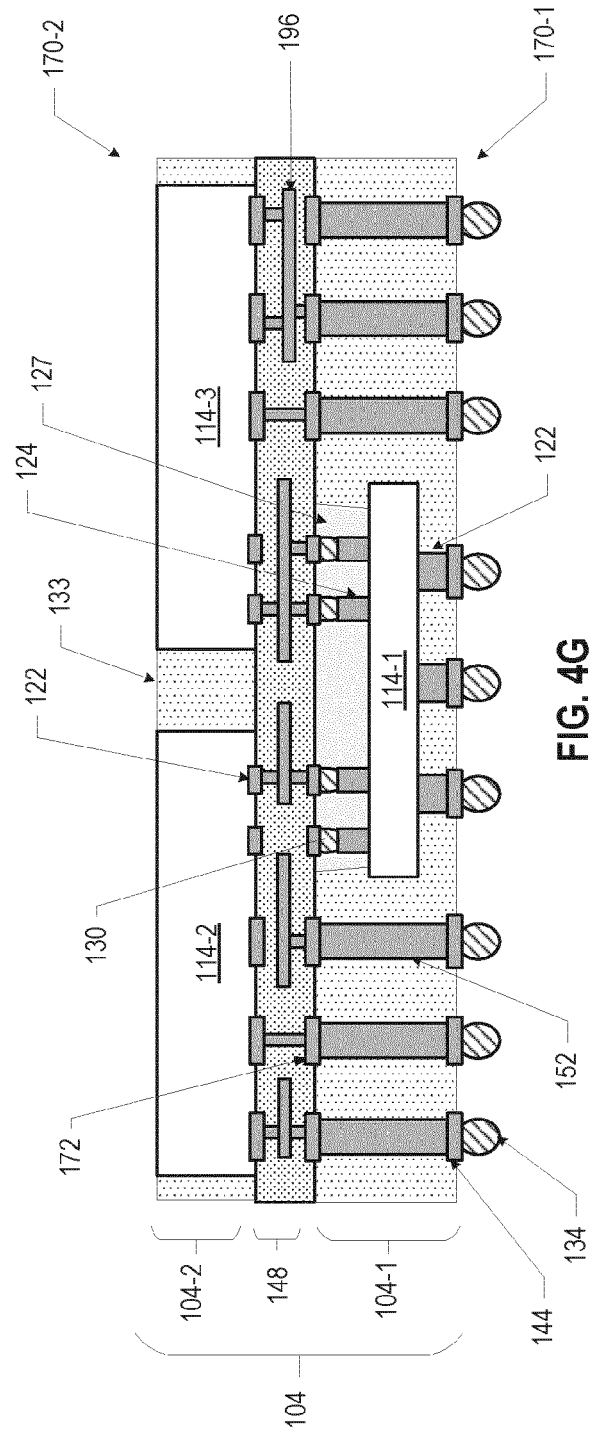


FIG. 4G

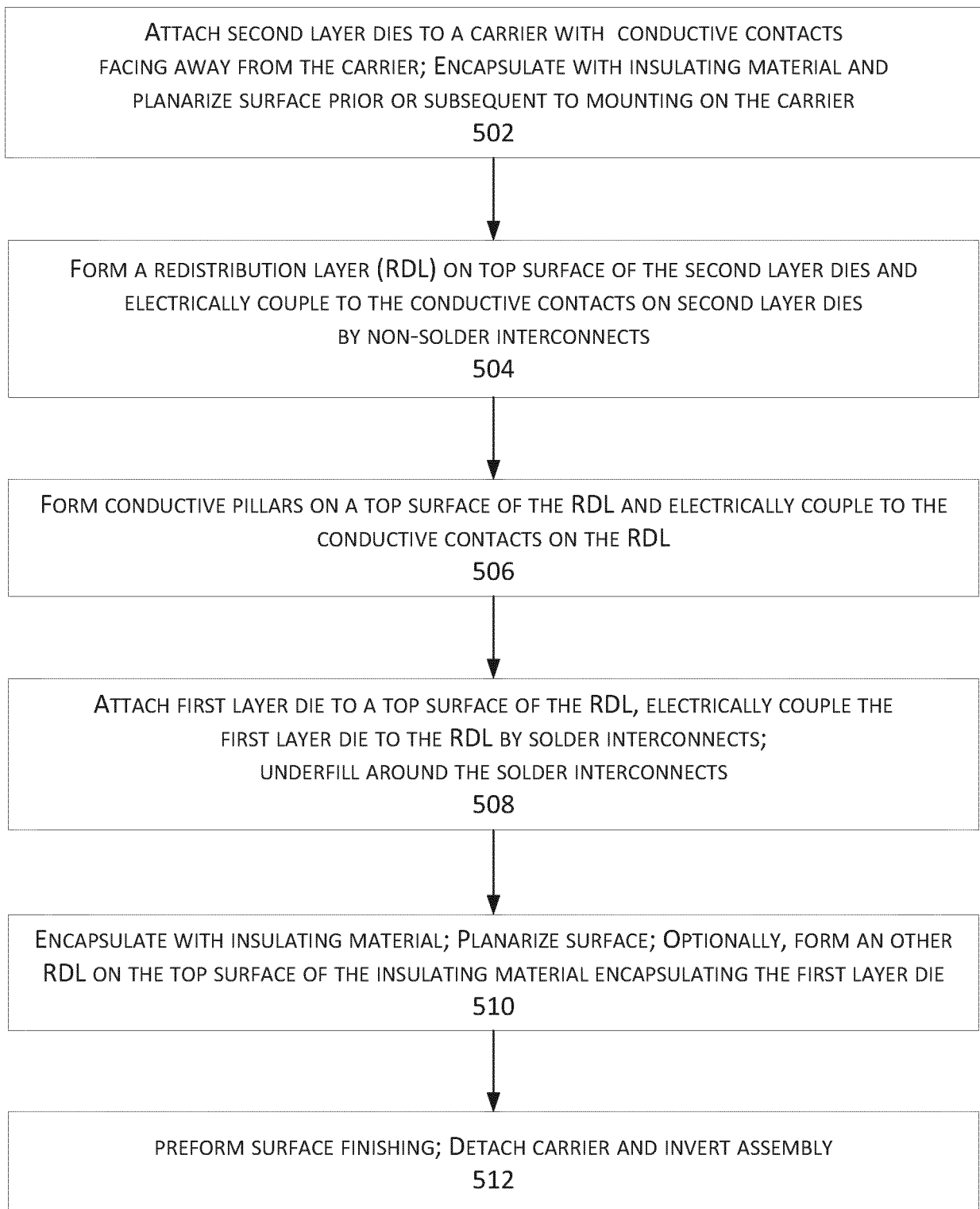


FIG. 5

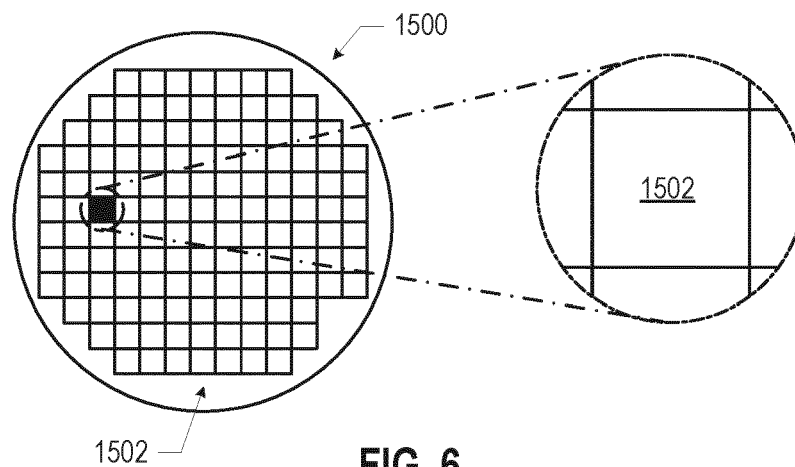


FIG. 6

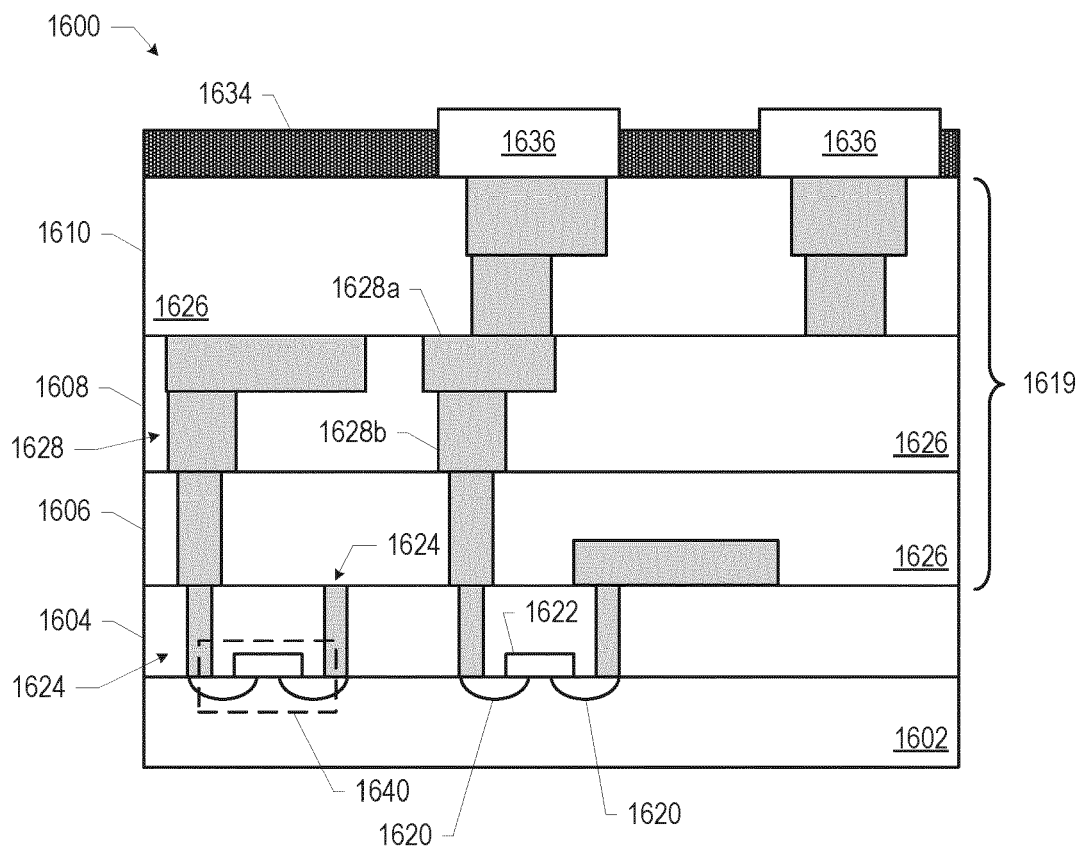


FIG. 7

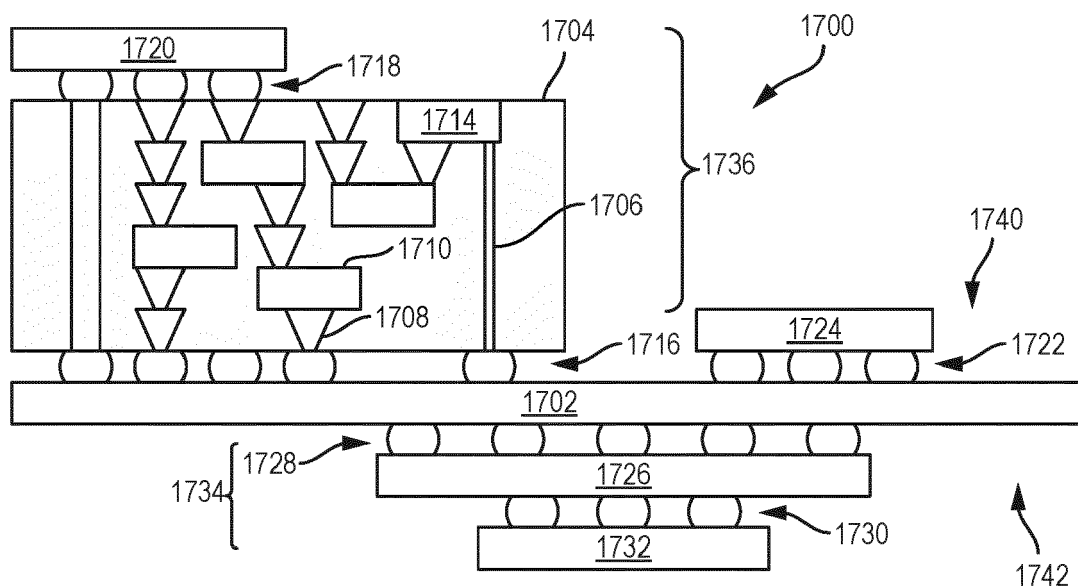


FIG. 8

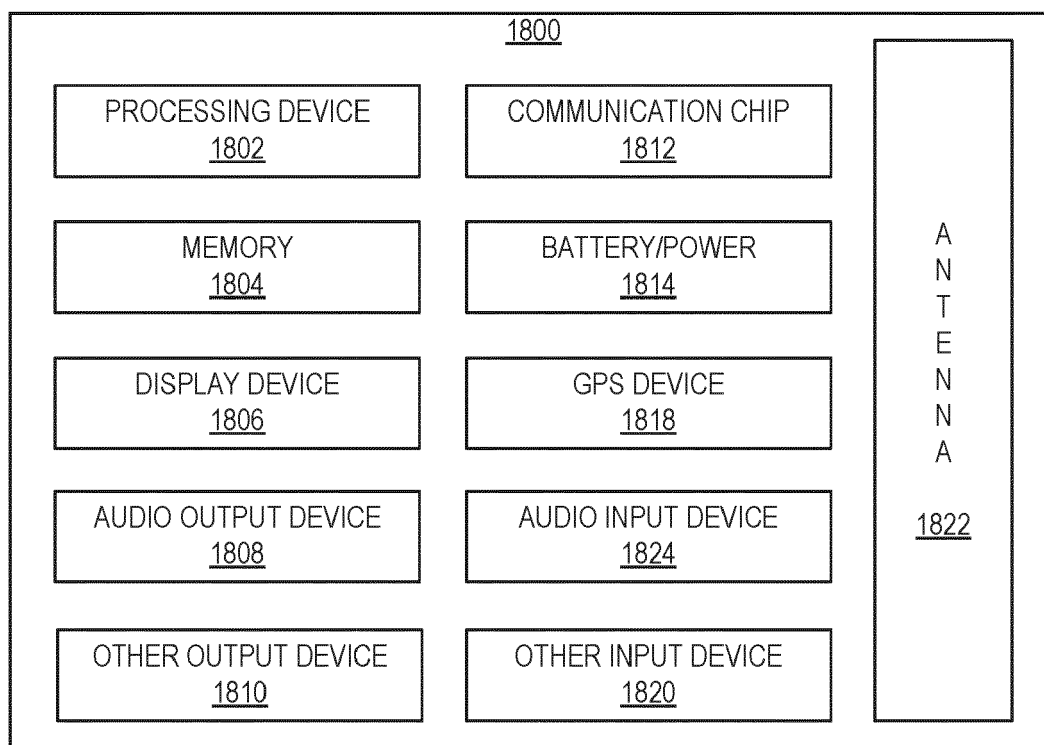


FIG. 9