PATENT SPECIFICATION (11) 1 589 685

1 589 685

(21) Application No. 49956/77 (22) Filed 30 Nov. 1977 (19)

(31) Convention Application No's. 51/144142(32)Filed 30 Nov. 1976
51/145944 3 Dec. 1976
52/023423 3 Mar. 1977
52/050521 30 Apr. 1977in

(33) Japan (JP)

(44) Complete Specification Published 20 May 1981

(51) INT. CL.[3] G09G 3/28

(52) Index at Acceptance
G5C A310 A315 A333 A350 HB

(54) DRIVING CIRCUITRY, FOR EXAMPLE FOR SELF-SHIFT GAS DISCHARGE PANELS

(71) We, FUJITSU LIMITED, a Japanese Corporation, of 1015, Kamikodanaka, Nakahara-ku, Kawasaki, Japan, do hereby declare the invention, for which we pray that a patent may be granted to us, and the method by which it is to be performed, to be particularly described in and by the following statement:-

The present invention relates to driving circuitry for electronic devices of the scanning kind, for example for self-shift gas discharge panels.

AC driven gas discharge panels providing a discharge spot shifting or scanning function have been proposed and are known, for example, as "self-shift plasma display panels". Such a self-shift plasma display panel is described in detail in U.S. Patent Specification No. 3,944,875, by Owaki et al., entitled "Gas Discharge Device having a Function of Shifting Discharge Spots", and an improved panel in which the necessity for insulated crossover areas, previously provided where shift electrodes of the panel crossed supply buses, is removed is described in West German Offenlegungsschrifts Nos. 2,729,659 and 2,731,008. A basic configuration for a previously proposed self-shift plasma display panel includes a plurality of shift electrodes arranged in a regular fashion adjacent to a gas discharge space of the panel. These shift electrodes are connected so that the discharge cells of the panel, formed where shift electrodes cross electrodes which oppose them across the gas discharge space, are divided in discharge cell groups of at least three different phases. The shift electrodes are led out to supply terminals via supply buses which are equal in number to the number of groups of discharge cells provided. Thus, by applying pulse voltages to the supply buses in a specified sequence, and so to the discharge cells of the different groups in sequence, a discharge spot generated in accordance with input date can be shifted sequentially from one discharge cell to an adjacent discharge cell, and so on, across the panel. However, in order to realize a self-shift driving system, at least two kinds of voltage pulses, one of which is comparatively wide, for use in receiving a discharge spot at a discharge cell, and the other of which is a comparatively narrow pulse for erasing wall charge remaining at a discharge cell from which a discharge spot has been shifted, are generally necessary, and it has generally been required to combine these pulses and to sequentially supply them to each supply bus. The following method has been proposed for general use as a means for distributing the abovementioned voltage pulses in a desired manner:- gate signals are provided in respect of each supply bus, and for each bus the gate signals control the application of pulse voltages (of at least the two above-mentioned kinds) to the bus. The gate signals for the different buses are of different phases and thus multi-phase driving pulse waveforms can be obtained by means of the gate signals. However, with such a gate control system, where the number of different bus phases increases or where the number of pulses to be applied to each bus for each unit cycle of shift operation increases, the differences in phase between the signals applied to the respective buses may not be uniform and the pulse waveforms to be supplied sequentially to each bus phase can become asymmetrical, and therefore the provision of a circuit configuration for driving and timing control can become very difficult. In addition, such difficulties in control can become more pronounced in a case of driving a self-shift type gas discharge panel having a meander-type electrode configuration as proposed in the above-mentioned West German Offenlegungsschrift No. 2731008 as will be described in more detail hereinbelow.

According to the present invention there is

provided driving circuitry, for a pulse-driven electronic device of the scanning type having a plurality of driving electrode inputs, comprising pulse-train generating circuitry having a plurality of outputs, for connection respectively to such inputs, and operable to deliver at the said outputs, within a predetermined unit supply period, respective pulse trains of predetermined respective waveforms at least one of which differs from the others, such delivery being repeated with cyclic change-over of each pulse train from one to another of the said outputs between one such unit supply period and the next so that in the course of a working cycle of the driving circuitry, made up of a plurality of such unit supply periods, all of the said respective pulse trains are delivered in sequence at each output, the sequential order of such delivery being different at each output from that at every other output of the plurality.

Drive circuitry embodying the present invention can be constructed which can be controlled easily and have a comparatively simple configuration for use with pulse driven multi-phase scanning electronic devices, for example self-shift plasma display (gas discharge) panels.

The use of drive circuitry embodying this invention can provide for the driving of a self-shift type gas discharge panel having an arrangement including a plurality of discharge cells to be driven by multi-phase pulse voltages.

By the use of drive circuitry embodying the present invention for driving such a panel stable and accurate shift and an improved operating margin can be provided.

Drive circuitry embodying the present invention can be constructed which is suitable for the drive of a self-shift type gas discharge panel having a meander electrode arrangement.

Drive circuits embodying the present invention used for driving self-shift panels are such that a plurality of basic pulse trains previously prepared are supplied to each phase group of discharge cells, via the appropriate supply bus. Each basic pulse train is supplied for a unit period, to the phase group concerned, and the basic pulse trains of the plurality are supplied in sequence, one after another in cyclical rotation. The different phase groups receive the basic pulse trains in different cyclic sequences in a working cycle. This can provide a very effective drive for the panel.

Drive circuitry embodying this invention can however be adapted for driving a variety of pulse driven scan type electronic display panels having a plurality of driving electrode inputs providing arrangements of pluralities of light emitting elements and to other pulse driven scanning electronic devices of the multi-phase multi-electrode input type involving shifting of charged particles.

In preferred driving circuits embodying this invention each basic pulse train is controlled in its timing on the basis of outputs of a read only memory (ROM) which is addressed by a counter output and the drive signal waveform can be selected for a self-shift panel in order to attempt to maximise the operating margin available.

For a better understanding of the present invention, and to show how the same may be carried into effect, reference will now be made, by way of example, to the accompanying drawings, in which:-

Figure 1(A) is a schematic partial plan view of a meander electrode type self-shift plasma display panel with which an embodiment of the present invention could be employed,

Figure 1(B) is a sectional view along the line BB' of Figure 1(A),

Figure 2 is a waveform diagram,

Figure 3(A) is a waveform diagram,

Figure 3(B) is a diagram explanatory of features of an embodiment of the present invention,

Figure 4 is a block circuit diagram,

Figure 5 is a block circuit diagram,

Figure 6 is a diagram explanatory of features of an embodiment of the present invention,

Figure 7 is a block circuit diagram,

Figure 8 is a diagram explanatory of features of an embodiment of the present invention,

Figure 9 is a waveform diagram,

Figure 10 is a waveform diagram,

Figure 11 is a graph,

Figures 12(A) and 12(B) are diagrams for assistance in understanding certain features of operation of gas discharge cells,

Figure 13 is a block circuit diagram, and

Figure 14 is a waveform diagram.

Figures 1(A) and 1(B) show plan and sectional views, respectively, of major portions of a self-shift type gas discharge panel as described in West German Offenlegungsschrift No. 2731008 mentioned above, and particularly illustrate the electrode configuration of the panel. In the panel shown in these Figures two shift channels SC 1 and SC 2 are shown by way of example. In the illustrated gas discharge panel, on one substrate 1, in each shift channel, a first electrode group $x11$, $x12$ ... and a second electrode group $x21$, $x22$ ..., the electrodes of which groups are alternate with one another along the shift channel, and which groups are connected to respective bus conductors $x1$ and $x2$, and a write electrode W, are provided. On the other substrate 2, in each shift channel, a third electrode group $y11$, $y12$ ... and a fourth electrode group $y21$, $y22$ ... are provided. Each electrode of the third and

fourth groups is arranged so as to face two adjacent electrodes one from each of the said first and second electrode groups. The electrodes of the third and fourth electrode groups alternate with one another along the shift channel and the groups are connected to respective bus conductors Y1 and Y2. The electrode surfaces are coated with dielectric layers 3 and 4, consisting of low melting point glass for example, and space 5 between the opposing surfaces of the coatings is filled with a mixed gas, neon (Ne) and a small amount of xenon (Xe) at a Pd value of about 4 to 5 Torr-cm for example.

Thus, in the sealed gas space 5, four kinds of discharge cells (discharge sites) *ai*, *bi*, *ci* and *di* ($i = 1, 2 \ldots$), corresponding to respective different possible combinations of facing electrodes providing those cells, are provided. That is to say, the four kinds of discharge cells are respectively cells for which an electrode of the first group faces one of the third, an electrode of the first group faces one of the fourth, an electrode of the second group faces one of the fourth, and an electrode of the second group faces an electrode of the third group. Cells of the four different kinds occur in a regularly defined sequence in each shift channel and a discharge spot generated at a write discharge cell *w* in accordance with input data supplied to a write electrode W_1 or W_2) can be sequentially shifted from one cell to an adjacent discharge cell along a shift channel by applying pulse voltages to the bus conductors X1, X2 and Y1, Y2 in accordance with a sequential switching operation. Here, as is clear from Figure 1(A), the four electrode groups defining the discharge cells have a meander type electrode arrangement. A gas discharge panel of this type will hereunder be called an "M type self-shift panel". The abovementioned M type self-shift panel has excellent features insofar as only two bus conductors are provided for each substrate and that a discharge spot can be shifted or scanned by the driving with pulse voltages of 2 phase x 2 phase. This panel also has an advantage in that insulated crossover areas for bus connection are not required on the substrates. On the other hand, each cell of a pair of adjacent discharge cells in a shift channel uses in common one electrode on one of the substrates (opposite ends of the common electrode arranged face-to-face with respective different electrodes on the other substrate provide the cells of the pair). Therefore, it is necessary in the selection of pulse waveforms for each driving phase, and the timing of switching, to take into account influences of one cell on an adjacent discharge cell at the time of electrode driving.

Figure 2 is a waveform diagram which shows driving pulse waveforms employed for driving such an M type self-shift panel by means of an embodiment of the present invention. In Figure 2, VW is a write voltage waveform applied to a write electrode W; VY1, VX1, VY2 and VX2 are pulse voltage waveforms for the respective supply bus phases, which are applied respectively to the abovementioned bus conductors Y1, X1, Y2 and X2; VA, VB, VC and VD are pulse voltage waveforms applied to discharge cells of the respective kinds as mentioned above, formed between facing electrodes of the four groups, via the bus conductors as indicated, with pulses supplied to the X side of the panel taken as being of positive polarity, and pulses supplied to the Y side as negative. It should be noted particularly in Figure 2 that the pulse voltage waveforms supplied to each group of electrodes each comprise a number of recurring pulse trains ①, ②, ③ and ④ which are supplied sequentially in rotation in respective unit supply periods TO, T1, T2 and T3. In each pulse voltage waveform supplied to an electrode group the recurring pulse trains occur with a phasing different to that of the pulse voltage waveforms supplied to the other electrode groups, but in each pulse voltage waveform switching between different recurring pulse trains occurs at the same time, in rotation.

Three kinds of voltage pulses SP, EP and OP necessary for self-shift operation are provided in basic pulse trains ① to ④ which are supplied to each of the four phase groups as shown in Figure 3(A) and these pulse trains in each pulse voltage waveform supplied to a group of electrodes, as shown in Figure 2, are rotated (supplied in a cyclically repetitive sequence) from one unit supply period to the next in a pre-determined manner as shown in Figure 3(B) and sequentially applied to each bus Y1, X1, Y2, X2. Here, the first kind of pulse SP is included in a basic pulse train as a shift pulse and has comparatively wide time width of 5 to 10 μsec; such pulses also act as sustain pulses for sustaining discharge spots during display. The second kind of pulse EP functions as an erase pulse. It has a narrow time width, of about 1 μsec or less for example, and erases wall charge remaining on the dielectric layer of a discharge cell after transfer of discharge spot from that cell. The third kind of pulse OP is called a control or overlap pulse. As shown, it has a comparatively narrow time width, of about 2 μsec, but may take the same form as the abovementioned shift pulse in some cases. This overlap pulse is applied to a discharge cell from which a discharge spot is about to be transferred in accordance with the timing of the shift operation in a temporally overlapping relationship with a shift pulse SP applied to the discharge cell to which the discharge spot is about to be transferred. In addition, this overlap pulse can be useful for improving shift operation margin

as proposed in our pending Patent Application No. 13000/77 (Serial No. 1570817). Thus, shift operation will be explained with reference to Figure 2 and Figure 1(B). By feeding in a write pulse WP in the unit supply period TO, a discharge spot is generated at the write discharge cell *w* defined where areas of the write electrode W and electrode *y*11 of the phase group of bus Y1 face one another. Then, when an overlap pulse OP is supplied to the write electrode W at a timing wherein a shift pulse SP is applied to the electrode *x*11 connected to the bus X1 in the succeeding unit supply period T1, the initially written discharge spot at the write discharge cell is shifted to the adjacent discharge cell *a*1 defined by the electrodes *y*11 and *x*11. In the unit supply period T2, the next stage of a shift cycle, an overlap pulse OP is applied to the electrode *y*11 via the bus Y1 and a shift pulse SP is applied to the electrode *y*21 via the bus Y2. Thus, the discharge spot is shifted to the discharge cell *b*1. As explained above, basic pulse trains are supplied to the electrodes of each phase group, connected to respective buses, sequentially in rotation in successive unit supply periods TO, T1, T2, T3, TO ... for the purpose of discharge spot shift operation, and simultaneously data writing is performed in every complete cycle (TO-T3) of this rotation, whereby every fourth discharge cell in a channel may carry data in the form of a discharge spot. During a shifting cycle, erase pulses EP are automatically applied to discharge cells from which a discharge spot has been transferred in accordance with the abovementioned phase rotation of basic pulse trains and there is no substantial risk of erroneous discharges being caused due to previously carried data even when a shift pulse is applied again to that discharge cell in the next unit period via a bus conductor that supplies the cell in common with others.

Figure 4 is a block circuit diagram showing drive circuitry embodying the present invention for putting into effect driving of an M type self-shift panel as described above. This drive circuitry can be said to comprise, in broad terms, a counter circuit unit 10, a basic pulse train generating circuit unit 20, a rotation circuit unit 30 and a control circuit unit 40.

The counter circuit unit 10 comprises a clock pulse generating circuit 11 and two 4-bit binary counters 12 and 13. The bit outputs *t*1, *t*2 and *t*3 of the upper three bits (the three least significant bits) of the first 4-bit counter 12 are input to an 8-line decoder 21 of the basic pulse train generating circuit unit 20 in the succeeding stage by said counter circuit unit. From the output of said 8-line decoder 21, signals corresponding to the 1st (9th) and the 2nd (10th), and to the 5th (13th) and the 6th (14th) counting outputs of the 4-bit counter (i.e. signals corresponding to 1st and 9th, 2nd and 10th, 5th and 13th, and 6th and 14th clock pulses from generating circuit 11) can be extracted through the pair of OR gates 22 in dependence upon the counting outputs of the said upper three bits, from among the 1st to 16th counting outputs of 4-bit counter 12 (e.g. from among 1st to 16th clock pulses). On the other one hand, the signals corresponding to the 1st (9th) and 2nd (10th) counting outputs serve for the provision of pulses in a pulse train corresponding to the shift pulses SP of pulse train ① of a unit period length, as shown in Figure 3(A), the pulses corresponding to those counting outputs appearing on the conductor line ① in the form of logical sum. On the other hand, these signals also serve for the provision of a pulse train corresponding to pulse train ③ of unit period length as shown in Figure 3(A); via a one shot multi-vibrator 23 and conductor line ③ these signals cause the output of narrow erase pulses EP.

The signals corresponding to said 5th (13th) and 6th (14th) counting outputs provided by an OR gate 22 are also used to provide two pulse trains. On one hand, the signals are used to provide pulses corresponding to the shift pulses SP in a unit period of pulse train ② of Figure 3(A) that are output to the conductor line ② in such a manner that those shift pulses are provided at a phase shift of 180° from the shift pulses of pulse train ①, while, on the other hand, such signals are input to each of two one shot multivibrators 24 and 25 for the purpose of generating pulses corresponding to the overlap pulse OP and the erase pulse EP in the pulse train ④ shown in Figure 3(A). The one shot multi-vibrator 24 outputs, via OR gate 29, to the conductor line ④, an overlap pulse having a predetermined time width which rises in correspondence with said 5th count signal, via AND gate 27, which gate is in an ON condition until an 8-count output is obtained by inversion of the 4th bit output t4 of the 4-bit counter 12 by means of the inverter 26. The AND gate 27 is thus ON for the passage of a pulse from the one shot multivibrator 25 during the first half of the unit period length of pulse train ④. The other one shot multi-vibrator 25 outputs, via OR gate 29, to the conductor line ④, a narrow erase pulse EP which rises in correspondence with the 13th count signal, in the second half of the unit period length of pulse train ④, via AND gate 28 which is opened after the 8-count output is obtained from the 4th bit output t4 of the 4-bit counter 12.

The four conductor lines ① to ④ are respectively connected as indicated in Figure 4 to the respective inputs of respective AND gates of each of four groups of AND gates 311 to 314, 321 to 324, 331 to 334 and 341 to 344. Each group thus has four AND gates,

and the groups are provided in the rotation circuit unit 30. The outputs of the AND gates of each group are delivered via a respective OR gate (of OR gates 31 to 34) to a respective shift driver (not shown) of a respective bus conductor of bus conductors Y1, X1, Y2, X2 of the abovementioned M type self-shift panel. Further inputs of the respective AND gates of each AND gate group are connected in the manner shown in the Figure to respective ones of four outputs of a 4-line decoder 35 and the pulse trains from the conductor lines ① to ④ are switched and supplied in a cyclical sequence to the shift drivers connected to bus conductors Y1, X1, Y2 and X2 in dependence upon the changes of the outputs from said decoder 35.

The control circuit unit 40 comprises flip-flops 41 and 42 in a 2-stage shift register configuration which operate in dependence upon the 2nd bit output $t22$ of said 2nd 4-bit counter 13 included in the counter circuit unit 10 and inputs the output of each stage to the aforementioned 4-line decoder 35 as cycle switching signals A and B. Accordingly, since a signal which rises at the count of 16 basic clock pulses and falls at the count of 32 clock pulses is derived from the 2nd bit output $t22$ of the 2nd 4-bit counter 13 (which counter counts the 4th bit output $t4$ of the 1st counter 12) a switching signal is supplied to the decoder 35 in every 16 basic clock pulses, and therefore the signals supplied from decoder 35 are switched in the sequence 1′, 2′, 3′ and 4′ in each unit shift cycle. Thereby, the basic pulse trains for the bus conductors Y1, X1, Y2, X2 can be applied in a cyclically rotating manner as explained above.

The control unit 40 also includes a binary 3-bit counter 43 which counts the outputs of flip-flop 42 of the 2nd stage of the 2-stage shift register. This 3-bit counter is not directly related to the subject of the present invention, but it is shown in order to illustrate control in a case where characters conforming to a pattern of 5 × 7 dots are to be written and shifted. As described above, in an M type self-shift panel each 4th discharge cell along a shift channel carries data in the form of a discharge spot and therefore a cycle of shift operations is completed in four unit time periods as illustrated in Figures 2 and 3. Thus, one character pattern can be written in five shift operation cycles for each of seven shift channels. When a spacing of 2 lines is provided between adjacent characters an 8th cycle of shift operations can be considered as the timing of commencement of writing of a next character. For this purpose, entry of a new character is controlled by means of the output of said 3-bit counter 43.

When the 3-bit counter 43 counts up to 8 and its outputs all become "1" the application of counting inputs to the counter from the flip-flop 42, is blocked at the AND gate 46 by the output of NAND gate 44. The counter 43 is then reset by means of an output from a one shot multi-vibrator 47 controlled by an output of a flip-flop 45 which receives the 4th output $t24$ of the 2nd 4-bit counter 13 and a strobe signal STB (via inverters) and simultaneously a signal which enables writing of a next character is sent to a write control circuit (not shown) via the line MR and inverter 48.

The driving circuit of Figure 4 described above is useful for explaining features of the present invention, but the circuit configuration in Figure 4 is a little complicated. Therefore, another embodiment of the present invention will be described below in which circuit configuration is simplified by the employment of a ROM (read only memory) in a basic pulse train generating circuit unit.

Figure 5 is a block diagram of this embodiment of the present invention, and in Figure 5 the same reference numerals as in Figure 4 are used for items of similar functions. In Figure 5, ROM 202 constituting part of the basic pulse train generating circuit unit 20 is of a 4 × 16 bit configuration as shown in Figure 6, for example. The 4-bit outputs $t1$ to $t4$ of the counter circuit unit 10 are input to an address decoder 201 and timing signals are read out sequentially in a 4-bit parallel form from the ROM 202. Pulse trains ① to ④ of unit period length as shown in Figure 3(A) can be obtained by means of the contents of addresses 0 to 15 of the ROM, as illustrated in Figure 6. Pulse trains ① to ④ are distributed to shift drivers (not shown) connected to the buses Y1, X1, Y2, X2 in a cyclically rotating sequence in accordance with signals from the control circuit unit 40 supplied to the rotation circuit 30.

The phase relationships between the pulse trains ① to ④ in a unit period (and pulse widths) can be set more precisely by increasing the number of bits of the ROM202. In such a case, the number of bits of the counter of the counter circuit unit 10 is of course increased. The read only memory ROM 202 may be constructed as a PROM (programmable read only memory) which can provide an advantage in that modification of the patterns of pulses in the pulse trains can be more readily effected by changing or replacing the content of ROM 202. Moreover, by using a ROM constructed as an integrated circuit, the basic pulse train generating circuit unit 20 can readily be miniaturized to a significant degree.

Furthermore, in accordance with another embodiment of this invention, said basic pulse train generating circuit unit 20 and the rotation circuit unit 30 can be provided jointly by means of a single ROM. Figure 7 illustrates this embodiment. In Figure 7, the counter circuit unit 10 comprises a clock generator 101 and an 8-bit counter 102, and

the control circuit unit 40 comprises a flip-flop 401, AND gates 402, 403, an inverter 404 and inverters for delivering a strobe signal STB to the flip-flop 401. Circuit unit 50 comprises an address decoder 51 and a ROM 52. ROM 52 has a 4 × 256 bit configuration, for example, and its memory contents are as shown in Figure 8 for example. The content of addresses 0 to 63 relates to the unit period TO, for example as shown in Figure 2 (though it will be appreciated that the detailed contents of the ROM do not relate to pulse trains as in Figure 2, but to Figure 9, as explained hereinafter), and the four rows of the addresses relate to respective basic pulse trains ① to ④ as indicated. The address content sequences corresponding to basic pulse trains ① to ④ are interchanged between the rows as shown in the Figure in the succeeding unit periods T1 to T3 as indicated.

When the strobe signal STB is "O", a shift mode of operation is effected. The flip-flop 401 is in the set condition and all outputs of the 8-bit counter 102 are applied to the address decoder 51. Therefore, the content of the addresses from 0 to 255 of ROM 52 shown in Figure 8 are sequentially read out in a cyclically repeated manner and applied to the buses Y1, X1, Y2, X2 in a rotating cyclical manner (via shift driver unit 60).

On the other hand, when the strobe signal STB becomes "1" a display mode of operation is effected. Since in this case the flip-flop 401 is reset when the highest bit output of 8-bit counter becomes "1", the AND gates 402, 403 are closed and only 6 output bits of the 8-bit counter are applied to the address decoder 51. Therefore, the contents of the ROM relating to unit period TO are repeatedly read out and a static display mode is given. In the configuration of Figure 7, the signals IY1, IX1, IY2 and IX2 read out from the ROM 52 of circuit unit 50 are applied to a shift driver unit 60 including drivers 61 to 64 corresponding to the respective buses X1 to Y2 as basic timing signals. As is shown for driver 61, each driver includes an up-transistor (pnp) 611 and a down-transistor (npn) 612 being connected between a power source voltage of + V_{sh} and ground potential and each transistor is driven selectively by the common inverted timing signal IY1.

Driving pulse voltages for the panel PDP are supplied to respective buses from connecting terminals.

Figure 9 shows driving pulse voltage waveforms generated in shift mode operation when the content of ROM 52 of Figure 7 is as shown in Figure 8, with reference to the driving of an M type self-shift panel as described with reference to Figure 1. In Figure 9, VY1, VX1, VY2 and VX2 are pulse waveforms respectively applied to the buses Y1, X1, Y2, X2 as in the case of Figure 2, and VW*i* indicates write voltage pulses to be applied to a write electrode W*i*. Waveforms VA, VB, VC and VD represent pulse voltage waveforms applied to the discharge cells of the four kinds *ai*, *bi*, *ci* and *di*, as explained with reference to Figure 1, being voltage waveforms formed by combinations of the pulse voltages applied to the buses. V*wi* represents a composite write voltage waveform applied to the write discharge cell W*i*.

As can be seen from Figure 9, to each of the bus conductors Y1, X1, Y2 four basic trains of pulses ①, ②, ③ and ④ are applied, each in a unit period of time T, in a regular cyclical sequence, in such a manner that each of the four basic trains is applied to each bus in one cycle of shift operations through unit periods TO to T3. In this case, all of the pulses of the four basic trains of pulses have a positive polarity and have the same pulse width, which differs from the situation in Figure 2, and have their voltage value selected to be a shift voltage level V*sh*. However, in each unit period of time T the four basic pulse trains being supplied to respective bus conductors have the following mutual phase relationships according to the present embodiment. The pulse trains ② and ④ are in phase with each other and are 180° out-of-phase with the pulse train ①, while pulse train ③ has a phase difference with respect to pulse trains ② and ④ equal to the duration τ_e of an erase pulse between its rising and falling times. Thus, to a discharge cell to which the pulse train ① is applied through one of the crossing electrodes between which it is formed, and to which a pulse train ② or ④ is applied from the other electrode of the crossing electrodes, alternately directed shift voltage pulses P*s* are applied, and to a discharge cell to which the pulse train ③ is applied from one crossing electrode and to which a pulse train ② or ④ is applied from the other crossing electrode, pairs of short duration oppositely directed erase pulses P*e* are applied, corresponding to the phase difference between those pulse trains ③ and ② or ③ and ④.

Reference should be made to the unit period TO in Figure 9, for example, in which, when a write voltage pulse Pw is applied to the write electrode W*i*, developing a write voltage waveform such a V*wi* at the write discharge cell, an initial discharge spot is generated at the appropriate discharge cell. At this moment a shift voltage pulse waveform such as VA is supplied via bus conductors Y1 and X1 to the cell group *ai* to which the first discharge cell (the cell nearest a write cell) of each shift channel belongs. The priming effect of the above-mentioned write discharge spot causes a discharge spot to be developed simultaneously at the first discharge cell *a*1 adjacent to the write discharge cell *wi*. During this period, a shift

voltage pulse waveform such as VD is also being supplied through bus conductors Y1 and X2 to discharge cells of the group *di* so that there arises a mode in which a discharge cell of the group *di* and an adjacent discharge cell of the group *ai* can share a discharge spot which represents the information previously written. During the period TO, to the discharge cells *bi* and *ci* of the remaining groups are applied pairs of erase pulses Pe of narrow width, as a result of the phase difference between the pulse train ③ applied through bus conductor Y2 and pulse trains ② and ④ applied through bus conductors X1 and X2. During the succeeding unit period T1, the change of the order in accordance with which the pulse trains are delivered to the bus conductors Y1, X1, Y2 and X2, from ①, ②, ③ and ④ for the respective conductors Y1, X1, Y2, X2 during the period TO, to ④, ①, ② and ③ causes a shift pulse voltage waveform such as shown at VB to be applied across discharge cells of the group *bi* so that a discharge spot at a discharge cell of the group *ai* is shifted to an adjacent discharge cell of the group *bi* and is thus shared by the adjacent discharge cells. In the meantime, to the discharge cells of the group *di* that have held discharge spots during the period TO there are applied erase pulses of narrow width obtained as a result of the phase difference between the basic pulse trains ③ and ④ in the pulse waveforms VX2 and VY1, as shown in the waveform VD as applied during the period T1, thus erasing wall charge remaining on the dielectric layer of the panel at those cells. During this period, erase pulses of narrow width are effectively applied to the discharge cells of group *ci* also. During a further period T2, the order in which the basic pulse trains are applied to the respective buses Y1, X1, Y2 and X2 changes to the order ③, ④, ① and ② so that shift voltage pulses are applied across the discharge cells of the groups *ci* and *bi*. Thus, discharge spots are shifted by one further phase and are shared by adjacent cells of the groups *bi* and *ci*. After shift of discharge spots, narrow width erase pulses are then applied to the discharge cells of the group *ai* and the discharge cells of the group *di* to which the discharge spots are next to be shifted. During the next unit period T3, the basic pulse trains take the order ②, 3^8, ④ and 1^8, and a similar shift operation takes place.

In accordance with the embodiment of the present invention shown in Figure 7, four basic pulse trains comprising pulses of the same pulse width and voltage level are sequentially distributed on the basis of the output of ROM52 to the bus conductors Y1, X1, Y2 and X2 in a cycle of application which consists of four unit periods TO to T3, and in the course of shift operation narrow width erase pulses obtained as a result of a phase difference between basic pulse trains are effectively applied to discharge cells from which discharge spots have been shifted. In this case, as described in the shifting of a discharge spot, the discharge spot is shared by two adjacent discharge cells.

Thus, in this embodiment, the necessity for directly supplying narrow width erase pulses and overlap pulses is eliminated and consequently relatively low cost and simple circuit configurations can be employed for shift drivers without the need for overly great care in selection of switching speeds of the switching transistors of the drivers.

The driving pulse waveforms shown in Figure 9 are different from those shown in Figure 2 as described previously, in that two adjacent cells are always activated together in the course of shifting instead of using a narrow width overlap pulse, and in that narrow width erase pulses are applied as a result of phase difference between larger width pulse voltages supplied to the respective electrodes arranged face-to-face at a discharge cell.

Here, when an evaluation was made for the above-described driving methods applied to an M type self-shift panel, in experiments performed by the inventors, the "double cell" shifting system of Figure 9 was found to be superior to the "single cell" shifting system of Figure 2 insofar as a wider operating margin could be obtained and the configuration and control of driving circuitry were simplified. However, consideration should always be given, when selecting driving signal waveforms, to the panel characteristics and it is desirable to provide that modification of signal waveform supplied by drive circuitry is possible in order to obtain the maximum operating margin for the panel, and where such modification of waveform is required, the rotation driving system offered by embodiments of this invention can very effectively facilitate it. Figure 10 shows an example of modified driving pulse waveforms, wherein the reference symbols used and basic shift operation correspond to those of Figure 9. However, in comparison with Figure 9, it should be noted that in Figure 10 in each unit period T one pair of erase pulses Pe which are applied to a discharge cell in Figure 9, after the shifting of a discharge spot, is cancelled by a same phase pulse CP.

In general, the stability of operation of a self-shift plasma display panel is expressed in terms of the range of variation of shift voltage which the panel can accommodate and yet give reliable shift operation. This range is known as the shift margin and this shift margin depends not only on the panel structure but also upon the driving signal waveform employed. For example, according to experiments carried out by the inventors, it has

been shown that if a driving signal waveform such as illustrated in Figure 9 is used, the shift margin is a maximum when the pulse width of the erase pulses applied effectively to a discharge cell after shifting of a discharge therefrom is 0.5 μsec. For lesser erase pulse widths the upper limit shift voltage determining the shift margin decreases so as to reduce the shift margin, and for greater erase pulse widths the lower limit shift voltage determining the shift margin increases so as to reduce the shift margin. The graph of Figure 11 illustrates the dependence of shift margin upon erase pulse width. In this graph, the erase pulse width τ_e is shown on the horizontal axis, while the shift voltage V_{sh} is shown on the vertical axis. The upper and lower limit values of shift voltage corresponding to different erase pulse widths are indicated by the solid line curves V_{US} and V_{LS}, respectively for the use of driving signal waveforms of Figure 9.

It has been found that the dependence of shift margin upon erase pulse width is significantly decreased where driving waveforms providing an erase pulse cancellation period, as in Figure 10, are used. In Figure 11, the improvement of shift margin which can be provided by such driving waveforms is illustrated by the upper limit voltage curves V_{US}, and the lower limit voltage curve V_{LS}, indicated by the broken curves. In particular the flatness of the lower limit shift voltage curve contributes to stability of operation.

The reason for the improvement of shift margin when driving signal waveforms as shown in Figure 10 are used to drive an M type self-shift plasma display panel, will be explained. Figures 12(A) and 12(B) illustrate internal discharge phenomenon that take place between two adjacent discharge cells, and the pulse voltage supply relationship for those cells in relation to the waveforms of Figures 9 and 10 respectively. Figure 12(A) relates to shift operation as in Figure 9, when shifting a discharge spot presently existing at a pair of discharge cells D and A, which share electrode y1 in common, to a next pair of discharge cells B and A (at the beginning of period T1 in Figure 9). As shown in Figure 12(A), shift pulse voltage V_{sh} is applied simultaneously to the electrodes $y1$ and $y2$, in order to generate a discharge spot at adjacent discharge cell B by plasma coupling with a discharge at discharge cell A. At this time, since the shift pulse voltage V_{sh} which is applied to electrode X2 has a phase difference relative to the voltage supplied to electrode $y1$, between which electrodes the discharge cell D, from which discharge is to be erased, is defined if the phase difference ($t2$-$t1$) and ($t4$-$t3$) corresponding to the erase pulse width becomes relatively long, a part of the space charge generated at the discharge cell A can be attracted to the discharge cell D wherein wall charge is retained under the initial field conditions and the supply of initial charge to the discharge cell B to which the discharge spot should be shifted can be reduced. Therefore, as explained with reference to Figure 11 previously, when the erase pulse is applied to a cell immediately after shifting of a discharge spot therefrom, the lower limit shift voltage defining shift margin V_{LS}, that is the minimum voltage required for causing discharge at discharge cell to which the discharge spot is to be shifted, by means of plasma coupling, increases as the width of erase pulse employed increases.

However, when employing waveforms as shown in Figure 10, wherein an erase pulse cancellation period is provided, as is clear from the representation given in Figure 12(B), at a timing when the discharge cell A, which becomes the charge supply source, and the discharge cell B, to which a discharge spot is to be shifted, are activated simultaneously by the shift pulse voltages V_{sh} applied to the electrodes $y1$, $y2$, there is supplied simultaneously to the electrode $x2$, which faces electrode $y1$ to define the discharge cell D, after shifting of the discharge spot, a shift pulse voltage V_{sh} (CP) of the same polarity and the same phase as the abovementioned shift pulse V_{sh} supplied to the above common electrode $y1$, which cancels the effect of the shift pulse applied to electrode $y1$, at cell D. Therefore, the relevant discharge cell D is placed in a neutral condition in which, essentially, it is not subject to any external field, and as a result the space charge generated by the discharge at the discharge cell A effectively contributes to discharge at the discharge cell B to which the discharge spot should be shifted, in other words, the priming effect is increased. In Figure 11, the upper and lower limit data lines for shift margin shown by the broken lines V_{US}, and V_{LS}, represent data confirmed by the experiment with an embodiment of the present invention as explained previously and illustrate the effects of such phenomenon and indicate that a wide shift margin can be obtained uniformly in spite of variation of erase pulse width. The driving waveforms illustrated in Figure 10 can be attained relatively easily by modifying in part the memory content of ROM 202 or ROM 52 in Figure 5 or Figure 7 and moreover they can also be realized with a circuit configuration as shown in Figure 13.

The self-shift display panel driving circuitry shown in Figure 13 consists broadly of a basic timing signal generator circuit unit 100, a control signal generator circuit unit 200, a rotation circuit unit 300, a shift driver unit 400, a write signal generator circuit unit 500 and a write driver unit 600, each item being enclosed in broken lines in Figure 13. The basic timing signal generator circuit unit

200 controls the timing with which the above-described four basic pulse trains ①, ②, ③ and ④ shown in Figure 10 are generated, and consists essentially of a binary 6-bit counter 120 which counts clock pulses from a clock pulse generator 110. Inverted 1st and 2nd bit outputs from the 6-bit counter provided by 1st and 2nd inverters 130 and 140 are applied to AND-gate 150 which provides a 1st timing signal corresponding to the basic pulse train ① on a line ① at every count of four clock pulses. The inverted 1st bit output and the (univerted) 2nd bit output from 6-bit counter 120 are applied to AND-gate 160 which provides a 2nd and 4th timing signal corresponding to basic pulse trains ② and ④ respectively on lines ② and ④. Four signals, the 2nd and 4th timing signal itself, a delayed signal obtained by feeding the 2nd and 4th timing signal to the delay circuit 170, and 3rd and 4th bit outputs of said 6-bit counter 120, are combined in a logic operation by means of a phase switching circuit 180 (boxed in by broken lines in Figure 1(B)) and thereby a 3rd timing signal corresponding to the above-mentioned basic pulse train ③ can be obtained on the line ③. In other words, when a 1st timing signal pulse is output onto the lines ② and ④, each unit period T being a period in which 16 clock pulses are generated, a timing signal pulse (corresponding to CP in Fig. 10 mentioned above) which is in phase with the timing signal on line ② is output to the line ③ via AND gate 182 and OR gate 183, subject to there being an output "1" from NOR gate 181 which receives the 3rd bit and 4th bit outputs from the counter 120. However, at the pulse generation timing of 3rd or succeeding timing signal pulses, since at least one of the 3rd and 4th bit outputs of the counter 120 is of high level, the application to line ③ of a signal of the same phase as the output on the line ② is blocked by the AND gate 182 and during this blocking period, a signal pulse (corresponding to EP in Fig. 10) which is delayed at the delay circuit 17 by a delay time corresponding to the erase pulse width is output to the line ③ via AND gate 185 which opens in dependence upon the output of inverter 184 which receives the output of NOR gate 181. The control signal generating circuit unit 200 allows the 5th and 6th bit outputs of the said 6-bit counter 120 to pass through AND gates 210 and 220 and supplies those outputs to 4-line decoder 350 of the rotation circuit unit 300 as rotation cycle switching signals A and B. The AND gates 210 and 220 are controlled by the output of 3-bit counter 230 via NAND gate 240. The 3-bit counter 230 counts the 6th bit output of said 6-bit counter 120 and outputs rotation cycle switching signals A, B until it counts the 6th bit output of counter 120 eight times. That is to say, when writing in a panel is effected in terms of letters formed by 5 × 7 dot patterns, since discharge cells belong to each of four kinds, as explained above, and the discharge cells of the four kinds are arranged in a regular periodic manner in an M type self-shift plasma display panel having the meander electrode structure as shown in Figure 1, one cycle of shift operation is effected in four unit time periods, and therefore a pattern corresponding to one alphanumeric character can be written by five cycles of shift operation in each of seven shift channels. Here, if an intercharacter spacing as wide as 2 lines is provided, an 8th cycle period provides the timing at which writing of a new letter is commenced, and entry of this new letter is controlled by the output of said 3-bit counter 230. When the 3-bit counter 230 counts up to 16, in other words, when eight complete shift cycles are completed, each consisting of four unit periods, each unit period being equal to the time in which 16 clock pulses are generated, and the outputs of the 3-bit counter become all "1", the AND gates 210, 220 are closed by the output of NAND gate 240 thereby to terminate supply of the 5th and 6th bit outputs of the said 6-bit counter as the switching signals A and B. At the same time, a next letter write operation command MR is sent out, via an inverter as illustrated.

The rotation circuit unit 300 comprises, as in the case of that in Figure 4, four groups of AND gates 311 to 314, 321 to 324, and 341 to 344, respectively, and four OR gates 310, 320, 330 and 340 connected to respective AND gate groups. To inputs of respective AND gates of each group the lines ①, ②, ③, ④, which respectively deliver the abovementioned basic timing signals, are connected, in the manner illustrated in the Figure, and to other inputs of the respective AND gates of each group respective outputs of 4-line decoder 350, which decodes said rotation switching signals A, B, are connected in the manner shown in the Figure. In addition, the outputs (IY1, IX1, IY2, IX2) of the OR gates which receive the outputs of the AND gates of the respective groups are connected to the shift driver unit 400.

Since the output of 4-line decoder 350 is switched for every count of 16 clock pulses corresponding to one unit period, as described previously, the distribution sequence of the basic timing signals is also switched in a cyclically repeating sequence. Thus, four drivers 410, 420, 430 and 440 of the shift driver unit 400, which are driven upon reception of basic timing signals delivered from respective OR gates 310 to 340, supply shift voltage pulse trains, as shown in Figure 10, of which the distribution sequence is changed each unit period, to respective bus conductors Y1, X1, Y2, X2 of the self-shift type gas discharge panel PDP. Each driver, as shown for driver 410, includes a pair of

transistors, a pnp up-transistor 411 and an npn down-transistor 421, connected between a $+V_{sh}$ power supply and ground, which are driven alternately by basic timing signals supplied thereto, shift voltage pulses being delivered from a neutral common connection point of the up-and down-transistors.

In the configuration of Figure 13, the write signal generating circuit unit 500 is controlled in dependence upon externally supplied letter code data signals and includes a character generator 580, which outputs a selected character pattern signal of 5 × 7 dots in a sequence of units relating to 7 dots, one unit of 7 dots in every 4 unit shift period, and the AND gates 510 to 570 which match the output of each 7 dot unit to the timing of the basic pulse train ④. Character pattern signals from the abovementioned AND gates 510 to 570 are applied in parallel to write drivers 610 to 670 included in write driver unit 600, and write pulses of a write voltage level +Vw are applied in the manner shown in Figure 10 to the write electrodes W1 to W7 which correspond to respective shift channels of panel PDP. Thus, data corresponding to a character pattern is written sequentially into 7 shift channels for one character line, and discharge spots generated thereby are sequentially shifted in the manner employing in common two adjacent discharge cells, as described above, by cyclic shift operations.

In the above embodiment, shift operations which mainly utilize plasma coupling due to the space charge between adjacent discharge cells are described. The mechanism of such plasma coupling, known as the priming discharge effect, involves the phenomenon whereby firing voltage of an "off" cell adjacent to a firing cell (an "on" cell) is reduced below a normal value therefor as a result of the supply of space charge, in the form of electrons, ions and meta-stable atoms, from the firing cell to the "off" cell. However, in an AC driven self-shift plasma display, effective stabilization of shift operation can be provided if use is made in shift operations not only of the abovementioned plasma coupling but also of wall charges generated by discharges. It is to be considered that since adjacent discharge cells are arranged in a form such that opposite respective ends of a common electrode are employed thereby, in an M type self-shift panel having a meander electrode configuration as shown in Figure 1, wall charge generated on a dielectric layer should be easily employable for shift operation. In order to employ wall charge in such circumstances, shift pulses should be applied to a discharge cell which is to receive a discharge spot of such a polarity that the wall charge generated on the dielectric layer at that side of the cell at which the common electrode that it shares with the adjacent cell from which the spot is to be delivered is formed can assist the shift operation, when shifting a discharge spot between two adjacent discharge cells defined with one electrode in common. When wall charge is employed for assisting shift operation, the use of positively charged ions has been found to be generally desirable.

Figure 14 illustrates an example of driving signal waveforms for putting into effect such shift operations in an M type self-shift panel, and in Figure 14 similar items are denoted by the same reference symbols as are used in Figure 2, Figure 9 and Figure 10. As can be understood from Figure 14, each electrode normally has a constant positive shift voltage potential Vs applied thereto from the corresponding bus conductor, but the electrodes are sequentially clamped to ground potential so that they can attract positive ions from the corresponding common electrodes at each shift timing instant $t1$, $t2$, $t3$, and thereafter they are driven for a specified stabilizing period of several pulse application cycles (four cycles shown).

In other words, referring to Figure 1(B) and Figure 14, during a write period TO in which a train of pulses VY1 which are switched between voltage levels O and Vs is supplied to electrode $y11$, write pulses pw are applied to write electrode W, causing a voltage such as VW shown in Figure 14 to be applied across write discharge cell w, said voltage VW generating a discharge which is accompanied by a wall voltage Vwc, as a result of the generated wall charge, as shown by broken lines in Figure 14. During the above period, a pulse voltage train VA, generated by the combination of voltages applied through bus conductor X1 and bus conductor Y1 is applied across the adjacent discharge cell $a1$ which employs electrode $y11$, also used by the discharge cell w, and when the electrode $x11$ is at a voltage 0 and the electrode $y11$ is at a voltage Vs, wall charge of positive polarity, positive ions, adjacent the common electrode $y11$ and produced as a result of the above write discharge, is then shifted to the electrode $x11$ so that discharge shifting is aided by the wall voltage Vwc developed by the write discharge in order to provide a shifted discharge at the discharge cell ai. One electrode, $x11$, of the electrodes defining this discharge cell ai there-between is used in common by a next discharge cell bi adjacent to said discharge cell ai. Consequently, when a voltage is applied across the next adjacent discharge cell bi at the timing $t1$ in such a manner that a voltage Vs is applied to the common electrode $x11$ and a voltage 0 is applied to the common electrode $y21$, for example as shown at VB in Figure 14, after the common electrode $x11$ at the discharge cell ai has been given a voltage 0 and the opposite electrode $y11$ has been given a voltage Vs so that a

discharge can take place at cell *ai*, then the positive wall charge generated on the side of the common electrode $x11$ is attracted to the electrode $y21$, thus helping discharge shift to take place. When a pulse voltage Vs of a polarity which makes the electrode $x21$ negative (0), such as shown at VC, is applied between the electrodes $y21$ and $x21$, defining the next adjacent discharge cell ci therebetween, at the timing $t2$, after alternate pulses have been applied furing a period T1 to cell *bi* for stabilizing wall charge produced by discharge shifted thereto, the positive wall charge developed at the common electrode $y21$ by the pulse voltages applied across the discharge cell *bi* is then shifted to the electrode $x21$ and discharge shift takes place to cell *ci*, in a manner similar to that described above.

As described above, the shift operation illustrated in Figure 14 is achieved by applying pulse voltages for use in shifting, of such polarity that wall charge produced on the electrode which is used in common by the discharge cell which is to receive a discharge spot and the cell from which the spot is to be shifted is attracted, to assist shifting, to the electrode arranged on the opposite side to the common electrode of the cell which is to receive the spot. Therefore, the shift pulse voltage effective at a cell at shift timing must have a polarity opposite to that of the pulse voltage previously applied to the discharge cell (charge source cell) from which a discharge spot is being shifted and which has one electrode in common with the cell which is to receive the spot. The wall charge to be used for the shift operation may be positively charged ions, or electrons, but when consideration is given to erasing effects at discharge cells from which the discharge spot has been shifted, it is found to be preferable that ions should be used as described in the above embodiment. In other words, the wall charge remaining at the opposite electrode (the electrode not used in common by the cell to which the discharge spot is shifted) of a discharge cell from which the discharge spot is shifted must be erased before a pulse voltage belonging to a succeeding shift period is applied through the bus conductors, and in this case, if positive ions at the common electrode are used for assisting shift operation the wall charge remaining at the opposite electrode comprises electrons which are of a lesser mass than the ions, which can readily be neutralized and erased by means of the shift discharge of the adjacent discharge cell without any particular erase operation. However, in order to obtain an erase effect of greater accuracy, it is preferable to apply an erase pulse of relatively short duration to a discharge cell from which a discharge spot has been shifted, and when such an erase pulse is employed, positive or negative wall charge can be used for the shift operation. If electrons, forming negative wall charge, are used for shifting, it is necessary of course to supply shift voltage pulses Vs sequentially to the bus conductor with each electrode normally fixed to ground potential, the opposite of the waveforms shown in Figure 14.

When performing discharge spot shift operations employing wall charge shifting as described above, it will be noted from the waveforms of Figure 14 that several cycles of alternate shift pulses are continuously applied to a discharge cell which has received a discharge spot before a next shift. This train of shift pulses is used for the purpose of stabilizing the wall charge produced by discharge shift, and is significant in relation to improving shift operation margin.

In an experiment made by the inventors, where the pulse width was selected to be 12 μsec and frequency to be 40 kHz, if a discharge spot received at one discharge cell by making 0 a shift pulse is driven by a next following pulse to be shifted again to an adjacent discharge cell, the shift pulse voltage has a margin of only 2V between the upper and lower permissible limits thereof, whereas interposition of a train of alternate pulses comprising four cycles of shift pulses enables the voltage margin to be enlarged, particularly at its lower limit, to about 10V. This indicates that a single pulse of a discharge spot which takes place at shift timing does not produce sufficient wall charge at the appropriate discharge cell to give reliable further shifting, but repeated pulses of a discharge spot several times can produce sufficient wall charge to permit a next diagonally opposite electrode to discharge.

Several major embodiments of the present invention have been described above, but various modifications or alternatives will be apparent to the appropriately skilled person. For example, various described embodiments may be combined together or with previously proposed systems. Moreover, the present invention can be adapted not only to a panel having a 2 × 2- phase-driven meander electrode structure as explained with reference to Figure 1 but also to panels having a matrix electrode structure as described in U.S. Patent No. 3,944,875, panels having a parallel electrode structure as described in U.S. Patent No. 3,775,746, and to other panels described in West German Offenlegungsschrifts Nos. 2729659 and 2731008, and can be adapted also to other scanning type electronic devices.

Thus, an embodiment of the present invention can provide drive circuitry for driving a self-shift type gas discharge panel, which circuitry provides a plurality of basic pulse trains that are required for discharge spot shift operations and, for each phase of the multi-phase discharge cell array of the

panel can supply such basic pulse trains in a cyclically repeated sequence in which each pulse train is applied for a unit period of time. Timing control for switching between different pulse trains for each phase can be effected relatively easily and in addition stable and accurate shift operations can be realized by selection of the combinations of basic pulse train employed.

WHAT WE CLAIM IS:-

1. Driving circuitry, for a pulse-driven electronic device of the scanning type having a plurality of driving electrode inputs, comprising pulse-train generating circuitry having a plurality of outputs, for connection respectively to such inputs, and operable to deliver at the said outputs, within a predetermined unit supply period, respective pulse trains of predetermined respective waveforms at least one of which differs from the others, such delivery being repeated with cyclic change-over of each pulse train from one to another of the said outputs between one such unit supply period and the next so that in the course of a working cycle of the driving circuitry, made up of a plurality of such unit supply periods, all of the said respective pulse trains are delivered in sequence at each output, the sequential order of such delivery being different at each output from that at every other output of the plurality.

2. Driving circuitry as claimed in claim 1, wherein the pulse-train generating circuitry comprises a clock pulse generator and bit-sequence supply means which are operable, in dependence upon clock pulses delivered from the clock pulse generator, to supply a plurality of predetermined sequences of data bits in parallel bit by bit, in a cyclically repeating manner such that the sequences are each supplied once in each unit supply period, to change-over control means which are operable in each unit supply period to pass on the sequences to respective pulse generators that are operable in response to deliver to respective said outputs respective such pulse trains the waveforms of which are determined by the bit values of the sequences of bits received at the pulse generators, and to cyclically change over, from one unit supply period to the next, the pulse generators to which the respective sequences are passed on, thereby to provide such cyclic change-over of each pulse train from one to another of the said outputs.

3. Driving circuitry as claimed in claim 2, wherein the said bit-sequence supply means comprise a memory for storing the said plurality of predetermined sequences of data bits.

4. Driving circuitry as claimed in claim 2, wherein the said bit-sequence supply means comprise multi-bit counter means arranged to count the said clock pulses and to provide from a plurality of outputs thereof, at any given time, in a bit-parallel form, a binary number indication of the count value currently achieved, and logic circuitry operable by predetermined logic processing of successive bit-parallel count value indications provided from outputs of the multi-bit counter means in each unit supply period to supply the said predetermined bit sequences.

5. Driving circuitry as claimed in claim 4, wherein the said change-over control means comprise a decoder, connected to receive more significant bits of such bit-parallel form binary number indications from the multi-bit counter means, in dependence upon an output signal of which change over of the pulse generators to which the respective sequences are passed on is caused each time those more significant bits indicate that, since a last change over, a number of clock pulses representative of the elapse of a unit supply period have been counted at the multi-bit counter means.

6. Driving circuitry as claimed in claim 1, wherein the pulse-train generating circuitry comprises memory means for storing a plurality of predetermined sequences of data bits, a clock pulse generator in dependence upon clock pulses from which the predetermined sequences are supplied in parallel bit by bit, such that the complete sequences are supplied once in each working cycle of the driving circuitry, to pulse generators connected respectively to receive the predetermined sequences of bits and operable in response to deliver to respective said outputs, in the course of each working cycle, all of the said respective pulse trains, in the different sequential orders.

7. Driving circuitry as claimed in any preceding claim, for a gas discharge device of the scanning kind having first and second substrates, respective surfaces of which confront one another across a discharge gas space of the device, first and second arrays of electrode members provided on the first and second substrates respectively, on the said respective surfaces, electrode members of the first array being arranged so as to cross or overlap electrode members of the second array to define respective discharge cells of the device where respective electrode members cross or overlap, and a plurality of supply buses connected to the electrode members of the arrays, there being a shift path in the device providing a sequence of discharge cells through which a discharge spot can be shifted, from one cell to a next adjacent cell, in response to the application of pulse voltages to the supply buses of the said plurality, each discharge cell of the sequence being defined by electrode members connected to respective buses of a pair of the supply buses and along the shift path from one cell to the next the pair combinations of supply buses to

which the cell-defining electrode members are connected being repeated in a cyclical manner, the supply buses of the said plurality being connected to respective driving electrode inputs of the device.

8. Driving circuitry as claimed in claim 7, for a gas discharge device of the said scanning kind in which electrode members of first and second electrode member groups, of the first array of electrode members, are arranged so that individual electrode members of the first group alternate, along the shift path, with individual electrode members of the second group, and in which electrode members of the third and fourth electrode member groups, of the second array of electrode members, are arranged so that individual electrode members of the third group alternate, along the shift path, with individual electrode members of the fourth group, electrode members of each said group on the first or second substrate each overlapping two adjacent consecutive electrode members one from each of the two said groups on the second or first substrate, respectively, and the electrode members of each said group being connected in common to a respective supply bus of the said plurality.

9. Driving circuitry as claimed in claim 8, wherein there are four such pulse trains in all, each being delivered once to each of four such outputs of the pulse-train generating circuitry that are connected respectively to the supply buses of the said electrode member groups in each such working cycle, whereby a discharge spot can be shifted from one cell to a next adjacent cell along the shift path of the gas discharge device, the discharge spot being shifted in each working cycle through a series of cells defined one each by electrodes connected to the four different pair combinations of the supply buses of the said electrode member groups.

10. Driving circuitry as claimed in claim 9, wherein the four pulse trains and the sequential orders of delivery of those pulse trains to the supply buses of the said electrode member groups in each working cycle are such that first and second pulse trains comprising respective phased apart series of pulses are applied to respective supply buses connected to electrode member groups provided on different ones of the first and second substrates in each unit supply period, the first and second pulse trains being such that when they are applied via the supply buses to the electrodes defining a cell to which a discharge spot is shifted they cause repeated discharging at that cell, and the first pulse train and a third pulse train, comprising a series of pulses, are applied to respective supply buses connected to electrode member groups provided on different ones of the first and second substrates in each unit supply period, pulses of the pulse series of the first and third pulse trains being phased apart such that when they are applied via the supply buses to a discharge cell erase pulses, of a width corresponding to the difference in phasing between those pulse trains, are effectively applied at the cell, the pulses of the pulse series of each of the first, second and third pulse trains all being of the same pulse width.

11. Driving circuitry as claimed in claim 10, wherein a fourth pulse train, comprising a series of pulses, is applied to a supply bus connected to the other electrode member group provided on that substrate one electrode member group on which is currently having the first pulse train applied thereto, in each unit supply period, the first and fourth pulse trains comprising like, in-phase, series of pulses.

12. Driving circuitry as claimed in claim 10 or 11, wherein a first pulse of the pulse series of the third pulse train is of like phase to the first pulse of the pulse series of the first pulse train.

13. Driving circuitry, for a pulse driven electronic device of the scanning type having a plurality of driving electrode inputs, substantially as hereinbefore described.

14. Driving circuitry, for a gas discharge device of the kind set forth in claim 8, substantially as hereinbefore described with reference to Figures 1(A), 1(B), 2, 3(A), 3(B) and 4, or Figures 1(A), 1(B), 2, 3(A), 3(B), 5 and 6 or Figures 1(A), 1(B), 7, 8 and 9, or Figures 1(A), 1(B), 7 and 10, or Figures 1(A), 1(B), 10 and 13, or Figures 1(A), 1(B) and 14, of the accompanying drawings.

15. A method of driving a self-shift gas discharge device of the kind having first and second substrates, respective surfaces of which confront one another across a discharge gas space of the device, first and second arrays of electrode members provided on the first and second substrates respectively, on the said respective surfaces, electrode members of the first array being arranged so as to cross or overlap electrode members of the second array to define respective discharge cells of the device where respective electrode members cross or overlap, and a plurality of supply buses connected to the electrode members of the arrays, there being a shift path in the device providing a sequence of discharge cells through which a discharge spot can be shifted, from one cell to a next adjacent cell, in response to the application of pulse voltages to the supply buses of the said plurality, each discharge cell of the sequence being defined by electrode members connected to respective buses of a pair of the supply buses and along the shift path from one cell to the next the pair combinations of supply buses to which the cell-defining electrode members are connected being repeated in a cyclical manner, the sup-

ply buses of the said plurality being connected to respective driving electrode inputs of the device, wherein first and second adjacent successive dishcarge cells along the shift path are defined respectively where an electrode member of the first array overlaps first and second electrode members of the second array; in which method, in order to shift a discharge spot from the first discharge cell to the second discharge cell, shift voltage pulses of like polarity are applied to the said electrode member of the first array and the said second electrode member of the second array alternately, thereby to activate the second discharge cell to receive the discharge spot, and shift voltage pulses of the said like polarity are applied to the said first electrode member of the second array with a phase difference from the shift voltage pulses applied to the said electrode member of the first array such that successive narrow erase pulses are effectively applied at the said first discharge cell.

16. A method as claimed in claim 15, wherein there is applied to the said first electrode member of the second array, prior to the application of the said shift voltage pulses of the said like polarity, with the said phase difference, to the said first electrode member, a shift voltage pulse of like polarity and phasing to one of the said shift voltage pulses applied to the said electrode member of the first array.

17. A method of driving a self-shift gas discharge device which device is of the kind set forth in claim 15, substantially as hereinbefore described with reference to Figure 9 or Figure 10 of the accompanying drawings.

18. A method of driving a self-shift gas discharge device which device is of the kind set forth in claim 15, in which method, in order to shift a discharge spot from the first discharge cell to the second discharge cell, a first pulse voltage of a predetermined polarity is applied between the said electrode member of the first array and the said first electrode member of the second array, thereby to generate wall charges on a dielectric layer provided over the said electrode member of the first array, and thereafter a second pulse voltage of polarity opposite to the said predetermined polarity is applied between the said electrode member of the first array on the said second electrode member, whereby the wall charges generated by the said first pulse voltage are attracted to the location of the said second discharge cell to assist the shifting of the discharge spot thereto.

19. A method as claimed in claim 18, wherein the said predetermined polarity is such that when the first pulse voltage is applied the said electrode member of the first array and the said first electrode member of the second array are negative and positive respectively and when the said second pulse voltage is applied the said electrode member of the first array and the said second electrode member of the second array are positive and negative respectively.

20. A method of driving a self shift gas discharge device, which device is of the kind set forth in claim 18,substantially as hereinbefore described with reference to Figure 14 of the accompanying drawings.

21. Driving circuitry as claimed in claim 7, for driving a scanning gas discharge device in accordance with a method as set forth in claim 15, 16, 17, 18, 19 or 20.

HASELTINE, LAKE & CO.,
Chartered Patent Agents,
Hazlitt House,
28 Southampton Buildings,
Chancery Lane,
London WC2A 1AT.
also
Temple Gate House,
Temple Gate,
Bristol B81 6PT.
and
9 Park Square,
Leeds LS1 2LH,
Yorks.

Printed for Her Majesty's Stationery Office,
by Croydon Printing Company Limited, Croydon, Surrey, 1981.
Published by The Patent Office, 25 Southampton Buildings,
London, WC2A 1AY, from which copies may be obtained.

1589685 COMPLETE SPECIFICATION
12 SHEETS *This drawing is a reproduction of the Original on a reduced scale*
Sheet 1

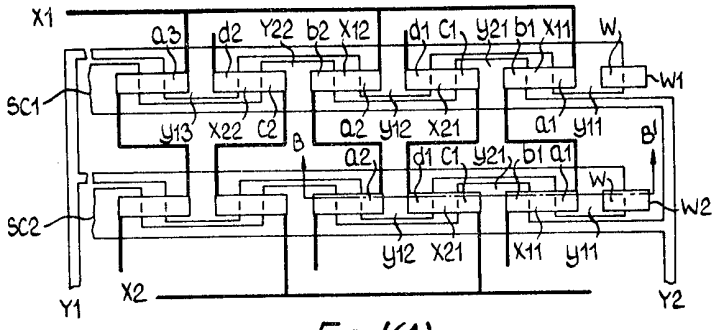


FIG. 1(A)

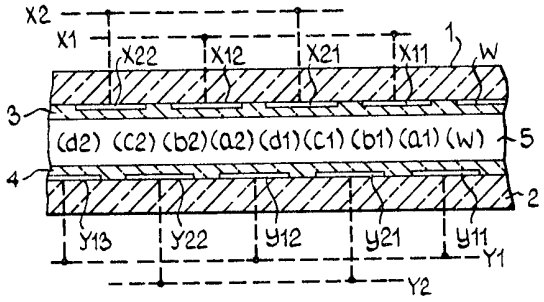
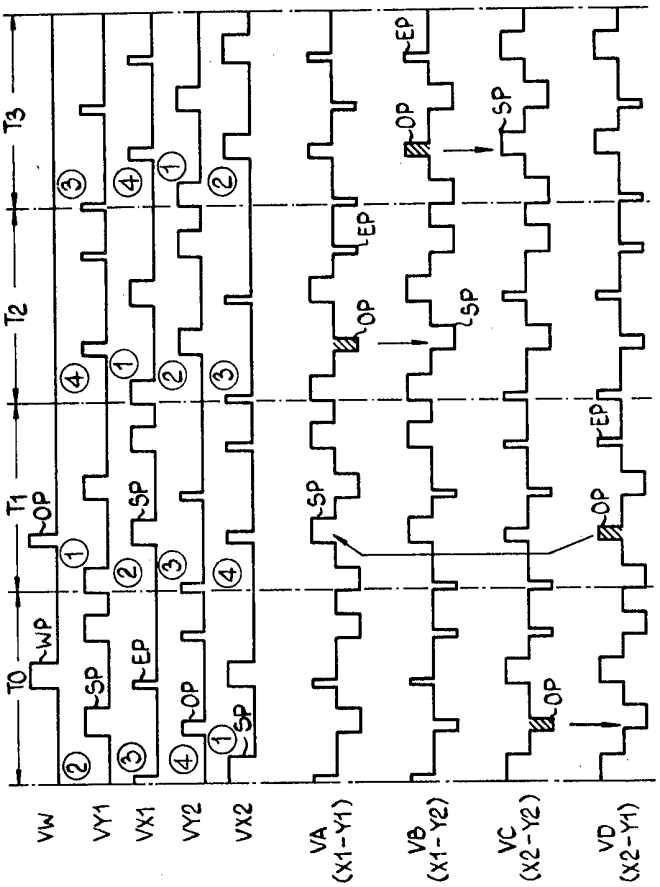


FIG. 1(B)

1589685 COMPLETE SPECIFICATION
12 SHEETS *This drawing is a reproduction of the Original on a reduced scale*
Sheet 2

FIG. 2.



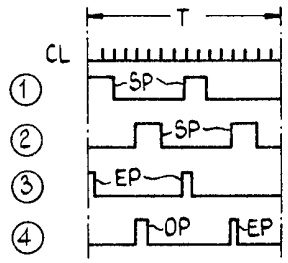


FIG. 3 A

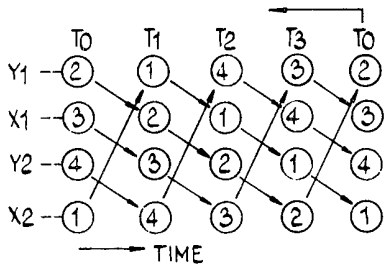
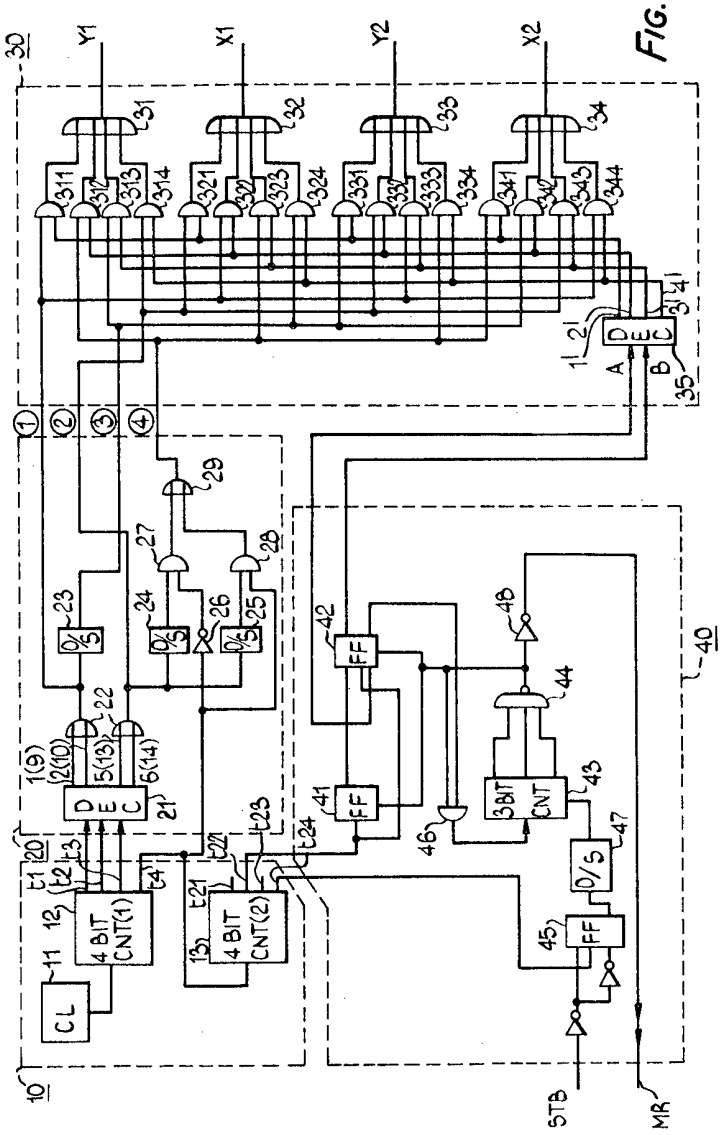


FIG. 3 B

FIG. 4.


30
Y1
X1
Y2
X2
31
32
33
34
311
312
313
314
321
322
323
324
331
332
333
334
341
342
343
344
D
E
C
A
B
35
1
2
3
4
29
27
28
23
24
25
26
22
1(9)
2(10)
5(13)
6(14)
21
20
E1
E2
E3
E4
E21
E22
E23
E24
12
4 BIT CNT(1)
13
4 BIT CNT(2)
11
CL
10
42
FF
41
FF
46
44
3BIT CNT
43
47
D/5
45
FF
48
40
STB
MR

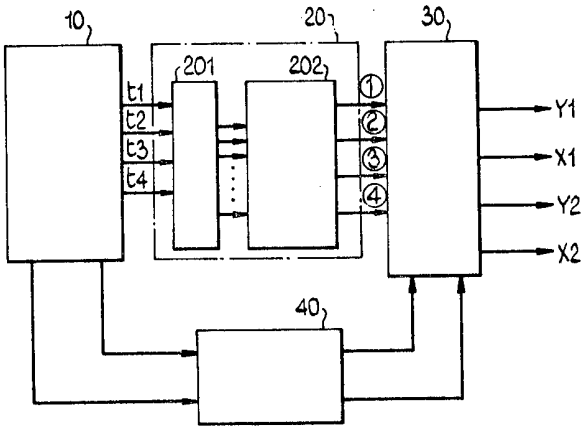


FIG. 5.

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	
1	1	0	0	0	0	0	0	1	1	0	0	0	0	0	0	→ ①
0	0	0	0	1	1	0	0	0	0	0	0	1	1	0	0	→ ②
1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	→ ③
0	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0	→ ④

FIG. 6.

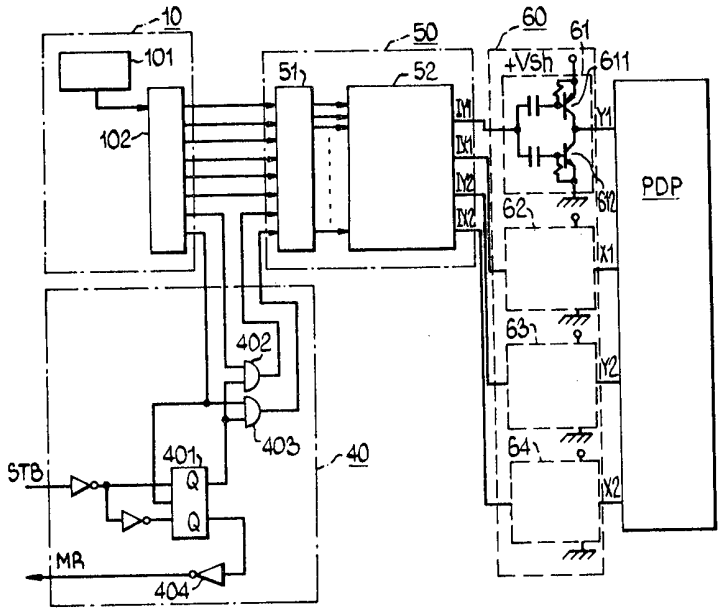

10
101
102
50
51
52
60
61
611
+Vsh
PDP
62
63
64
402
403
401
Q
Q
40
STB
MR
404

FIG. 7

1589685 COMPLETE SPECIFICATION

12 SHEETS *This drawing is a reproduction of the Original on a reduced scale*

Sheet 7

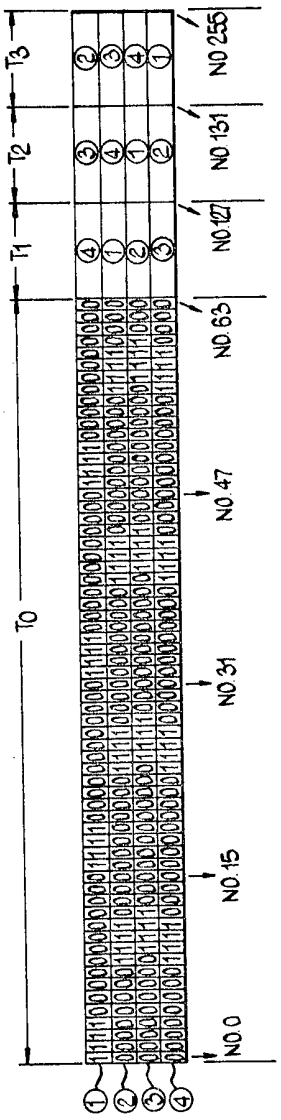


FIG. 8.

1589685 COMPLETE SPECIFICATION

12 SHEETS *This drawing is a reproduction of the Original on a reduced scale*

Sheet 8

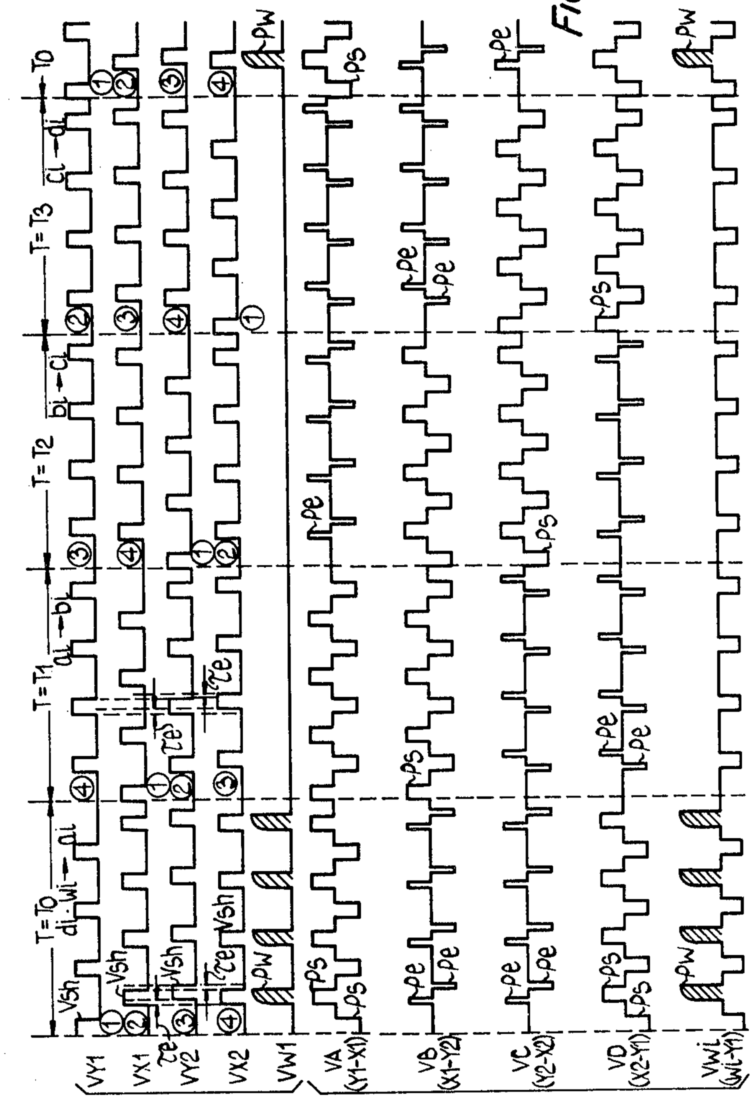
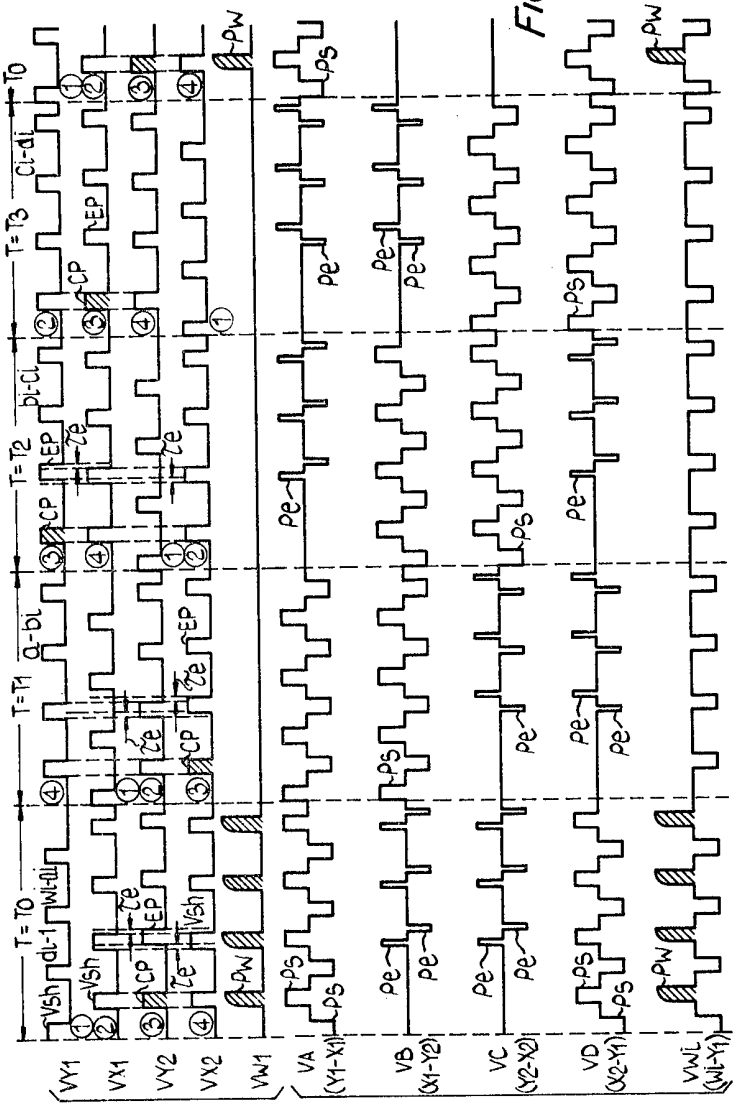


FIG. 9

FIG. 10.


T=T0
T=T1
T=T2
T=T3
T0
Vsh
dl-1
Wi-dl
Q-bl
bl-cl
cl-dl
CP
EP
Te
Pe
Ps
Pw
VY1
VX1
VY2
VX2
VW1
VA (Y1-X1)
VB (X1-Y2)
VC (Y2-X2)
VD (X2-Y1)
VW1 (W1-Y1)

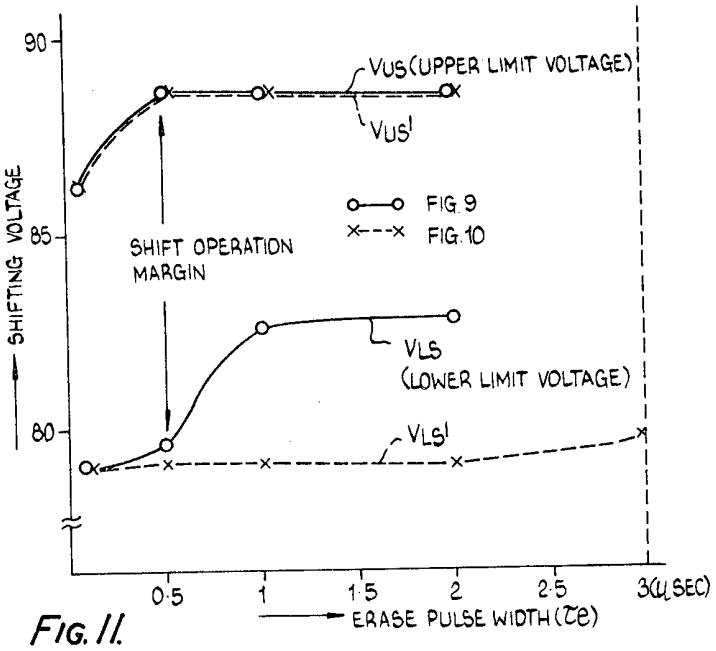


FIG. 11.

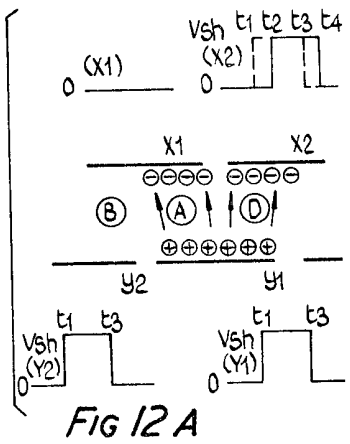


FIG 12 A

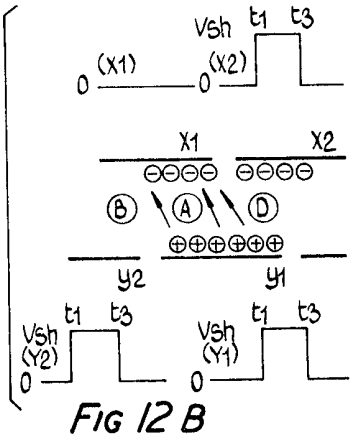


FIG 12 B

1589685 COMPLETE SPECIFICATION
12 SHEETS *This drawing is a reproduction of the Original on a reduced scale*
Sheet 11

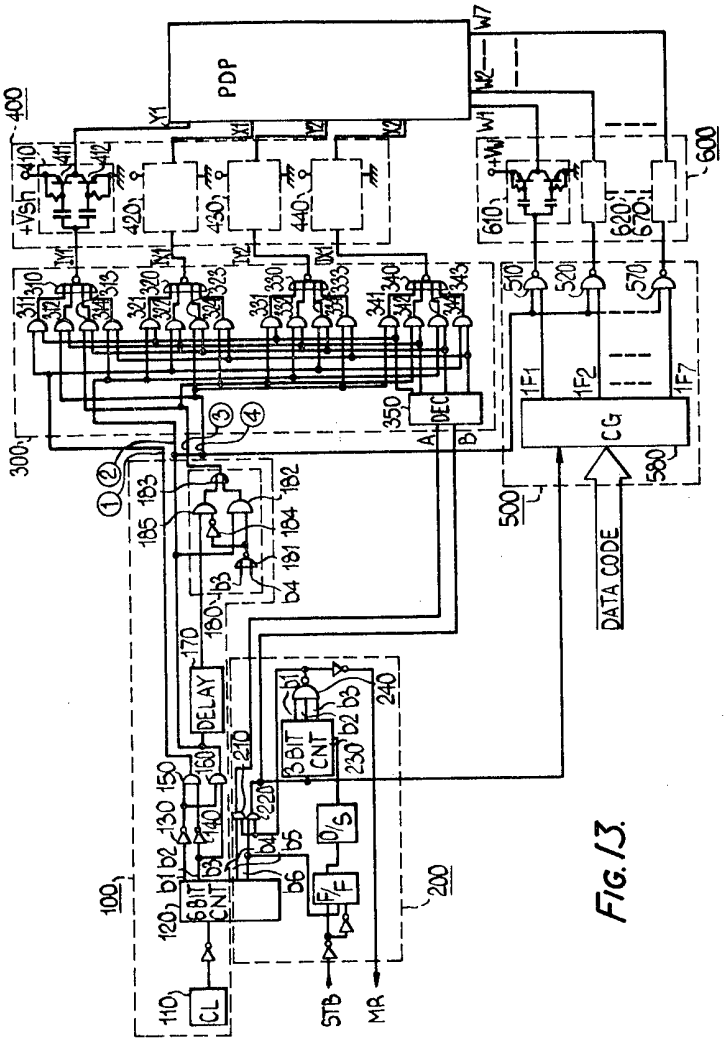
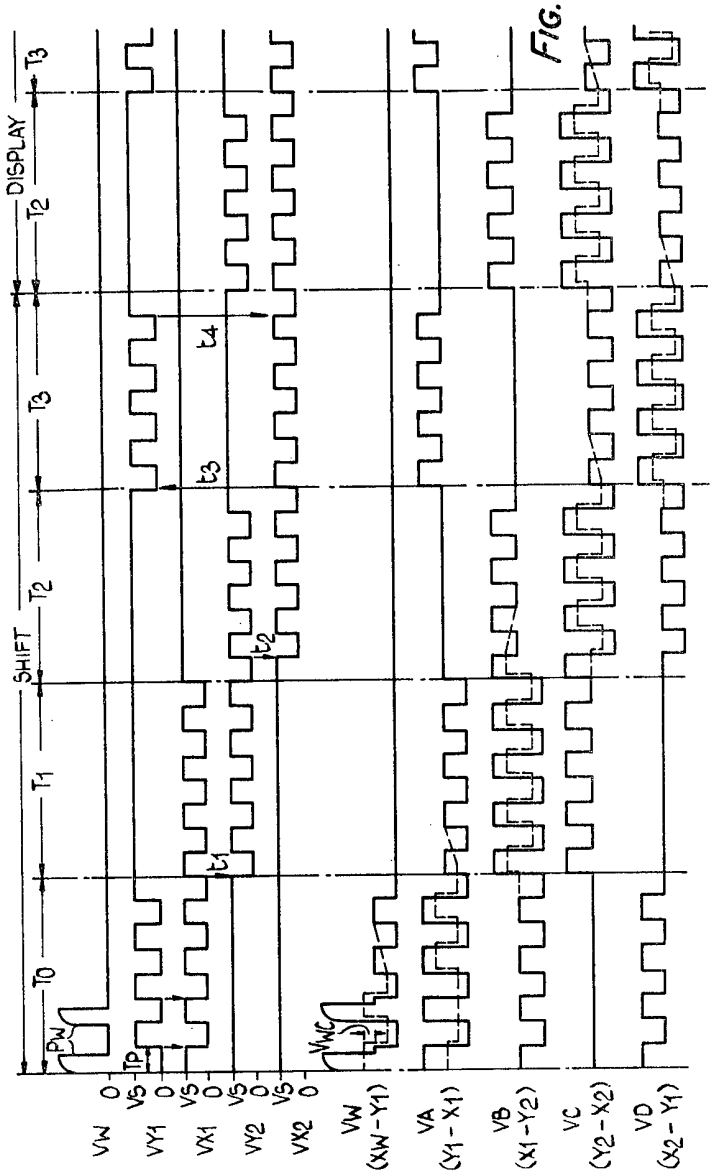


FIG. 13.

FIG. 14.


DISPLAY
SHIFT
T0
T1
T2
T3
T2
T3
PW
TP
t1
t2
t3
t4
VW
VY1
VX1
VW2
VX2
VW (XW-Y1)
VA (Y1-X1)
VB (X1-Y2)
VC (Y2-X2)
VD (X2-Y1)
VS
0