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(54) **Title**: CONTROLLING A MODULAR CONVERTER

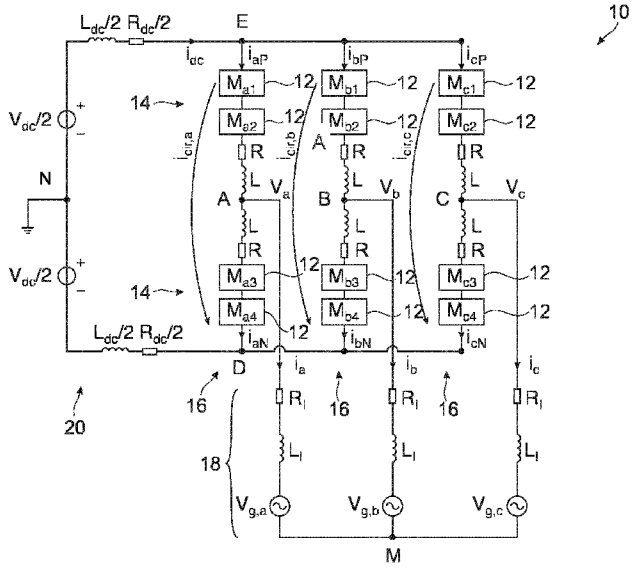

Fig. 1

(57) **Abstract**: A method for controlling a modular converter (10) with a plurality of converter modules (12) comprising the steps of: selecting possible future switching sequences of the converter (10) based on an actual converter switching state, wherein a switching sequence is a series of converter switching states with at least one converter switching state and a converter switching state comprises switching states of the converter modules;predicting a future current trajectory for each switching sequence based on actual internal currents and on actual internal voltages;determining candidate sequences from the switching sequences, wherein a candidate sequence is a switching sequence with a current trajectory that respects predefined bounds with respect to a reference current or, when a predefined bound is violated, moves the current closer to such a predefined bound;predicting future module voltages for each candidate sequence based on actual module voltages and the current trajectory of the respective candidate sequence;evaluating a cost function for each candidate sequence, wherein the cost function is based on the converter switching states of the switching sequence, the future module voltages and/or future currents;and selecting the next converter switching state as a first converter switching state of a candidate sequence with minimal costs.

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DESCRIPTION

Controlling a modular converter

FIELD OF THE INVENTION

The invention relates to a method for controlling a modular converter, a controller for controlling a modular converter and a modular converter.

BACKGROUND OF THE INVENTION

Electrical converters, in particular in the medium and high voltage area, are used for converting a first current with a first frequency and a first voltage into a second current with a second frequency and a second voltage. Many types of converters are known such as for converting AC to AC, AC to DC, DC to AC and DC to DC.

Usually, converters comprise high power semiconductors for switching internally currents to produce the desired output current. In modular converters, these power semiconductors are distributed among converter modules, which also may comprise further components like a controller for the semiconductors or a capacitor for storing energy in the converter module.

For example, the M2LC topology has become popular in both medium and high voltage applications. An M2LC converter or modular multi-level converter comprises converter arms with converter modules connected in series for generating a multi-level output voltage. In an M2LC converter the converter modules each comprise a capacitor themselves.

The standard approach to achieve closed-loop control for an M2LC converter is to divide the control problem into two hierarchical layers. The upper layer is based on vector control with a modulator. The vector control scheme operates in a orthogonal reference frame rotating with a certain angular velocity. By manipulating the voltage reference to the modulator, closed-loop control of the load currents can be achieved. Typically, carrier-based pulse width modulation (PWM) or space vector modulation (SVM) is used as

modulator. The circulating currents and/or the energy balance within the converter arms may be addressed by adding additional control loops.

The lower control layer utilizes the redundancy in the converter states (e.g. groups of switching states that produce the same line to line voltage, and/or groups of switching states that produce the same arm voltage) in order to balance the capacitor voltages. The capacitor voltages are sorted in an ascending/descending order of their voltage values. For a charging current the capacitors with the lowest voltages are selected first, and conversely, the capacitors with the highest voltages are prioritized for discharging currents.

DESCRIPTION OF THE INVENTION

It is an objective of the invention to provide an alternative solution for controlling a modular converter, to reduce the switching losses of a modular converter, to balance the capacitor voltages, and to reduce harmonics in the input and output currents of a modular converter.

It is a further objective of the invention to provide a control schema with good performance during steady-state as well as during transient operating conditions.

These objectives are achieved by the subject-matter of the independent claims. Further exemplary embodiments are evident from the dependent claims and the following description.

An aspect of the invention relates to a method for controlling a modular converter with a plurality of converter modules. A converter module may comprise a number of power semiconductors and optionally a capacitor or more generally an energy storage and/or an energy source. For example, the power semiconductors are interconnected in such a way, that two power connectors of each of the modules may be short-circuited in a first switching state and may be connected to the energy storage and/or the energy source in a second switching state.

The method comprises the steps of: selecting possible future switching sequences, predicting a future current trajectory for each switching sequence, determining candidate sequences from the switching sequences, predicting future module voltages for each candidate sequence, evaluating a cost function for each candidate sequence and selecting the next converter switching state based on the result of the cost function.

The possible future switching sequences of the converter are selected based on an actual converter switching state, wherein a switching sequence is a series of converter switching states with at least one converter switching state and a converter switching state comprises switching states of the converter modules.

The future current trajectory for each switching sequence is predicted based on actual internal currents of the modular converter and on actual internal voltages of the modular converter. The current trajectory may be a trajectory of a load current, an arm current or a circulating current. The future current trajectory may be predicted for more than one time step in the future. For example, the actual internal currents comprise arm currents and/or a DC link current and/or circulating currents, the actual internal voltages may comprise phase voltages and/or arm voltages and/or the DC link voltage. For example, based on an internal state-space model of the converter, the trajectories of key system variables, such as load currents, circulating currents and/or capacitor voltages, are predicted for all admissible switching sequences.

The candidate sequences are determined from the switching sequences such that a candidate sequence is a switching sequence with a current trajectory that respects predefined bounds with respect to a reference current or, when a predefined bound is violated, moves the current trajectory closer to the predefined bound. For example, a load current may be kept within symmetrical bounds around its sinusoidal references. The total harmonic distortion of the current may be adjusted by varying the width of the predefined bounds. The relationship between the total harmonic distortion and the bound width is usually effectively linear.

Switching sequences that keep the load currents within their bounds or move them closer to the bounds (when they are violated) are determined and called candidates. These candidate trajectories are extrapolated or extended until a certain criterion is met such as the violation of a hysteresis bound. At this point new switching vectors can be considered and another extrapolation step can be performed, and so on.

The future module voltages for each candidate sequence are predicted based on actual module voltages and the current trajectory of the respective candidate sequence. For example, from predicted currents and the switching states the voltage between the outputs of a converter module and/or across a capacitor of the converter module may be calculated.

The cost function is evaluated for each candidate sequence. The cost function is based on the converter switching states of the switching sequence, the future module voltages and

or future currents. For example, the value of the cost function may be based on the number of switchings between switching states and/or the switching losses caused by the switchings of a switching sequence. In general, the cost function may include the predicted short-term switching frequency (or switching losses), the violation of the current bounds, the deviation of the capacitor voltages from their references, the mismatch between capacitor voltages within an arm, etc. The future currents may be internal current determined for the current trajectories and/or may be future load currents.

The next converter switching state is selected as the first converter switching state of a candidate sequence with minimal costs. Minimizing the cost function yields the optimal switching vector. At the next sampling instant, new measurements or estimates may be obtained and the above described optimization process may be repeated over a shifted horizon, according to a so-called receding horizon policy. With the method, the switching states are manipulated directly. An intermediate stage, such as a modulator, is not required.

The method features an online optimization process to determine the future control inputs, without using a modulation stage, to directly control the load currents and offers a great flexibility to handle various system objectives.

The method may be implemented in a controller with only a single control loop, while the considered currents are kept within upper and lower bounds around their references.

The method has the advantages of direct current control without a modulation stage, of a fixed and controlled ripple of the load currents, and of very short response times during transients. At steady-state, the desired trade-off may be set by the weights in the cost function.

Furthermore, the capacitor voltages may be balanced around their nominal voltages. In this case, the energy stored in the converter may be controlled, the converter modules may be equally voltage stressed, the arm currents may be optimized, circulating currents may be reduced, and conduction losses are lowered.

At steady-state operating conditions and for a given load current distortion, the lowest possible switching frequency may be achieved.

According to an embodiment of the invention, each converter module has exactly two power connectors which are short-circuited in the first switching state of the semiconductors and are connected to the energy storage and/or energy source in the second switching state of the semiconductors.

According to an embodiment of the invention, the cost function is based on a number of switching operations between two consecutive converter switching states. In such a way, the number of switching operations may be reduced or minimized.

According to an embodiment of the invention, the cost function is based on a difference between module voltages of converter modules of a converter arm comprising at least two converter modules connected in series. In such a way, the differences between capacitor voltages may be minimized.

According to an embodiment of the invention, the cost function is based on a difference between a module voltage and a supply voltage at an input of the converter. In such a way, a reference value for the phase voltage may be set and ripples around the reference value may be reduced.

According to an further embodiment of the invention, the cost function is based on a difference between a module voltage and a supply voltage of the converter divided by the number of modules per arm. In such a way, a reference value for the phase voltage may be set and ripples around the reference value may be reduced.

According to an embodiment of the invention, the cost function is based on a difference between the sum of module voltages of a first converter arm for a phase and the sum of module voltages of a second converter arm for the same phase or a different phase. In such a way, the imbalance in capacitor voltages of different converter arms may be minimized.

According to an embodiment of the invention, the cost function is based on a difference between the sum of module voltages of a first phase and the sum of module voltages of a second phase. In such a way, the imbalance in capacitor voltages of different converter phases may be minimized.

According to an embodiment of the invention, the method further comprises the step of: deselecting candidate sequences for which future module voltages do not stay within predefined bounds. Also the module voltages may be constrained to predefined bounds. Furthermore, the number of admissible candidate sequences may be reduced on which the cost function has to be evaluated.

According to an embodiment of the invention, each converter module comprises a module capacitor. In particular, a modular multi-level converter may comprise converter modules with a capacitor that is adapted for storing energy in the converter module. The module voltages that are predicted and optimized with the method may be capacitor voltages over module capacitors.

According to an embodiment of the invention, a switching sequence comprises a switching step associated with a converter switching state, in which switching step the future current of the converter is predicted when switching the converter into the associated converter switching state; and /or a switching sequence comprises an extrapolation step, in which the load current is extrapolated over at least one time step until it violates the bounds for the load current. In general, a switching sequence may comprise a plurality of steps which either are switching steps or extrapolation steps.

The set of switching sequences determined by the method may be established by using the notion of S ("switch") and E ("extend", "extrapolate"), forming the switching horizon. The switching horizon may comprise any combination of S and E steps. The extrapolation step may be approximated, for example using linear or quadratic extrapolation, or prediction with quadratic interpolation. Higher order approximations are possible, too. The notion of switch and extend achieves long prediction horizons, and therefore better steady-state performance, while using a short switching horizon, ensuring that the computational burden is kept at bay. The switching horizon may be composed of an arbitrary sequence of elements S and E.

According to an embodiment of the invention, the future current trajectory is predicted based on a first internal model of the converter. The future module voltages may be predicted based on a second internal model of the converter, which is dependent on the first internal model. The two internal models may be state space models of the converter. The first model may capture the evolution of the currents, including the load and the circulating currents, while the second model may capture the evolution of the capacitor voltages. The second model may be dependent on the first model in such a way, that it is based on values predicted by the first model. For example, the two models may be expressed as matrix equations and/or may be linear models.

The first model may be based on linear equations between future currents, actual currents, actual internal voltages and switching states.

The second model may be based on linear equations between future internal voltages, actual internal voltages, actual currents and switching states

According to an embodiment of the invention, the method further comprises the steps of: changing the converter topology by bypassing a converter module; and adapting the first and/or the second model to the changed converter topology. The converter modules of the converter may be monitored in real-time. If a module fails and its terminals have to be

shortened to bypass it, the number of converter modules available is automatically updated and the internal prediction models of the controller is adjusted accordingly. The method may take into account that one or some converter modules are shortened and uses only switching states/sequences that, within the physical limitations of the converter, compensate for these shortened converter modules.

A further aspect of the invention relates to a computer program, which, when being executed on a processor, is adapted for executing the steps of the method as described in the above and in the following. For example, the computer program may be executed in a processor of a controller of the modular converter.

A further aspect of the invention relates to a computer-readable medium in which such a computer program is stored. A computer-readable medium may be a floppy disk, a hard disk, an USB (Universal Serial Bus) storage device, a RAM (Random Access Memory), a ROM (Read Only Memory) and an EPROM (Erasable Programmable Read Only Memory). A computer-readable medium may also be a data communication network, e.g. the Internet, which allows downloading a program code.

A further aspect of the invention relates to a controller for controlling a modular converter, wherein the controller is adapted for executing the steps of the method as described in the above and in the following. The proposed controller may achieve very fast current responses during transients, such as power up or down, or faults. This is in contrast to methods, which focus on the steady-state operation and are, as a result, very slow during transients. The capacitor voltages may be kept more closely to their references i.e. may be better balanced. The switching frequency can be reduced, compared to methods using PWM or SVM.

For example, the controller comprises a DSP and/or FPGA, in which the method is implemented.

A further aspect of the invention relates to a modular converter with a plurality of converter modules each having a capacitor; and a controller that is adapted for executing the steps of the method as described in the above and in the following.

For example, the modular converter is a modular multi-level (M2LC) converter, which may have at least one converter arm with at least two converter modules connected in series. In general, the method may be used for any M2LC control problem. It may be used in M2LC converters with a few modules per arm. It is applicable to all M2LC applications, including variable speed drives, high-voltage direct current transmission, flexible AC

transmission systems, static synchronous compensators, grid-interfaces for battery energy storage systems or PV modules, traction applications, etc. The control scheme is highly flexible allowing one to incorporate and address different control objectives and operation requirements.

These and other aspects of the invention will be apparent from and elucidated with reference to the embodiments described hereinafter.

BRIEF DESCRIPTION OF THE DRAWINGS

The subject matter of the invention will be explained in more detail in the following text with reference to exemplary embodiments which are illustrated in the attached drawings.

Fig. 1 schematically shows a modular converter according to an embodiment of the invention.

Fig. 2 schematically shows a converter module of the converter of Fig .1.

Fig. 3 shows a flow diagram for a method for controlling a modular converter according to an embodiment of the invention.

Fig. 4 shows current trajectories according to an embodiment of the invention.

Fig. 5 schematically shows a controller according to an embodiment of the invention.

Fig. 6 schematically shows a modular converter according to a further embodiment of the invention.

Fig. 7 schematically shows a converter module for the converter of Fig. 6.

Fig. 8 schematically shows a modular converter according to a further embodiment of the invention.

Fig. 9 schematically shows a modular converter according to a further embodiment of the invention.

Fig. 10 schematically shows a modular converter according to a further embodiment of the invention.

Fig. 11 schematically shows a modular converter according to a further embodiment of the invention.

Fig. 12 schematically shows a modular converter according to a further embodiment of the invention.

Fig. 13 schematically shows a modular converter according to a further embodiment of the invention.

In principle, identical parts are provided with the same reference symbols in the figures.

DETAILED DESCRIPTION OF EXEMPLARY EMBODIMENTS

Topology and internal models for a modular converter

Fig.1 shows the topology of a DC-AC modular multi-level converter 10 with two converter modules 12 per converter arm 14. The embodiment of Fig. 1 show M=3 converter phases 16 each comprising an upper and a lower converter arm 14. However, it has to be understood that embodiments of method described in the above and in the following may be applied to converters with an arbitrary number of converter modules 12 per converter arm 14 and with an arbitrary number of converter phases 16.

In case the converter 10 has N=2 converter modules 12 per converter arm 14 and three converter phases 16, the converter has a total of $6N$=12 converter modules. The modules are referred to by $M_{pq}, p \in \{a, b, c\}, q \in \{1, 2, 3, 4\}$.

Besides the two converter modules 12, each arm 14 comprises a resistor R that models conduction losses and an arm inductor L connected in series with the converter modules 12.

The two converter arms 14 of a converter phase 16 are connected in series with a connection point A, B, C for a load 18, which may be a three phase load. Each of the converter phases 16 is connected in parallel to a DC voltage supply 20 via the connection points E and D. The DC voltage supply 20 comprises a DC supply inductor L_{dc} and a resistor R_{dc} that model the parasitic inductance and resistance, respectively. The current driven by the DC link voltage of the DC voltage supply 20 is referred to as the DC link current i_{dc} .

The converter 10 shown in Fig. 1 provides three voltages levels, $\frac{V_{dc}}{2}$, 0, $-\frac{V_{dc}}{2}$, at its output terminals V_a, V_b, V_c, with respect to the supply ground (node N). The output terminals V_a, V_b, V_c are connected to the load 18. The load 18 shown in Fig. 1 is modeled by load inductor L_l in series with a load resistor R_l and the grid voltage $V_{g,p}$.

Fig. 2 shows a converter module 12 for the converter of Fig. 1. The converter module 12 comprises two power semiconductor switches $S_{pq,T}$ and $S_{pq,B}$ which are connected in series and in parallel to a capacitor C_{pq}. The converter module 12 acts like a chopper cell with the capacitor C_{pq}. The converter module 12 has two switching states, $u_{pq} \in \{0,1\}$, where 1 means that the capacitor C_{pq} is connected in the circuit, i.e. switch $S_{pq,T}$ is on, and 0 means that the capacitor is disconnected from the circuit, i.e. switch $S_{pq,T}$ is off. The operation of the switches $S_{pq,T}, S_{pq,B}$ is complementary to one another. The resistor R_{cap} is connected in parallel to the capacitor C_{pq} to model the leakage current of the capacitor C_{pq}.

The converter module 12 has two power connectors 21, 22, which are acting as the input as well as the output of the converter module. Beside the power connectors 21, 22 the converter module might have further connections for controlling the converter module, for diagnose purposes and other control objectives. The power connectors 21, 22 can either short circuited or connected to the capacitor by the power semiconductors switches.

The two power connectors 21, 22 of each converter module are also referred to as the inputs. Further, the voltage $V_{c,pq}$ of the capacitor C_{pq} is referred to as the module voltage as well as capacitor voltage $V_{c,pq}$.

An embodiment of the method is described hereafter for the specific case of a three-level M2LC converter 10 with N=2 modules per arm and M=3 phases. In a subsequent section, the approach is generalized.

The output equations for the load current in phases a, b and c are as follows:

$$i_a(t) = i_{aP}(t) - i_{aN}(t)$$
$$i_b(t) = i_{bP}(t) - i_{bN}(t)$$
$$i_c(t) = -i_{aP}(t) + i_{aN}(t) - i_{bP}(t) + i_{bN}(t)$$

The equation which defines the circulating currents in phases a, b and c is as follows:

$$i_{cir,p}(t) = \frac{i_{pP}(t)}{2} + \frac{i_{pN}(t)}{2} - \frac{i_{dc}}{3}, p \in \{a,b,c\}$$

Two internal models of the converter 10 are derived from these equations to predict the arm currents i_{pP}, i_{pN} and the capacitor voltages $V_{c,pq}$. The state equations of the arm currents i_{pP}, i_{pN} are derived by applying Kirchhoff's voltage law around the five circuit meshes.

The state vector of the first model is $\boldsymbol{x}_i = [\, i_{aP}\ i_{aN}\ i_{bP}\ i_{bN}\ i_{dc}]^T$ and its input vectors are the switching states $\boldsymbol{u} = [u_{a1}\ u_{a2}\ u_{a3}\ u_{a4}\ u_{b1}\ u_{b2}\ u_{b3}\ u_{b4}\ u_{c1}\ u_{c2}\ u_{c3}\ u_{c4}]^T \in \{0,1\}^{12}$ and the grid voltages and the DC voltage across the converter's input terminals $\boldsymbol{V_{gd}} =$

$[V_{g,a}\ V_{g,b}\ V_{g,c}\ V_{ED}]^T$. The load currents $\boldsymbol{y}_i = [\ i_a\ i_b\ i_c\ ]^T$ constitute the output vector of the first model. Note that the index i in $\boldsymbol{x}_i$ and $\boldsymbol{y}_i$ refers to the arm currents.

The first discrete-time model is as follows:

$$\boldsymbol{x}_{\mathrm{i}}(k+1) = \boldsymbol{A}_{\mathrm{i}}\boldsymbol{x}_{\mathrm{i}}(k) + \boldsymbol{B}_{\mathrm{i}1}\boldsymbol{u}(k) + \boldsymbol{B}_{\mathrm{i}2}\boldsymbol{V}_{gd}$$

$$\boldsymbol{y}_{\mathrm{i}}(k+1) = \boldsymbol{C}_{\mathrm{i}}\boldsymbol{x}_{\mathrm{i}}(k+1)$$

The model matrices $\boldsymbol{A}_{\mathrm{i}}, \boldsymbol{B}_{\mathrm{i}1}, \boldsymbol{B}_{\mathrm{i}2}$ and $\boldsymbol{C}_{\mathrm{i}}$ may be derived from the above equations and by applying Kirchhoff's laws to the topology of the converter 10.

The capacitors C_{pq} are charged or discharged depending on the switching state of the converter model 12 and the polarity of the arm current i_{pP}, i_{pN}. The state equations of the capacitor voltages $V_{c,pq}$ can be derived by applying Kirchhoff's current law.

The vector $[V_{c,a1}\ V_{c,a2}\ V_{c,a3}\ V_{c,a4}\ V_{c,b1}\ V_{c,b2}\ V_{c,b3}\ V_{c,b4}\ V_{c,c1}\ V_{c,c2}\ V_{c,c3}\ V_{c,c4}]$ is both state $\boldsymbol{x}_{\mathrm{c}}$ and output $\boldsymbol{y}_{\mathrm{c}}$ vector of the second model. The second discrete-time model is as follows:

$$\boldsymbol{x}_{\mathrm{c}}(k+1) = \boldsymbol{A}_{\mathrm{c}}\boldsymbol{x}_{\mathrm{c}}(k) + \boldsymbol{B}_{\mathrm{c}}\boldsymbol{u}(k)$$

$$\boldsymbol{y}_{\mathrm{c}}(k+1) = \boldsymbol{C}_{\mathrm{c}}\boldsymbol{x}_{\mathrm{c}}(k+1)$$

The definition of the model matrices $\boldsymbol{A}_{\mathrm{c}}, \boldsymbol{B}_{\mathrm{c}}$ and $\boldsymbol{C}_{\mathrm{c}}$ may be derived from the above equations and by applying Kirchhoff's laws to the topology of the converter 10.

Control method

Fig. 3 shows a flow diagram for a method for controlling the converter 10.

In the optional step 110, it is determined whether one converter module 12 has to be bypassed, for example in the case of a fault. In this case, the first and the second model are adapted to the changed converter topology. Furthermore, in the future only switching sequences may be selected that do not rely on the converter module that has been bypassed. In step 102, at time step k, possible future switching sequences of the converter are enumerated based on an actual converter switching state $\boldsymbol{u}(k-1)$. For example, the future switching sequences comprise the admissible switching states $\boldsymbol{u}(k)$, the converter 10 may be switched to at time-step k. In general, a switching sequence may comprise one or more future switching states $\boldsymbol{u}(k), \boldsymbol{u}(k+1)$ ... .

In step 104, a future current trajectory is predicted for each switching sequence based on actual internal currents and on actual internal voltages. For example, the current trajectories are determined with a "SE" scheme, i.e. in a first step, the future current is predicted for the time step k+1 based on the first model and, in a second step, the future current is extrapolated to later time steps.

It has to be noted that other switching schemes may be used, for example "SSE", "SESE", "SSESE" or "SESESE".

The above referred internal currents are the internal currents of the converter 10 such as e.g. DC link current i_{dc}, circulating currents $i_{cir,p}$ and/or arm currents i_{pP}, i_{pN}. The above referred internal voltages are the internal voltages of the converter 10 such as e.g. the DC link voltage V_{dc} of the DC voltage supply 20, the phase voltages V_a, V_b, V_c at its connection points A, B, C and/or module voltage or capacitor voltage $V_{c,pq}$ of each converter module 12.

Fig. 4 shows current trajectories for load current i_a of phase a (top) and for load current i_b of phase b (bottom). As an example, for phases a and b, only three out of j_{max}=216 predicted load current trajectories are shown in Fig. 4.

Given the arm currents i_{pP}, i_{pN} and the capacitor voltages $V_{c,pq}$ at time-step k, the load currents i_p are predicted at time-step $k+1$ using the first model for all j_{max}=216 possible switching sequences. This implements the first part, S, of the "SE" scheme.

In step 106, candidate sequences are determined from the switching sequences, wherein a candidate sequence is a switching sequence with a current trajectory that respects predefined bounds with respect to a reference current.

For example, candidate sequences $j \in J$ with $J = \{1,2,3\ldots,j_{max}\}$, based on the predicted load currents $i_p\,(k+1)$ are determined, wherein those switching sequences have been rejected for which a load current $i_p\,(k+1)$ violates bounds at $k+1$. Here, the candidate sequences are those switching sequences that yield current trajectories that are either inside of the bounds or their violation decreases with time.

As an example, in Fig. 4, the bounds are defined by an offset value δ that is one half of the allowable ripple band around the reference currents $i_{ref,p}$. Note that δ is a design parameter that adjusts the current distortions.

The TDD of the load current can be controlled by adjusting the ripple δ. There is a linear relationship between the Total Demand Distortion (TDD) and the δ band, where the TDD is a measure of the load current harmonic distortion.

The load current ripple $i_{r,p}(k+1)$ for a current trajectory may be determined for each phase by subtracting the predicted load current $i_p(k+1)$ from the sinusoidal reference $i_{ref,p}$ for all switching sequences, $i_{r,p}(k+1) = i_p(k+1) - i_{ref,p}$, where $i_{ref,p}$ is the future load current reference.

In the example of Fig. 4, the switching sequence 30a is not a candidate sequence because the respective load current trajectory violates the upper bound, for both phase a and b, at time-step $k+1$. For the second sequence 30b, the current i_p at $k+1$ will remain outside of its bound for phase a, but its violation decreases from k to $k+1$, making it a candidate sequence. When selecting the third switching sequence 30c, the predicted load current i_p at $k+1$ is predicted to be within the hysteresis bounds, making it a candidate sequence.

In step 108, the current for a switching sequence is extrapolated over at least one time step until it violates the bounds for the respective current.

For example, the candidate trajectories are linearly extrapolated from time-step $k+1$ onwards until they violate the predefined bounds. This may implement the second part, E, of the "SE" scheme. This extrapolated length, N_j, may be represented in multiples of the sampling period T_s. For example for the switching sequence 30b at time-step $k+1$, the load current trajectories can be kept within the bounds for a length of $N_2 = min(N_{a2}, N_{b2}, N_{c2})$, before requiring a new switching event at time-step $k+N_2$.

In step 110, future module voltages for each candidate sequence are predicted based on actual module voltages, the predicted current trajectory of the respective candidate sequence and the candidate (switching) sequence. For example, the capacitor voltages $V_{c,pq}$ are predicted using the second state-space model, for all the predetermined candidate sequences. The capacitor voltages $V_{c,pq}$ are then extrapolated for the number of time steps determined in step 108. The capacitor voltages $V_{c,pq}$ at time-step $k+N_j, j \in J$ may be denoted as terminal capacitor voltages, $V_{c,pq}\ (k+N_j)$.

It has to be noted, that step 110 may be included in step 102, 104, 106 or 108.

Optionally, candidate sequences may be deselected for which future module voltages do not stay within predefined bounds. Analogously to the currents, bounds may be defined for the module voltages (for example the capacitor voltages $V_{c,pq}$), and the candidate sequences may be constrained to switching sequences with module voltages within these bounds.

In step 110, a cost function is evaluated for each candidate sequence. Possible embodiments of cost functions will be given below. In such a way, every candidate sequence is associated with a cost value calculated with the cost function.

In step 112, the next converter switching state is selected as the first converter switching state of a candidate sequence with minimal costs. The switching sequence with minimum

cost, i.e. with a minimal cost value, is selected and its first switching state implemented at time-step k.

A receding horizon policy may be implemented by repeating the steps 100 to 112 at the next sampling instant. For example, sampling period T_s, i.e. the time between two steps may be 25 µs.

Controller

Fig. 5 shows a system 38 with a controller 40 that is adapted to execute the method of Fig. 3.

The controller 40 receives the state vector of the first model $x_i(k)$ and the state vector of the second internal model $x_c(k)$ via two A/D transformers 42, 44 that receive the corresponding measurement values $x_i(t)$ and $x_c(t)$ from the converter 10. Furthermore, the offset value δ and the reference currents $i_{ref,p}$ are external parameters for the controller 40.

From these inputs, the controller 40 generates the next switching state u(k) that is directly applied to the switches of the converter 10.

The state vectors $x_i(k)$ and $x_c(k)$ are inputs to an arm current prediction module 46 that predicts the state vector $x_i(k+1)$ (including the arm currents i_{pP}, i_{pN}) for the next time step k+1.

The state vectors $x_i(k)$ and $x_c(k)$ are inputs to a voltage prediction module 48 that predicts the state vector $x_c(k+1)$ (i.e. the capacitor voltages $V_{c,pq}$) for the next time step k+1.

From the state vectors $x_i(k+1)$, the circulating currents $i_{cir,p}(k+1)$ are predicted by a circulating current module 50 and the load current ripples $i_{r,p}(k+1)$ by a current ripple module 52.

A candidate, extrapolation and cost function evaluation module 54 receives the state vector $x_c(k+1)$, the circulating currents $i_{cir,p}(k+1)$ and the load current ripples $i_{r,p}(k+1)$ and determines a set of costs c_j with the aid of the offset value δ and the reference currents $i_{ref,p}$.

The modules 46, 48, 50, 52, 54 additionally receive a set of possible future switching states u(k) that are used for determining the respective outputs of the modules.

The set of possible future switching states u(k) is determined by an enumeration module 56 from the previous switching state u(k - 1), which may be stored in an intermediate storage for one time step.

A minimum cost and switch selection modules receives the set of costs c_j, selects the candidate sequence with the minimal cost and generates the next switching state u(k) to be applied to the converter 10.

Cost functions

As a first example, given the last switching state $\boldsymbol{u}(k-1)$, the following cost function may be evaluated for all candidate sequences

$$C_j = \lambda_1 \frac{\left\|\boldsymbol{u}_j(k) - \boldsymbol{u}(k-1)\right\|}{N_j} + \lambda_2 \left\|\boldsymbol{V}_{cDiff}(k+N_j)\right\|_2^2 + \lambda_3 \left\|\boldsymbol{V}_{cNom}(k+N_j)\right\|_2^2, j \in J$$

where,

$$V_{cDiff}(k) = \begin{bmatrix} V_{c,a1}(k) - V_{c,a2}(k) \\ V_{c,a3}(k) - V_{c,a4}(k) \\ V_{c,b1}(k) - V_{c,b2}(k) \\ V_{c,b3}(k) - V_{c,b4}(k) \\ V_{c,c1}(k) - V_{c,c2}(k) \\ V_{c,c3}(k) - V_{c,c4}(k) \end{bmatrix}$$

$$V_{cNom}(k) = \begin{bmatrix} V_{c,a1}(k) - \frac{V_{ED}}{2} \\ V_{c,a2}(k) - \frac{V_{ED}}{2} \\ V_{c,a3}(k) - \frac{V_{ED}}{2} \\ V_{c,a4}(k) - \frac{V_{ED}}{2} \\ V_{c,b1}(k) - \frac{V_{ED}}{2} \\ V_{c,b2}(k) - \frac{V_{ED}}{2} \\ V_{c,b3}(k) - \frac{V_{ED}}{2} \\ V_{c,b4}(k) - \frac{V_{ED}}{2} \\ V_{c,c1}(k) - \frac{V_{ED}}{2} \\ V_{c,c2}(k) - \frac{V_{ED}}{2} \\ V_{c,c3}(k) - \frac{V_{ED}}{2} \\ V_{c,c4}(k) - \frac{V_{ED}}{2} \end{bmatrix}$$

The first term in the cost function is based on a number of switching operations between two consecutive converter switching states. The first term penalizes the number of switch

transitions discounted over the prediction horizon, allowing one to minimize the switching effort. It is evaluated by dividing the number of switch transitions by the total length of the predicted switching trajectory, including the extrapolation segment.

The second term in the cost function is based on a difference between module voltages of converter modules 12 of a converter arm 14 comprising at least two converter modules 12 connected in series. The second term is used to minimize the difference in the capacitor voltages within the upper arm 14 and the lower arm 14, respectively.

The third term in the cost function is based on a difference between module voltages and a supply voltage. The third term minimizes the difference between the terminal capacitor voltages and one half of the supply voltage, $\frac{V_{ED}}{2}$. It sets a reference for the average value of the capacitor voltages and minimizes the ripple around that reference value. Here, λ_1, λ_2 and λ_3 are the weighting coefficients.

It is important to note that the cost function without the second term may lead to unsymmetrical capacitor voltage waveforms. In that case, the third term will just control the average of the capacitor voltages and the ripple of the capacitor voltages can be higher.

There are possible additions to and modifications of the cost function. The previously presented cost function may be augmented to achieve stricter control over the capacitor voltages by using the following terms:

$$C_j = \lambda_1 \frac{\|\boldsymbol{u}_j(k) - \boldsymbol{u}(k-1)\|}{N_j} + \lambda_2 \|\boldsymbol{V}_{cDiff}(k+N_j)\|_2^2 + \lambda_3 \|\boldsymbol{V}_{cAvg}(k+N_j)\|_2^2 + \lambda_4 \|\boldsymbol{V}_{cPhAvg}(k+N_j)\|_2^2, \qquad j \in J$$

where,

$$V_{cAvg}(k) = \begin{bmatrix} V_{c,a1}(k) + V_{c,a2}(k) - V_{c,a3}(k) - V_{c,a4}(k) \\ V_{c,b1}(k) + V_{c,b2}(k) - V_{c,b3}(k) - V_{c,b4}(k) \\ V_{c,c1}(k) + V_{c,c2}(k) - V_{c,c3}(k) - V_{c,c4}(k) \end{bmatrix}$$

$$V_{cPhAvg}(k) = \begin{bmatrix} V_{c,a1}(k) + V_{c,a2}(k) + V_{c,a3}(k) + V_{c,a4}(k) - V_{c,b1}(k) - V_{c,b2}(k) - V_{c,b3}(k) - V_{c,b4}(k) \\ V_{c,b1}(k) + V_{c,b2}(k) + V_{c,b3}(k) + V_{c,b4}(k) - V_{c,c1}(k) - V_{c,c2}(k) - V_{c,c3}(k) - V_{c,c4}(k) \\ V_{c,c1}(k) + V_{c,c2}(k) + V_{c,c3}(k) + V_{c,c4}(k) - V_{c,a1}(k) - V_{c,a2}(k) - V_{c,a3}(k) - V_{c,a4}(k) \end{bmatrix}$$

The first and second term in the second cost function is the same as presented in the first cost function.

The third term of the second cost function is based on a difference between the sum of module voltages of a first converter arm for a phase and the sum of module voltages of a second converter arm for the same phase. The third term of the second cost function

minimizes the difference in the terminal average value of the capacitor voltages between the top and the bottom arm.

The fourth term of the second cost function is based on a difference between the sum of module voltages of a first phase and the sum of module voltages of a second phase. The fourth term minimizes the difference in the average value of the capacitor voltages in all the three phases.

Another possible third cost function, which balances the capacitor voltages and reduces the circulating currents, is presented below:

$$C_j = \lambda_1 \frac{\|\boldsymbol{u}_j(k) - \boldsymbol{u}(k-1)\|}{N_j} + \lambda_2 \|\boldsymbol{V}_{cDiff}(k+N_j)\|_2^2 + \lambda_3 \|\boldsymbol{i}_{cir}(k+N_j)\|_2^2, \qquad j \in J$$

$$i_{cir}(k) = \begin{bmatrix} i_{cir,a}(k) \\ i_{cir,b}(k) \\ i_{cir,c}(k) \end{bmatrix}$$

The first and second term in the third cost function is the same as presented in the first cost function.

The third term of the third cost function is based on circulating currents in the converter. It minimizes the terminal circulating currents, i.e. the linearly extrapolated circulating currents at the end of the prediction horizon.

It has to be understood that the different terms of the different cost functions may be mixed with each other to generated further embodiments of cost function.

Generalization to converters with *N* arm modules and *M* phases

When considering M2LC topologies with an arbitrary number of arm modules *N* and any number of phases *M*, the dimension of the vectors and matrices of the models is changed, but the control method in general remains the same.

Specifically, when considering *N* arm modules (instead of *N*=2) and *M*=3 phases (as previously), the following changes occur:

The modified switching state vector is $\boldsymbol{u} = [u_{a1} \dots u_{a2N}\, u_{b1} \dots u_{b2N}\, u_{c1} \dots u_{c2N}]^T \in \{0,1\}^{4N}$

The system matrices $\boldsymbol{A}_\mathrm{i}, \boldsymbol{B}_\mathrm{i1}, \boldsymbol{B}_\mathrm{i2}$ and $\boldsymbol{C}_\mathrm{i}$ of the first system are changed accordingly.

The modified vector of the capacitor voltages is $[V_{c,a1} \dots V_{c,a2N}\, V_{c,b1} \dots V_{c,b2N}\, V_{c,c1} \dots V_{c,c2N}]$

The system matrices $\boldsymbol{A}_\boldsymbol{c}, \boldsymbol{B}_\boldsymbol{c}$ and $\boldsymbol{C}_\mathbf{c}$ of the second system are changed accordingly.

The total number of switching sequences to be considered for the 'SE' scheme is j_{max}, which increases, as N is increased.

When evaluating the cost function, the dimension of the vectors in the cost function, including u, V_{cdiff} and V_{cNom} is modified accordingly. The same applies to the alternative cost function formulations.

When considering arbitrary M (number of phases different from three), the control algorithm remains unchanged; only the system matrices, j_{max} and the dimension of the vectors in the cost function change. These changes are similar to the ones detailed above for arbitrary N (number of modules per arm).

Generalization to other topologies

The control method is applicable to modular converters and modular multi-level converters with an arbitrary number N of modules 12 per arm and an arbitrary number M of phases 16.

In the following different topologies for modular converters are shown, which may be controlled by embodiments of the method as described above.

These topologies may be grouped into the following groups and sub groups:

- double-star topologies:
    - DC-AC. An example for N=2 arm modules and M=3 phases is shown in Fig. 1.
    - AC-DC. It may have the same topology as the DC-AC converter shown in Fig. 1, but with the standard power flow being from AC to DC, i.e. an active rectifier.
- (single) star and (single) delta topologies, as shown in Fig. 10 and 11
- AC-AC topologies:
    - Three-phase AC to three-phase AC: see Fig. 6, where one module may be represented as shown in Fig. 7
    - Single-phase AC to single-phase AC
    - Single-phase AC to three-phase AC
    - Hexverter: see Fig. 8
- DC-DC topologies: see Figs. 9 and 12
- Dual modular multi-level converters: see Fig. 13

Embodiments of the proposed control method are applicable to all topologies. All converters shown in the following may have a controller 40, which is adapted for executing the method as described above. The control concept remains unchanged. Only the system matrices, j_{max} and the dimension of the vectors in the cost function may have to be adapted to the specific topology.

Fig. 6 shows an AC-AC modular multi-level converter 10a with nine converter arms 14. The converter 10 has a three-phase input 60 connected to a three-phase AC system 62 and a three-phase output 64 connected to a three phase AC machine or load 18.

The arms 14 are connected in such a way that each arm 14 is connected to one input phase of the three-phase input 60 and to one output phase of the three-phase output 64. The arms 14 may be grouped into groups of three arms 14 that form subconverters 66, 68 of the converter 10.

Each of the three rows of the converter 10a forms a single-phase AC to three-phase AC subconverter 66. The three arms 14 of the subconverter 66 are star-connected with the respective input phase.

Each of the three columns of the converter 10a forms a three-phase AC to single-phase AC subconverter 68. The three arms 14 of the subconverter 68 are star-connected with the respective output phase.

The converter arms 14 of the modular converter 10 shown in Fig. 1 comprise converter modules 12 with so-called unipolar cells, which comprise two switches. The module 12 is also called a chopper module.

The arms 14 of the modular converter 10a shown in Fig. 6 comprise converter modules 12a connected in series with so-called bipolar cells. The module 12a is also called a bridge module.

Such a converter module 12a with a bipolar cell with four switches is shown in Fig. 7. The converter module 12 provides only unidirectional power flow, while the converter module 12a allows for bidirectional power flow. For the DC-AC and AC-DC topologies, both types of modules 12, 12a may be used. For all the other topologies usually the bridge converter module 12a is used.

The converter module 12a shown in Fig. 7 has compared to the converter module 12 shown in Fig. 2 an extended functionality. The converter module 12a has two power connectors 21, 22, which are acting as the input as well as the output of the converter module 12a. Beside the power connectors 21, 22 the converter module might have further

connections for controlling the converter module 12a, for diagnose purposes and other control objectives. The power connectors 21, 22 can either short circuited or connected to the capacitor by the power semiconductors switches. Compared with the converter module 12 shown in Fig. 2 the converter module 12a shown in Fig. 7 allows to connect the positive pole of the capacitor to ether one of the power connectors 21, 22. The same applies to the negative pole of the capacitor.

The two power connectors 21, 22 of each converter module are referred to as the inputs. Further, the voltage of the capacitor is referred to as the module voltage or capacitor voltage.

Fig. 8 shows another topology for a direct AC-AC modular converter, a so-called hexverter 10b, which comprises six converter arms 14 with series connected converter modules 12. The converter modules 12 comprise bipolar cells.

The hexverter 10b interconnects a first three-phase system 62 with a second three-phase system 18. Each phase of the first system 62 and of the second system 18 is connected to a connection point between two arms 14, such that the phases of the first system 62 and of the second system 18 alternate, when going around the ring of converter arms 14.

Fig. 9 shows a modular DC-DC converter 10c, which comprises an active rectifier 70, which may be seen as a modular DC-AC subconverter 70, and an AC-DC subconverter 72, which are interconnected by a transformer 74. Both subconverters 70, 72 have a topology analogous to the topology of the converter 10 of Fig. 1. However, each of the subconverters 70, 72 only has two phases 16.

Fig. 10 shows a modular converter 10d connected to a multi-phase power line 76. The converter 10d has a converter arm 14 connected to each of the phases of the power line 76. At the other end, the converter arms 14 are star-connected.

Fig. 11 shows a modular converter 10e also connected to a multi-phase power line 76. However, the converter arms 14 are delta-connected with phases of the power line 76, i.e. each converter arm 14 is directly connected to two different phases.

The converter arms 14 of the modular converters 10d and 10e comprise series-connected converter modules 12a with bipolar cells.

The modular converters 10d and 10e may be used in STATCOMs.

Fig. 12 shows a modular converter 10f with a DC-DC topology. The converter 10 comprises one arm 14 with series-connected converter modules 12a. Multiple DC sources 80, for example batteries, are connected in parallel to each converter module 12a. The ends of the arm 14 are connected to a DC-source 82.

The modular converter 10d may be used for charging and discharging batteries in a battery storage unit.

Fig. 13 shows a modular converter 10g with a DC-AC dual topology. A DC source 90 is connected to one phase 16 comprising two converter arms 14. Each of the converter arms has two converter modules 12c connected in parallel. The converter modules 12c of one arm 14 share a common capacitor 92.

In the converters 10, 10a to 10f, the converter modules are connected in series so as to increase the voltage. In the modular converter 10g, the modules are connected in parallel to achieve higher current ratings.

In the above examples and embodiments, the converter modules were described having the capacitor. Instead of the capacitor also a different energy storage or energy source could be used such as a battery, an fuel cell or photovoltaic cell. Such energy sources or energy storages could also be installed in addition to the described capacitor. For such cases also the capacitor voltage $V_{c,pq}$ must be generalized to a module voltage $V_{c,pq}$.

While the invention has been illustrated and described in detail in the drawings and foregoing description, such illustration and description are to be considered illustrative or exemplary and not restrictive; the invention is not limited to the disclosed embodiments. Other variations to the disclosed embodiments can be understood and effected by those skilled in the art and practising the claimed invention, from a study of the drawings, the disclosure, and the appended claims. In the claims, the word “comprising” does not exclude other elements or steps, and the indefinite article “a” or “an” does not exclude a plurality. A single processor or controller or other unit may fulfil the functions of several items recited in the claims. The mere fact that certain measures are recited in mutually different dependent claims does not indicate that a combination of these measures cannot

be used to advantage. Any reference signs in the claims should not be construed as limiting the scope.

CLAIMS

1. A method for controlling a modular converter (10) with a plurality of converter modules (12), each converter module (12) comprises two power connectors, power semiconductors and an energy storage and/or and energy source, wherein the power connectors are short-circuited in a first switching state of the semiconductors and are connected to the energy storage and/or energy source in a second switching state of the semiconductors,

the method comprising the steps of:

selecting possible future switching sequences of the converter (10) based on an actual converter switching state, wherein a switching sequence is a series of converter switching states with at least one converter switching state and a converter switching state comprises switching states of the converter modules;

predicting a future current trajectory for each switching sequence based on actual internal currents and on actual internal voltages;

determining candidate sequences from the switching sequences, wherein a candidate sequence is a switching sequence with a current trajectory that respects predefined bounds with respect to a reference current or, when a predefined bound is violated, moves the current trajectory closer to the predefined bound;

predicting future module voltages for each candidate sequence based on actual module voltages and the current trajectory of the respective candidate sequence;

evaluating a cost function for each candidate sequence, wherein the cost function is based on the converter switching states of the switching sequence, the future module voltages and/ or future currents;

selecting the next converter switching state as a first converter switching state of a candidate sequence with minimal costs.

2. The method of claim 1,

wherein the cost function is based on a number of switching operations between two consecutive converter switching states.

3. The method of claim 1 or 2,

wherein the cost function is based on a difference between module voltages of converter modules (12) of a converter arm (14) comprising at least two converter modules connected in series.

4. The method of one of the preceding claims,

wherein the cost function is based on a difference between a module voltage and a supply voltage at an input of the converter (10).

5. The method of one of the preceding claims,

wherein the cost function is based on a difference between the sum of module voltages of a first converter arm (14) for a phase (16) and the sum of module voltages of a second converter arm (14) for the same phase (16) or a different phase (16).

6. The method of one of the preceding claims,

wherein the cost function is based on a difference between the sum of module voltages of a first phase and the sum of module voltages of a second phase.

7. The method of one of the preceding claims, further comprising the step of:

deselecting candidate sequences for which future module voltages do not stay within predefined bounds.

8. The method of one of the preceding claims,

wherein each converter module (12) comprises a module capacitor; and/or

wherein the module voltages are capacitor voltages over module capacitors.

9. The method of one of the preceding claims,

wherein a switching sequence comprises a switching step associated with a converter switching state, in which switching step the future current of the converter is predicted for switching the converter into the associated converter switching state; and /or

wherein a switching sequence comprises an extrapolation step, in which the current is extrapolated over at least one time step until it violates the bounds for the current.

10. The method of one of the preceding claims,

wherein the future current trajectory is predicted based on a first internal model of the converter and/or

wherein the future module voltages are predicted based on a second internal model of the converter, which is dependent on the first internal model.

11. The method of one of the preceding claims, further comprising the steps:

changing the converter topology by bypassing a converter module (12);

adapting the first and/or the second model to the changed converter topology.

12. A computer program, which, when being executed on a processor, is adapted for executing the steps of the method of one of the claims 1 to 11.

13. A computer-readable medium in which a computer program according to claim 12 is stored.

14. A controller (40) for controlling a modular converter (10), wherein the controller is adapted for executing the steps of the method of one of claims 1 to 11.

15. A modular converter (10), comprising:

a plurality of converter modules (12) each having a capacitor; and

a controller (40) according to claim 14.

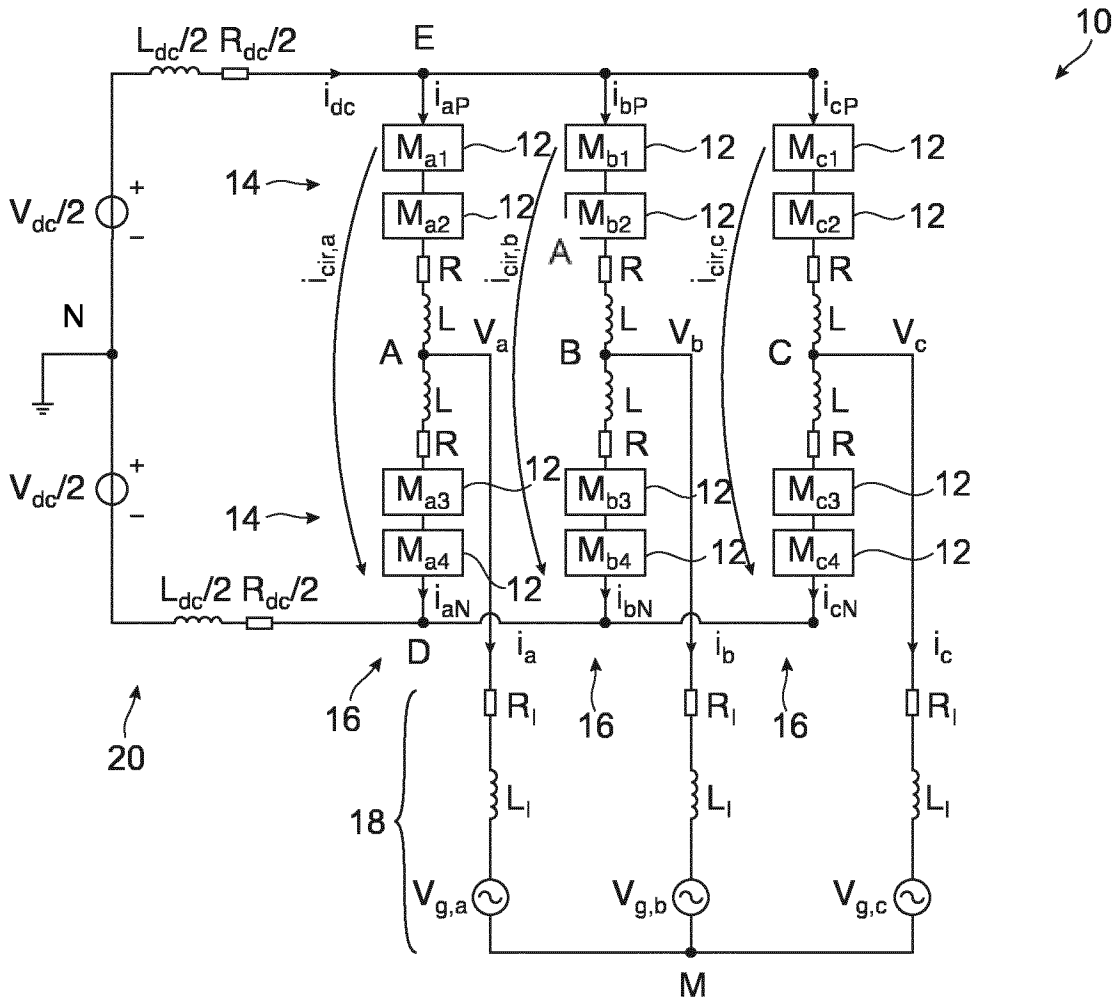

10
$L_{dc}/2$ $R_{dc}/2$
E
i_{dc}
i_{aP}
i_{bP}
i_{cP}
M_{a1}
M_{b1}
M_{c1}
M_{a2}
M_{b2}
M_{c2}
M_{a3}
M_{b3}
M_{c3}
M_{a4}
M_{b4}
M_{c4}
12
14
$V_{dc}/2$
N
R
L
A
B
C
V_a
V_b
V_c
$i_{cir,a}$
$i_{cir,b}$
$i_{cir,c}$
i_{aN}
i_{bN}
i_{cN}
D
i_a
i_b
i_c
16
R_l
L_l
18
20
$V_{g,a}$
$V_{g,b}$
$V_{g,c}$
M

Fig. 1

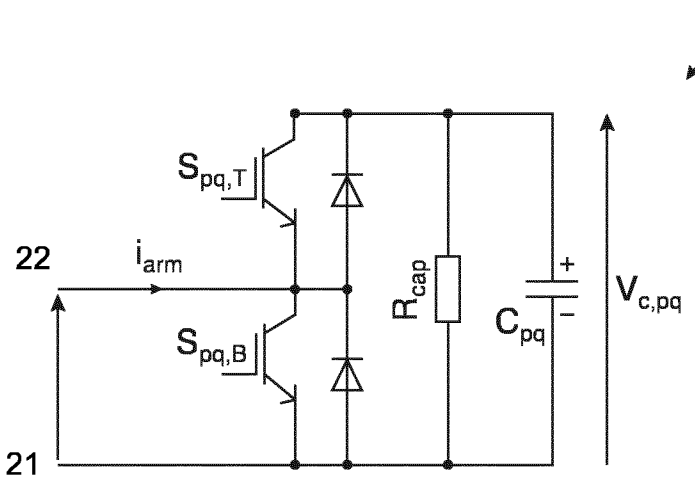

12
$S_{pq,T}$
22
i_{arm}
$S_{pq,B}$
21
R_{cap}
C_{pq}
$V_{c,pq}$

Fig. 2

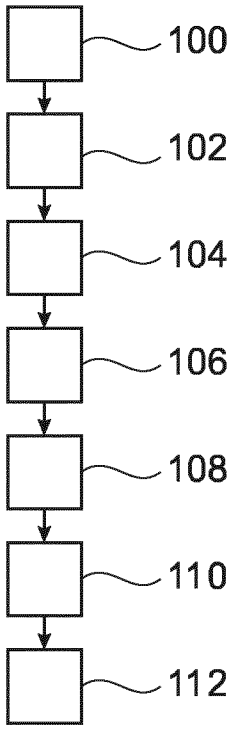

100
102
104
106
108
110
112

Fig. 3

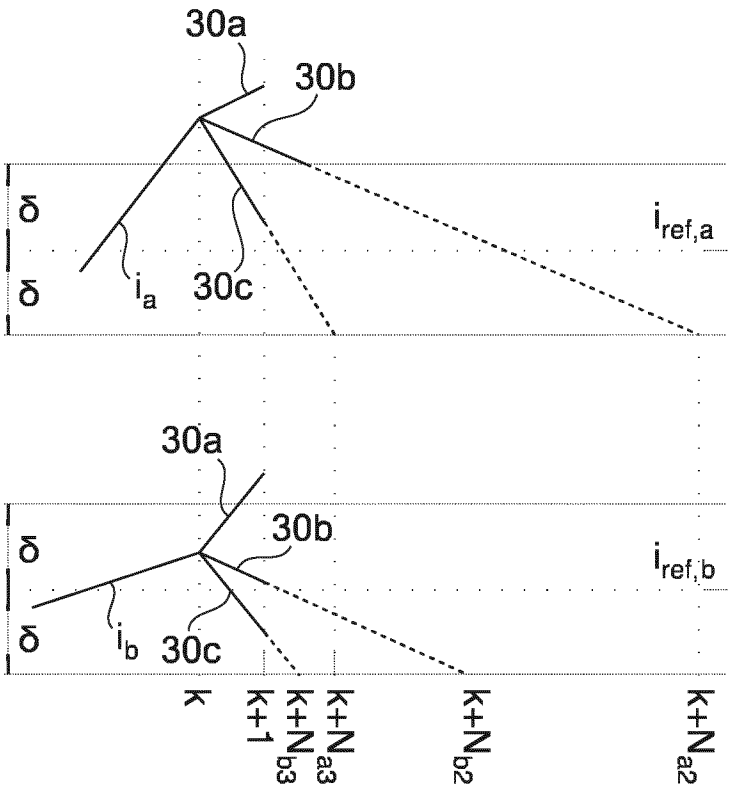

30a
30b
δ
δ
i_a
30c
$i_{ref,a}$
30a
30b
δ
δ
i_b
30c
$i_{ref,b}$
k
k+1
$k+N_{b3}$
$k+N_{a3}$
$k+N_{b2}$
$k+N_{a2}$

Fig. 4

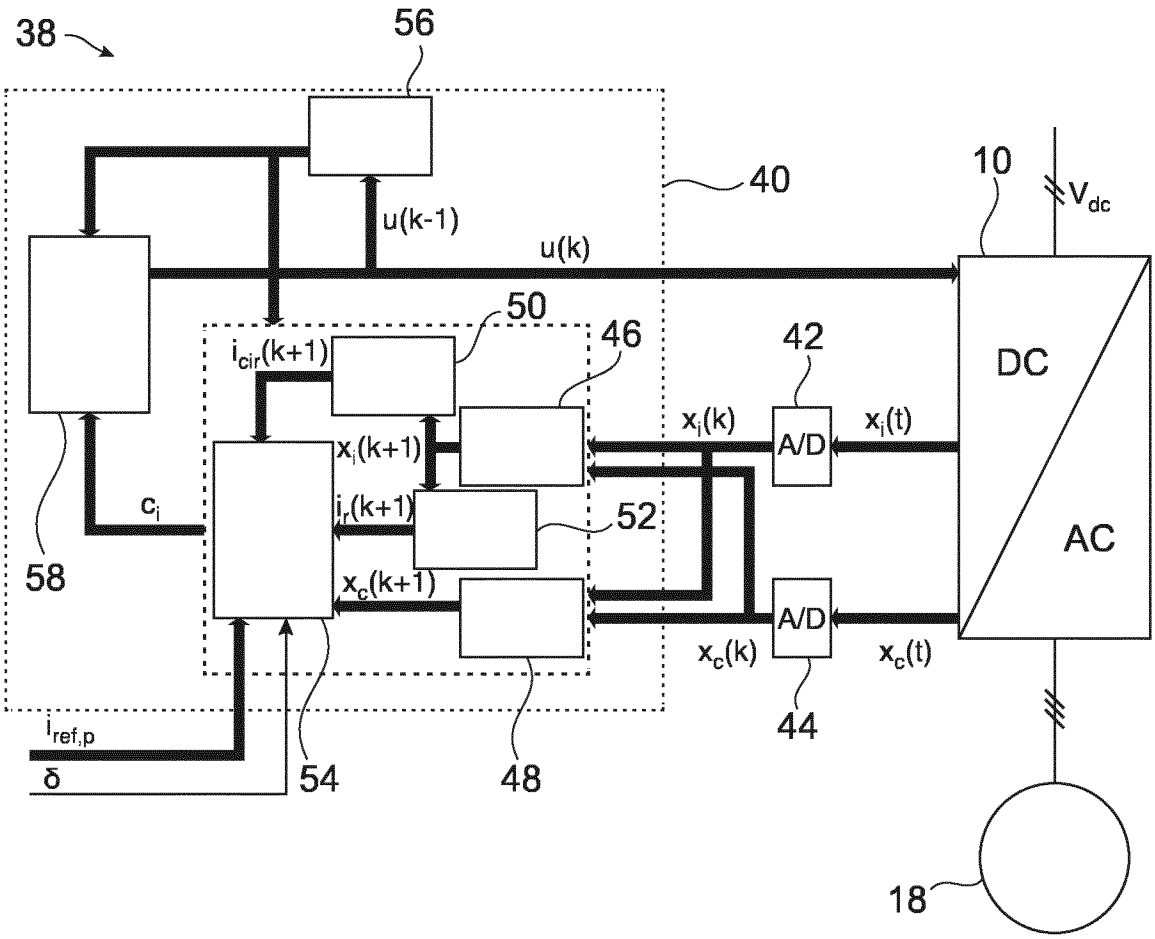

38
56
40
10
V_{dc}
u(k-1)
u(k)
50
46
42
$i_{cir}(k+1)$
$x_i(k)$
A/D
$x_i(t)$
DC
$x_i(k+1)$
c_i
$i_r(k+1)$
52
AC
58
$x_c(k+1)$
A/D
$x_c(k)$
$x_c(t)$
44
$i_{ref,p}$
δ
54
48
18

Fig. 5

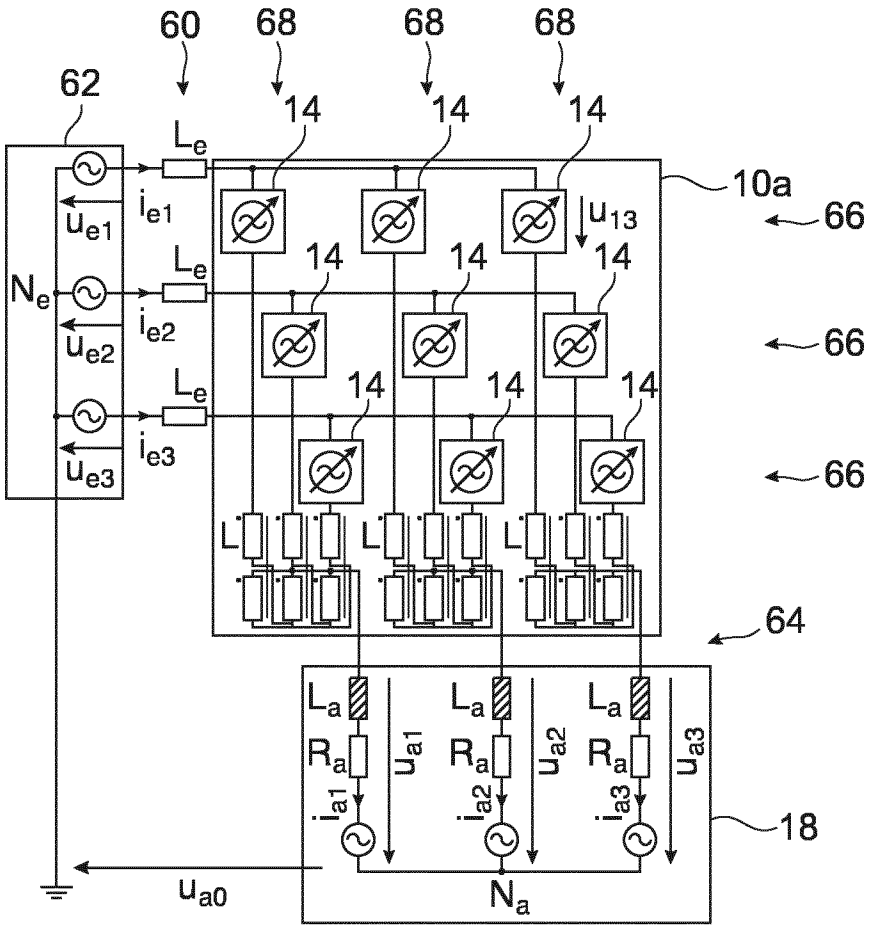

60
68
68
68
62
14
14
14
L_e
10a
66
i_{e1}
u_{e1}
u_{13}
N_e
L_e
14
14
14
66
i_{e2}
u_{e2}
L_e
14
14
14
66
i_{e3}
u_{e3}
L
L
L
64
L_a
L_a
L_a
R_a
R_a
R_a
u_{a1}
u_{a2}
u_{a3}
i_{a1}
i_{a2}
i_{a3}
18
u_{a0}
N_a

Fig. 6

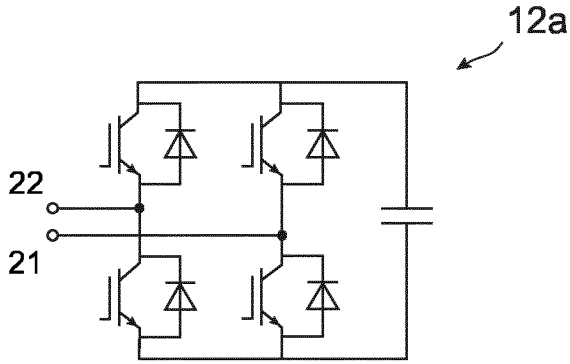

12a
22
21

Fig. 7

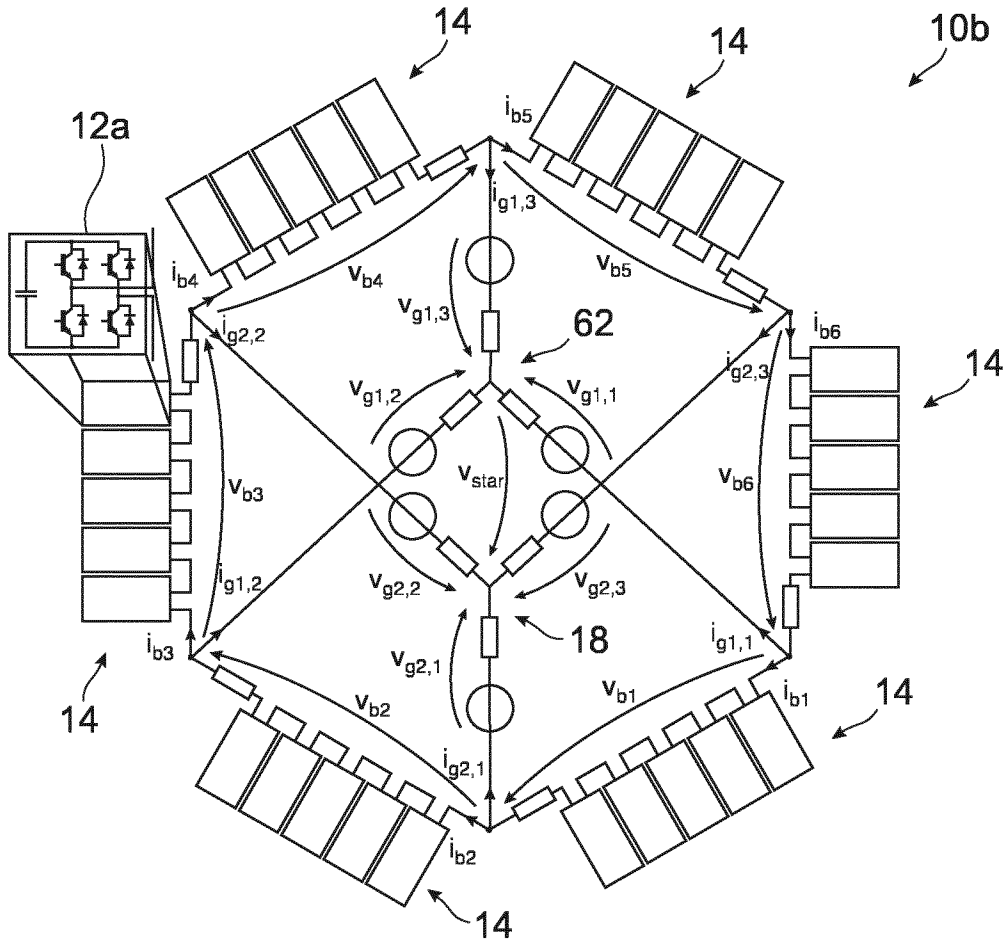
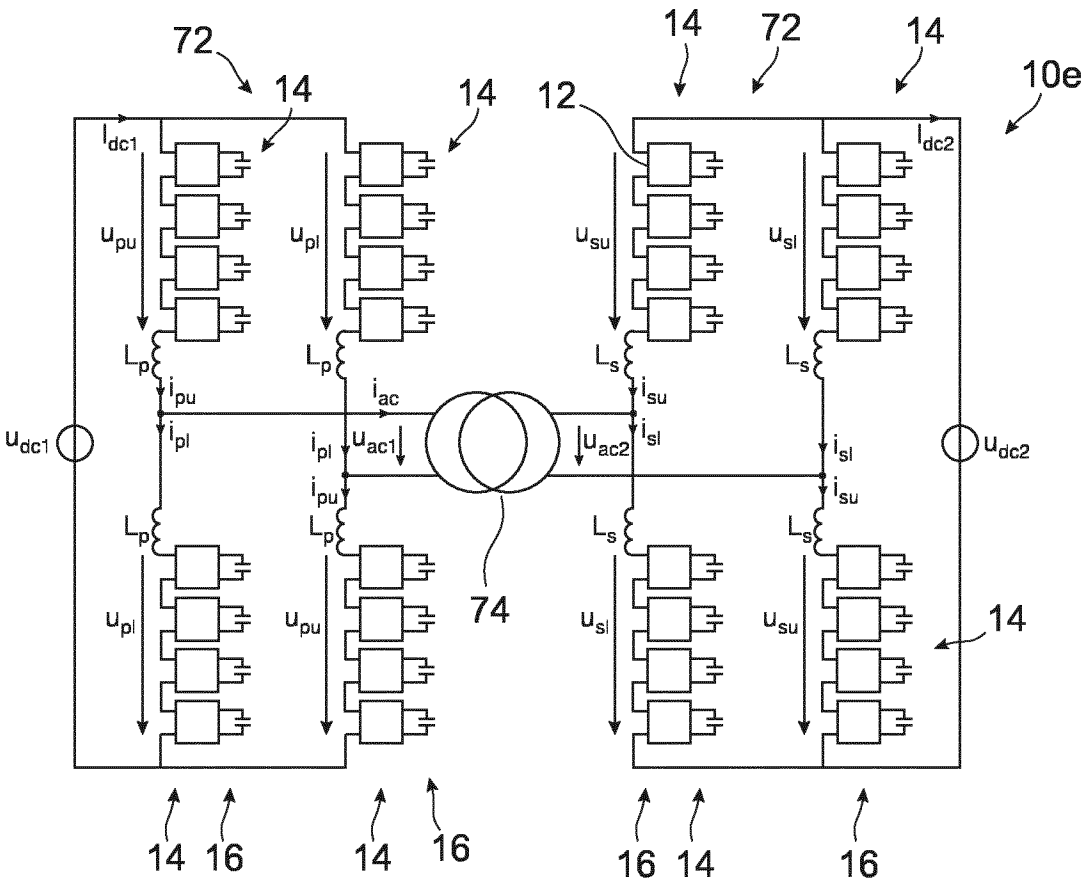

14
14
10b
12a
i_{b5}
$i_{g1,3}$
i_{b4}
v_{b4}
v_{b5}
$v_{g1,3}$
62
$i_{g2,2}$
i_{b6}
$i_{g2,3}$
14
$v_{g1,2}$
$v_{g1,1}$
v_{star}
v_{b3}
v_{b6}
$i_{g1,2}$
$v_{g2,2}$
$v_{g2,3}$
18
i_{b3}
$i_{g1,1}$
$v_{g2,1}$
v_{b1}
i_{b1}
14
14
v_{b2}
$i_{g2,1}$
i_{b2}
14

Fig. 8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14
14
12
14
72
14
10e
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I_{dc2}
u_{pu}
u_{pl}
u_{su}
u_{sl}
L_p
L_s
i_{pu}
i_{ac}
i_{su}
u_{dc1}
i_{pl}
u_{ac1}
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i_{sl}
u_{dc2}
74
14
14
16
14
16
16
14
16

Fig. 9

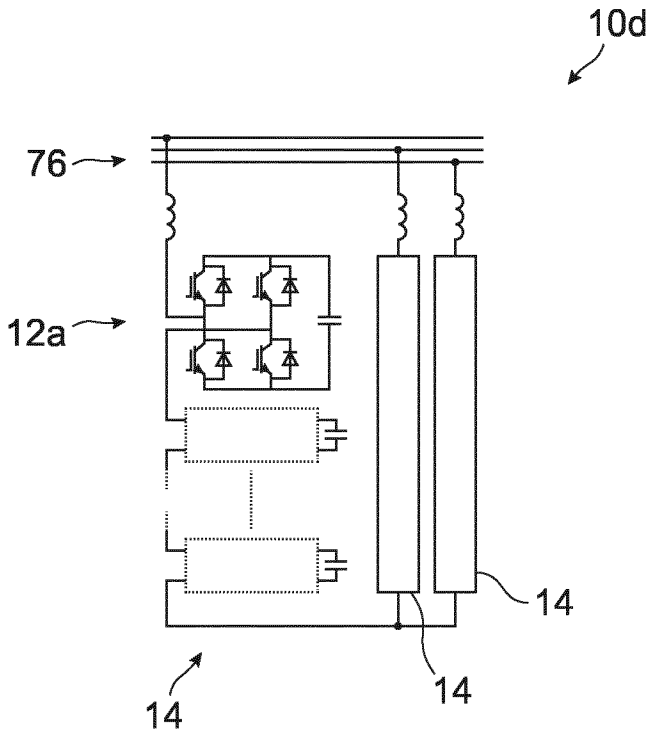


Fig. 10

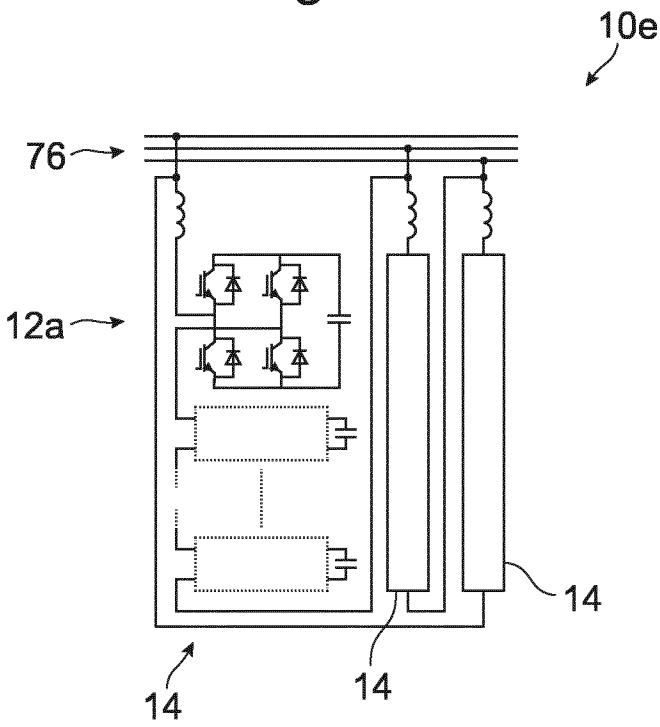
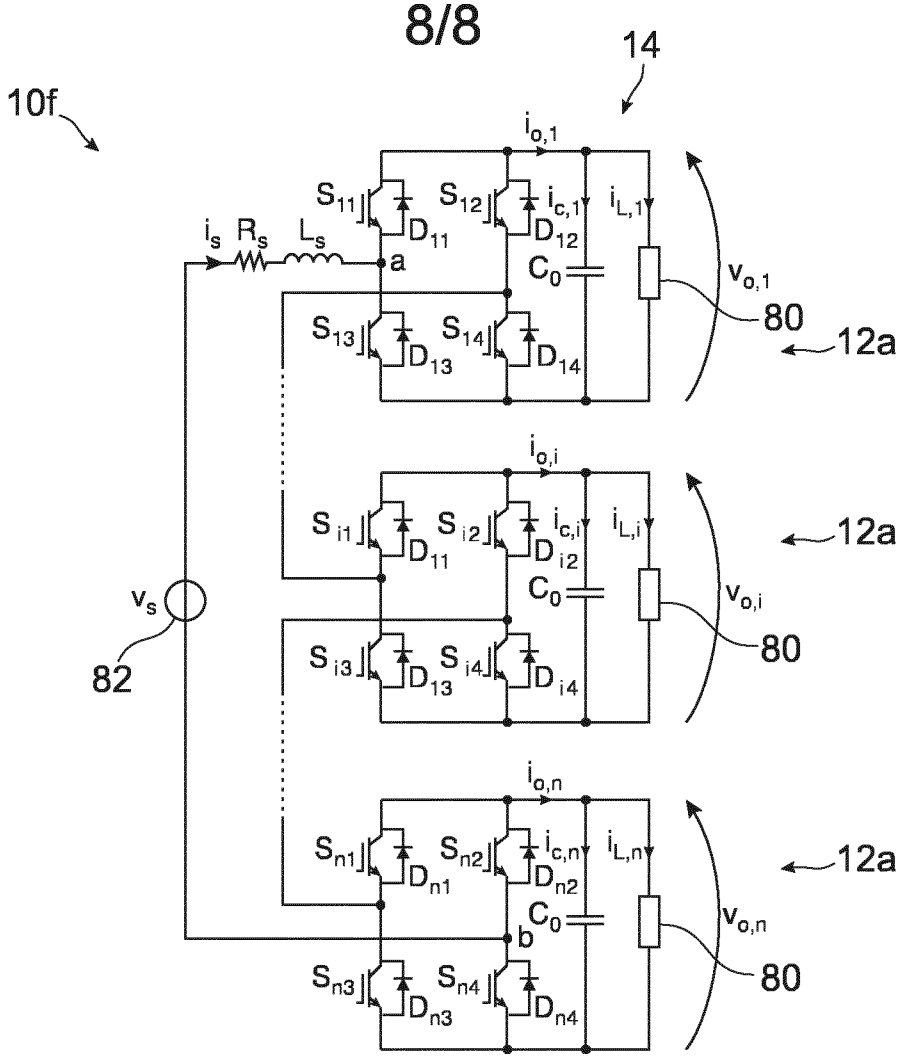


Fig. 11


10f
14
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S_{11}
S_{12}
$i_{c,1}$
$i_{L,1}$
D_{11}
D_{12}
i_s R_s L_s
a
C_0
$v_{o,1}$
80
12a
S_{13}
S_{14}
D_{13}
D_{14}
$i_{o,i}$
S_{i1}
S_{i2}
$i_{c,i}$
$i_{L,i}$
D_{11}
D_{i2}
12a
C_0
$v_{o,i}$
v_s
80
82
S_{i3}
S_{i4}
D_{13}
D_{i4}
$i_{o,n}$
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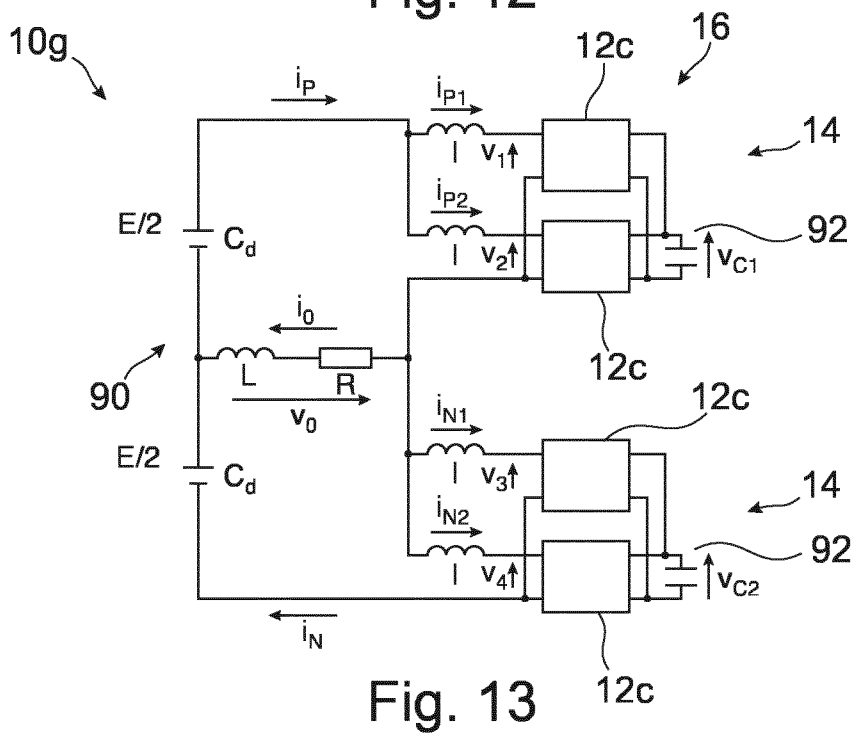
$i_{c,n}$
$i_{L,n}$
D_{n1}
D_{n2}
12a
C_0
b
$v_{o,n}$
80
S_{n3}
S_{n4}
D_{n3}
D_{n4}

Fig. 12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16
12c
i_P
i_{P1}
14
v_1
i_{P2}
E/2
C_d
92
v_2
v_{C1}
i_0
12c
90
L
R
v_0
12c
i_{N1}
E/2
C_d
v_3
14
i_{N2}
92
v_4
v_{C2}
i_N
12c

Fig. 13

INTERNATIONAL SEARCH REPORT

International application No
PCT/EP2013/064297

A. CLASSIFICATION OF SUBJECT MATTER
INV. H02M7/797 H02M7/487 H02M1/00
ADD.

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H02M

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
EPO-Internal, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US 2011/181225 A1 (GEYER TOBIAS [NZ]) 28 July 2011 (2011-07-28) the whole document -----	1-15
Y	MARCELO A PEREZ ET AL: "Predictive Control of AC AC Modular Multilevel Converters", IEEE TRANSACTIONS ON INDUSTRIAL ELECTRONICS, IEEE SERVICE CENTER, PISCATAWAY, NJ, USA, vol. 59, no. 7, 1 July 2012 (2012-07-01), pages 2832-2839, XP011417620, ISSN: 0278-0046, DOI: 10.1109/TIE.2011.2159349 the whole document ----- -/--	1-10, 12-15

[X] Further documents are listed in the continuation of Box C.

[X] See patent family annex.

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"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
5 September 2013	17/09/2013

Name and mailing address of the ISA/	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Fax: (+31-70) 340-3016	Mapp, Graham

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C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	SALVADOR CEBALLOS ET AL: "Analysis of voltage balancing limits in modular multilevel converters", IECON 2011 - 37TH ANNUAL CONFERENCE ON IEEE INDUSTRIAL ELECTRONICS SOCIETY, IEEE, 7 November 2011 (2011-11-07), pages 4397-4402, XP032105155, DOI: 10.1109/IECON.2011.6120032 ISBN: 978-1-61284-969-0 the whole document -----	11

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INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No
PCT/EP2013/064297

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		EP 2348631 A1	27-07-2011
		EP 2528225 A1	28-11-2012
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		KR 20110086520 A	28-07-2011
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		US 2011181225 A1	28-07-2011