United States Patent [19]

Norris

[11] **3,895,704**

[45] **July 22, 1975**

[54] **WORD PROCESSOR WITH RIGHT-HAND MARGIN CONTROL**

[75] Inventor: **Richard C. Norris,** Belmont, Mass.

[73] Assignee: **Arthur D. Little, Inc.,** Cambridge, Mass.

[22] Filed: **May 18, 1972**

[21] Appl. No.: **254,750**

[52] **U.S. Cl.** **197/19**

[51] **Int. Cl.** **B41j 5/30**

[58] **Field of Search** 197/19, 20, 66, 133; 199/18

[56] **References Cited**

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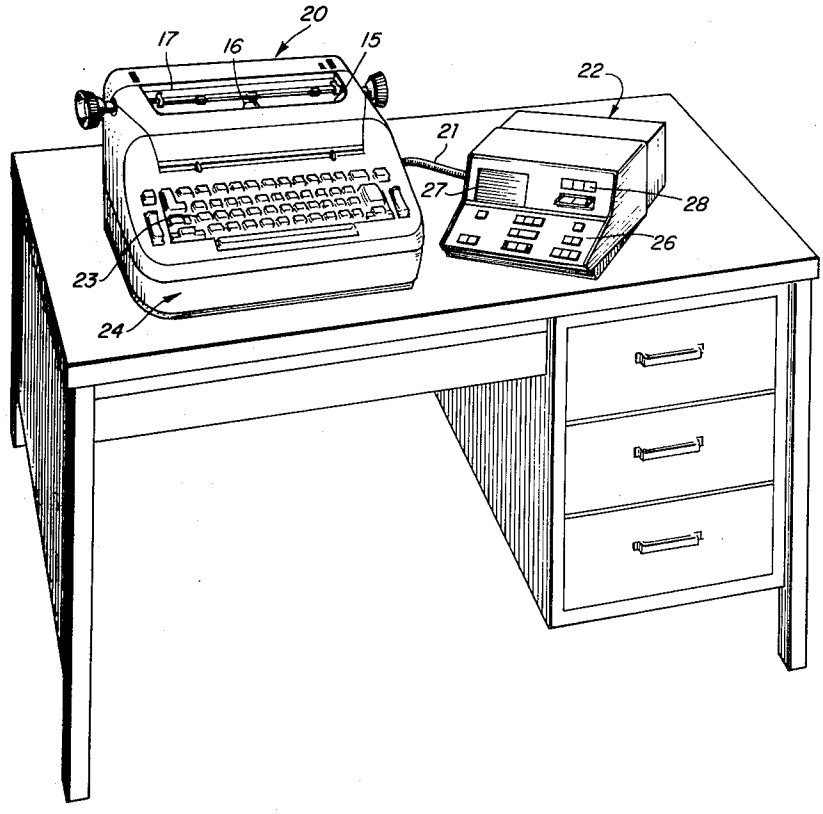
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Primary Examiner—Ernest T. Wright, Jr.
Attorney, Agent, or Firm—Schiller & Pandiscio

[57] **ABSTRACT**

The invention comprises a right hand margin control for a typewriter that serves as the input/output terminal of an electronically controlled word recording and printing system. The right hand margin adjustment means is operative only when the typewriter is printing out previously recorded data. As the typewriter reaches its so-called "return zone," the right hand margin adjust means looks ahead at data about to be printed in the return zone and determines whether or not a return opportunity (such as a space, hyphen or carriage return) is in the recorded data. If a space or hyphen is present in such data, the margin adjust means allows the typewriter to continue to operate in response to all data up to and including the data representing the return opportunity, and then causes the typewriter to return to its left margin position. If the return opportunity is a carriage return, the typewriter operates in response to all data preceding the carriage return and then executes the carriage return. If no return opportunity is present, the typewriter is caused to stop at the beginning of the return zone so as to give the operator an opportunity to intervene and determine whether to allow the typewriter to print out beyond the normal right-hand margin limit or to hyphenate a word that would otherwise extend beyond the right hand margin limit.

23 Claims, 15 Drawing Figures



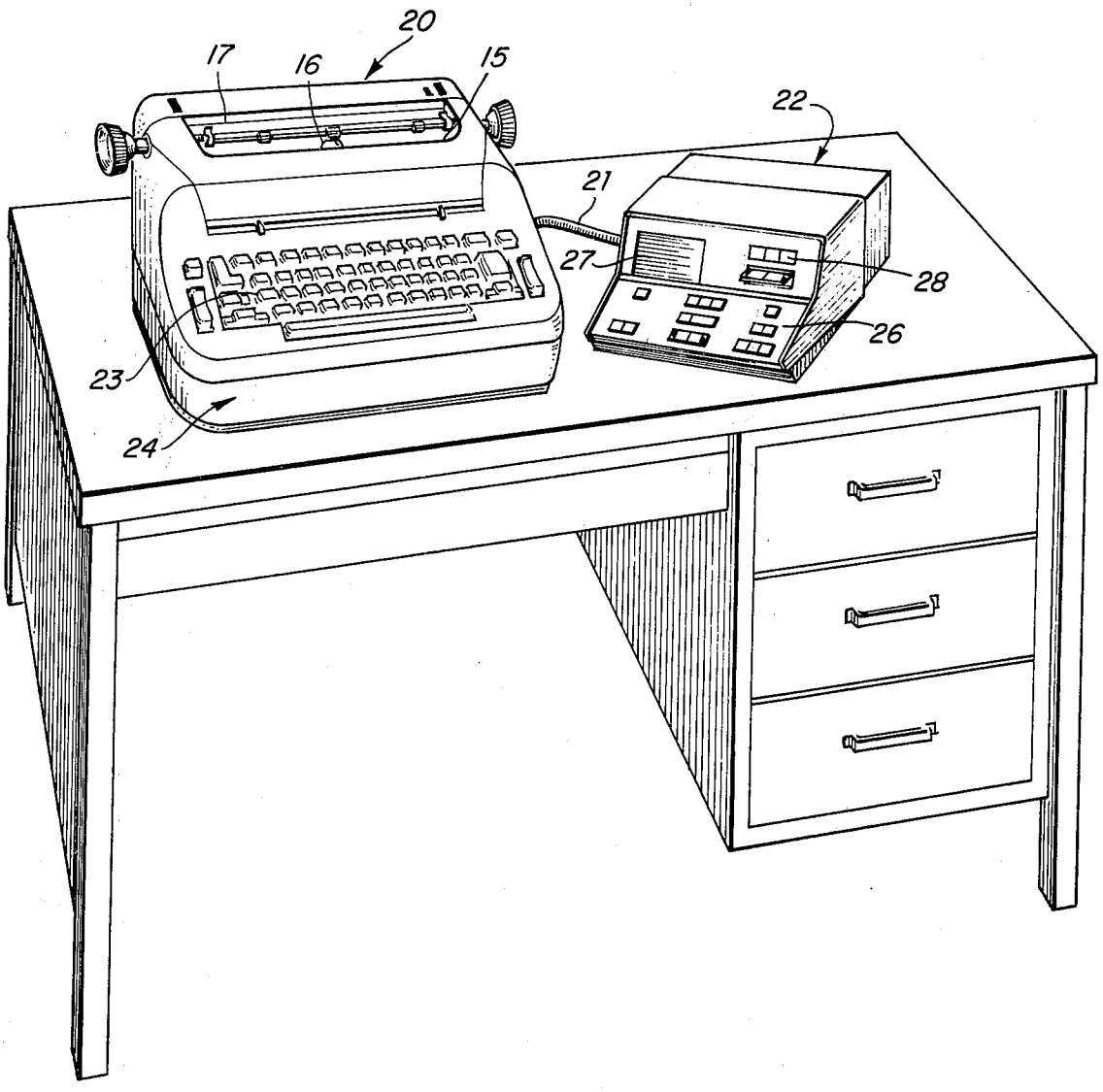


FIG. 1.

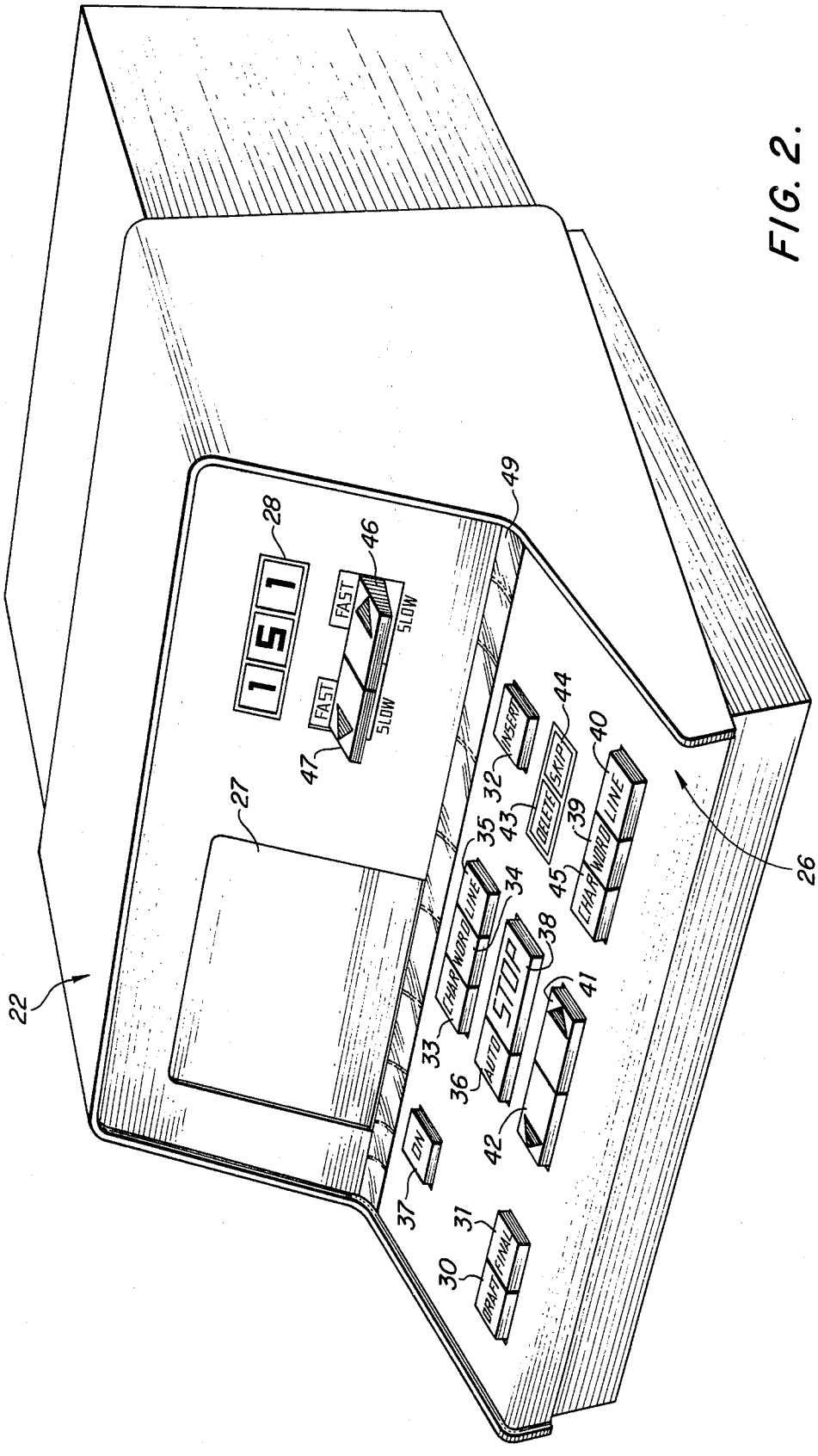

151
FAST
SLOW
FAST
SLOW
INSERT
DELETE
SKIP
CHAR
WORD
LINE
CHAR
WORD
LINE
AUTO
STOP
DN
DRAFT
FINAL
22
26
27
28
30
31
32
33
34
35
36
37
38
39
40
41
42
43
44
45
46
47
49

FIG. 2.

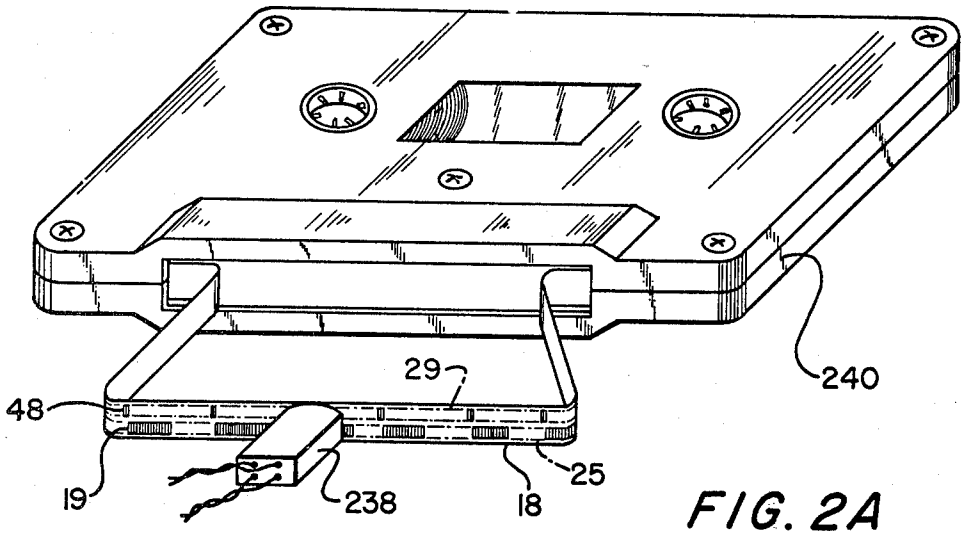


FIG. 2A

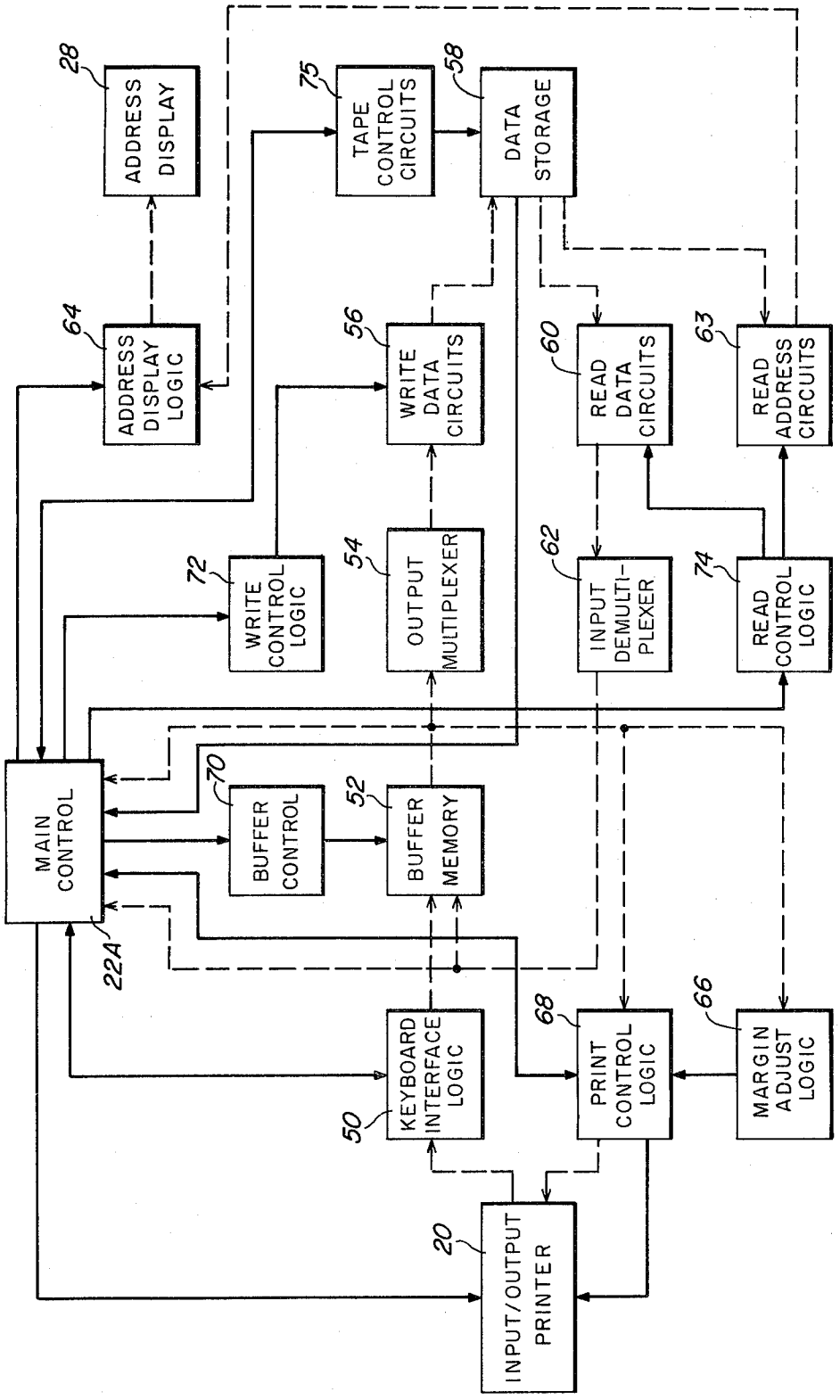

28
ADDRESS DISPLAY
75
TAPE CONTROL CIRCUITS
58
DATA STORAGE
64
ADDRESS DISPLAY LOGIC
56
WRITE DATA CIRCUITS
60
READ DATA CIRCUITS
63
READ ADDRESS CIRCUITS
72
WRITE CONTROL LOGIC
54
OUTPUT MULTIPLEXER
62
INPUT DEMULTI-PLEXER
74
READ CONTROL LOGIC
MAIN CONTROL
70
BUFFER CONTROL
52
BUFFER MEMORY
224
68
PRINT CONTROL LOGIC
66
MARGIN ADJUST LOGIC
50
KEYBOARD INTERFACE LOGIC
20
INPUT/OUTPUT PRINTER
CONTROL SIGNAL LINES
DATA SIGNAL LINES

FIG. 3.

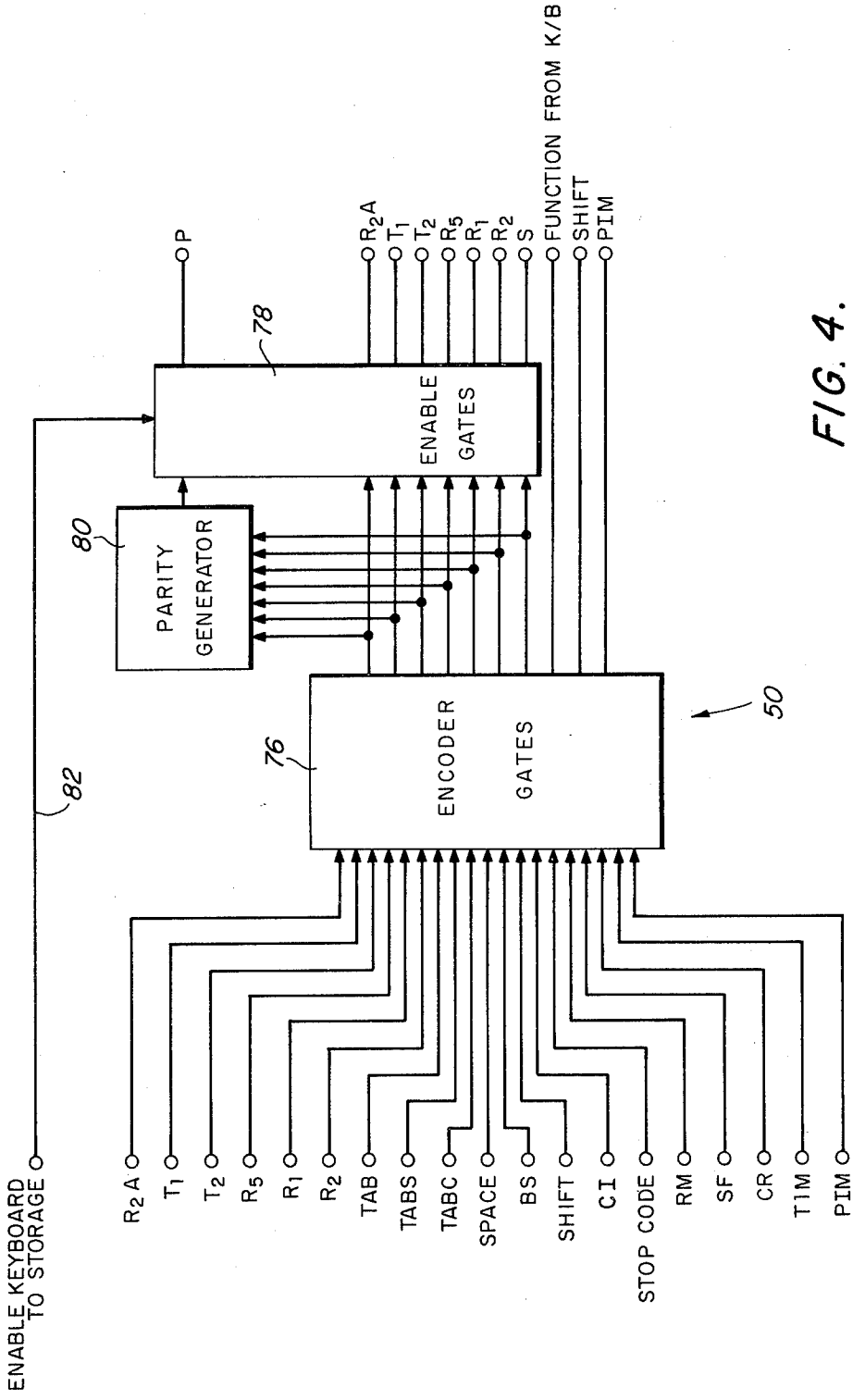

P
78
R_2A
T_1
T_2
R_5
R_1
R_2
S
FUNCTION FROM K/B
SHIFT
PIM
ENABLE GATES
80
PARITY GENERATOR
76
ENCODER GATES
50
82
ENABLE KEYBOARD TO STORAGE
R_2A
T_1
T_2
R_5
R_1
R_2
TAB
TABS
TABC
SPACE
BS
SHIFT
CI
STOP CODE
RM
SF
CR
T1M
PIM

FIG. 4.

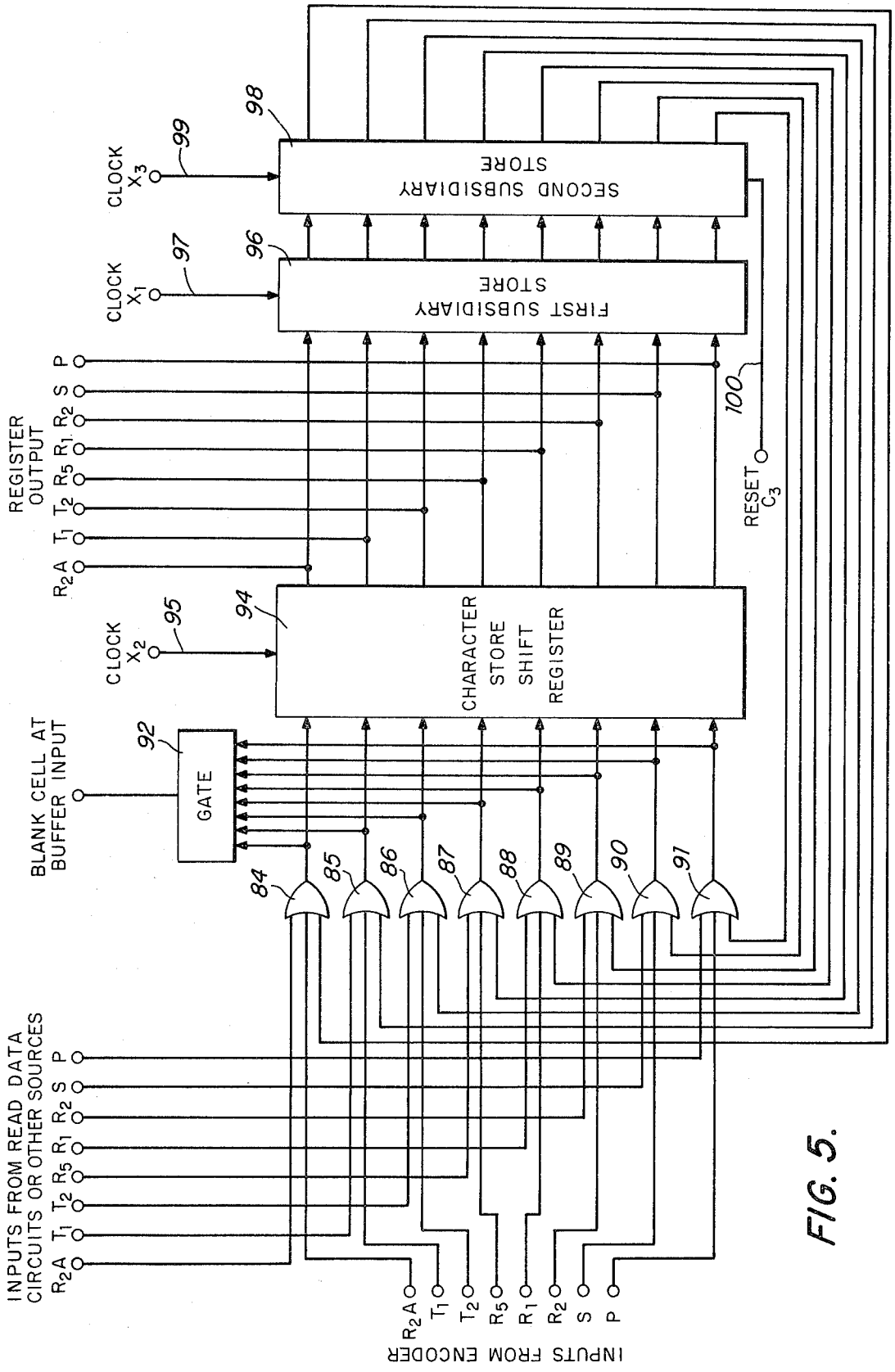

SECOND SUBSIDIARY STORE
FIRST SUBSIDIARY STORE
CHARACTER STORE SHIFT REGISTER
GATE
CLOCK X_3
CLOCK X_1
CLOCK X_2
RESET C_3
REGISTER OUTPUT
R_2A T_1 T_2 R_5 R_1 R_2 S P
BLANK CELL AT BUFFER INPUT
INPUTS FROM READ DATA CIRCUITS OR OTHER SOURCES
INPUTS FROM ENCODER
84 85 86 87 88 89 90 91
92 94 95 96 97 98 99 100

FIG. 5.

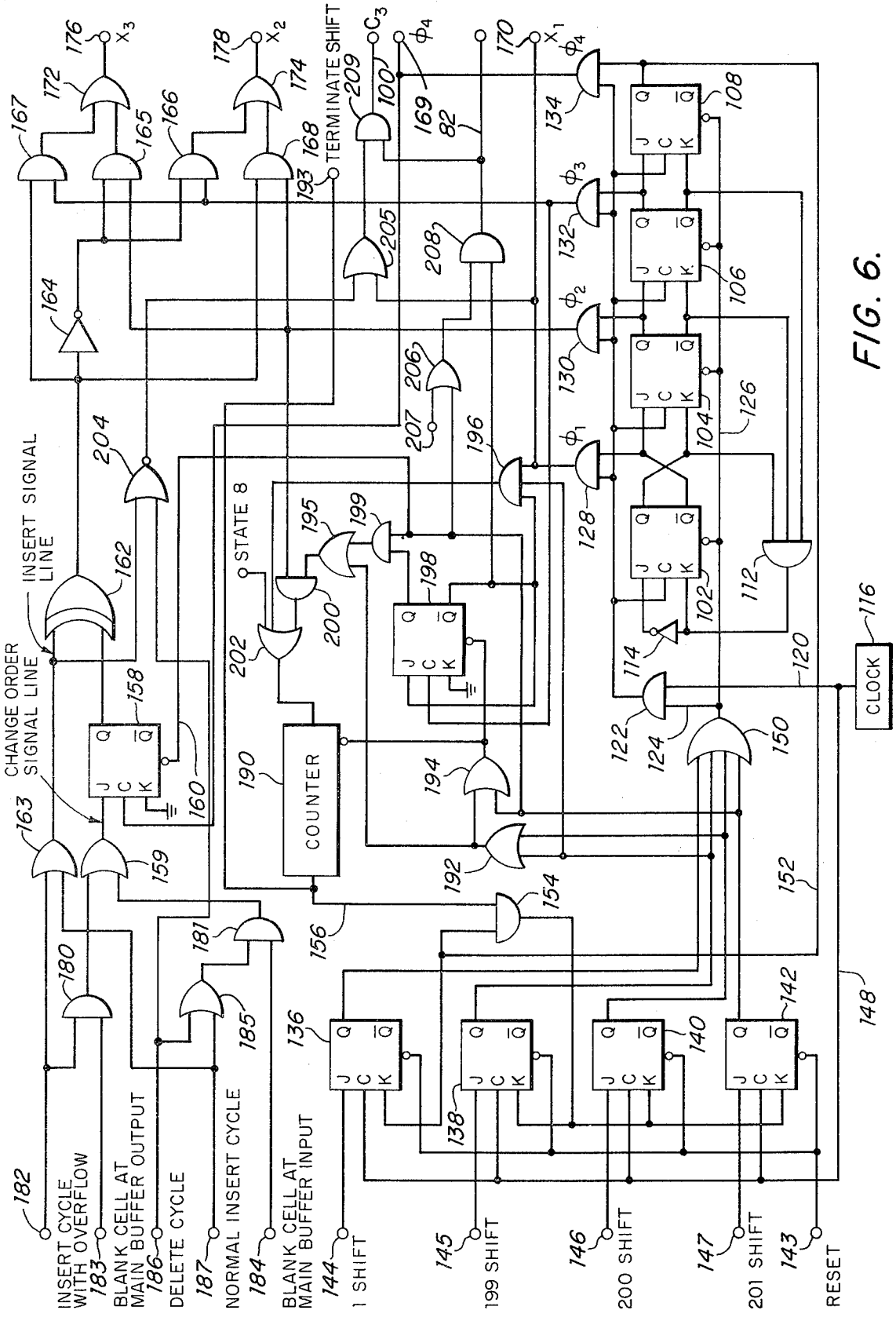

INSERT CYCLE WITH OVERFLOW
BLANK CELL AT MAIN BUFFER OUTPUT
DELETE CYCLE
NORMAL INSERT CYCLE
BLANK CELL AT MAIN BUFFER INPUT
1 SHIFT
199 SHIFT
200 SHIFT
201 SHIFT
RESET
CHANGE ORDER SIGNAL LINE
INSERT SIGNAL LINE
STATE 8
COUNTER
TERMINATE SHIFT
CLOCK

FIG. 6.

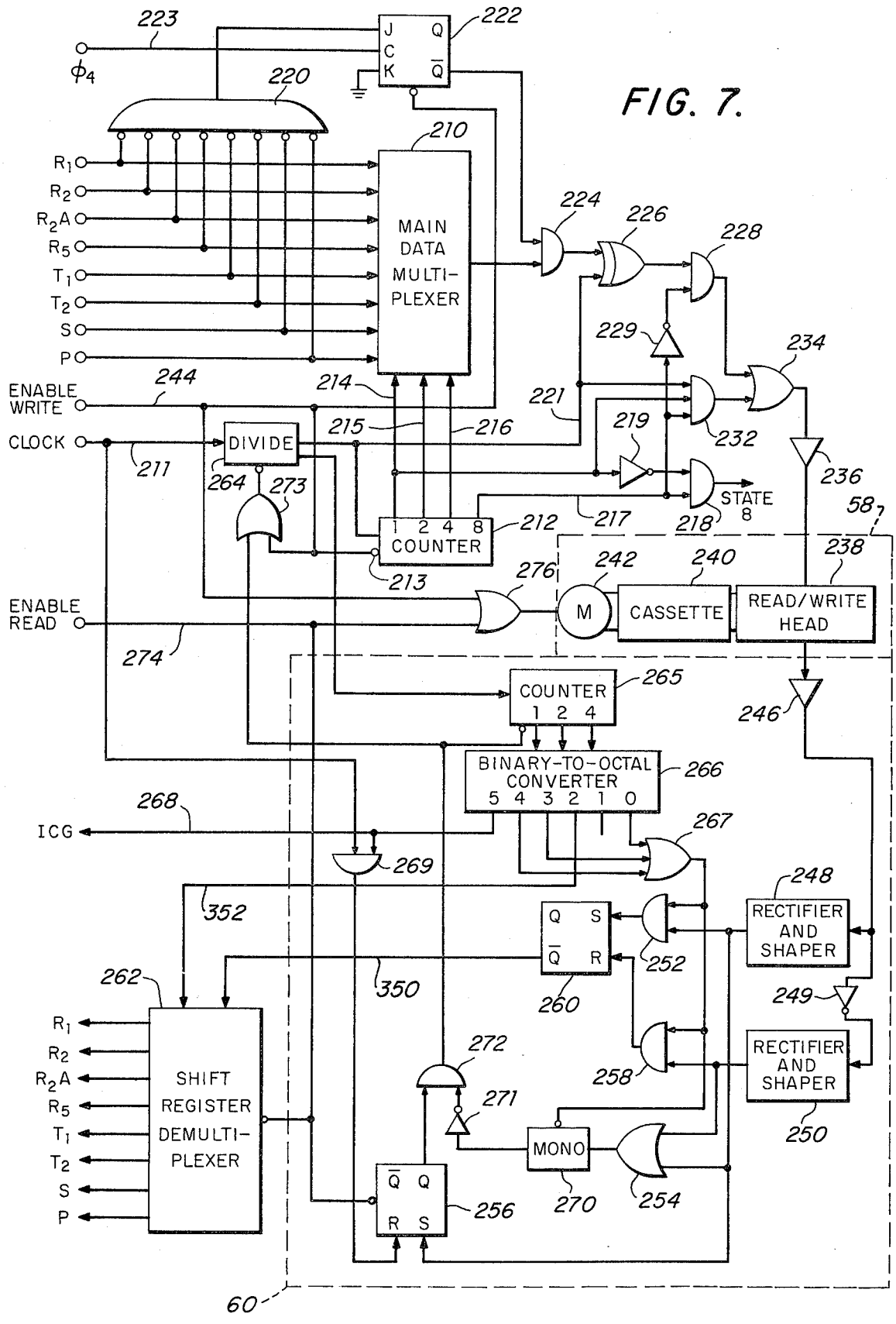

223
222
J Q
C
K Q̄
ϕ_4
220
210
R_1
R_2
R_2A
R_5
T_1
T_2
S
P
MAIN DATA MULTI-PLEXER
224
226
228
229
234
ENABLE WRITE
244
214
221
219
232
236
CLOCK
211
DIVIDE
215
216
264
273
STATE 8
218
217
1 2 4 8 COUNTER
212
213
58
238
276
242
240
ENABLE READ
274
M
CASSETTE
READ/WRITE HEAD
COUNTER 1 2 4
265
246
BINARY-TO-OCTAL CONVERTER 5 4 3 2 1 0
266
268
ICG
267
269
352
Q S
Q̄ R
248
RECTIFIER AND SHAPER
252
260
350
262
249
R_1
R_2
R_2A
R_5
T_1
T_2
S
P
SHIFT REGISTER DEMULTI-PLEXER
272
271
258
RECTIFIER AND SHAPER
250
MONO
270
254
Q̄ Q
R S
256
60

FIG. 7.

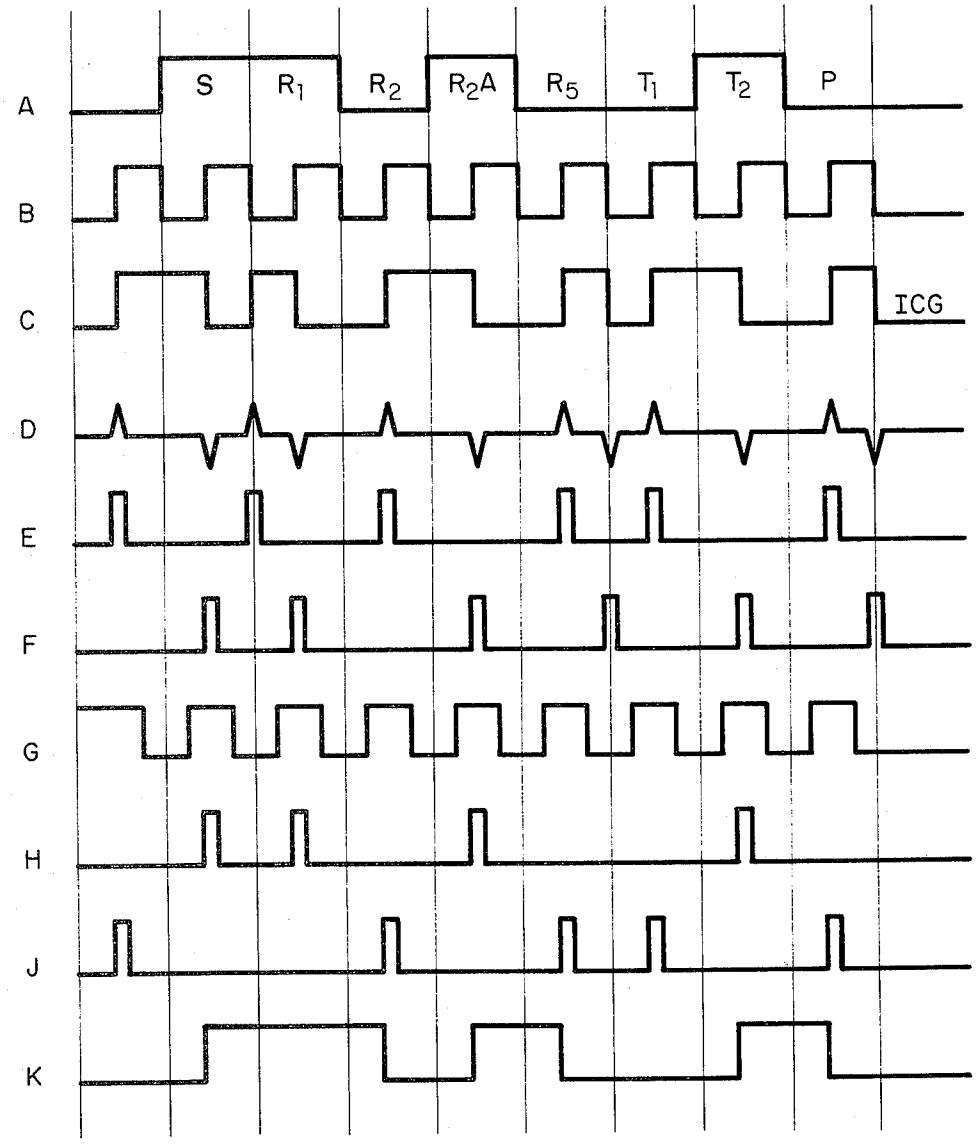


FIG. 8.

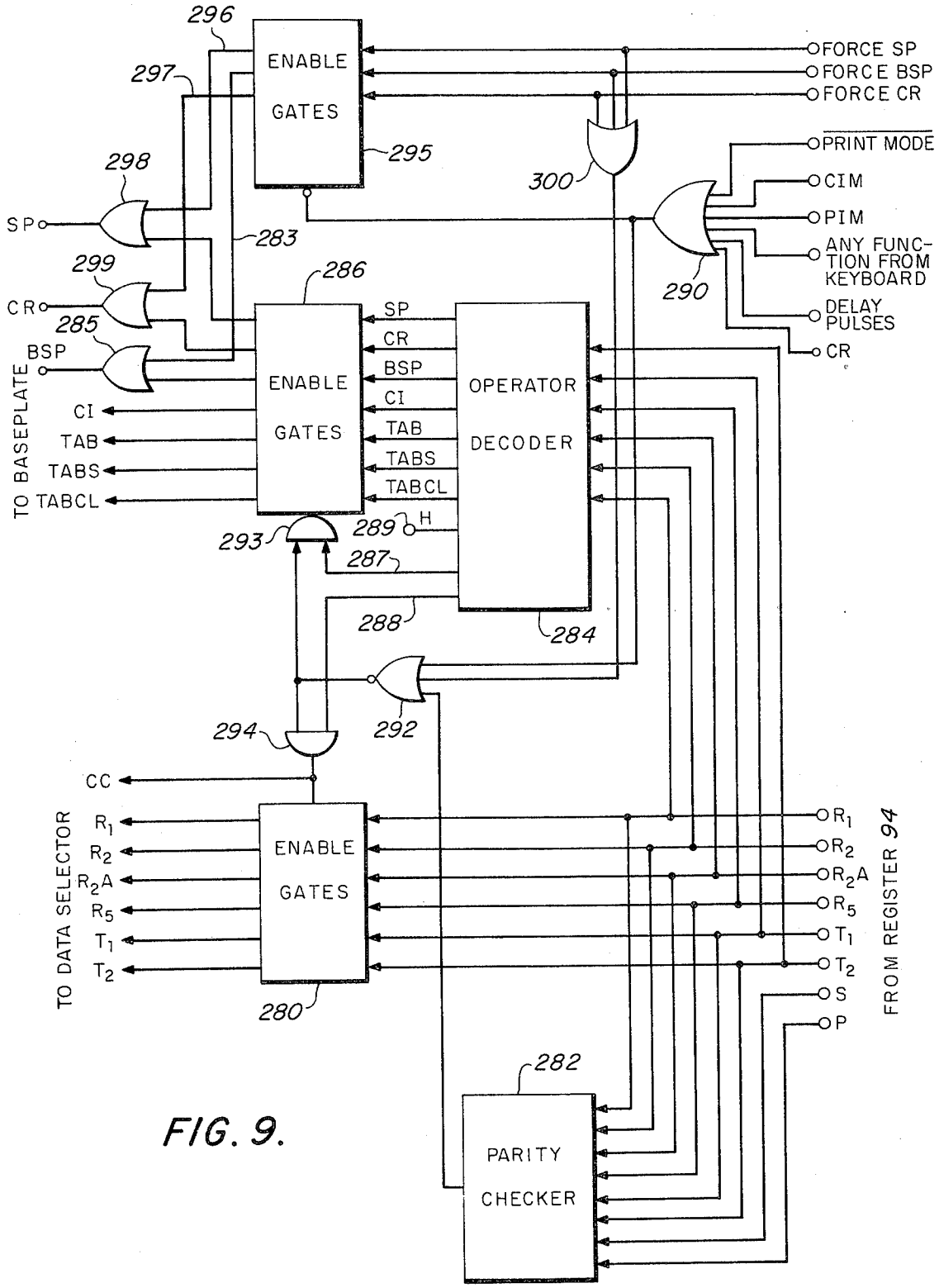

296
297
ENABLE GATES
295
FORCE SP
FORCE BSP
FORCE CR
300
PRINT MODE
CIM
PIM
ANY FUNC-TION FROM KEYBOARD
DELAY PULSES
CR
290
298
SP
283
299
CR
285
BSP
286
ENABLE GATES
SP
CR
BSP
CI
TAB
TABS
TABCL
OPERATOR DECODER
TO BASEPLATE
CI
TAB
TABS
TO TABCL
293
289
H
287
288
284
292
294
CC
TO DATA SELECTOR
R1
R2
R2A
R5
T1
T2
ENABLE GATES
280
FROM REGISTER 94
S
P
282
PARITY CHECKER

FIG. 9.

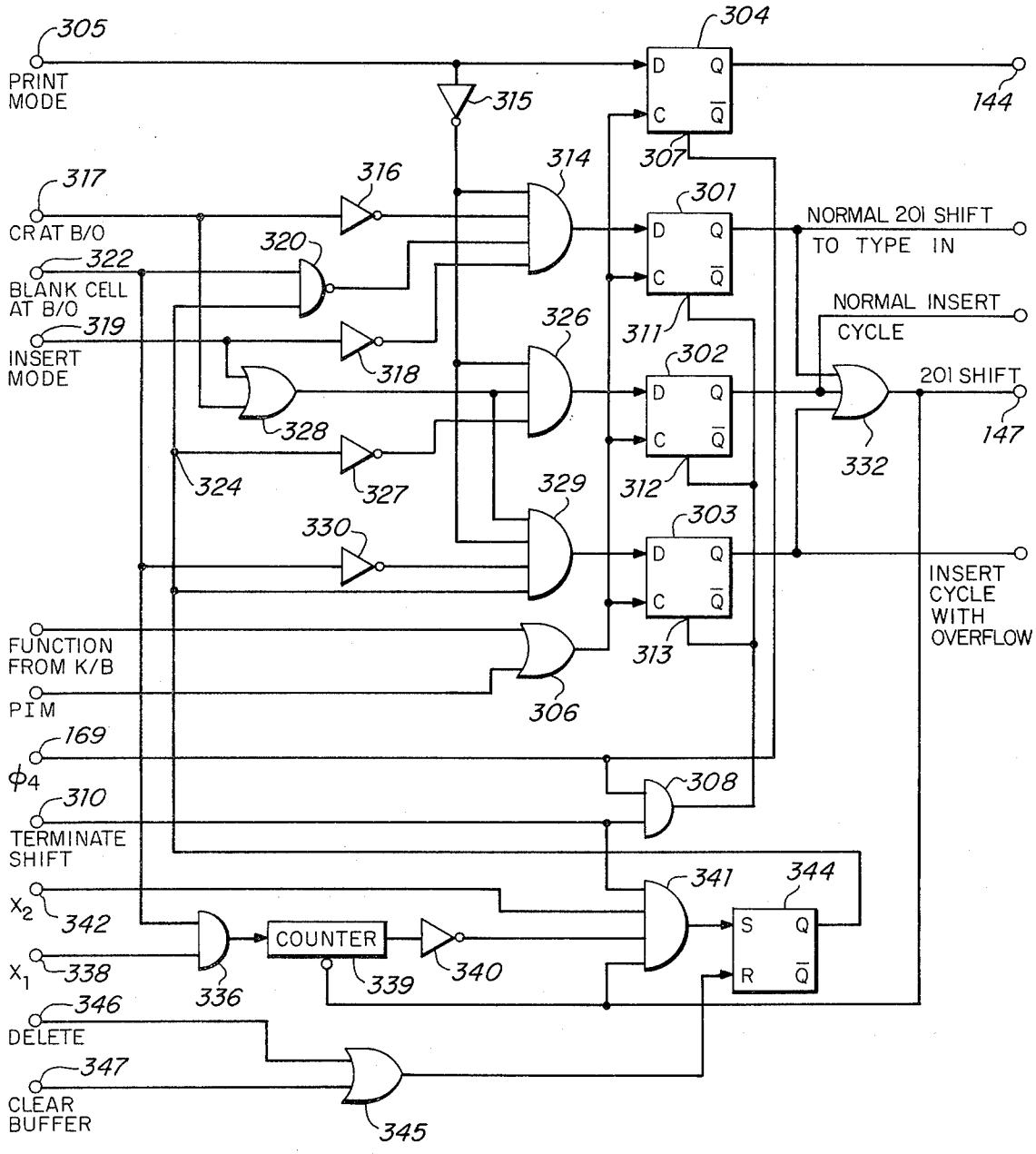

305
PRINT MODE
304
144
315
307
317
CR AT B/O
316
314
301
NORMAL 201 SHIFT TO TYPE IN
320
322
BLANK CELL AT B/O
319
INSERT MODE
326
311
NORMAL INSERT CYCLE
302
201 SHIFT
147
318
328
332
324
327
312
329
303
330
INSERT CYCLE WITH OVERFLOW
313
FUNCTION FROM K/B
306
PIM
169
ϕ_4
308
310
TERMINATE SHIFT
341
344
X_2
342
COUNTER
S
Q
R
$\bar{Q}$
X_1
338
336
339
340
346
DELETE
347
CLEAR BUFFER
345

FIG. 10.

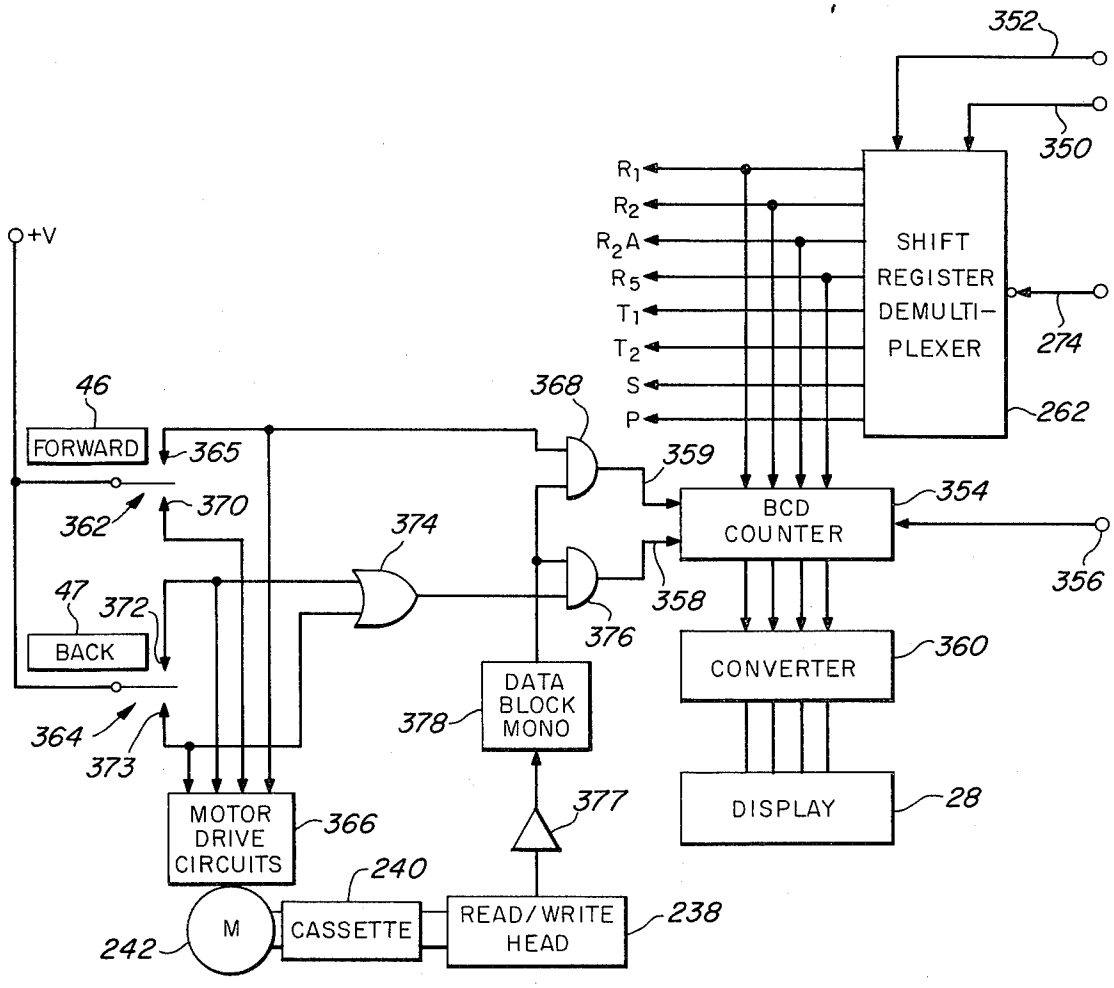

352
350
SHIFT REGISTER DEMULTI-PLEXER
274
262
R1
R2
R2A
R5
T1
T2
S
P
+V
46
FORWARD
365
362
370
368
359
354
BCD COUNTER
356
374
47
372
BACK
358
376
360
CONVERTER
364
373
DATA BLOCK MONO
378
377
DISPLAY
28
MOTOR DRIVE CIRCUITS
366
240
M
CASSETTE
READ/WRITE HEAD
238
242

FIG. 11.

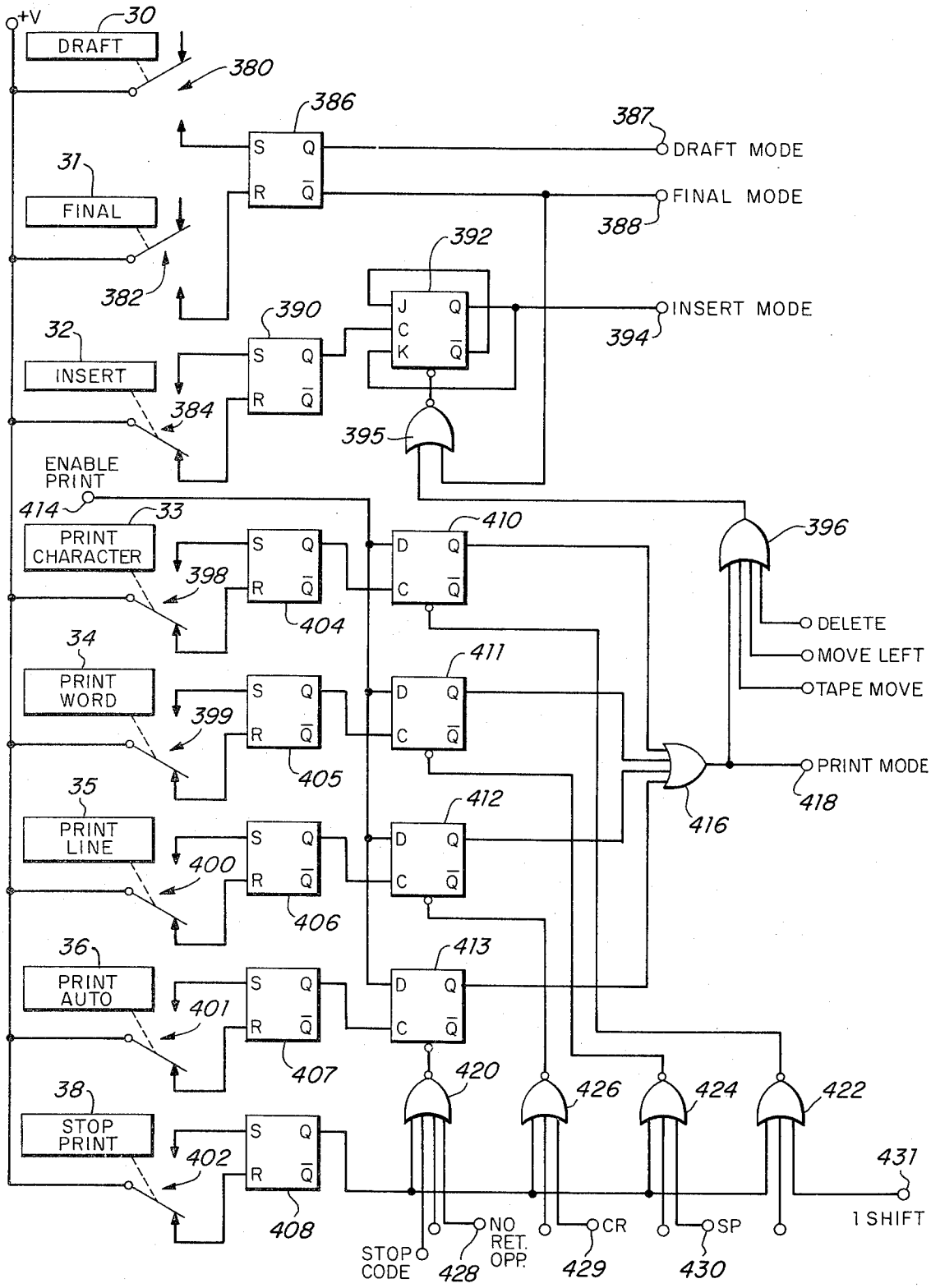

+V
30
DRAFT
380
386
387
DRAFT MODE
31
FINAL
FINAL MODE
388
382
392
390
INSERT MODE
32
INSERT
394
384
395
ENABLE PRINT
414
33
PRINT CHARACTER
410
396
398
404
DELETE
34
PRINT WORD
411
399
405
MOVE LEFT
TAPE MOVE
35
PRINT LINE
412
PRINT MODE
400
406
418
416
36
PRINT AUTO
413
401
407
420
426
424
422
38
STOP PRINT
402
408
431
1 SHIFT
NO RET. OPP.
CR
SP
STOP CODE
428
429
430

FIG. 12.

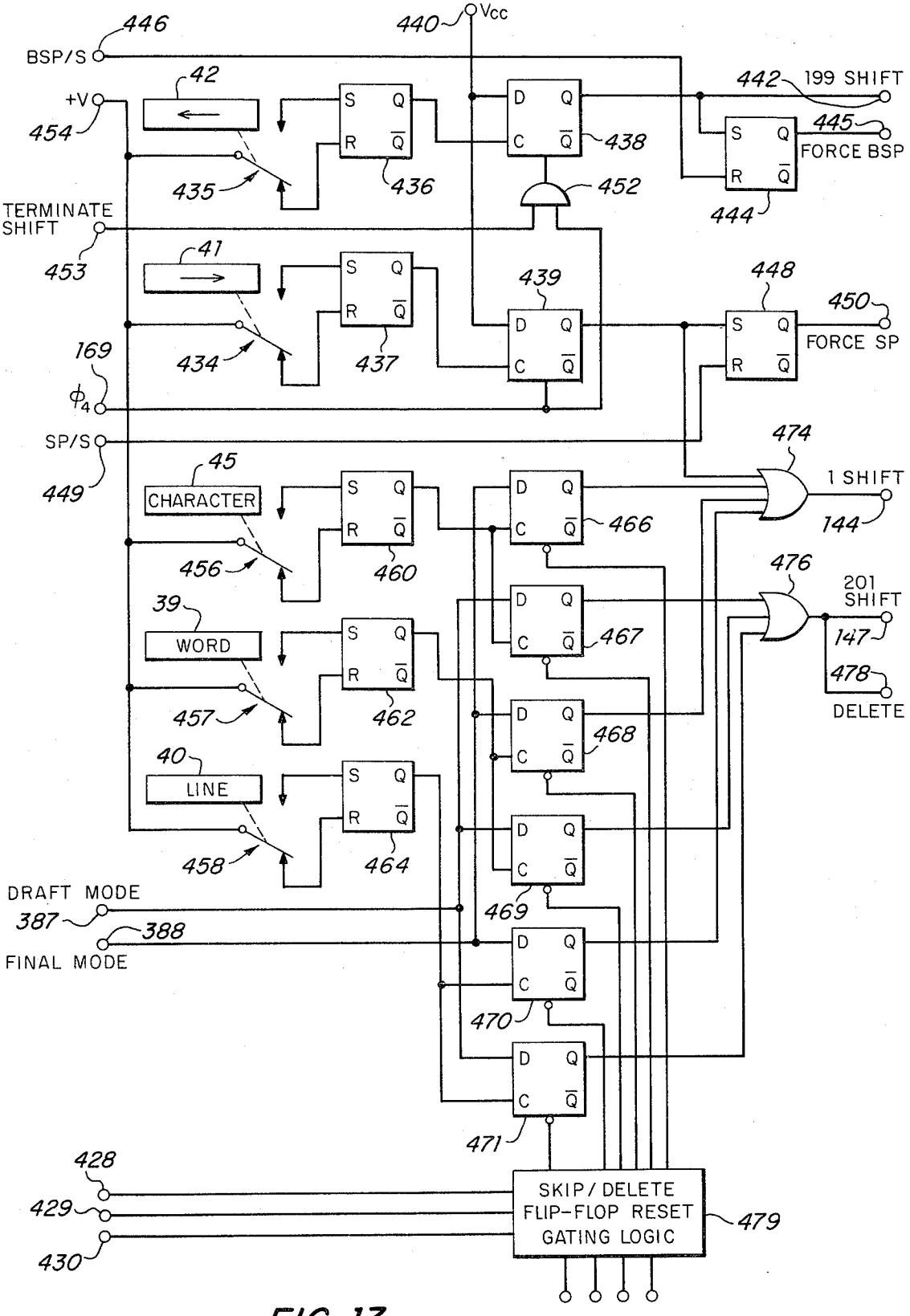

446
BSP/S
440
Vcc
42
+V
454
442
199 SHIFT
445
FORCE BSP
435
436
438
452
444
TERMINATE SHIFT
453
41
439
448
450
FORCE SP
434
437
169
ϕ_4
SP/S
449
474
45
CHARACTER
1 SHIFT
144
456
460
466
476
39
WORD
201 SHIFT
147
457
462
467
478
DELETE
468
40
LINE
458
464
DRAFT MODE
387
388
FINAL MODE
469
470
471
428
429
430
SKIP/DELETE FLIP-FLOP RESET GATING LOGIC
479

FIG. 13.

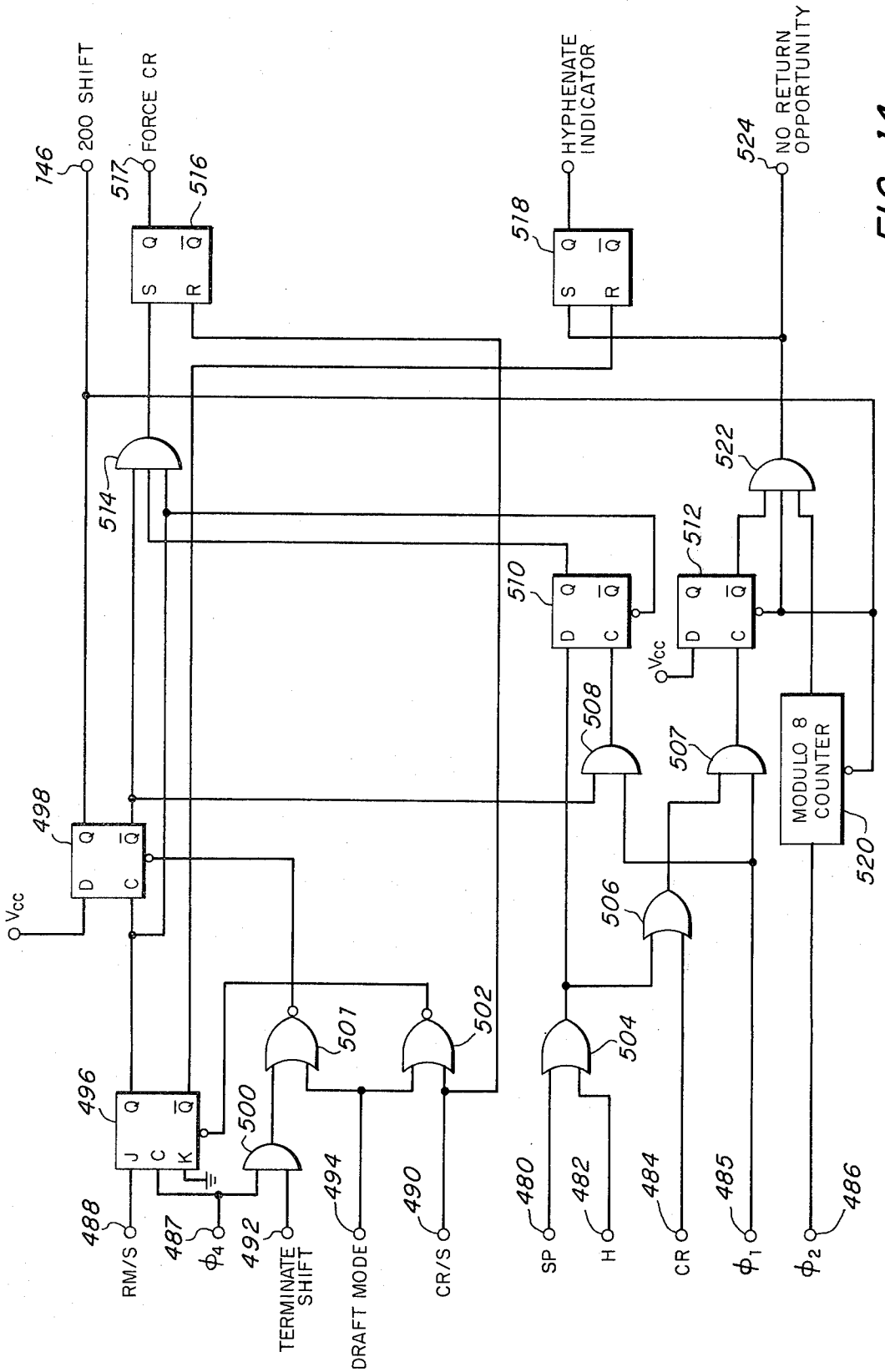

146
200 SHIFT
517
FORCE CR
516
518
HYPHENATE INDICATOR
524
NO RETURN OPPORTUNITY
514
522
512
510
508
507
506
504
502
501
500
498
496
488
487
492
494
490
480
482
484
485
486
520
MODULO 8 COUNTER
RM/S
ϕ_4
TERMINATE SHIFT
DRAFT MODE
CR/S
SP
H
CR
ϕ_1
ϕ_2
V_{CC}
V_{CC}

FIG. 14.

WORD PROCESSOR WITH RIGHT-HAND MARGIN CONTROL

This invention relates to word processing systems and more particularly to word processing systems incorporating electronically-controlled data recording and printing systems employing a typewriter as the input-/output terminal and including an automatic right hand margin control mechanism.

In typewriters used in word processing systems means are normally provided to define a so-called return zone located adjacent the right-hand margin of a typed line, i.e., a zone of a predetermined number of character positions in which a "return opportunity" is desirably to be found. A return opportunity will always be provided by a space between words and it may be provided by a hyphen in a compound word or by a recorded Carriage Return.

In the prior electronically-operated word processors, when the return zone is reached, automatic printing continues until a return opportunity is encountered. Once a return opportunity is found, the printer is caused to execute a Carrier Return after executing the hyphen, if appropriate. If, however, no return opportunity is encountered, then printing will continue until the right-hand margin is reached and then it will stop. The typist must now play out beyond the right-hand margin to hyphenate the last word or to cause a Carrier Return to be executed at the end of the last word if it cannot be hyphenated. Such a system has the disadvantage that it is necessary to print outside and beyond the established right-hand margin. In such situations, the width of the return zone is effectively increased by a significant amount and the right-hand margin of the final typing is ragged.

It would, therefore, be desirable to have a means of right-hand margin control which is capable of determining, upon entry of the return zone, if a return opportunity exists in the recorded data about to be played in the return zone. If a return opportunity is not found, then printing can be halted at the beginning of the return zone and the operator is free to intervene and hyphenate a word that would normally extend beyond the limits of the return zone. The anticipatory margin control system of this invention provides such a capability.

It is, therefore, a primary object of this invention to provide an improved means for adjusting the right-hand margin of a word processing system incorporating electronically-controlled data recording and printing systems employing a typewriter as the input/output terminal. It is another object to provide a right-hand margin adjustment means of the character described which has the ability to "look ahead" at data about to be printed in the return zone to determine whether or not the operator must intervene and hyphenate a word. An additional object of this invention is to provide a word processing system capable of automatically printing out text material wherein the right-hand margin is more easily and more evenly adjusted.

In the copending application of Heitman et al. Ser. No. 254,727, filed May 18, 1972 for Data Processing Apparatus now U.S. Pat. No. 3,828,323 issued Aug. 6, 1974 and assigned to the same assignee as the present application, there is disclosed a new word processing system that conveniently incorporates an input/output device, a buffer memory for temporary data storage, and a mass data storage means. The input/output printer is conveniently a typewriter such as is described in U.S. Pat. No. 2,919,002 to palmer, so that data retrieved from the mass data storage means via the buffer memory is printed out line-by-line on paper. This new word processing system also is adapted to operate in a Draft or Final operating mode. In the Draft mode, data recording and data retrieval and display (playing) are all possible. In the Final mode, data recording is not permitted. Further, in the Draft mode, editing changes in the nature of selective deletion of a character, a word, or a line is possible; while in the Final mode, it is possible to skip selectively over a character, a word or a line without deleting any data from the mass data storage means. In the aforesaid system, play character, play word, and play line controls are provided which causes a recorded character, word or line to be printed out or displayed on the output device. Another "auto" play control causes continuous playing out until the end of a document or some other condition is encountered. The play controls are operative regardless of whether the system is in the Draft or Final operating mode.

Accordingly, another object of this invention is to provide a word processing system as described in said copending application in which data display is under the control of means for automatically adjusting the right hand margin. Another object of this invention is to provide in a word processor of the character described in said copending application a right hand margin control means that is selectively operable but only when the processor is operating in the Final Mode.

Described briefly, the preferred embodiment of the invention comprises a word processor in which data retrieval and display involves transferring data from a mass data storage means to a buffer memory and then applying that data to the input/output printer for display. The "look ahead" capability of this invention is provided by the buffer memory which stores data temporarily in blocks on a line-by-line basis. The word processor is adapted to sense when the printer has reached the return zone, and before printing out any character in that zone, to examine the contents of the buffer memory to determine whether an opportunity exists to return the carrier or print head among data stored in the buffer memory corresponding to characters to be printed out or operations to be carried out while the carrier or print head is in the return zone. More specifically, the buffer memory is a shift register, and when the return zone is reached, the contents of the shift register are circulated once around the register and the first n data codes are examined for a return opportunity (n defines the effective width of the return zone). If no such opportunity exists, a signal is generated which causes the printer to stop and which is used to provide a visual or audio indication that the operator is required to intervene to complete the line, with or without hyphenation as desired, and to return the print head or carrier to the left-hand margin. The system also includes means, operative when a return opportunity is found in the return zone, to allow the printer to execute a carrier or print head return if the sensed return opportunity is a Carrier Return code and to force the printer to execute a carrier or print head return if the sensed opportunity is a Space or a Hyphen code.

The right-hand margin adjustment is adapted to operate with any selected return zone length. However, it has been determined that the optimum return zone

length is between four and ten characters. The longer zone lengths require less intervention by the operator but also produce a right-hand margin of greater variation in width; while the shorter zone lengths require more intervention but give rise to a neater right-hand margin. For example, the operator will have to intervene less than about 5% of the lines when the return zone is eight characters wide and about 25% of the lines when the return zone is four characters wide. Return zone widths of less than four characters are not practical since syllabic hyphenation points may not exist in the return zone when a long word is encountered.

Although the look ahead capability in the right hand margin control mechanism of this invention is particularly suitable for a word processing system using a buffer memory, it is also possible to use it to search down a magnetic tape medium character-by-character, across or along a magnetic card, or down a punched tape storage means in like manner. However, any of these procedures would be relatively slow in comparison with the circulating buffer memory.

Other objects, features and advantages of the invention are set forth in or rendered obvious by the following detailed description of a word processor that is constructed as disclosed in said copending application and incorporates a preferred embodiment of the invention.

The following description is to be considered together with the accompanying sheets of drawing wherein:

FIG. 1 is a perspective illustration of a typewriter and coupled console embodying the principles of the present invention;

FIG. 2 is an enlarged view of the console of FIG. 1 showing various control buttons, displays and other elements;

FIG. 2A is a perspective view of a standard tape cassette illustrating in phantom the organization of information on the tape according to the principles of the present invention;

FIG. 3 is a block diagram illustrating the organization of the invention;

FIG. 4 is a block diagram showing details of the keyboard interface logic of FIG. 3;

FIG. 5 is a block diagram showing details of the buffer memory of FIG. 3;

FIG. 6 is a logic diagram, partly in block form, illustrating a clocking control system forming part of the buffer control of FIG. 3;

FIG. 7 is a logic diagram, partly in block form, illustrating output multiplexer, input demultiplexer and read-and-write circuits shown in FIG. 3;

FIG. 8 is a timing diagram illustrating the operation of elements in FIG. 7;

FIG. 9 is a logic diagram, partly in block form, showing the print control logic system of FIG. 3;

FIG. 10 is a diagram illustrating some logic employed in the main control of FIG. 3 for controlling clocking of the buffer memory;

FIG. 11 is a diagram, partly in block form, showing address display logic coupled with the control console;

FIG. 12 is a diagram illustrating logic in the main control of FIG. 3;

FIG. 13 is an additional logic diagram illustrating the main control of FIG. 3; and

FIG. 14 is a logic diagram, partly in block form, showing some of the margin adjust logic of FIG. 3.

Referring now to the sheets of drawing, there is shown in FIG. 1 a preferred arrangement of equipment in which the invention is incorporated. The apparatus of the invention includes an input/output printer **20** interconnected by an electrically conductive cable **21** to a control console unit **22** for controlling recording, reproducing, and editing. Printer **20** typically includes a manually operable keyboard **23** for controlling a single head printer of the Palmer-type which has been adapted (for example, by being emplaced on a baseplate **24** which is capable of detecting the condition of the latch and cycle shaft switches in the printer **20** and also having solenoids capable of driving the latches and cycle shaft of the printer **20**) for producing an output indicative of the condition of those switches. Such a baseplate **24** is described in U.S. Pat. Nos. 3,452,851 and 3,453,379 issued to L. Holmes, Jr. As well known, the print head **16** of a Palmer type printer is intended to strike a sheet carrier or platen **17** to form or print alphanumeric characters. Printer **20** preferably also includes within its housing, means **15** for moving print head **16** along a line between predetermined margins and means for indexing platen **17,** all by mechanisms described in detail in the aforesaid Palmer patent. In printers of the Palmer type each character is automatically encoded when typed. When such a printer **20** is combined with a Holmes type baseplate **24** the combination will be capable of translating or interconverting formation of typed characters and performance of printing functions with corresponding coded character and function signals.

Unit **22** has a control panel **26** shown in more detail in FIG. **2,** the panel **26** including a spring-loaded, normally closed cassette door **27** which is moveable so that a magnetic tape cassette **240** (shown in more detail in FIG. 2A) can be loaded into a tape transport mechanism located behind the door **27.** Adjacent door **27** is a display **28** for indicating a record number corresponding to the position of a data location on the tape **18** in a cassette **240** which may be loaded into the machine. On control panel **26** are also a number of keys or buttons and display lights associated with data entry, editing and playback. The system of the invention is intended to have three basic operating modes, a draft mode, a final mode and an insert mode. To provide for selection of the mode of operation of this system there are provided a Draft button **30,** a Final button **31,** and an Insert button **32.** To provide for control of printing out onto the printer **20** of a character, word, or line from storage, either while the system is in draft or final mode, there are included a Character button **33,** a Word button **34,** and a Line button **35,** plus an Automatic button **36** for allowing the system to print continuously. An On button **37** is also provided for starting the system. Stop button **38** is included for stopping any printing operation by the machine. The deleting or skipping of characters, words and lines respectively is provided by manipulation of Character, Word and Line buttons **45, 39** and **40.**

A brief description of the functional consequences of the operation of the various buttons on control panel **26** will be helpful in understanding the detailed structural description of the device. It is intended that the system be capable of both recording data onto a cassette **240** or printing data from a cassette **240** onto printer **20** when operating in the draft mode. Specifically, it is intended during draft mode operation that

any data entered by manipulation of keyboard **23** of printer **20** should be stored in a magnetic storage or record in the system with any previously recorded characters being overwritten by new data being stored at the same data locations. In order to accomplish this end one need merely start the system, select the record location, press Draft button **30** and proceed to type in data on the keyboard **23.** To cause the data thus stored to actuate printer **20** and therefore to be type out, it is only necessary to return to the beginning of the stored data, to push Character button **33** to obtain print out of a single character, to push Word button **34** to obtain a single word, to push Line button **35** to obtain a single line, or to push Automatic button **36** to permit the entire stored data to be reproduced on printer **20.**

If one should now press Final button **31,** the system is conditioned so that no storage of data manually typed or entered on printer **20** can occur, but that only the data stored in the machine can be printed by printer **20.** When playing in the Final mode it will be later seen that an automatic right margin control system operates. The Draft and Final modes of operation are mutually exclusive and the system provides that if either the Draft or Final buttons **30,31** are pushed, the machine is switched from the one to the other mode of operation.

Depression of Insert button **32** while the system is in the Final mode will be ineffective, i.e. will not in any sense allow the machine to operate other than in normal Final Mode operation. On the other hand, if the Insert button **32** is depressed while the system is in the Draft mode, the system switches to an Insert Mode of operation, and if desired, visual indication can be given that the machine is in an Insert Mode, as by lighting Insert button **32** or the like. The Insert Mode is intended to provide an operation such that data entered on printer **20** by manual operation of the keyboard **23** will be inserted into storage, up to a limit, without overwriting or otherwise destroying previously stored data. Only typing and recording can take place while in the Insert Mode since pushing any other buttons (except the Draft or Final buttons **30,31**) on the control panel **26** will cause the machine to trip out of the Insert mode and revert to the Draft mode. If Insert button **32** is pushed again, the system will switch out of the Insèrt Mode back to the Draft Mode and, of course, any visual indication of Insert Mode operation will terminate. If Final button **31** is pressed, the system will switch to Final mode operation.

The play or print buttons **33, 34, 35, 36** or **38** control the extent to which data will be read out of storage, either in Draft or Final mode operation, and displayed on printer **20.** Each time Character button **33** is pushed, the next character in storage will be read out on printer **20.** Similarly, depression of Word button **34** or Line button **35** will cause the next word or line in storage to be read out on the printer **20.** When the Automatic button **36** is pushed, the system will cause the printer **20** to type out the data in storage continuously until some stopping command occurs. The latter can be obtained by pressing Stop button **38,** or by certain special conditions which will be described hereinafter.

Step Right and Step Left buttons **41** and **42** control the shifting of data in storage. Each time either is pushed the data in storage is shifted by one character in the appropriate direction and the single print head **16** or carrier on the printr **20** similarly steps. In this respect buttons **41** and **42** actuate the print head **16** to move in the same manner as the space bar and backspace key on the printer keyboard **23** with certain exceptions as will be explained later. Prferably, if one of the buttons **41** and **42** is held down, repetitive action is initiated so that the system steps sequentially character by character.

As described, there are three delete/skip buttons **45,** 39 and **40.** When the system is in Draft mode depression of these buttons **45, 39, 40** will serve to delete a recorded character, word or line from storage. When the system instead is in the Final mode, these buttons **45, 39, 40** act as skip buttons which cause the system to skip the appropriate character, word or line in storage without striking or otherwise destroying the skipped data. Because the functioning of these buttons **45, 39, 40** to cause either deletion or skipping depends upon the mode in which the system is then operating, means are provided in the form of visual indicating lights **43** and **44** which respectively light up to indicate the nature of the function of the buttons, **45, 39, 40** i.e. delete or skip as the case may be.

There are two buttons for controlling tape motion, a Tape Forward button **46** and a Tape Back button **47.** These are preferably of the spring-loaded type and each has a first or up position and a second or down position. Pushing either of the tape buttons **46** or **47** to its down position causes the system to move the tape **18** either back or forward (as the case may be) to the beginning of the next of a number of predetermined data blocks **19** or stations on the tape **18.** This motion from predetermined station to predetermined station on the tape **18** will continue as a smooth sequence until the appropriate button **46** or **47** is released. After release of the button **46** or **47,** the motion of the tape **18** in the cassette **240** will continue until the next predetermined station on the tape **18** is reached, at which time the motion of the tape **18** is stopped. Similarly pushing either buttons **46** or **47** to their up position causes the system to shift to a fast forward or fast rewind movement (as the case may be) during which the tape **18** winds continuously. Fast winding due to pushing the Tape Back button **47** to its up position will continue until the button **47** is released, at which point the system then shifts to slow forward speed and continues to move the tape **18** until the next predetermined station on the tape **18** is located. A similar operation in the opposite direction is effected by manipulation of the Tape Forward button **46.**

In the preferred embodiment the cassette tape **18** is at least a two track (**25** and **29**) tape, and two read/write heads, one for each of tracks **25** and **29,** (or a single two-channel head such as head **238**) are incorporated into the system. One of the tracks **25** of the tape **18** is for the data to be stored. The other tape track **29** is intended to contain data addresses **48,** preferably in the form of coded conversions of sequentially numbered three decimal digits, each data address **48** being physically located substantially adjacent the beginning of a data block **19** on track **25.** Thus, when the tape **18** is moved either forward or back in the cassette **240,** circuitry associated with the address read/write head **238** and the record number display **28** will cause the latter to be appropriately indexed each time an address **48** corresponding to a data block **19** or record moves past the read head **238.** If desired, one can provide an erase mechanism associated with the tape transport mecha-

nism and the control panel **26** so as to erase selectively all data from the tape **18**, and also if desired to regenerate the addresses **48** on the tape **18.**

Also in the preferred embodiment, associated with the control panel **26** are a number of visual indicators or special lights **49** in addition to the delete/skip light and insert indicator light discussed earlier. Similarly, a number of audio signal devices to indicate certain conditions of the apparatus can also be provided and will be described hereinafter.

The operation of the device thus described can be advantageously described in connection with a typewriter as an example of the printer **20.** There are three basic situations to be described:

1. Basic entering of data through the typewriter keyboard **23,** i.e. recording an initial draft;
2. Insertion, deletion and other operations made on data after entry of the latter, i.e. editing; and
3. Data retrieval, i.e. typing of final copy.

In order to record data initially, the operator will first activate the typewriter **20** and also will depress button **37** to turn on the remainder of the system. The operator should first set margins and tabs on the typewriter **20** as desired although one or more embodiments of the invention may include the ability to set and clear tabs on the basis of prior stored information. Then a magnetic tape cassette **240** is placed in the carrier behind door **27** and the operator then depresses button **30** to place the system in the draft mode of operation. The position of the tape **18** in the cassette **240** will be indicated by the address **48** displayed at display **28.** If the cassette **240** is not rewound and it is desired to start from the beginning of the cassette **240,** the latter can be rewound by pushing Tape Back button **47** to its up position and waiting until rewind is completed. If the operator wishes to start beyond previously recorded material that is to be preserved, the tape **18** can be moved with buttons **46** and **47** until the appropriate address **48** is noticed at display **28.**

Hereafter, recording in the Draft mode is accomplished automatically merely by typing the desired information on the typewriter keyboard **23.** Each time the operator types a Carrier Return, the data associated with the preceding typed line is then transferred from the buffer memory **52** of the system onto magnetic tape **18.** if the operator observes that a wrong key has been struck, correction can be made by depressing the Step Left button **42** which causes the typewriter **20** to automatically backspace. When the typewriter **20** has been backspaced to the error, the operator can strike over the error with the correct character key. To get back to the point where recording had been interrupted, the Step Right button **41** can be depressed, or as will appear later, one can play out the intervening material which has been recorded, or lastly one can retype the intervening material and rerecord it.

If the operator wishes to underscore a word upon entry, the word can be typed and then, using the regular backspace key on the typewriter keyboard **23** which will provide a recorded backspace, the typewriter **20** should be backed up to the beginning of the word. The word can then be underscored, the underscoring being recorded also.

When the operator has completed the draft, a Stop Code should be entered. The Stop Code is generated by depressing the shift key and striking Stop button **38** on the control panel **26.**

Editing of a draft can be done in three basic ways:

1. A new draft can be generated in the Draft mode of operation, combining the desired parts of the old draft with typed and recorded corrections;
2. Only specific lines requiring editing can be modified; or
3. A final copy can be generated in the Final mode of operation with corrections being entered on the copy as the document is printed, without recording the corrections.

Normally, the first approach would be used especially if further author revisions are anticipated. The third approach is appropriate if only final, minor corrections are to be made and a final copy is desired.

In generating a new draft, the following situations are likely to be encountered. First, one can edit simple typographical errors by playing back the tape **18** in the Draft mode, by first striking any one of buttons **33, 34,** 35 or **36.** This will cause the material recorded on the cassette **240** to be printed by the typewriter **20,** assuming of course that the cassette **240** has been rewound to the appropriate starting position. The material is then played up to but not through the error and the error is corrected by overstriking. Overstriking using the keyboard **23** will automatically erase the erroneous material from the system and insert the corrected material in the appropriate place.

If the error in the draft is surplusage of material such as an extra letter or the like, it can be corrected by printing the material out on the printer **20** up to but not through the extra matter. The latter can now be deleted by simply pressing the appropriately selected one of Delete/Skip buttons **45, 39** or **40** inasmuch as these buttons **45, 39, 40** generate signals to place the system in condition to delete the material when the system is also in the Draft mode.

If the error in the Draft mode is due to missing material, the latter can be added by playing out the recorded material (in the Draft mode) up to the appropriate position, pushing Insert Button **32** and typing on keyboard **23** the missing characters or words. The machine can then be taken out of the Insert mode simply by pushing any of the buttons **33** to **36** inclusive, all of which when actuated switch the system back to the Draft mode of operation.

Final copy can be typed in either the Draft or Final mode. In typing out copy, the basic difference in operation between the two modes is simply that in the Draft mode the system will execute each carrier return signal that has been recorded whereas, in the Final mode the carrier returns may or may not be executed depending upon the operation of an automatic right margin control feature.

If no further editing is required, the operator merely inserts paper into the printer **20,** sets the tabs and margins of the latter, puts the cassette **240** into the machine, and moves tape **18** to the beginning of the document with buttons **46** and **47.** The machine then is placed in automatic play by striking Automatic button **36.** The material or text stored in the machine will now be printed by the printer **20** on a substantially continuous basis until the printing is stopped by either striking Stop button **38** or because the operator has preferably recorded an appropriate Stop Code at the end of each page of text. If manual entry of certain material such as the name and address of the person to whom a letter is to be sent is to be inserted on the final copy, a Stop

Code should have been recorded when the original draft was recorded so that automatic printing stops at the point where the special material is to be manually entered. In order to prevent a recording of the manually entered material if the system is not operating in the Final mode, the system should then be switched temporarily to that mode of operation by depressing button **31**.

If the final copy is being printed out in the Final mode of operation, the system will stop printing whenever it detects that it cannot automatically find a carrier return opportunity such as a recorded Carrier Return or Space or Hyphen signal in a predetermined return zone adjacent the right margin of the printed text. When this occurs, the operator may use key **33** to cause machine printing, character by character, up to the point where a Hyphen and a Carrier Return can be manually entered on the keyboard **23** after which automatic typing can then be reinitiated, e.g. by again depressing the Automatic key **36**. Normally, this manually entered Hyphen and Carrier Return will not be recorded so that any reruns from the same tape **18** will encounter the same stopping conditions. If, however, the operator wishes to record the Hyphen and Carrier Return, this may be done by pressing Draft button **30** and Insert button **32**, typing the Hyphen and Carrier Return, then pushing Final button **31** to switch the system operation back to Final mode, and finally pushing one of the buttons **33–36** inclusive to resume printing. As long as no further changes are made in the paragraph up to this point, subsequent reruns will always find the Carrier Return and hyphen when needed and will continue playing without automatically stopping.

In typing final copy, it may be necessary to make some minor corrections in the recorded material. As long as these changes need not be recorded on the tape **18**, the procedure is simple while operating in the Final mode. Simply by depressing any of the Delete/Skip buttons, **39**, **40** and **45**, one may cause the system to skip over unwanted characters, words, or lines in the material being played back and additional material may be manually typed in.

Before describing some of the more complex editing operations, it will be advantageous to describe briefly the general organization of the system embodying printer **20**, baseplate **24** and control console unit **22**. With reference particularly to FIG. **3**, there is shown a block diagram of the organization of a system in simplified form. In order to clarify the diagram, all of the control connections are shown as solid lines whereas all of the data carrying lines are shown as dashed lines. The embodiment of FIG. **3** includes input/output printer **20** which, as previously described, is connected via baseplate **24** to the control console unit **22**. Data flow from the printer **20**, in the form of electrical signals, is applied to keyboard interface logic **50**. The latter primarily serves to encode electrical signals from the printer **20**. The output of the interface logic **50** is then fed along an appropriate connection to the input of a buffer memory **52**. As will be described later, the buffer memory **52** is preferably in the form of a shift register capable of storing, for example, 200 characters each of eight bits.

It will be appreciated that one may however employ a random access type buffer memory such as a core array as memory **52**, but because a random access memory might involve complex addressing logic, a shift register type of memory is preferred. The output of the buffer memory **52** in turn is connected to means such as a multiplexer **54** for converting the eight parallel bit per character format of the data organization in the buffer memory **52** to a serial train of data bits. The output of multiplexer **54** is then in turn fed to the input of write-data circuitry **56** which conditions the data and places it in single-channel format for storage, such as on the tape **18** in a cassette **240** mounted in a magnetic recording apparatus indicated as data storage **58**.

Alternatively, if one employs an eight-track tape with corresponding read-write channels, data need not be multiplexed but can be read out directly from buffer storage to tape.

The organization shown in FIG. **3** also includes a return path for reading data out of data storage **58** so that it can be printed out by printer **20**. To this end, data storage **58** is connected to read-data circuits **60** and to read-address circuits **63**. The latter is intended to read the address track **29** on the two-channel tape **18** and provides an output which is connected to address-display logic **64** which serves to actuate address-display **28**. Read-data circuits **60** are intended to read the data stored in serial form on the other track **25** of the tape **18**. The output of read-data circuits **60** is fed to means, such as input demultiplexer **62**, for converting the serial form of the data into an eight parallel bit per character code, suitable for injection into the buffer memory **52**. To that end the output of demultiplexer **62** is coupled to the input of buffer memory **52**. The output of buffer memory **52** is also connected as an input to both margin-adjust logic **66** and print-control logic **68**. Margin-adjust logic **66** serves to examine the contents of buffer memory **52** so as to decide if, within a predetermined printing zone along the right hand margin of the carrier travel set on printer **20**, a Hyphen, Space or Carrier Return code will occur, thereby providing the basis for a right hand margin adjustment system. Print-control logic **68** is primarily employed to control printer **20** in accordance with the character and functional signals received from the buffer memory **52** and the signals received from margin-adjust logic **66**. Additionally, print-control logic **68** is intended to decode the contents of buffer memory **52** into a form suitable for actuating printer **20**.

Console unit **22** and the controls contained therein are shown as main control block **22A** which is connected for controlling the operation of printer **20**. Main control block **22A** is interconnected with the keyboard interface logic **50** for controlling the sum of the encoding functions of the latter and is also in turn connected to receive signals from the keyboard interface logic **50** for use elsewhere in the system. Similarly, main control block **22A** is connected so as to view the data flowing both into buffer memory **52** and out of buffer memory **52**. Print-control logic **68** includes preferably a parity check system whereby it examines data flowing out of buffer memory **52** for odd parity and provides a control signal to main control block **22A** to indicate if parity is or is not correct. Buffer memory **52** is connected so as to be controlled by a buffer control system **70** which in turn is under the control of main control block **22A**. The system also includes write-control logic **72** which is connected so as to be responsive to main control block **22A** and is also coupled to control write-data circuits **56**. Similarly, the system includes read-control logic **74** which is connected to be responsive to main

control block 22A and serves to control both read-data circuits 60 and read-address circuits 63. The system also includes tape control circuits 75 which are responsive to main control block 22A and serve to control operation of mechanisms for transporting the data storage record or tape 18.

For convenience, the form of encoding employed in the system of the invention is based to a large extent upon the nature of the basic structure of a printer 20 of the Palmer-type and a baseplate 24 of the Holmes type. Thus, the print or informational characters can be defined in binary form according to the following Table I, wherein the eight data lines carrying each bit are respectively identified as R1, R2, R2A, R5, T1, T2, P (parity) and S (case), all collectively referred to hereafter as the data lines.

TABLE I

BIT POSITION	1 R1	2 R2	3 R2A	4 R5	5 T1	6 T2	PARITY	CASE
Character:								
a	0	0	1	1	1	0	0	0
b	0	0	0	0	0	1	0	0
c	0	0	1	1	0	1	0	0
d	1	0	1	1	0	1	1	0
e	1	0	1	0	0	1	0	0
f	0	1	1	1	0	0	0	0
g	1	1	1	1	0	0	1	0
h	1	0	0	0	0	1	1	0
i	0	0	1	0	1	0	1	0
j	1	1	1	0	0	0	0	0
k	0	0	1	0	0	1	1	0
l	1	0	0	1	0	1	0	0
m	1	1	1	1	1	0	0	0
n	0	1	1	0	0	1	0	0
o	1	0	0	1	1	0	0	0
p	1	0	1	0	0	0	1	0
q	0	0	1	0	0	0	0	0
r	1	0	1	1	1	0	1	0
s	1	0	0	0	1	0	1	0
t	1	1	1	0	0	1	1	0
u	0	1	1	1	0	1	1	0
v	0	1	1	1	1	0	1	0
w	0	0	0	0	1	0	0	0
x	1	1	1	1	0	1	0	0
y	1	0	0	0	0	0	0	0
z	1	1	1	0	1	1	0	0
1	1	1	1	1	1	1	1	0
2	0	1	1	0	1	1	1	0
3	0	1	1	1	1	1	0	0
4	1	0	0	1	1	1	1	0
5	1	0	1	0	1	1	1	0
6	0	0	1	0	1	1	0	0
7	1	0	1	1	1	1	0	0
8	0	0	1	1	1	1	1	0
9	0	0	0	0	1	1	1	0
0	1	0	0	0	1	1	0	0
;	1	0	1	1	0	0	0	0
,	0	0	1	1	0	0	1	0
.	0	1	1	0	1	0	0	0
'	1	0	1	0	1	0	0	0
/	1	0	0	1	0	0	1	0
=	0	1	1	0	0	0	1	0
+	1	1	1	1	1	1	1	0
Hyphen	0	0	0	0	0	0	1	0

Upper case characters, of course, use a 1 bit in place of the case bit in each instance, and also for upper case characters the parity bit is the complement of the parity bit for the lower case character, in order to maintain odd parity. It will be appreciated that other encoding systems can be used, but the foregoing is the more convenient.

As known, baseplate 24 has six output data lines on which appear information character signals identified as R1, R2, R2A, R5, T1, and T2 (see FIG. 4). Each information character generated by the printer 20 in response to operation of the keyboard 23 is partially encoded in the form of combination of bits represented by these information character signals. These signals are direct outputs of the baseplate 24.

Additionally, other signals representing operation of the functional keys of the printer 20 are produced by the baseplate 24 as uncoded or simple signals. These signals are Tab (TAB), Tab Set (TABS), Tab Clear (TABC), Backspace (BS), Line Feed or Carrier Index (CI); Space (SP), Shift (SH) and Carrier Return (CR). Still another output obtained directly from baseplate 24 is a Printer-Head-in-Motion signal (PIM). All of the foregoing signals are fed as input signals to the keyboard interface logic 50 (FIGS. 3 and 4). In addition to the foregoing signals received directly from the baseplate 24, other simple signals may be supplied as inputs to the keyboard interface logic 50. Included are such signals as a Stop Code signal generated by depressing the shift key on the keyboard 23 of the printer 20 and concurrently depressing Stop button 38 on the control console unit 22. The shift and stop signals produced are then gated in known manner to produce the Stop Code signal which is then encoded by keyboard interface logic 50 as shown in Table III.

Referring now to FIG. 4, the keyboard interface logic 50 includes an encoder which comprises a plurality of encoder gates 76 having input lines which carry the

foregoing keyboard logic input signals. The keyboard interface logic **50** also includes a plurality of enable gates **78**, a parity generator **80**, and an enable line **82** connected to provide an enabling signal to enable input terminals of enable gates **78**. Encoder gates **76** have data output lines connected to the input terminals of enable gates **78** and parity generator **80** has a plurality of input terminals connected to receive the signals being carried by the data output lines of encoder gates **76**. The output of parity generator **80** is also connected as an input to enable gates **78**.

To the extent shown in FIG. **4**, the keyboard interface logic **50** performs a number of related functions. A basic function is to complete the encoding of characters generated by operation of the keyboard **23** so that each informational character is now coded as a unique combination of eight bits as earlier identified in Table I. This is accomplished by adding a parity bit and a case bit to the partial code produced by the informational character signals appearing on the six output data lines of the baseplate **24**. Another function is to encode as other unique combinations of eight bits, as identified in Table II, the various machine key-board controlled functions that appear as direct baseplate out-puts — namely Tab, Tab Set, Tab Clear, Space, Backspace, Carrier Return and Carrier Index (i.e. Line Feed).

A third function is to encode as still other unique combinations of eight bits other logic inputs that do not arise directly or solely from that baseplate **24** — namely, the Stop Code, and certain special or required functions. The preferred coding for the Stop Code is shown in Table III together with the coding for Blank Cell.

TABLE II

BIT POSITION	1 R1	2 R2	3 R2A	4 R5	5 T1	6 T2	PARITY	CASE
Functions:								
Tab Set	0	1	0	0	0	0	0	0
Tab Clear	0	1	0	0	0	1	1	0
Tab	0	1	0	1	0	1	0	0
Space	0	1	0	1	1	1	1	0
Backspace	0	1	0	1	0	0	1	0
Carrier Index	1	1	0	1	0	1	1	0
Carrier Return	1	1	0	1	1	0	1	0

TABLE III

BIT POSITION	1 R1	2 R2	3 R2A	4 R5	5 T1	6 T2	PARITY	CASE
Functions:								
Stop Code	1	1	0	0	0	0	1	0
Blank Cell	0	0	0	0	0	0	0	0

A fourth function is to provide three other outputs, an SH signal, a PIM signal and a signal identified, for convenience, as Function from Keyboard. This latter signal appears whenever any one of several signals indicative of keyboard function (specifically Tab, Tab Set, Tab Clear, Space, Backspace, Carrier Index and Carrier Return) appear at the inputs to encoder gates **76**. These encoding functions are performed by encoder gates **76** and by parity generator **80**, with the case (S), parity bit signal (P) and information character signals appearing as outputs of enable gates **78**. Enable gates **78** produce outputs in response to signals appearing in the output data lines of encoder gates **76** and parity generator **80** only when an enable signal appears on enable line **82**. Parity generator **80** is of a known type which generates a **1** bit along an output line to provide a parity signal P according to whether the parity of the signals appearing on its seven output lines is even or odd. The system herein disclosed uses odd parity so that a **1** bit is generated by parity generator **80** only when it determines that its input data signals have even parity. Parity signal P is passed to an appropriate output terminal of enable gates **78** when the latter are enabled.

The encoder output shown in FIG. **4** from enable gates **78** and from encoder gates **76**, as previously indicated in FIG. **3**, are applied to buffer memory **52**. The latter is shown in FIG. **5** as comprising eight input OR gates **84, 85, 86, 87, 88, 89, 90** and **91**. The outputs from enable gates **78** are respectively connected to OR gates **84** through **91** inclusive. The latter are also connected to eight other input terminals, each identified by the corresponding code bit, to which are applied information character, case and parity signal inputs derived from the Red Data Circuits **60** or other sources. The output from OR gates **84–91** inclusive are fed to a blank cell detector in the form of gate **92** which forms part of main control block **22A** and are also fed in to the respective inputs of a main storage memory, preferably in the form of a static shift register **94** capable of storing **200** eight bit characters. Clock line **95** is provided for introducing a clocking signal X_2 for initiating storage or buffer shifting. The outputs of shift register **94**, again eight lines which correspond to the inputs from enable gates **78** are connected to corresponding output terminals each identified by the appropriate corresponding code in the drawing. The eight output lines are also connected to the corresponding inputs of a first subsidiary storage device **96** which is preferably an eight-bit single character register having an input clock line **97** at which clocking signal X_1 is intended to be applied. First subsidiary storage device **96** has eight output lines, each corresponding of course to one of the eight input lines thereto and each connected to a

corresponding input of a second eight-bit single character register **98** which is clocked by a signal X_3 over line **99** and can be cleared by a reset-signal C_3 over a line **100.** Register **98** again has eight output lines each corresponding to a respective input line to the register **98,** the output lines from register **98** each being connected to a corresponding one of input OR gates **84–91** inclusive so that, for example, OR gate **91** which has an input connected to the parity bit line from parity generator **80** also has an input connected to the corresponding parity bit line from register **98.** Similarly, all of the other input lines to the various OR gates **84–91** are matched. The path thus defined from the respective input OR gates **84–91** through the main storage memory or static shift register **94,** through registers **96** and **98** and back to the respective input OR gate **84–91,** will be seen to constitute a complete feed back path around the main storage memory or static shift register **94.** In the embodiment shown, two subsidiary storage registers **96** and **98** are employed to minimize problems arising from possible differences in the operating speed of the main and subsidiary storages. However, the feedback loop may comprise but one single-character register if the latter is closely matched in terms of operating speed to the main storage memory or static shift register **94.**

It is now important for an understanding of the invention to appreciate how data is passed through the buffer memory **52** during the various operating modes heretofore described.

As previously noted, the main storage memory is static shift register **94.** Assuming that it is an eight-line 200 bit register, i.e. can store 200 eight bit characters, each time a clocking signal X_2 is applied over line **95,** a new character will be entered at the left hand end of the register **94** via OR gates **84–91** and whatever characters are already stored in the register **94** will shift one cell, i.e. one bit position to the right. If a character is already stored in the **200**th cell, it will be ejected from the right hand of the cell when the register **94** shifts in response to an X_2 clocking signal. The subsidiary registers **96, 98** also are static shift registers. Accordingly, occurrence of a clocking signal X_1 on line **97** will cause the first subsidiary storage register **96** to respond to and store the data signals that appear on the output lines of register **94.** Occurrence of a clocking signal X_3 on line **99** will cause the second subsidiary storage register **98** to respond to and store the data signals appearing on the output lines of the first subsidiary storage register **96.** Occurrence of a C_3 reset pulse on clear line **100** clears the second subsidiary storage register **98** to prevent a character previously stored therein from being circulated back to the register **94** via OR gates **84–91.** Clearing the second subsidiary storage register **98** is performed when it is desired to clear the main storage memory or static shift register **94** or to enter new data into the main storage memory or static shift register **94.**

The clocking pulses for the buffer memory **52** are derived from a four-phase clock pulse generator. As described hereinafter, the clock pulse generator is gated to provide a series of four clock pulses or tetrads occurring at times ϕ_1, ϕ_2, ϕ_3, ϕ_4. The clock pulse generator also is adapted to generate such tetrads as in four different clusters or groups characterized by a quantifier depending upon the operating mode of the system. The clock pulse generator is gated to provide a train of clock pulses each time a printer key is depressed or the printer **20** prints a character or executes a function in response to an output from the buffer memory **52** or each time the system is caused to delete or skip a character as a result of depressing one of the delete/skip buttons **45, 39** and **40.** The reason for slaving the clock pulse generator (and thus the buffer memory **52**) to the printer **20** when the system is set so that the typewriter **20** will print out in accordance with the output from the buffer memory **52,** is that the printer **20** takes longer to execute some operations than others. Similar reasoning is the basis for adapting the clock pulse generator to generate pulse groups according to one of four different quantifiers depending upon the operating mode of the system. As will be seen, the quantifiers in the preferred embodiment are **1, 199, 200** and **201.**

As hereinafter described, provision is made for clocking the buffer memory **52** so that it can be made to undergo a single shift cycle or a **201** shift cycle (assuming buffer memory **52** is of a 200 character type). In the single shift cycle the main storage memory or static shift registers **94** is shifted as a result of an X_2 clocking signal. In the **201** shift cycle, the second subsidiary register **98** is held clear during the main register **94** shift to prevent circulation of old data from the second subsidiary register **98** back to the main register **94.** When typing in a character from the keyboard **23** in the Draft mode, there is no need to clock the subsidiary registers **96, 98** in order to effect a single shift whereby the typed character is entered into the left hand end of the main storage memory or static shift register **94;** in practise however, all three registers **94, 96,** and **98** are clocked according to a $X_1X_3X_2$ sequence (i.e. clocking signals X_1, X_3, and X_2 occur in the order named at times ϕ_1, ϕ_2, and ϕ_3 respectively). In a **201** shift cycle, the main register **94** is shifted **201** times, with all three registers **94, 96,** and **98** being clocked according to the normal sequence $X_1X_3X_2$, or a second special $X_1X_2X_3$ sequence. In this latter sequence, the clocking signals X_1, X_2, and X_3 occur in the order named at times ϕ_1, ϕ_2, and ϕ_3 respectively. Provision is also made for clocking the buffer memory **52** so that it can undergo a **199** or **200** shift cycle (again assuming a **200** character main storage memory or static shift register **94**). The **199** shift cycle is used to shift the contents of the main storage memory or static shift register **94** to the left (backward) one cell while the **200** shift cycle is used to clear the main storage memory or static shift register **94** and for other actions.

A large number of buffer memory clocking modes are employed in operation of the system. Some of these modes are described as follows:

Typing Data Into Store in the Draft Mode

In this case a single or a **201** shift cycle is used, with the clocking occurring in the $X_1X_3X_2$ sequence and the second subsidiary storage register **98** being held clear during the single shift cycle and during the first of the **201** shifts to prevent circulation of old data and to enable a new character to be entered into the main storage memory or static shift register **94.** No reset signal is applied to clear line **100** during the remaining **200** shifts so that the contents of the main storage memory or static shift register **94** can be circulated and so that the new character sits at the left hand end of the main storage memory or static shift register **94** just as if a single shift cycle had been executed. The advantage of using the **201** shift cycle rather than the single shift

cycle for this purpose is because the **201** shift cycle permits one to examine the buffer contents to detect a full buffer condition.

Printing Out From the Buffer Memory

Single shifts are used in this mode, with the $X_1X_3X_2$ sequence providing normal circulation of data through the main and subsidiary storage registers **94, 96** and **98.** Data signals from the typewriter sensors in the baseplate **24** during the time that the typewriter **20** is printing out are prevented from appearing on the input lines to OR gates **84–91.**

Inserting Data Into Store in the Insert Mode

This mode can be utilized when the machine has been set for Insert mode operation. It involves a **201** shift cycle. The clocking order is initially $X_1X_2X_3$, but is caused to revert to $X_1X_3X_2$ at a point in the **201** shift cycle when a blank cell is detected at a selected point in the buffer memory **52.** Two variations are provided. In one case the clocking order will change to $X_1X_3X_2$ when a blank cell is first seen at the output of the second subsidiary register **98** (i.e. at the input of the main storage memory or static shift register **94**) in ϕ_4 time, i.e. immediately after completion of an $X_1X_2X_3$ clocking sequence. The second variation is when the system includes an insert overflow feature to be described hereinafter. If **199** cells of the available **200** in the main register **94** are filled with stored characters, a potential insert overflow situation arises. Accordingly, any further insertions are made with the buffer memory **52** clocking order reverting to the $X_1X_3X_2$ sequence, when a blank cell is detected at the output of the main storage memory or static shift register **94** immediately after completion of an $X_1X_2X_3$ clocking sequence. A second blank cell detector, similar to gate **92,** is connected to the output lines of the main storage memory or static shift register **94.**

Delete Mode

This mode can be utilized only when the machine has been set for Draft Mode Operation. Deletion of a character is accomplished by a **201** shift cycle, initially in the normal $X_1X_3X_2$ clocking sequence but switching to the $X_1X_2X_3$ sequence when a blank cell is first detected at the output of the second subsidiary register **98** in ϕ_4 time. Deletion of a group of characters is achieved by repetitive cycles of **201** shifts.

Skip Mode:

This mode can be used only when the system has been set for Final Mode operation. It involves single shifts with the $X_1X_3X_2$ clocking sequence. The behavior of the system is the same as when printing out from the buffer memory **52,** except that the printer **20** is prevented from typing out the skipped character.

Clearing Buffer:

This mode involves a **200** shift cycle and may be conducted according to either clocking sequence. Preferably, however, it is conducted with the $X_1X_3X_2$ clocking sequence.

Examining the Buffer Memory Contents for Any Purpose:

This mode involves a **200** shift cycle and may be conducted in the $X_1X_3X_2$ clocking sequence.

The effect of the clocking sequence on the buffer memory **52** will now be described. In the normal $X_1X_3X_2$ clocking sequence, the first subsidiary register **96** is clocked first (ϕ_1 time) to store the data signals appearing at the output of the main storage memory or static shift register **94,** i.e. it assumes the state of the last cell of the main storage memory or static shift register **94.** Then the second subsidiary register **98** is clocked (ϕ_2 time) so that it will assume the state of the first subsidiary register **96.** When this occurs the second subsidiary register **98** will have steady state output signals indicative of its new state and these output signals appear at the inputs of OR gates **84–91.** Next the main register **94** is clocked (ϕ_3 time) so that its contents will undergo a single shift to the right (forward) and its first cell will assume the state of the signals appearing at the input terminals of OR gates **84–91.** However, if a C_3 reset signal is applied to clear line **100** at the time that the second subsidiary register **98** is clocked (or afterward) and before the main storage memory or static shift register **94** is clocked, the first cell of the main storage memory or static shift register **94** will assume a clear state when the main storage memory or static shift register **94** is clocked by the X_2 clock pulse. If however OR gates **84-92** have inputs from the keyboard **23** or other sources, then when clocked by the X_2 clock pulse the first cell assumes a state determined by such inputs. This procedure of using an $X_1X_3X_2$ clocking sequence accompanied by a C_3 reset signal is called the "non-circulate mode" and is used when entering characters from the keyboard **23.** The procedure of using the $X_1X_3X_2$ clocking sequence without a C_3 reset signal is called the "normal circulate mode" and is used when it is desired merely to circulate data from one end to the other of the main storage memory or static shift register **94.**

In the $X_1X_2X_3$ sequence, the first subsidiary register **94** again assumes the state of the last cell in the main storage memory or static shift register **94** when the X_1 clock pulse occurs. Then the main storage memory or static shift register **94** is clocked to execute a single step shift. When this occurs the first cell of the main storage memory or static shift register **94** assumes the state of the second subsidiary register **98.** Next the second subsidiary register **98** is clocked to store the signals appearing at the output of the first subsidiary register **96.** As just described, this $X_1X_2X_3$ clocking sequence permits circulation of data from one end to the other of the main storage memory or static shift register **94.** If a C_3 reset signal is applied to the second subsidiary register **98** before the main storage memory or static shift register **94** is clocked (ϕ_2 time), the first cell of the main storage memory or static shift register **94** will not be able to assume the state of the second subsidiary register **98** when it shifts, and thus will be blank or will assume a state determined by whatever other signals are present at the inputs of OR gates **84-91.** However, when the second subsidiary register **98** is clocked at ϕ_3 time, it will assume the state of the first subsidiary register **96.** This procedure of using an $X_1X_2X_3$ clocking sequence is called the "enhanced circulation mode" since its net result is to increase the buffer memory capacity by one character. More explicitly, it permits circulation of a group of stored characters without loss while permitting a new character to be inserted into that group. Essentially this enhanced circulation mode delays transfer of a character from the output of the

main storage memory or static shift register **94** back to the input of the main storage memory or static shift register **94** so as to permit a character to be inserted from the keyboard **23** during an insert cycle. In other words, it serves to increase temporarily the effective size of the main register **94** by a single character. It also permits a character to be deleted during a delete cycle, as explained hereinafter.

FIG. **6** illustrates the four-phase clock pulse generator and the associated logic circuit for changing the clocking order. FIG. **6** and other logic diagrams hereinafter will be described in terms of positive logic for clarity in exposition, but it is to be understood that negative logic can also be used. Essentially the four phase clock pulse generator is a self-correcting twisted ring counter comprising four JK master-slave flip-flops **102, 104, 106** and **108** interconnected so that the Q and $\overline{Q}$ output terminals of flip-flop **102** are connected to the K and J terminals of flip-flop **104,** while the Q and $\overline{Q}$ terminals of flip-flop **104** are connected to the J and K terminals of flip-flop **106** and the Q and $\overline{Q}$ terminals of the latter are connected to the J and K terminals of flip-flop **108.** The Q terminal of flip-flop **102** and the Q terminals of flip-flops **104** and **106** are connected to the input terminal of AND gate **112** whose output terminal is coupled directly to the K terminal of flip-flop **102** and also to the input of inverter **114.** The output of inverter **114** is applied to the J terminal of flip-flop **102.** The clock pulse generator also includes clock **116** whose output is applied e.g. at 455 KHz, on line **120** to one input terminal of AND gate **122.** The latter is enabled by an enable generator signal that is applied to AND gate **122** on line **124.** This enable generator signal also is applied on line **126** to the clear terminals of flip-flops **102** and **108** inclusive. The output terminal of AND gate **122** is connected to the clocking input terminal C of all four flip-flops **102** to **108** inclusive. As hereinafter described, the four flip-flops **102–108** operate sequentially to produce corresponding output clock signals denoted ϕ_1, ϕ_2, ϕ_3 and ϕ_4. These latter signals are derived from the $\overline{Q}$ terminal of flip-flop **102** and the respective Q terminal of each of flip-flops **104, 106** and **108** and are applied to the input terminals of four AND gates **128, 130, 132** and **134.** These latter AND gates **128-134** have second input terminals that are each connected to the output terminal of AND gate **122.** The Q terminal of flip-flop **108** is connected, as will be shown later, to control the duration of the enable generator signal so that the four phase clock pulse generator can operate for **1, 199, 200** or **201** cycles of tetrads as required.

Typically, the clock signals from clock **116** and enable generator signals on line **124** are positive pulses. The leading edge of the enable generator signal is immediately preceded by the trailing edge of a clock pulse.

Assume for purposes of discussion that AND gate **122** is enabled with an enable generator signal so that the AND gate **122** will pass clock pulses from clock **116.** The enable generator signal appearing also on line **126** will enable the four flip-flops **102** to **108** to be clocked. As a consequence, the output of AND gate **112** will initially be low, so that the J and K terminals of flip-flop **102** will be high and low respectively. At the same time the J and K terminals of flip-flop **104** will be high and low respectively while the J and K terminals of each of flip-flops **106** and **108** will be low and high respectively. The first flip-flop clocking pulse produced by AND gate **122** will cause the Q and $\overline{Q}$ terminals of flip-flops **102** and **104** to go high and low respectively but will not cause any change in the signal level appearing at the $\overline{Q}$ terminals of flip-flops **106** and **108.** The second or next flip-flop clocking pulse will cause the $\overline{Q}$ terminals of flip-flops **104** and **106** to go high and low respectively but will not cause any change in the signal level appearing at the Q and $\overline{Q}$ terminals of flip-flops **102** and **108** respectively. On the third flip-flop clocking pulse, the $\overline{Q}$ terminals of flip-flops **106** and **108** will become high and low respectively while no change in signal level will occur at the Q and $\overline{Q}$ terminals of flip-flops **102** and **104.** The fourth flip-flop clocking pulse will cause the signals appearing at the Q and $\overline{Q}$ terminals of flip-flops **102** and **108** to go low and high respectively, while the signal levels at the $\overline{Q}$ terminal of flip-flops **104** and **106** remain unchanged. At this point the four flip-flops **102–108** are in the same state as when held clear by the absence of the enable generator signal appearing on line **126.** A fifth flip-flop clocking pulse will cause the signals appearing at the Q and $\overline{Q}$ terminals of flip-flops **102** and **104** to change as on the first clocking pulse, while leaving the output at the $\overline{Q}$ terminals of flip-flops **106** and **108** unchanged. At the end of this fifth clocking pulse, the four flip-flops **102–108** have the same states as after the first clock pulse. The next three flip-flop clocking pulses will cause the flip-flops **102–108** to assume successively the same states produced by the second, third and fourth clocking pulses. This mode will continue to be repeated so long as clocking pulses are applied to the four flip-flops **102–108.**

As previously noted, the clock signal from AND gate **122** is applied to AND gates **128** to **134** inclusive. The timing arrangement is such that (a) when the first clock signal arrives at AND gates **128** to **134,** the $\overline{Q}$ terminal of flip-flop **102** is high and the $\overline{Q}$ terminals of flip-flops **104, 106** and **108** are low, with the result that only AND gate **128** produces an output pulse; (b) when the next clock signal arrives at AND gates **128** to **134,** the $\overline{Q}$ terminal of flip-flop **102** and the Q terminals of flip-flops **106** and **108** are low and the Q terminal of flip-flop **102** is high so that only AND gate **130** produces an output pulse; (c) on the third clock signal, the Q terminal of flip-flop **106** is high and the $\overline{Q}$ terminal of flip-flop **102** and the Q terminals of flip-flops **104** and **108** are low, so that only AND gate **132** produces an output pulse; (d) on the fourth clock signal, the $\overline{Q}$ terminal of flip-flop **102** and the Q terminal of flip-flops **102** and **106** are low while the Q terminal of flip-flop **108** is high, so that only AND gate **134** produces an output signal; and (e) on the fifth clock signal the Q terminal of flip-flop **102** is high and the Q terminals of flip-flops **104, 106** and **108** are low so that only AND gate **128** produces an output signal. The next three clock pulses will cause AND gates **130, 132** and **134** to pass pulses sequentially as occurred on the second, third and fourth clock pulses. Essentially flip-flops **102** to **108** inclusive act as a commutator so that pulses are passed sequentially by AND gates **128** to **134** inclusive repetitively as long as these AND gates **128–134** are enabled and clock **116** operates. The sequential outputs from AND gates **128, 130 132** and **134** identified as ϕ_1, ϕ_2, ϕ_3 and ϕ_4 respectively obviously will occur at the same repetition rate as the clock pulses. Resetting of the flip-flops **102–108** by the absence of an enable generator

signal on line **126** assures that the flip-flops **102–108** will always be in the correct state when the clock pulse generator is required to produce one or more tetrads of $\phi_1 - \phi_4$ clocking pulses.

The enable generator signal is provided by another portion of the circuit shown in FIG. **6.** This latter portion of the circuit comprises four JK flip-flops **136, 138,** 140 and **142** whose reset terminals are all connected to input terminal **143** at which a negative reset signal is applied when the machine is turned on. Each J terminal of flip-flops **136** to **142** is connected to a respective corresponding input terminal **144, 145, 146** and **147** at which are applied different signals identified as 1 shift, **199** Shift, **200** Shift, and **201** Shift respectively. The C or clocking terminals of all four flip-flops **136-142** are connected by common line **148** to the output of clock **116.** The Q terminals of all of flip-flops **136, 138, 140** and **142** are connected to separate input terminals of OR gate **150** whose output is connected by line **124** to input AND gate **122** of the 4-phase clock pulse generator. The K terminal of flip-flop **136** is connected by line **152** from the Q terminal of the fourth flip-flop **108** of the 4-phase clock pulse generator, and is also connected to one input terminal of AND gate **154.** The latter has a second input terminal to which is applied, by line **156,** a Terminate Shift signal or pulse derived from counter **190** of the circuit hereinafter described for counting the number of times the buffer memory **52** shifts or is clocked. The output of AND gate **154** is applied to the K terminals of flip-flops **138, 140** and **142.**

Operation of the above described circuit for controlling the clock generator control signal will now be described. The 1 Shift, **199** Shift, **200** Shift, and **201** Shift signals are positive pulses which are respectively and selectively applied to the corresponding J input of flip-flops **136, 138, 140** and **142** coincidentally with a clock pulse on line **148.** The four flip-flops **136** to **142** are cleared by the reset signal at terminal **143** and are clocked by the pulses on line **148.** In the cleared condition the Q terminals of the four flip-flops **136–142** are all low. Assuming that one of the flip-flops **136–142** has a shift signal applied to its J terminal, when a clock pulse is applied on common line **148** the one flip-flop **136–142** will change states so that its Q terminal goes high. Because of other logic in the system only one shift signal can be present at any one time. Thus only one flip-flop **136–142** can change state when a clock pulse occurs. For example, if the **1** Shift signal is present, the Q terminal of flip-flop **136** will go high and the corresponding Q terminals of the other three flip-flops **138–142** will remain low. Assuming for purposes of discussion that the **199** Shift signal is applied at terminal **145,** OR gate **150** will have one high and three low inputs; accordingly its output will be a generator enable signal which will cause the clock pulse generator to produce tetrads of $\phi_1 - \phi_4$ timing pulses as above described. The generator enable signal will continue until coincidence of the terminate shift signal on line **156** and of the input signal on line **152** applied through AND gate **154** cause the K terminal of flip-flop **138** to go high whereupon the Q terminal of that flip-flop **138** will go low on the next clock pulse on line **148.** With all four inputs to OR gate **150** then low, the latter will now produce a low output, thus terminating the enable generator pulse on line **126.**

Similarly, it will be seen that the application of any of the shift signals to its corresponding flip-flop **136–142** will initiate a generator enable signal at the output of OR gate **150,** and that the 4-phase clock pulse generator will continue to run until the generator enable signal terminates due to coincidence of signals on lines **152** and **156.**

FIG. **6** also includes the logic for changing the clocking order of the buffer memory **52** which logic comprises JK flip-flop **158** whose J terminal is connected to the output of OR gate **159** from which is provided a Change Order signal hereinafter described. The C or clocking terminal of flip-flop **158** is connected to the output terminal of AND gate **134.** The reset terminal of flip-flop **158** is connected to a line **160** on which may be applied a reset signal from the Q output terminal of flip-flop **142.** The Q terminal of flip-flop **158** is connected to one input terminal of an exclusive OR gate **162.** Exclusive OR gate **162** has a second input terminal which is connected to the output of OR gate **162** which provides an Insert signal derived as hereinafter described. The output terminal of exclusive OR gate **162** is connected through inverter **164** to input terminals of two AND gates **165** and **166.** The output terminal of exclusive OR gate **162** is also connected to input terminals of two more AND gates **167** and **168.** A second input terminals of each of AND gates **165** and **168** are connected to the output terminal of AND gate **130,** while the second input terminals of each of AND gates **166** and **167** are connected to the output terminal of AND gate **132.** The output terminals of AND gates **134** and **128** are simply connected respectively to output terminal **169** and **170.** The output terminals of AND gates **165** and **167** are connected to respective input terminals of OR gate **172** and the output terminals of AND gates **166** and **168** are connected to different input terminals of OR gate **174.** The output terminals of OR gates **172** and **174** are connected to output lines **176** and **178** respectively.

OR gate **163** has a pair of input terminals respectively connected to terminals **182** and **187** to which are applied respectively an Overflow Insert Cycle signal and a Normal Insert Cycle signal.

OR gate **159** has a pair of inputs respectively connected to the outputs of AND gates **180** and **181.** AND gate **180** has a pair of inputs connected to terminals **182** and **183.** Terminal **183** is intended to have applied thereto a Blank Cell Detected at Main Buffer Output signal. The latter signal typically is derived from gating which is preferably connected to the output of main storage memory or static shift register **94** of FIG. **5.** AND gate **181** has a pair of input terminals one of which is connected to input terminal **184** at which may appear a Blank Cell at Buffer Input signal from gate **92** shown in FIG. **5.** The other input terminal of AND gate **181** is connected to the output of OR gate **185** which also has two input terminals **186** and **187.** Terminal **186** has applied thereto respectively a Delete Cycle Signal.

Operation of the logic circuit for changing the clocking order of the buffer memory **52** will now be described. The Change Order signal applied to the J terminal of flip-flop **158** will occur by operation of gates **159, 180, 181** and **185** whenever (1) a blank cell is detected at the output of the second subsidiary storage register **98** of the buffer memory **52** and the machine is ordered to insert a character into the buffer memory **52** without an overflow, or to delete a character, or (2) a blank cell is detected at the output of the main storage memory or static shift register **94** and the machine

is ordered to insert with overflow a character into the buffer memory **52.** The Insert signal applied to one of the inputs of exclusive OR gate **162** will occur, by operation of OR gate **163** whenever the machine is ordered to insert a character into the buffer memory **52,** with or without overflow. According to the logical operation of exclusive OR gate **162,** the latter will provide a high output when either input signal is high but not when both input signals are simultaneously high or simultaneously low.

Flip-flop **158** is clocked by the ϕ_4 output signal from AND gate **134.** If a Change Order Signal is present on the J terminal of flip-flop **158** when the ϕ_4 signal occurs, the Q terminal of that flip-flop **158** will go high. If a high Insert signal from OR gate **163** is applied to exclusive OR gate **162,** the latter will provide an output signal only when the Q terminal of flip-flop **158** is low. As noted, a Change Order Signal can occur only during an Insert Cycle or a Delete cycle in accordance with the buffer memory Insert and Delete Clocking modes previously described.

If the output of exclusive OR gate **162** is high, it enables AND gates **167** and **168;** if it is low, it enables AND gates **165** and **166.** Accordingly, if for example it is ϕ_2 time and the output of exclusive OR gate **162** is high, AND gate **168** will pass the ϕ_2 signal to OR gate **174.** Since at that time both inputs of AND gate **166** are low, the other input to OR gate **174** will be low, the ϕ_2 signal will appear on line **178.** At the same time the output of AND gates **167** and **165** will also be low because ϕ_3 is a low input to AND gate **167** and the output of inverter **164** is a low input to AND gate **165.** Accordingly, the output of OR gate **172** will also be low. If now the output of exclusive OR gate **162** goes low, the ϕ_2 signal will appear instead at the output of OR gate **172** and the other OR gate **174** will have a logical zero at its output. It is to be noted that lines **170, 178,** 176, 169 are connected to terminals identified as X_1, X_2, X_3, and ϕ_4. The signals appearing at terminals X_1, X_2, and X_3 are the clocking signals for the buffer memory **52.** Hence the buffer memory **52** will be clocked in the $X_1X_3X_2$ mode if the output of exclusive OR gate **162** is low and in the $X_1X_2X_3$ mode if the output of exclusive OR gate **162** is high. That is, the ϕ_2 and ϕ_3 signals appear at the X_3 and X_2 terminals only when both the Insert signals and Change Order signal are either present together or absent together, and the ϕ_2 and ϕ_3 signals appear respectively at the X_2 and X_3 terminals only when one of the Insert and Change Order signals is present and the other absent. In essence, the gating scheme of gates **162, 165, 166, 167, 168, 172** and **174** together with inverter **164** is the equivalent of a double-pole, double-throw switch automatically actuated by a set of circumstances.

The circuit of FIG. **6** includes means for counting the number of times the buffer memory **52** is clocked, and to this end the circuit of FIG. **6** includes a counter **190** for generating an output signal after counting **200** pulses, and input logic for adding or deleting a pulse as will be hereinafter explained. The logic here includes OR gate **192** having a pair of input terminals connected to the Q terminals of flip-flops **138** and **140.** The output of OR gate **192** is connected to an input of OR gate **194** and also to an input of OR gate **195.** The Q terminal of flip-flop **142** is connected to the other input of OR gate **194.** A three-input AND gate **196** has two of its inputs connected respectively to the output of AND gate **128** and the Q terminal of flip-flop **138.** Another J-K flip-flop **198** is provided, having its J and $\overline{Q}$ terminals tied together and connected to the third input of AND gate **196.** Flip-flop **198** has its clock terminal connected to the output of AND gate **132** so as to be clocked by the ϕ_3 pulses from the latter. The clear terminal of flip-flop **198** is connected to the output of OR gate **194.**

The Q terminal of flip-flop **198** and the Q terminal of flip-flop **142** are connected as inputs to AND gate **199.** The output of AND gate **199** is connected as an input to OR gate **195.** The output of OR gate **195** and the output of AND gate **130** are connected as inputs to AND gate **200.** The outputs of AND gate **200** and of AND gate **196** are connected as inputs to OR gate **202** and the output of the latter is connected as the count input to counter **190.** Counter **190** is preferably any of a large number of digital counters well known in the art having a clear terminal at which application of a low signal will reset or clear the counter **190** to its initial state, and, in a preferred embodiment will provide an output signal when it has counted two hundred input pulses. The clear terminal of counter **190** is connected also to the output of OR gate **194.** The output terminal of counter **190** is connected as the terminate shift line input to AND gate **154** and to terminate shift terminal **193.**

In operation, it will be seen that when the signal from OR gate **194** goes high, it serves to enable both flip-flop **198** and counter **190** so that both can be clocked. This will occur when according to OR gates **192** and **194** any of the **199** shift, **200** shift or **201** shift signals are applied to the J terminals of flip-flops **138, 140** and **142** respectively. Counter **190** will count ϕ_2 pulses passed by gates **200** and **202** when AND gate **200** is enabled. And gate **200** is enabled immediately if the Q terminal of either of flip-flops **138** and **140** goes high. However, AND gate **196** when enabled provides an alternative pulse source, being connected to AND gate **128** which provides ϕ_1 pulses. This enablement only occurs when flip-flop **198** is off, i.e. its $\overline{Q}$ terminal is high and when the **199** shift signal has turned flip-flop **138** on, i.e. its Q terminal is high. But, if the $\overline{Q}$ terminal of flip-flop **198** is high because it is connected to the J terminal, when a ϕ_3 clock pulse clocks flip-flop **198,** the latter turns on and its $\overline{Q}$ terminal goes low. This operation thus provides a single pulse to counter **190** prior to any counting of ϕ_2 pulses by the latter. Because AND gate **200** is enabled by the output of flip-flop **138** counter **190** will then count ϕ_2 pulses. When the counter **190** has counted a single ϕ_1 pulse and **199** ϕ_2 pulses, it yields a terminate shift signal on line **156.** Effectively then it has counted only **199** shifts in the butter memory **52.**

When the Q terminal of flip-flop **142** goes high due to the **201** shift signal, flip-flop **158,** flip-flop **198** and counter **190** are enabled and the first ϕ_2 pulse is not counted by counter **190** because AND gate **200** is disabled by the absence of a high signal at the output of OR gate **195.** However the first ϕ_3 pulse clocks flip-flop **198** so that its Q terminal goes high, AND gate **199** is enabled and AND OR gate **195** passes the signal from OR gate **195** to enable AND gate **200.** Counter **190** then counts the next 200 ϕ_2 pulses and yields the output signal on line **156.** Effectively however, because it was forced to skip counting an initial ϕ_2 pulse, the counter **190** has counted through **201** shifts of the buffer memory **52.**

Obviously when flip-flop **140** is triggered, counter **190** will simply count up to the full 200 shifts and then will provide a Terminate Shift signal on line **156** to AND gate **154.**

Lastly, the remainder of FIG. **6** includes logic for generating the C_3 signal which is to be applied to line **100** (FIG. **5**) and also for generating the Enable Keyboard to Storage signal which is to be applied to line **82** (FIG. **4**). To this end, the circuit of FIG. **6** includes NOR gate **204** having one input connected to the output from OR gate **163,** and another input connected to terminal **186.** The output of NOR gate **204** is connected as one input to OR gate **205.** Another input to OR gate **205** is connected to the output of AND gate **128.**

Yet another OR gate **206** is provided, having one input connected to the Q output terminal of flip-flop **142** and another input connected to terminal **207.** The output of OR gate **206** is connected to the one input of AND gate **208.** A second input to AND gate **208** is connected to the $\overline{Q}$ terminal of flip-flop **198.** The output of AND gate **208** is shown connected to line **82,** inasmuch as the signal from AND gate **208** is the desired Enable Keyboard to Storage signal. The output of OR gate **205** and line **82** are also connected as respective inputs to AND gate **209.** The output of the latter is shown as line **100** along which the requisite C_3 signal can be provided.

AND gate **209** and OR gate **205** define the length of the C_3 pulse. As indicated, a relatively long C_3 pulse is used when overwriting a character in the buffer memory **52** and a relatively short C_3 pulse is employed when inserting or deleting a character. If the output of NOR gate **204** is low, the only high input signal to OR gate **205** will be the ϕ_1 pulse from AND gate **128** so the output signal from OR gate **205** will be quite short. The output of NOR gate **204** will be low if there is an insert or delete signal present at any of terminals **182, 186** or **187.** The output from OR gate **205** will then enable AND gate **209** only for the duration of the ϕ_1 pulse.

On the other hand, if the system is not in a Delete or Insert mode, the output from OR gate **205** will stay high and the duration of any high output from AND gate **209** will depend on the output from AND gate **208.** OR gate **206** will provide a high output where the buffer memory **52** is undergoing a **201** shift (i.e. the Q output from flip-flop **142** is high) or where an appropriate signal is present at terminal **207.** AND gate **208** will be enabled by the "off" condition of flip-flop **198** wherein the $\overline{Q}$ output of the latter is high. It will be remembered that the $\overline{Q}$ output goes low after the ϕ_3 pulse from AND gate **132** clocks flip-flop **198,** so that AND gate **208** is enabled for the time from the beginning of a ϕ_1 pulse (or when flip-flop **198** is enabled) to the end of the following ϕ_3 pulse. This "long" output pulse from AND gate **208** is applied on line **82** to provide the Enable Keyboard to Storage Signal described in conjunction with FIG. **4,** and is also applied to AND gate **209.**

When the output pulse from OR gate **205** is the "short" pulse, the output from AND gate **209** will be similarly short. When there are no insert or delete commands to NOR gate **204,** the output from OR gate **205** will be long, hence the C_3 output pulse from AND gate **209** will then also be long.

A Carrier Return signal provided from the baseplate **24** will ordinarily cause the buffer memory **52** to empty into magnetic storage through repetitive one-shift cycles as heretofore noted. The emptying process for a completely full **200** character buffer memory **52** requires about the amount of time needed for the print head **16** on the printer **20** to return from a typical right margin position to a typical left margin position. However, if the data stored in the buffer memory **52** is only a portion of a line, the print head **16** would be expected to return to its left margin position well before the entire buffer memory **52** could be emptied of meaningful and blank or empty characters. Hence, the invention includes means for making the buffer memory **52** available for input thereto of new data immediately after the meaningful data has been transferred out.

Thus, as shown in FIG. **7** the invention includes means for transferring the contents of the buffer memory **52** into magnetic storage and for releasing the buffer memory **52** to further entry therein immediately following transfer of the meaningful contents into magnetic storage. The foregoing means preferably comprises multiplexer **210** (shown earlier at block **54** in FIG. **3**) having a plurality of parallel inputs respectively connected to the eight output lines of shift register **94** (FIG. **5**). Multiplexer **210** is an eight-input channel digital multiplexer well known in the art for coverting eight parallel input bits to a serial chain on a single output channel.

A decade counter **212** is provided for counting pulses in modulo ten and having an input terminal connected to a source of timing pulses (such as divider **264** which in turn has an input from line **211** to clock **116** (FIG. **6**)). Counter **212** is of the type having an inverting disable terminal **213** so that an appropriate signal at terminal **213** will hold the counter **212** to an initial state, usually zero or nine. Counter **212** typically is an arrangement of interconnected bistable stages such as flip-flops having output lines **214, 215, 216** and **217,** as from the Q terminals of the flip-flops, for providing signals corresponding to counts of **1, 2, 4** and **8.** Only the first three output lines **214, 215** and **216** from counter **212** need be connected to multiplexer **210** in known manner for controlling the sequencing of the signals on the input lines from register **94** into a serial signal at the multiplexer output. In order, for reasons adduced hereinafter, to determine each time a count of **8** is reached by counter **212,** a "state **8**" detector is provided and comprises AND gate **218** having one input connected to the count of **8** line **217** and another input connected through inverter **219** to the count of **1** line **214.**

Means, such as AND gate **220,** is provided for determining if a blank cell is present at the output of the buffer memory **52** or register **94.** AND gate **220** as shown, has eight inverting inputs respectively connected to the eight output lines from register **94.**

It is preferred to phase encode the output of the multiplexer **210** and to this end there is provided a control flip-flop **222** which is preferably a J-K type device having its clock input connected by line **223** to the output of AND gate **134** (FIG. **6**), its J input connected to the output of blank cell detector or AND gate **220,** and its K input grounded. The $\overline{Q}$ output of flip-flop **222** is connected as one input to AND gate **224.** The other input of AND gate **224** is connected to the output of multiplexer **210.** The outputs of AND gate **224** and clock line **221** from divider **264** are connected as inputs to exclusive OR gate **226.**

The output of exclusive OR gate **226** is connected as one input to AND gate **228.** Another input to AND

gate 228 is connected through inverter 229 to line 217 from counter 212. Counter output lines 214, 217 and clock line 221 are connected as inputs to AND gate 232. The outputs of the latter and from AND gate 228 are connected as respective inputs to OR gate 234. The output from the latter is connected through amplifier 236 to magnetic read/write head 238.

The system shown in FIG. 7 as thus described, functions as follows: A Carrier Return signal starts a series of one shifts in the buffer memory 52, until the bits representing the first character of a line are shifted to the eight output lines of the multiplexer 210 which converts the eight parallel bits to eight serial bits in sequence and with a timing determined by the output from decade counter 212. The latter starts counting clock pulses on line 221 from a count of nine as soon as an enable write signal at terminal 213 enables the counter 212.

From the zero to seventh count by decade counter 212, the eight input lines are sequenced to provide a serial input to AND gate 224. Because in the absence of a high signal at the J input to flip-flop 222, the Q terminal of the latter is high, AND gate 224 is enabled to pass the serial bits of each character thus multiplexed. Exclusive OR gate 226, clocked by the signals on line 221 converts the output of multiplexer 210 into Ferranti coded signals wherein the value of a bit is indicated by its transition direction as explained hereinafter. When counter 212 provides the eighth and ninth counts by high signals on line 217 and line 214, no corresponding bits are provided at that time by the encoding logic. Instead, on the eighth count, the high signal on line 217, being inverted by inverter 229, disables AND gate 228. On the ninth count, the high signals on lines 214 and 217 together with the clock pulse on line 211 enable AND gate 232 which provides a regular pulse or bit to OR gate 234. Thus the eighth and ninth counts by decade counter 212 yield respectively no signal at all and one regular clock pulse at the input to amplifier 236. The eighth count space or lack of signal (hereinafter referred to as an inter-character gap or ICG) is intended to provide spacing between serially recorded sets of character bits, whilst the ninth count pulse is intended to indicate the beginning of a character and is hereinafter referred to as the start bit. The output of amplifier 236 is applied to read/write head 238 so that as a magnetic storage medium such as a tape 18 in cassette 240 is transported past head 238 as by tapetransport motor 242, the serial phase-encoded characters, the ICG and the start bit are all recorded on the tape 18.

The output from AND gate 218 is applied as hereinafter described to cause the buffer memory 52 to execute another one shift. The foregoing will continue until a blank cell (which as noted in Table III is characterized as a sequence of eight zero bits) appears at the output of register 94. The blank cell will be detected by AND gate 220 which causes the J terminal of flip-flop 222 to go high and the $\overline{Q}$ terminal to go low. Thus, as soon as the meaningful data in register 94 has been transferred, the output of flip-flop 222 disables AND gate 224, effectively freeing the register 94, i.e. making it available for further entry of data from encoder gates 76.

The output of AND gate 218 is also preferably connected as through another input to OR gate 202, to counter 190 (FIG. 6) so that each character written on tape 18 is counted by counter 190. At the 200th count of 8, as recorded by counter 190, the latter will provide a signal on line 156 which resets the Enable Write line 244.

As noted below, the same signal, directed along Enable write line 244, serves to stop motor 242. Enable Write line 244 is also connected to terminal 213 of counter 212 and to the clear terminal of flip-flop 222 to stop or disable counter 212 and to clear flip-flop 222 so that AND gate 224 is no longer disabled.

In the event, however that for example register 94 only had ten characters recorded therein, upon depression of the Carrier Return key by the operator, the print head 16 would quickly return to its left hand margin position. By the time the print head 16 so returned, AND gate 220 would have detected the blank cell on the eleventh shift and inasmuch as register 94 would then have been cleared, AND gate 224 would have been disabled. However, counter 190 would only have counted eleven pulses, hence decade counter 212 would continue to operate and clock pulses along line 221 would be phase encoded by exclusive OR gate 226 as simply all zero bits. Of course, every eighth and ninth count would be recorded as proper ICG and start bits by operation of gates 232, 228 and 234. In this manner, null characters or sequences of eight zero bits will continue to be generated and recorded, until counter 190 reaches the count of two hundred, whereupon counter 212 and motor 242 will become disabled and the zero character generation and recording ceases.

The recording or data storage system 58 exemplified by motor 242, read/write head 238 and cassette 240, is preferably a dual capstan, bidirectional machine with a read and write tape speed typically of 10 inches per second. Such recording system, well known in the art, is capable of driving a tape 18 in a cassette 240 at its writing and reading speed and also at some higher rate of speed for search purposes. Read/write head 238 is preferably a known two-track digital type as heretofore noted.

The data are recorded on tape 18 in blocks 19 of 200 characters each block 19 corresponding then to a complete buffer load, each character, as noted before, having eight bits corresponding to the bits of a character stored in the main register 94, an additional start bit and an ICG. These bits are Ferranti or phase-encoded which is a known system of encoding wherein the first half of each bit is recorded as the true sense of the bit (i.e. either a high or low level) and the second half is recorded as the bit complement. Thus, as noted, the direction of the transition from first to second half identifies the bit.

An example of a character which might appear at the output of register 94 is shown in FIG. 8A wherein the sequence of signals as shown is S, R_1, R_2, R_2A, R_5, T_1, T_2 and P. The foregoing signals then form a character with the sequence of bits 11010010. It is recognized that this character has even parity but is merely used in this description for the sake of simplicity. A sequence of clock pulses, shown in FIG. 8B, synchronize the operation of multiplexer 210 and exclusive OR gate 226 to produce the phase encoded signals shown in FIG. 8C. It should be noted in FIG. 8C that in accordance with the logical exclusive OR function of exclusive OR gate 226, the signal is high if and only if either the signal in FIG. 8A is high or the signal in FIG. 8B is high but not when both the signals in FIG. 8A and FIG. 8B

are high. It will also be recognized as noted that the first transition of the signal in FIG. 8C constitutes a "start" bit or transition and, corresponding to the last "bit" of the signal is a low level or ICG.

As shown in FIG. 3 and FIG. 7 the system also includes read data circuits **60** for reading the phase-encoded data from tape **18** and for converting or demultiplexing in demultiplexer **62** the decoded data back into eight parallel bit characters suitable for insertion into the buffer memory **52** for ultimate writing out by the printer **20** or for editing or revision. The remainder of the circuit of FIG. 7 thus includes read amplifier **246** connected to the output from read/write head **238.** The output of amplifier **246** is connected to means such as rectifier/shaper **248** for half-wave rectifying the signal from amplifier **246** to provide an output train of, for example, positive rectangular pulses representing only the positive signal in the output of amplifier **246.** Similarly the output of amplifier **246** is connected through inverting amplifier **249** to means, such as rectifier/-shaper **250** for half-wave rectifying the signal from amplifier **246** to provide another output train, of, for example, positive rectangular pulses which however represent only the negative signals in the output of amplifier **246.** The output of rectifier/shaper **248** is connected as one input to AND gate **252,** as one input also to OR gate **254** and is connected to the set (S) terminal of RS type flip-flop called Control flip-flop **256.** Similarly the output of rectifier/shaper **250** is connected as one input to AND gate **258** and also as another input to OR gate **254.** The output of AND gates **252** and **258** respectively are connected to the set (S) and reset (R) inputs of another RS type flip-flop called data flip-flop **260.** The $\overline{Q}$ output terminal of data flip-flop **260** is connected to the data input terminal of demultiplexer **62** which is shown preferably as an eight-bit shift register demultiplexer **262.**

Means are provided for clocking the decoding of the signals from head **238,** and to this end clock line **211** is connected to digital scaler or divider **264** which has an output pulse train which is a sub-multiple of the input clock frequency. An output of digital divider **264** (at a frequency four times greater than is provided to counter **212**) is connected to counter **265,** which is typically a simple binary counter formed of three cascaded flip-flop stages. The three outputs from counter **265,** typically the Q terminals of the respective flip-flop stages, are connected as inputs to a binary-to-octal converter **266.** The latter is a known system of gates which simply converts the binary output of counter **265** (which runs from zero to 7) to individual signals appearing in eight output lines each representing respectively the zero to seventh count or state of counter **265.** Thus, for example, the first output line from converter **266** will be high if and only if the counter **265** has counted a first input pulse and has not counted the next pulse. The zero, third and fourth state output lines from converter **266** are all connected as inputs to OR gate **267.** The output of the latter in turn is connected to input terminals of AND gates **252** and **258.** The second state or count output line of converter **266** is connected to the clocking input terminal of shift register demultiplexer **262.** The fifth state or count line from converter **266** is connected to output line **268** and also as one input to AND gate **269.** Clock line **211** is also connected as input to AND gate **269.** The output of AND gate **269** is connected to the reset (R) terminal of control flip-flop **256.**

The output of OR gate **254** is connected to the input of a monostable multivibrator **270,** the enable input terminal of multivibrator **270** being connected to the output of OR gate **267.** The output of monostable multivibrator **270** is connected through inverter **271** as one input terminal to AND gate **272.** The Q terminal of flip-flop **256** is connected as the other input to AND gate **272.** The output of AND gate **272** is connected to the clear input terminal of counter **265** and to an input of OR gate **273.** Another input to OR gate **273** is connected to Enable write line **244.** The output of OR gate **273** is connected to the clear input terminal of divider **264.** Lastly, there is provided an Enable Read line **274** over which an enabling signal can be propagated to initiate reading and phase decoding a record. Enable Read line **274** is connected through OR gate **276** to control the starting of motor **242.** Similarly, Enable Write line **244** is connected to motor **242** through OR gate **276.**

In operation of the phase decoding portion of FIG. 7, reference should be had also to the timing diagram of FIG. 8. When it is desired to read data which has been stored in the tape **18** in cassette **240,** an Enable Read signal on Enable Read line **274** starts motor **242** so that the tape **18** in cassette **240** is moved past read/write head **238.** This produces a bipolar output shown typically at FIG. 8D, where each pulse or peak represents the location and sense of a transition in the phase-encoded signal stored on tape **18** and shown in FIG. 8C.

The read/write head output is amplified in amplifier **246** and is rectified and shaped by rectifier/shaper **248** to produce a train, typically of positive, shaped output pulses, as shown in FIG. 8E. By inversion of the output of read/write head **238** in inverter **249** and by operation of rectifier/shaper **250,** a similar train of positive, shaped pulses, such as are shown in FIG. 8F, is produced representing however only the negative peaks of the original output train of FIG. 8D. It will be apparent then that the two trains of pulses applied as inputs respectively to AND gates **252** and **258** represent respectively all of the positive-going transistions in the original base encoded signal of FIG. 8C and all of the negative-going transitions of FIG. 8C, and that some of these transitions are "midbit" while some are "interbit". The phase decoder system is intended to reconstruct the original sequence of bits (as shown in FIG. 8A), from the information provided by the midbit transitions only. Thus it is intended to reject the signals corresponding to the interbit transitions and this is accomplished by establishing a gating signal or time "window" after each detected midbit transition and during an interval when the next midbit transition can be expected to occur. This window, shown as the pulse train of FIG. 8G is produced as the output signal from OR gate **267** which is applied as an enabling or window signal to AND gates **252** and **258** and monostable multivibrator **270.**

Divider **264** is arranged so that counter **265** counts four pulses during each bit time of the original signal of FIG. 8A. Thus, when the counter **265** sequences to count the first pulse, the count zero output line from converter **266** goes down and the first count output line, which is not used here, goes high. Thus, OR gate **267** has no output and there is no enabling window

present at AND gates 252 and 258. Any pulse appearing during that time in the inputs of AND gates 252 and 258 from the shapers 248,250 will be discarded. This is also true when the counter 265 sequences to the next or second count. However, the leading edge of the pulse appearing on the second count line from converter 266 is used to clock shift register demultiplexer 262 and shiftfs the data in the latter along one bit. When the third pulse from divider 264 is counted by counter 265 the third count line from converter 266 brings the output of OR gate 267 high and enables AND gates 252 and 258. As will be seen, the window provided by OR gate 267 continues high during the fourth count and then goes low at the beginning of the fifth count.

Although converter 266 is an octal converter, only five of the eight output lines are used. It should be noted that all pulses in the outputs of both rectifier/-shapers 248 and 250 are applied as inputs to OR gate 254, and that monostable multivibrator 270 is enabled by each window because the output of OR gate 267 is connected to the enable input of the multivibrator 270. Thus, if a pulse appears at either input to OR gate 254 at any other time than during a window, that pulse will neither trigger multivibrator 270 nor be passed by AND gates 252 or 258. On the other hand, when a pulse does appear during the third and fourth count in counter 265, that input pulse to OR gate 254 will also be passed by either AND gate 252 or 258, and because multivibrator 270 is enabled during that time, that pulse will also trigger the multivibrator 270. The output of the latter, then serves to disable AND gate 272 so that counter 265 is reset and held in its reset state until the pulse from multivibrator 270 disappears, whereupon the counter 265 resumes counting. Thus, as soon as a transition from OR gate 254 appears during the third or fourth count, counter 265 is reset and the zero count line then goes up and the window signal in the output of OR gate 267 stays up. In this manner all of the interbit transitions are effectively rejected because they cannot pass AND gates 252 and 258 and the counter 265 is reset after each detection of a midbit to thereby provide another window signal. For each of the eight data bits in the original signal there will be a corresponding mid pulse transition which will appear either at the input of AND gate 252 or at the input of AND gate 258. All of the midbit transitions appearing at the input of AND gate 252 as shown in FIG. 8J of course are applied to the set terminal of flip-flop 260 and all of the midbit transition pulses appearing at the input of AND gate 258 as shown in FIG. 8H, will similarly be applied to the reset terminal of flip-flop 260. Thus the output of flip-flop 260 at its $\overline{Q}$ terminal will be a rectangular wave form which has positive-going transitions corresponding to the negative polarity midbit signals in the read/write head output, and will have negative-going transitions corresponding to the polarity midbit transitions in the read/write head output. This provides a wave form shown in FIG. 8K which is a reconstruction of the original wave form shown in FIG. 8A, phase-displaced ideally by one half of a bit.

If during the window time no midbit transition is detected, it is apparent that an intercharacter gap (ICG) instead has been found. At that point multivibrator 270 is enabled, but there will be no output from the latter to reset counter 265 back to zero because OR gate 254 has provided no triggering pulse. Instead, counter 265 will count a fifth count and consequently a signal will appear on the fifth count line of converter 266. This latter signal, indicative of the detection of an ICG, enables AND gate 269 so that the next clock pulse can be applied to the reset terminal of control flip-flop 256. The Q terminal of the latter then goes low, the output of AND gate 272 goes low and counter 265 is thus reset and held in its zero count state. Also, when an ICG appears, the signal on line 268 is also applied to terminal 144 (FIG. 6) to actuate flip-flop 136 and sequence the main storage memory or static shift register 94 by a single shift, transferring the output signals at the eight outputs of demultiplexer 262 to the main storage memory or static shift registers 94.

Because the counter 265 is then at zero count state, the zero count line from converter 266 is high and the output of OR gate 267 is high and thus enables AND gates 252 and 258. The midbit transition then seen by the gates 252, 258 is the start transition corresponding to the positive-going transition in the original clock pulse used in the phase-encoding of the next character of the original signal. The pulse corresponding to that start transition is applied to the S terminal of flip-flop 260 through AND gate 252 so that the $\overline{Q}$ terminal of the latter goes low if it is not already low Also, the output of OR gate 267, being high, sets control flip-flop 256 so that the latter provides a high input signal to AND gate 272. This output of OR gate 267 also triggers multivibrator 270 which thus keeps AND gate 272 disabled despite the setting of flip-flop 256, but AND gate 272 is disabled only until the signal from multivibrator 270 subsides. At that point AND gate 272 enables counter 265 which starts to count from zero again, so that on the first count, OR gate 267 is disabled and the sequence described above reoccurs.

It is apparent from the nature of phase-encoding and the details of the read logic used that data can be decoded reliably despite considerable timing errors such as might be due to tape speed variation and the like.

The decoded signals, appearing at respective lines on the output of demultiplexer 262 are then the respective R1, R2, R2A, R5, T1, T2, S and P signals. These output lines from demultiplexer 262 are connected to the respective terminals identified as Inputs From Read Data Circuits 60 shown in FIG. 5 and thereby can be introduced back into the main storage memory or static shift register 94.

All 8 lines at the output of the main register storage memory or static shift 94 are also connected as inputs to print control logic 68 as noted in FIG. 3. As shown particularly in FIG. 9, the R1, R2, R2A, R5, T1, and T2 lines from register 94 are connected to respective input terminals of a like plurality of enable gates 280. All of the output lines from register 94 are also connected to respective input terminals of parity checking circuit 282.

In order to decode the characters which represent operator functions, there is provided operator decoding circuit or decoder 284 having six input terminals respectively connected to the R1, R2, R2A, R5, T1, and T2 outputs from register 94. The decoder 284, well known in the art, is merely a group of gates connected so as to decode the operator function signals shown in Table II and provide an output signal on a corresponding operator line when the requisite input operator signal has been detected or decoded. Thus, decoder 284 has output lines respectively identified as SP (Space),

CR (Carrier Return), BSP (Back Space), CI (Carrier Index), TAB, TABS (Tab Set) and TABCL (Tab Clear). These latter output lines are connected as inputs to a plurality of enable gates **286.** Decoder **284** also includes gating which will provide an output on line **287** whenever the decoder **284** determines it has decoded an operator code, i.e. whenever an output signal appears on any other line from decoder **284.** Typically a simple OR gate will serve this function. If the signal at the input to decoder **284** is not an operator function signal but instead is an information character signal then decoder **284** provides an output signal on line **288.** In addition decoder **284** includes gating for detecting the presence of a hyphen code (Table I) at the output of register **94** and for providing responsively thereto an output signal on line H to terminal **289.**

It is desirable to inhibit transfer of information from the print control logic to the printer **20** when the latter is performing a function or is otherwise busy. To this end, there is provided Print-Busy OR gate **290** having a plurality of inputs thereto. One of the inputs is a $\overline{\text{Print Mode}}$ signal simply derived as the inverse of a signal generated by depression of Print Buttons **33, 34, 35** or **36** indicating that the device is not in the Print Mode and that the printer **20** is therefore available for operation of the keyboard **23** by the operator. Another of the inputs to OR gate **290** is a CIM (carrier-in-motion) signal indicating that the print head **16** of the output printer **20** is being transported from right to left; such signal is derived from a carrier-in-motion sensor in baseplate **24.** Yet another input line to OR gate **290** is a PIM line for carrying a signal indicating that the print head **16** is in motion or that some character is being printed out by the print head **16** and the latter is not ready to print another character. The PIM signal also is provided by an appropriate sensor in baseplate **24.** Another input line to OR gate **290** identified as Function From Keyboard from encoder gates **76** in FIG. **4,** is intended to carry signals from any sensor in baseplate **24** which provides a signal that an operator function such as space, carrier index or the like, is occurring. yet another input to OR gate **290** is a line for carrying a CR or carrier return signal from an appropriate sensor in baseplate **24.** An additional line to OR gate **290** is intended to carry, in a preferred embodiment of the invention, delay pulses which are related to typewriter dynamics and which are intended to adjust the operation of the print control logic **68** to match the timing peculiarities or other operating idiosyncracies of the type of printer **20** being used with the system. The output of OR gate **290** is connected as one input to NOR gate **292,** another input to NOR gate **292** being the output of parity checking circuit **282.** The output of NOR gate **292** is applied as an input to both AND gate **294** and AND gate **293.** Another input to AND gate **294** is line **288,** and the output of AND gate **294** is connected to the enabling input terminal of enabling gates **280.**

The output of AND gate **294** is also connected to provide a signal (CC) to enable a cycle clutch in the printer **20,** in known manner, to permit the print mechanism to be driven. Similarly, the other input to AND gate **293** is line **287** and the output of AND gate **293** is connected to the enabling input terminal of enable gates **286.** The outputs of enable gates **286** are thus four lines, each connected to appropriate mechanisms in baseplate **24,** for carrying signals representing the functions CI, TABS, TABCL and TAB, and three other lines for respectively carrying signals representing the functions SP, BSP and CR.

The outputs of enable gates **280** are the six lines **R1, R2, R2A, R5, T1** and **T2,** connected to the baseplate **24** through a data selector or switching mechanism that will permit selectively the print out of data from the buffer memory **52** or addresses **48** in in one embodiment.

The schematic of FIG. **9** also includes three more input terminals, one marked Force SP, one marked Force BSP and the last marked Force CR. The input signals at Force SP and Force BSP terminals are derived from operation of the step Right and Step Left Buttons **41** and **42** and are intended to provide a compulsory Space signal and a compulsory Backspace signal to the baseplate **24.** Similarly, the input signal at Force CR terminal is derived from logic used for Right-Hand Margin Adjust and is intended to provide a compulsory Carrier Return signal to the baseplate **24.** Force CR, Force BSP and Force SP terminals and thus connected to appropriate input terminals of enable gates **295,** the latter having an inverting enabling terminal connected to the output of OR gate **290.** Enable gates **295** thus have three output lines **296, 283** and **297** respectively connectable to the Force SP, Force BSP, and Force CR inputs according as enable gates **295** are enabled or disabled. Line **296** and the SP output line of enable gates **286** are connected as inputs to OR gate **298,** the output of the latter then being connected as the SP input line to baseplate **24.** Line **283** and the BSP output line of enable gates **286** are inputs to OR gate **285** which has its output connected as the BSP input to the baseplate **24.** Similarly line **297** and the CR output line from enable gates **286** are connected as inputs to OR gate **299,** the output from OR gate **299** in turn being connected as the CR input line to baseplate **24.** Input Force SP, Force BSP and Force CR lines are all connected as inputs to OR gate **300.** The output of the latter is connected as an additional input of NOR gate **292.**

In operation of the system shown in FIG. **9,** as register **94** shifts, the 8-bit parallel signals appear in sequence at the register output and all eight bits are applied to parity check logic **282.** The latter, in known manner, sums the bits. Because the present system requires odd parity, logic **282** provides a high output signal to NOR gate **292** only if the sum of the bits is even. If any of the signals at the input of OR gate **290** are high then a high output signal is also applied to NOR gate **292.** Because the latter inverts, a high input signal to NOR gate **292** disables AND gates **293** and **294.** Similarly the output of OR gate **290** when high serves to disable enable gates **295.** Lastly, the output of OR gate **300,** when high, is applied as an input to NOR gate **292.** Thus, in the event that (1) a "wrong" or even parity signal is at the output of register **94,** or (2) signals indicate that the Printer **20** is busy, i.e. PIM, CIM, CR or Function from Keyboard, or (3) delay pulses are at the input of OR gate **290,** or (4) the system is not in the Print Mode of operation, or (5) a Force SP, Force BSP or Force CR signal is present, enable gates **280** and **286** will be disabled and thereby prevent initiation of any action of the printer **20** by any output of register **94.**

When the operator depresses Step Right button **41,** data in storage is shifted by one character and it is then necessary to command a corresponding step of one space by the carrier or print head **16** in the printer **20.**

Hence, Force SP signal is generated by depression of button **41** and is coupled through gates **295** and **298** to the appropriate input terminal of baseplate **24** to initiate such print head stepping.

In certain instances when printing out the register contents, it will be necessary for the system to initiate a Carrier Return signal to the printer **20** although no CR signal is recorded in the register **94** at that point. Hence, the system includes a source of the Force CR signal. Such source is typically a flip-flop activated responsively to appropriate logic covering a number of situations where a CR signal must be initiated. The Force CR signal is coupled through gates **295** and **299** to the proper input terminal of the baseplate **24** to compel a Carrier Return function by the print head **16.** In case of either a Force SP, Force BSP or Force CR signal being produced, these signals will serve to disable enable gates **286** and **280** so that the contents of register **94** cannot be used to activate the baseplate **24.**

As previously noted, when typing data into the register **94** when the system is in the Draft Mode, a single or a **201** shift cycle is used and the clocking of register **94** and the subsidiary registers **96, 98** occurs in the $X_1X_3X_2$ sequence. Similarly, inserting data from the keyboard **23** into the buffer memory **52** when the system is in the Insert Mode involves a **201** shift cycle where the clocking order is initially $X_1X_2X_3$ but changes to $X_1X_3X_2$ during the **201** shift cycle when a blank cell is detected in the buffer memory **52.** Similarly, the operation of deletion of a character is accomplished by a **201** shift cycle. As noted single shifts of register **94** are used along with the $X_1X_3X_2$ clocking sequence when in the Print Mode, i.e. to print out from the buffer memory **52.**

To effect the foregoing operations, the system includes logic in buffer control originally shown in block in FIG. **3** at **70** and which, in a simplified version is illustrated in FIG. **10** and includes four D-type flip-flops **301, 302, 303** and **304.** Flip-flop **304** is intended to provide signals controlling the single shifts when in the Print Mode. Thus, the D input terminal of flip-flop **304** is connected to terminal **305** at which a Print Mode signal, derived by operation of any of the print buttons **33,** 34, 35, or **36** is intended to be applied. The Q terminal of flip-flop **304** is connected to terminal **144** of flip-flop **136** (FIG. **6**). The C or clock input terminal of flip-flop **304** is connected to the output of OR gate **306.** The latter has a pair of input terminals, which are respectively connected to the outputs from encoder gates **76** shown in FIG. **4** as PIM and Function from Keyboard. The output of OR gate **306** is also connected to the C input terminals respectively of flip-flops **301, 302** and **303.**

The logic diagram of FIG. **10** also includes input terminal **169** which is at the output of AND gate **134** (FIG. **6**). Terminal **169** is connected to the clear input terminal **307** of flip-flop **304.** Terminal **169** is also connected as an input to AND gate **308,** the other input to which is terminal **310** which is connected to output line **156** of counter **190** (FIG. **6**). The output of AND gate **308** is connected to clear input terminals **311, 312** and **313** of flip-flops **301, 302,** and **303** respectively. A group of logic gates are provided for operating flip-flops **301, 302** and **303,** and include AND gate **314** having its output connected to the D input terminal of flip-flop **301** and having four input terminals, one of which is connected to terminal **305** through inverter **315.** Another of the input terminals to AND gate **314** is connected through inverter **316** to terminal **317** which is the CR line output of decoder **284** (FIG. **9**). A third input to AND gate **314** is through inverter **318** from input terminal **319.** The last input terminal of AND gate **314** is connected to the output terminal of NAND gate **320.** The inputs to NAND gate **320** are respectively connected to terminal **322** and line **324** from RS flip-flop **344.** The D input terminal of flip-flop **302** is connected to the output of second AND gate **326** which has three input terminals, one of which is connected to the output of inverter **315,** a second of which is connected through inverter **327** to line **324** and the last of which is connected to the output of OR gate **328.** OR gate **328** has one input connected to terminal **319** and the other input connected to terminal **317.**

The third AND gate **329** has its output connected to the D input terminal of flip-flop **303.** AND gate **329** has four input terminals, one connected to the output of DR gate **328,** another connected to the output of inverter **315,** a third connected to line **324** and a fourth connected through inverter **330** to terminal **322.** Lastly, the Q output terminals of flip-flops **301, 302** and **303** are all connected as inputs to OR gate **332,** the output of the latter being connected in turn to terminal **147** (FIG. **6**).

The buffer control logic **70** shown in FIG. **10** controls the buffer memory **52** in accordance with the following operation. As previously noted, the signal intended to be applied at terminal **305** is derived from operation of any of the four print buttons **33–36.** The Q terminal of flip-flop **304,** as is typical of D-type flip-flops, will go high when simultaneously both the signal at input D is high and the signal at C terminal goes high. Thus, when the signal at terminal **305** is high and there is PIM or Function from K/B signal, then the Q terminal of flip-flop **304** will go high. When the signal at terminal **144** goes high, as previously described in connection with FIG. **6,** the Q terminal of flip-flop **136** goes high and the data in register **94** is shifted one cell. The first ϕ_4 pulse at terminal **169** will clear flip-flop **304** so that its Q terminal goes low. Thus each time a character is printed or a function is executed on the printer **20,** the buffer memory **52** is shifted one place so that the next stored character is available.

If however, the device is not in the Print Mode and the signal at terminal **305** is therefore not high, the output of inverter **315** will however apply a high signal to each of AND gates **314, 326** and **329.** As noted, terminal **317** is connected to the CR output line from decoder **284** in FIG. **9** and therefore is intended to carry a signal indicative that a carrier return function signal has been noted at the buffer memory output. Similarly, terminal **322** is connected to the output of AND gate **220** (FIG. 7) and thus is intended to provide a signal indicative of detection of blank cell at the buffer memory output. Line **324** is intended to have applied thereto a signal derived as hereinafter explained indicating that the buffer memory **52** is full. Lastly, at terminal **319** there is intended to be applied a signal indicating that insert button **32** has been depressed and that the system is therefore to operate in the Insert Mode. It will be seen then that the output signal from the AND gate **314** goes high only when (1) the system is not in the Print Mode, (2) there is no carrier return signal at the output of register **94,** (3) the device is not in the Insert Mode and (4) register **94** is not full with a blank cell at its output. All of these negative require-

ments therefore indicate that the device is to operate in its "normal mode". Hence, flip-flop **301** provides at its Q output a normal shift signal for typing in data from the keyboard **23** when the output of AND gate **314** is high and if either a PIM or Function from K/B signal is present.

Similarly, there will be high output from AND gate **326** when (1) the system is in an Insert Mode or a carrier return signal appears at the output of register **94,** (2) the system is not in the Print Mode and (3) the register **94** is not full. This output from AND gate **326** causes flip-flop **302** to also provide an output signal which indicates that a Normal Insert Cycle is to operate and which is fed both as in input to OR gate **332** and to terminal **187** (FIG. **6**).

AND gate **329** will provide a high output only when (1) the system is either in an Insert Mode or a carrier return signal appears at the output of register **94,** (2) a blank cell is not at the output (3) register **94** is full and (4) the system is not in the Print Mode. In such case, the resulting output signal from flip-flop **303,** applied as an input to OR gate **332,** also is applied at terminal **182** to control buffer clocking for the Insert Cycle with Overflow operation.

Resetting of flip-flops **301, 302** and **303** occurs when both a terminate shift signal is present at the output of counter **190** (FIG. **6**) and a ϕ_4 signal is present at terminal **169.** The output of OR gate **332** is applied to terminal **147** to bring the J input of flip-flop **142** (FIG. **6**) high and therefore initiate a **201** shift as previously described. It should be noted that D type flip-flops are used particularly because it is desired to do a **201** shift on the leading edge of the pulse from OR gate **306.**

Included in the circuit of FIG. **10** are means for detecting when the buffer memory **52** is "full". The foregoing means comprises AND gate **336** having one input connected to terminal **322** and the other input connected to terminal **338.** The latter is preferably connected to X_1 line **97** (FIG. **5**) so that any X_1 clocking signals applied to single-bit register **96,** will also be applied at terminal **338.** The output of AND gate **336** is connected to the input of counter **339.** The latter has an enable input terminal which is connected to terminal **147.** Counter **339** is a counter, which after being enabled, counts the first three input pulses from AND gate **336** and then provides a high output signal indicating that three pulses have been counted, whereupon the counter **339** stops counting. Such counter **339** can be readily formed of a pair of flip-flops as is well known in the art. The output of counter **339** is connected through inverter **340** as one input to AND gate **341.** AND gate **341** also has as inputs thereto a line connected to terminal **310,** another line connected to terminal **147,** and a fourth input connected to terminal **342.** Terminal **342** is connected to X_2 line **95** (FIG. **5**) so that any signals applied for clocking shift register **94** (FIG. **5**) will also be applied at terminal **342.**

The output of AND gate **341** is connected to the S input terminal of an RS type flip-flop **344.** The Q output terminal of the latter is connected to line **324.** Lastly, OR gate **345** is provided, having its output connected to the R terminal of flip-flop **344** and having a pair of input lines respectively connected to terminals **346** and **347.** At terminal **346,** there is intended to be applied a signal indicating that a Delete function is being performed, which signal is derived hereinafter described. The signal to be applied at terminal **347** is a signal which will cause a clearing of the buffer memory **52** and for example may be derived from Enable Write line **244** (FIG. **7**).

The portion of FIG. **10** just described detects the "full" buffer memory **52** in accordance with the following operation. A signal at the output of OR gate **332** will, as previously noted, initiate a **201** shift by being applied at terminal **147.** The same signal enables counter **339.** During the **201** shift, every X_1 pulse, being applied at terminal **338,** will serve to enable AND gate **336.** However, the output of the latter goes high only when a blank cell is detected at the output of register **94** and a corresponding pulse is therefore applied at terminal **322.** Counter **339** then counts, for example, the first three blank cells detected during that **201** shift, then stops counting as the output of the counter **339** goes high. Simultaneously, the input to AND gate **341** from OR gate **332** will remain high during the **201** shift, as will the periodic timing signals applied to AND gate **341** from terminal **342.** When the terminate shift input signal, indicating that the **201** shift has been completed, is applied at terminal **310,** AND gate **341** is then interrogated to see if less than three blank cells were counted.

If counter **339** has counted at least three blank cells, its output signal will be high and thus inverter **340** will apply a low signal to AND gate **341,** disabling the latter. If however, counter **339** has counted less than three blank cells, AND gate **341** then, when interrogated by the signal at terminal **310** and if all of its other inputs are high, will provide a set pulse to the S terminal of flip-flop **344** at X_2 time.

In other words, flip-flop **344** will be set when a **201** shift has been executed and less than three blank cells have been seen at the output of register **94** in X_1 time during that shift. Setting of flip-flop **344** provides an output signal on the Q terminal thereof which is applied to line **324** and which indicates that the buffer memory **52** is full. Flip-flop **344** will be reset by the output of OR gate **345** if anything is deleted from the buffer memory **52** as indicated by a Delete signal at terminal **346** or if a record is recorded on tape **18** as indicated as by a Write Enable signal which will clear register **94** and which is applied to terminal **347.**

It should be noted that if less than three blank cells are seen one may infer that only two or less are seen by counter **339.** This implies that if only two cells are seen, only one will be left when the **201** shift cycle is complete. Because for proper operation of the system at least one blank cell must be left at all times, it is apparent that a "full" buffer memory **52** can be defined as one in which, during the **201** shift, counter **339** counts less than three blank cells at the output of register **94.**

As shown in FIG. **11,** which is a simplified version of the tape control circuitry **75,** the address display logic **64** and read address circuits **63** include shift register demultiplexer **262** (FIG. **7**). The inputs shown to the latter are the same as in FIG. **7**: line **274** along which an Enable Read signal can be sent, line **350** which is the data line coupled to the $\overline{Q}$ output of flip-flop **260,** and line **352** which connects the second count output line of converter **266** to the clocking input terminal of shift register demultiplexer **262.** The decoded signals, appearing at respective lines at the output of demultiplexer **262** are of course the respective **R1, R2, R2A, R5, T1, T2,** S and P lines. Four of these lines are connected to the preset inputs of counter **354.**

Counter 354 is preferably an up-down, presettable, clocked counter, well known in the art, capable of counting in a binary coded decimal mode. The counter 354 has a load pin or terminal 356 which is preferably connected to line 268 (FIG. 7) so that the inter-character gap (ICG) signal can be applied to preset counter 354. Counter 354 also includes an input decrement line 358 and an input increment line 359. The output of counter 354 is connected to code converter 360 which is adapted to convert the count in counter 354 to a proper format for display in address display unit 28. Counter 354, converter 360 and display 28 are all shown, for the sake of simplicity as a single decimal digit unit, but it is to be understood that these elements are preferably multi-digit devices.

FIG. 11 also includes, in schematic form, Tape Forward button 46 and Tape Back button 47, connected to respective double-poled switches 362 and 364, the switch armature in each case being centrally spring-biased and coupled to a source of voltage +V. The up or fast forward terminal 365 of switch 362 is connected as an input to both motor drive circuits 366 and to AND gate 368. The down or slow forward terminal 370 of switch 362 is also connected as an input to motor drive circuits 366. Both the up or fast reverse terminal 372 and the down or slow reverse terminal 373 of switch 364 are connected as respective inputs to motor drive circuits 366 and also as inputs to OR gate 374. The output of OR gate 374 is connected as input to AND gate 376.

Motor drive circuits 366 are connected in known manner for controlling the direction and speed of motor or motors 242. Motor 242 is mechanically coupled to control the movement of tape 18 in casette 240 past read/write head 238, and the output of the latter is amplified in amplifier 377. The output of amplifier 377 is connected an input to data-block monostable multivibrator or one-shot 378. The output of the latter is connected to respective inputs to AND gates 368 and 376. The output of AND gate 376 is connected to input decrement line 358, and the output of AND gate 368 is connected to increment line 359.

The operation of the device of FIG. 11 to identify and display the address 48 of a block 19 of data on tape 18 in casette 240 can be described as follows. It will be appreciated that, as previously noted in connection with FIG. 2A, the data addresses 48 are typically prerecorded on a second track 29 on the casette tape 18 and are read from the tape 18 preferably by one of the dual read/write heads 238. The output of both heads 238 will however be applied through the decoding circuitry of FIG. 7, so that both the data on track 25 of the tape 18 and the address information on track 29 will appear on line 350 to shift register demultiplexer 262. To avoid the simultaneous appearance of information from both tracks 25 and 29, it is of course necessary to insure that the data recorded on track 25 is not positioned adjacent an address 48, so that the two tracks 25, 29 can only be read out in a mutually exclusive fashion. Alternatively, one can record addresses and other data in sequence on a single track. The addresses 48 are preferably read out into demultiplexer 262 in binary coded decimal form to appear on the four output lines of the demultiplexer 262 that are connected as the BCD preset inputs of counter 354. The latter is preset at each intercharacter gap associated with the recorded addresses 48 so that no data can be transferred from the shift register demultiplexer 262 to counter 354, except address information.

The output of counter 354 is converted in converter 360 to a form suitable for display in display device 28. The nature of converter 360 is dictated by the type of display desired. For example, if each display device 28 is a seven-segment display then the converter 360 will be a BCD-to-seven-segment converter. Similarly, if display device 28 is a Nixie tube display, then converter 360 would be a BCD-to-decimal converter. Such converters are, of course, well known in the art and need be described no further here.

If button 46 is displaced so that the armature of switch 362 contacts slow forward terminal 370, motor drive circuits 366 will control motor 242 to drive the tape 18 in cassette 240 at a slow speed. As the address 48 is then read from the tape 18, it is demultiplexed and sets the state of counter 354. The state of the counter 354 is converted by converter 360 to a visible display in device 28.

If however, button 46 is manipulated so that the armature of switch 362 contacts fast forward terminal 365, the resulting signal is applied both to AND gate 368 and to motor circuits 366 which then control motor 242 so that the tape 18 in cassette 240 is driven at comparatively high speed past read/write head 238, and ordinarily at a speed which is too fast for the circuit of FIG. 7 to decode the address 48. In such case, the output of amplifier 246, while it may be indecipherable, nevertheless is used to trigger the monostable multivibrator 378 so that its output is a pulse representing the envelope of the address signals read from the tape 18. Each such pulse, when applied to the then enabled AND gate 368, will be transferred to increment line 359 of counter 354 and hence change or increment the state of the counter 354 by one added count.

In a similar fashion, it will be recognized that in neither the fast reverse nor slow reverse modes of movement of the tape 18 in cassette 240, can a readily decipherable signal be obtained by demultiplexer 262. Hence signals from both the fast reverse and slow reverse terminals 372 and 373 of switch 364 are used to cause the counter 354 to be decremented and are applied through OR gate 374 to enable AND gate 376. When the tape 18 is moving in reverse, detection of an address 48 will trigger one-shot 378 and the resulting pulse is fed through AND gate 376 to line 358 to reduce the state of counter 354 by one count.

It will be appreciated that one-shot 378 will provide a pulse corresponding to every address 48 seen, whether in the slow or fast, forward or backward motion of the tape 18. However, the output of the one-shot 378 will not be passed by either AND gate 368 or AND gate 376 unless those AND gates 368, 376 are enabled by appropriate signals indicating appropriate positions of the tape move buttons 46 and 47.

Communication between the operator of the device and the system, to control the operation of the latter, is effected, of course, through both the printer keyboard 23 and control console unit 22. The schematics showing the details of the control console unit 22 connected with the operation of the various control buttons, are shown particularly in FIGS. 12 and 13. Referring particularly to FIG. 12, there will be seen eight of the control buttons identified by name and specifically shown as switch 380 which is connected to be controlled by Draft Mode button 30, switch 382 which is

connected to be controlled by Final Mode button 31, and switch 384 which is connected to be controlled by Insert Mode button 32. All of switches 380, 382 and 384 have armatures which are each connected to the common source of voltage, such as +V, and which are moveable between a corresponding pair of positions.

The armature of switch 380 is moveable between a first position at which the switch 380 is inoperative or has no effect, and a second position wherein the armature contacts a terminal connected to the S input terminal of RS type flip-flop 386. Similarly, switch 382 has a first or inoperative position and a second position wherein the armature is in contact with a terminal which is connected directly to the R or reset terminal of flip-flop 386. The $\overline{Q}$ output terminal of flip-flop 386 is connected to terminal 387 and the Q output terminal of flip-flop 386 is connected to output terminal 388.

Switch 384 has a first position wherein the armature thereof contacts the S input terminal of RS type flip-flop 390. In the second position of switch 384, the armature of the latter is connected to the R input terminal of flip-flop 390. The Q output terminal of flip-flop 390 is in turn connected to the C input terminal of J-K type flip-flop 392. The $\overline{Q}$ output terminal of the latter is connected to the J input terminal and the Q output terminal is connected to the K input terminal. The Q output terminal of flip-flop 392 is also connected to output terminal 394. The reset input terminal of flip-flop 392 is connected to the output line of NOR gate 395. One input of the latter is connected to terminal 388 and another input is connected to the output of OR gate 396.

It will be appreciated that switches 380, 382 and 384 respectively constitute the Draft, Final and Insert button control switches. Upon operation of button 30, flip-flop 386, being set, provides a high signal at its Q terminal and therefore at terminal 387. This high signal then indicates that the device is to operate in the Draft mode. Similarly, when button 31 is pressed, it serves to reset flip-flop 386 and produce a high output signal at terminal 388. This latter high output signal is of course indicative that the operation of the device is to be in the Final mode. It should be noted that the signals at terminals 387 and 388 are mutually exclusive signals so that the system can only operate in either the Draft or the Final mode, but not in both.

Similarly, Insert button 32 controls the operation of switch 384. The armature of switch 384 is normally spring biased into the position whereby flip-flop 390 is held in a reset state. When insert button 32 is depressed, an input signal is applied to the S input terminal of flip-flop 390 and serves to provide a high signal at the Q output terminal of the latter. When the insert button 32 is released, the armature of switch 384 will return to the reset position and the signal at the Q output terminal of flip-flop 390 will then again go low. It will be recognized that because flip-flop 392 is wired so that its input and output terminals are cross-coupled to one another, flip-flop 392 essentially constitutes a divide-by-two device. Thus, as the Q terminal of flip-flop 390 goes high, assuming that the Q terminal of flip-flop 392 is initially high, upon the trailing edge of the signal from flip-flop 390 due to the resetting of the latter, the $\overline{Q}$ output terminal of flip-flop 392 will go high, and provide an Insert Mode signal at terminal 394. This signal will persist until Insert button 32 is again depressed and an input signal is provided to the clock input terminal of flip-flop 392. On the trailing edge of such signal, terminal 394 will then go low.

NOR gate 395 provides an output which will automatically reset flip-flop 392 so that if terminal 394 has a high signal, that signal will then go low. It will be seen that one of the signals which will serve to reset flip-flop 392 is a high signal at terminal 388 indicating that the system is in the Final Mode of operation and that no inserts can be made. Other resetting signals to flip-flop 392 are derived from OR gate 396. OR gate 396 has a plurality of inputs thereto. Typically, one input to OR gate 396 is a Delete signal, which is derived as hereinafter explained in connection with FIG. 13. Another input signal to OR gate 396 is a Tape Move signal indicating that one of the Tape Forward or Tape Back buttons 46, 47 are being operated, as for example, a signal on one of the input lines to motor drive circuits 366 in FIG. 11.

Yet another input to OR gate 396 can be a line carrying a Step Right or Step Left signal derived from operation of buttons 41 or 42 as hereinafter described. Probably the most common signal which will serve to reset flip-flop 392 is an indication that the device is in the Print Mode and the derivation of that signal will be described hereinafter. It will be appreciated that the inputs shown to OR gate 396 are merely exemplary and that many other inputs from elsewhere in the system can be applied at corresponding inputs to either of gates 396 or 395 when it is desirable to take the system out of the Insert Mode of operation. It will also be seen that flip-flop 390 essentially serves to debounce switch 384 and that flip-flop 392 serves as a memory to remember when the system is or is not in the Insert Mode.

FIG. 12 also includes a number of the other buttons of the system and their associated switches. For example, there is shown Print Character button 33, Print Word button 34, Print Line button 35, Automatic Print button 36 and Stop button 38 respectively associated with switches 398, 399, 400, 401, and 402 so that the armature of each switch 398–402 is operated by manipulation of the respective button 33, 34, 35, 36 or 38. The armature of each of these switches 398–402 is connected to a source of potential such as +V, and is moveable between one of two positions. In each case, the armature is normally biased to be in contact with the R or reset terminal of a respective R-S type debouncing flip-flop 404–408, and is moveable to the second position wherein the armature applies the potential + V to the S or Set terminal of the corresponding flip-flop 404–408. Thus, switches 398–402 inclusive have associated therewith flip-flops 404, 405, 406, 407 and 408 respectively. The Q output terminals of flip-flops 404, 405, 406 and 407 are respectively connected to the C input terminals of D type flip-flops 410, 411, 412, and 413. All of the D terminals of flip-flops 410, 411, 412 and 413 are respectively connected to Enable Print input terminal 414. All of the Q output terminals of flip-flops 410–413 inclusive are connected as respective inputs to OR gate 416. The output of the latter is connected to terminal 418 and also, as previously described, as an input to OR gate 396. The reset terminals of flip-flops 410, 411, 412 and 413 are connected to the respective outputs of NOR gates, 422, 424, 426 and 420. The Q output terminal of flip-flop 408 is connected as an input to each of NOR gates 420, 422, 424 and 426. Depending on the complexity of the system, the latter NOR gates 420, 422, 424 and 426 will have

many other inputs. Typically, for example, one of the inputs to NOR gate **420** is connected to input terminal **428** at which there is intended to be applied a signal indicating that anticipatory margin control logic has determined that the printing should stop because no return opportunity has been found upon examination of a particular part of the buffer contents, as will be described hereinafter. Any other condition determined by logic in the system which requires that automatic printing be arrested, such as the appearance of a stop code signal at the output of the buffer memory **52** during printing, or some like condition, can be applied as an input to NOR gate **420** to reset flip-flop **413** and therefore arrest automatic printing.

Similarly, terminal **429** of NOR gate **426** is preferably connected to the output of OR gate **299** (FIG. **9**) so that a signal indicating that a carrier return signal has been detected at the output of the buffer memory **52** can be applied to NOR gate **426.** Again clearly, one can provide additional inputs to NOR gate **426** as shown by the unmarked terminal, from logic which determines that a condition exists in the system whereby it is desired to arrest the printing of a line.

Terminal **430** of NOR gate **424** therefore is connected to the output of OR gate **298** (FIG. **9**) so that an input signal indicating that a space signal has been detected at the output of the buffer memory **52** can be applied to NOR gate **424** and therefore that a word has terminated. As with NOR gates **420** and **426,** other inputs can be provided to NOR gate **424** from logic which determines when it is desirable to arrest the printing of the word.

Lastly, as an input to terminal **431** of NOR gate **422,** there is provided a connection to the Q terminal of flip-flop **304** (FIG. **10**) so that flip-flop **410** can be reset on a condition indicating that a one-shift has been completed by the buffer memory **52** and therefore a character has been printed out. Similarly other inputs can be provided to NOR gate **422** which indicate that it is desirable to stop a print condition where the system has been ordered to print out but one character.

In operation, when it is desired to place the system in a Print Mode of operation, it is only necessary to depress any of Print buttons **33–36** inclusive to effect printing respectively of a character, word, line or to effect automatic continual printing as earlier described. The depression of one of the Print buttons **33–36** will provide an appropriate signal at the input of OR gate **416** and therefore a Print Mode signal at the terminal **418.** It will be remembered that terminal **418,** is connected to terminal **305** (FIG. **10**) so that flip-flop **304** thereby provides a signal which triggers the one-shift flip-flop **136** (FIG. **6**) to clock the buffer memory **52** so that the latter shifts only a single cell. As soon as the shift is initiated, the Q terminal of flip-flop **304** goes high, and the latter signal will then, being applied through NOR gate **422,** reset flip-flop **410** terminating the Print Character mode. In like manner, the output of flip-flop **411,** being applied through OR gate **416,** will cause flip-flop **136** to be triggered through a series of single shifts until a Space signal is detected at the output of the buffer memory **52** and flip-flop **411** is reset, thereby terminating that printing operation. Similarly, signals provided at terminal **418** from flip-flops **412** or **413** will insure that a series of single shift operations of the buffer memory **52** will occur until terminated by conditions which indicated that a line has been completed (such as the occurrance of a carrier return signal at the output of the buffer memory **52**) or, when it is desired to terminate automatic printing, (as by the occurrence of a stop code at the output of the buffer memory **52.**)

Referring now to FIG. **13,** there will be shown the remainder of the control buttons from the control console unit **22,** together with the switching and logic immediately associated therewith. As shown in FIG. **13,** there are Step Right button **41** and Step Left button **42** each coupled for controlling the armature of a respective one of a pair of two-position switches **434** and **435.** The two terminals of switch **435** are respectively connected to the set and reset input terminals of RS type flip-flop **436.** Similarly, the S and R terminals respectively of flip-flop **437** are connected to the output terminals of switch **434.** The Q output terminal of flip-flop **436** is connected to the C input terminal of D type flip-flop **438.** In like manner, the Q output terminal of flip-flop **437** is connected to the C input terminal of flip-flop **439.** Both D input terminals of flip-flops **438** and **439** are connected to a source of voltage V_{cc} at terminal **440.**

The Q output terminal of flip-flop **438** is connected to output terminal **442** and is also connected to the S input terminal RS type flip-flop **444.** The Q output terminal of flip-flop **444** is connected to output terminal **445.** The R input terminal of flip-flop **444** is connected to input terminal **446** at which there is intended to be applied a signal BSP/S from a sensor in the baseplate **24** indicating that a backspace has been executed in the printer **20.**

The Q output terminal of flip-flop **439** is connected to the S input terminal of RS type flip-flop **448.** The R input terminal of flip-flop **448** is connected to input terminal **449** at which there is intended to be a signal SP/S applied which has been derived from a sensor in the baseplate **24** indicating that a spacing operation has been executed in the printer **20.**

The Q output terminal of flip-flop **448** is connected to output terminal **450.** The clear input terminal of flip-flop **438** is connected to the output of AND gate **452.** The latter has two inputs, one from terminal **453** which is connected to the output of counter **190** (FIG. **5**) and the other from terminal **169** (FIG. **6**). The clear input terminal of flip-flop **439** is also connected to terminal **169.** Lastly, the armatures of switches **434** and **435** are connected to some voltage source such as +V at terminal **454.**

In the operation of buttons **41** and **42,** it will be seen that the following sequence of events will typically occur: For example, if button **42** is manually manipulated, it applies a positive voltage at the set input terminal of flip-flop **436** bringing the Q output terminal of the latter high. This triggers flip-flop **438** so as to produce a high signal at terminal **442.** The latter is preferably connected to terminal **145** of flip-flop **138** (FIG. **6**) and therefore initiates a **199**-shift. In addition, the same signal which is applied then to the J input terminal of flip-flop **138** (FIG. **6**) is also applied at the set input terminal of flip-flop **444** and produces a high signal on the Q output terminal of the latter at terminal **445.** This latter signal is then a Force Backspace signal which, as previously noted in connection with FIG. **9,** is applied to Enable Gates **295** and forces the carrier or print head **16** in the printer **20** to backspace in synchronism

with the effective reversal of the movement of data in the buffer memory **52** due to the **199** shift.

Release of button **42** will permit the armature to then contact the reset terminal of flip-flop **436** and the Q terminal of the latter then goes low. On the first ϕ_4 pulse after counter **190** has completed the **199**-shift, flip-flop **438** will be reset and the Q terminal of the latter will go low. The execution of the Force Backspace signal, as determined by the sensor in the base-plate **24**, provides a signal at terminal **446** which then resets flip-flop **444**.

In like manner, if button **41** is manipulated so that a signal is applied at the set input terminal of flip-flop **437**, it serves to trigger flip-flop **439** which provides an output to the S input terminal of flip-flop **448** and thus brings terminal **450** high. This latter signal constitutes a Force Space signal which, as shown in FIG. **9**, is also applied at Enable Gates **295** in order to compel the print head **16** in the printer **20** to space one unit. The Q output of flip-flop **439** is also used, as will be described hereinafter, as an input signal to flip-flop **136** (FIG. **6**) to initiate a one-shift in the buffer memory **52**. Flip-flop **439**, of course, is cleared by the first ϕ_4 pulse applied at terminal **169** and flip-flop **448** is reset immediately upon the execution of a Space operation by the printer **20** as determined by the sensor in the baseplate **24**.

It will be apparent then that the operation of either of the Step buttons **41, 42** will result in either the buffer contents alternatively being shifted forward, or, in effect backward, with a synchronized attendant movement of the print head **16**. The logic for controlling the buffer memory **52** can be made considerably more complex to cover a number of special relations between the buffer contents and printer operation that may occur while stepping the print head **16** either as a series of spaces or as a series of backspaces.

Also included in FIG. **12** are three additional switches **456, 457** and **458** respectively associated with and operated by the Skip/Delete buttons **45, 39** and **40** which are intended respectively to control the skipping or deleting, as the case may be, of characters, words and lines. Each of the switches **456, 457** and **458** are two-position switches wherein the armature is normally spring biased into one position. The respective contacts of each switch **456–458** is connected to a corresponding pair of set and reset terminals of one of RS type flip-flops **460, 462** and **464**. The Q output terminal of flip-flop **460** is connected to the C input terminals of first and second D type flip-flops **466** and **467**. Similarly, the Q output terminal of flip-flop **462** is connected as an input to the C input terminals of both flip-flops **468** and **469**, and the Q output terminal of flip-flop **464** is connected to the C input terminals of flip-flops **470** and **471**. The D input terminals of flip-flops **466, 468** and **470** are connected to terminal **388**. The D input terminals of flip-flops **467, 469** and **471** are connected to input terminal **387**. The Q output terminals of flip-flops **466, 468** and **470** are all connected together with the Q output terminal of flip-flop **439** as inputs to OR gate **474**. The output of the latter is connected to input terminal **144** (FIG. **6**). The Q output terminals of flip-flops **467, 469** and **471** are all connected as inputs to OR gate **476**. The output of the latter is in turn connected to terminal **147** (FIG. **6**) and also to terminal **478**. Lastly, the armatures of switches **456, 457** and **458** are all connected to terminal **454**.

In operation of the Skip/Delete buttons **45, 39, 40** of FIG. **13**, the operation of Word button **39** will be described as being exemplary of the others. Manipulation of button **39** will apply the voltage at terminal **454** to the S input terminal of flip-flop **462** so that the Q output terminal of the latter then goes high. This high signal is then applied to the C input terminals of flip-flops **468** and **469**. One of the two latter flip-flops **468, 469** will then be triggered, depending upon which of the flip-flops **468, 469** has a high signal applied to its D input terminal. It will be appreciated that the signal applied at terminal **388** is indicative that the system is in the Final mode of operation because terminal **388** is connected to the $\overline{Q}$ output of flip-flop **386** (FIG. **12**). Similarly, if the signal at terminal **387** is high, it is indicative of that the system is in the Draft Mode of operation because terminal **387** is connected of course to the Q output of flip-flop **386** (FIG. **12**). Thus, depending upon whether the system is in the Final Mode or Draft Mode (as determined by the state of flip-flop **386**) either flip-flop **468** or **469** will provide an output. If the Q output of flip-flop **468** goes high because the system is in Final Mode then the signal is applied to terminal **144** and will initiate a one-shift cycle in the buffer memory **52**. If on the other hand the system is in the Draft Mode of operation, flip-flop **469** will be triggered and a signal will be applied at terminal **147** to initiate a **201** shift, and the same signal is applied at terminal **478** to provide a Delete signal which, among other things, is applied as an input to OR gate **396** (FIG. **12**), at terminal **346** (FIG. **10**) and at terminal **186** (FIG. **6**). In similar manner, the operation of line button **40** will trigger either flip-flop **470** or **471** depending upon whether the system is in the Final or Draft modes of operation and provides similar output signals either to terminals **144** or **147**. A similar situation would also be created by operation of character button **45**.

In any case, the various signals, either at terminal **144** which serves to initiate one-shift cycles or at terminal **147** which serves to initiate **201** shift cycles, will persist for variable lengths of time depending upon the resetting or clearing of the particular operative one of flip-flops **466–471** inclusive. The various flip-flops **466–471** are reset by a number of signals which are derived through flip-flop reset gating logic shown only generally at **479**. Logic **479** is quite similar to the reset logic shown in FIG. **12**, for example as NOR gates **420, 422**, 424 and **426** and have a plurality of inputs thereto, only a few of which are shown as exemplary as, for example, terminal **428** at which a signal indicative that there has been no Return Opportunity detected, or terminal **429** which indicates that a Carrier Return has been detected and therefore the line has terminated, or terminal **430** at which a Space signal is indicated as having been detected at the buffer output. The simple logic needed to reset flip-flops **466–471** according as character, word or line termination condition have been detected, is not shown inasmuch as it would unduly serve to complicate the drawing without enlarging the understanding of the operation of the system.

A better understanding of the capability of the system thus described can perhaps be better appreciated by contemplating the operation of the device when inserting a character in an existing line. As previously noted, this involves a **201** shift cycle where the change in clocking order from $X_1X_2X_3$ to $X_1X_3X_2$ is seen to give an insert capability. The order is changed when a

blank cell is seen in the buffer input at ϕ_4 time. Thus, when the insert button **32** is depressed, flip-flop **392** is triggered to produce an output at terminal **394.** The signal is then applied at input terminal **319** (FIG. **10**) to the change order gating, and starts the cycle of operation described in connection with the logic of FIG. **10** which provides that the clocking order will change during the **201** shift cycle when a blank cell is delected in the buffer memory **52.** During the first part of the cycle the buffer size is effectively increased by one character and changing the clocking order returns the buffer memory **52** to its original size and causes the blank cell to be lost from the buffer contents.

The procedure for deleting a character is similar to that for inserting except that as previously noted, the clocking order is initially $X_1X_3X_2$ and switches to $X_1X_2X_3$. Again, the order is changed when a blank cell is seen at the buffer input in ϕ_4 time. In this way a blank cell is added to the buffer contents at the expense of the deleted character. It will also be apparent that whether a delete or skip function occurs, depends on whether the system is respectively in Draft or Final mode.

Referring now to FIG. **14,** there will be seen a schematic diagram detailing elements of right-hand margin adjust logic otherwise shown in block at **66** in FIG. **3.** As shown, the schematic of FIG. **14** includes a plurality of input terminals, at least three of which, **480, 482** and **484** are respectively connected to the SP (Space) output line from decoder **284,** the H (Hyphen) line from decoder **284** and the CR (Carrier Return) output line from decoder **284** all shown in FIG. **9.** To provide clocking for the system of FIG. **14,** there are three input terminals, **485, 486,** and **487** which are respectively connected to the outputs of AND gates **128, 130** and **134** (FIG. **6**). Input terminal **488** is connected to a sensor on the baseplate **24** which provides a signal (RM/S) when the carrier or print head **16** has arrived at the beginning of a return zone, i.e. a predetermined distance from whatever righthand margin as may have been set by an operator of the printer **20.** Similarly, terminal **490** is connected to a sensor in the baseplate **24** which gives a signal (CR/S) indicating that a Carrier Return is being executed. Lastly there are two more input terminals, terminal **492** which is connected to the output of counter **190** (FIG. **6**) and terminal **494** which is typically connected to a source of a Draft Mode signal, indicating that the system is not in the Final mode of operation, such as terminal **387** (FIG. **12**).

Terminals **488** and **487** are respectively connnected to the J and clock terminals of J-K type flip-flop **496.** The Q output terminal of flip-flop **496** is connected to the C input terminal of D-type flip-flop **498.** The D terminal of the latter is clamped at some positive voltage V_{cc}. The Q output terminal of flip-flop **498** is connected to output terminal **146** (FIG. **6**). Terminals **492** and **487** are connected as inputs to AND gate **500.** The output of the latter is connected as one input to NOR gate **501.** Another input to NOR gate **501** is connected to terminal **494.** The output of NOR gate **501** is connected to a disabling input terminal of flip-flop **498.**

Terminal **494** is also connected as an input to NOR gate **502** and another input to NOR gate **502** is connected to terminal **490.** The output of NOR gate **502** is connected to a disabling input terminal of flip-flop **496.**

Terminals **480** and **482** are connected as inputs to OR gate **504.** The output of the latter and terminal **484** are both connected as respective inputs to OR gate **506.** The output of OR gate **506** and terminal **485** are both connected as inputs to AND gate **507.** Terminal **485** is also connected, together with the Q output of flip-flop **498** as inputs to AND gate **508.** The output of AND gate **508** is connected to the C input terminal of D-type flip-flop **510.** The D input terminal of flip-flop **510** is connected to the output of OR gate **504.**

The output of AND gate **507** is connected to the C input terminal of another D-type flip-flop **512.** The D terminal of the latter is clamped at voltage V_{cc}. An enabling input terminal of flip-flop **510** is connected to the Q output terminal of flip-flop **496.** Similarly, an inverting enabling input terminal of flip-flop **512** is connected to the Q output terminal of flip-flop **498.** The Q terminal of flip-flop **510,** the Q terminal of flip-flop **496** and the $\overline{Q}$ terminal of flip-flop **498** are all connected as inputs to AND gate **514.** The output of the latter is connected to the S input terminal of an RS type flip-flop **516.** The R input terminal of flip-flop **516** is connected to terminal **490.** The Q output terminal of flip-flop **516** is connected to terminal **517.**

A second RS type flip-flop **518** is provided, and its R terminal is connected to the $\overline{Q}$ terminal of flip-flop **496.** An in-modulo-8 counter **520** is also included and has its input connected to terminal **486.** An enable input terminal of counter **520** is connected to the Q output terminal of flip-flop **498.** The output of counter **520** is connected as one input to AND gate **522.** The $\overline{Q}$ terminal of flip-flop **512** and the Q terminal of flip-flop **498** are also connected as inputs to AND gate **522.** The output of AND gate **522** is connected to both terminal **524** and the S input terminal of flip-flop **518.**

The operation of the circuit shown in FIG. **14** is intended primarily to provide an anticipatory margin control i.e. to sense when the return zone has been entered and to return the print carrier or print head **16** to the lefthand margin if and when an opportunity to do so exists, or if no such opportunity exists then to indicate that hyphenation is going to be required, and to cause printing to halt at the beginning of the return zone. In order to do so, the circuit takes advantage of the fact that cycling the buffer memory **52** through a **200**-shift by triggering flip-flop **140** (FIG. **6**) can be done in an extremely short period of time and will permit a search through the buffer memory contents to indicate whether an opportunity exists to return the carrier or print head **16** before printing the first character in the return zone. These opportunities to return the print carrier or print head **16** exist when a space, a carrier return, or a hyphen is found to occur among data stored in the buffer memory **52** corresponding to characters to be printed or operations to be carried out while the carrier or print head **16** is in the return zone. If no return opportunity is found, then the system is intended to stop printing and provide some indication, visually, or audibly or otherwise, that the operator must intervene and hyphenate. It has been found that the optimum return zone, at least for ordinary text in the English language, should be between about four and about 10 spaces, and preferably is eight spaces long to afford a reasonable minimim of intervention by the operator. Thus the right margin sensor in the baseplate **24** is positioned so that it will provide a signal when the carrier or print head **16** is at the beginning of or entering the return zone. In the example shown in FIG. **14,** the return zone is intended to be eight spaces long.

Flip-flops **496** and **498** are not enabled unless the system is in the Final Mode, because of the signal applied at terminal **494** and passed by NOR gates **501** and **502.** When so enabled, and when the beginning of return zone is reached so that the baseplate sensor provides a signal at terminal **488,** flip-flop **496** will be triggered by the next ϕ_4 clock pulse at terminal **487,** and the Q and Q terminals of flip-flop **496** respectively go high and low. The Q output of flip-flop **496** then triggers flip-flop **498** so that its Q terminal goes high and a signal is therefore applied at terminal **146** to initiate a **200** shift in the buffer memory **52.** The same signal from flip-flop **498** enables counter **520** which starts counting ϕ_2 pulses at terminal **486.** The capacity of counter **520** should be matched to the number of spaces in the return zone, and therefore, in the example shown, counter **520** is an in-modulo-8 counter. When counter **520** has counted eight input ϕ_2 pulses, it provides an output signal to AND gate **522.** The Q terminal of flip-flop **498** which of course remains high during the execution of the **200** shift, is also connected as an input to AND gate **522.**

OR gates **504** and **506,** together constitute a three input OR gate which examines the signals at terminals **480, 482,** and **484,** so that as the buffer memory **52** is shifted, at least during the first eight shifts counted by counter **520,** the buffer contents are monitored for the three return opportunities of carrier return, hyphen or space. If no return opportunity is seen, the output of AND gate **507** remains low and the $\overline{Q}$ output terminal of flip-flop **512** therefore stays high. Thus if counter **520** has completed its count, AND gate **522** will provide an output signal only if no return opportunity existed within the time period during which counter **520** was counting. This output signal from AND gate **522,** then applied to terminal **524,** is used to reset the appropriate print mode flip-flop, e.g. **413,** so that the printing operation of the printer **20** is stopped. Simultaneously, the same output of AND gate **522** being applied to the set input terminal of flip-flop **518,** brings the Q output terminal of the latter up. The Q output terminal of flip-flop **518** is connected to some indicator such as a light, buzzer or the like which is identified by the operator as indicating that the printing has stopped, and that the operator should then continue to print out one character at a time until an opportunity to hyphenate occurs, whereupon the operator should add a hyphen by striking the hyphen key on the keyboard **23.** Then, by striking the carrier return key, which of course will not be recorded, the print head **16** or carrier will be brought back to the left margin and the platen **17** indexed.

If however, while counter **520** is counting, OR gate **504** detects either the presence of a Hyphen, a Carrier Return, or a Space signal at the output of the buffer memory **52,** flip-flop **512** will be triggered on the next ϕ_1 pulse. The output of the Q terminal of flip-flop **512** will then be driven low. Thus, no high signal will appear at terminal **524** to stop the printing operation, nor will flip-flop **518** be triggered to indicate that a need for hyphenation exists.

As soon as the **200**-shift has been completed, a Terminate Shift signal from counter **190** is applied to AND gate **500,** and on the ensuing ϕ_4 pulse flip-flop **498** is reset, bringing the $\overline{Q}$ terminal of the latter high. The high signal at the $\overline{Q}$ terminal of flip-flop **498** serves to enable AND gate **508** and also provides an input to AND gate **514.**

Because the system is still in the Final Mode of operation, the buffer memory **52** will continue being shifted one shift at a time to bring up at its output the successive characters or operators stored in the buffer memory **52.** Ultimately, the return opportunity (or the first of several) earlier detected will be present at the output of the buffer memory **52.** If that return opportunity is a Carrier Return signal then it will simply be executed by the printer **20,** and its execution will cause a signal at terminal **490** to reset flip-flops **496** and **516.** The Q terminal of the latter goes high and forces the Q terminal of flip-flop **518** to go low, essentially resetting the latter.

If however the return opportunity takes the form of a Space or Hyphen signal, then flip-flop **510** will be triggered on the ϕ_1 pulse associated with printing the Space or Hyphen. The Q terminal of flip-flop **510** then goes high and is applied to AND gate **514.** Because AND gate **514** now will have all of its inputs high, the Q terminal of flip-flop **516** goes high. The high signal on terminal **517** is intended to force a Carrier Return by being applied as the Force CR signal to enable gates **295,** (FIG. **9**). Thus the occurrence of a Space or Hyphen signal in the return zone will result in such a signal being executed, and immediately thereafter a Carrier Return signal being created to force the print head **16** to return to the lefthand margin and the platen **17** to index. It will be seen (referring particularly to FIG. **9**) that a high signal at terminal **517** will constitute an input to enable gates **295** and thus be applied through enable gates **300** and **292** to disable enable gates **280** and **286.** This serves to prevent printing of any operator or character then at the buffer memory output until the forced Carrier Return function has been completed.

While counter **520** preferably counts the same number of spaces as the return zone contains, the counter **520** need not be so limited and may be provided as an adjustable counter which can be set to count any arbitrary number. Thus, by simply adjusting the counter **520,** one can effectively change the length of the return zone for any given system, without mechanical alteration of the printer **20.**

While a preferred embodiment of the invention is illustrated in the sheets of drawing and has been described herein, modifications which do not depart from the essence of the invention may be made and will be apparent to those skilled in the art. Therefore, it is intended that the invention not be limited by the precise structure shown and described, but rather that the full scope of the invention be construed in accordance with the appended claims.

What is claimed is:

1. Apparatus for processing data in conjunction with formation of characters and performance of selected functions by a printer having a printing means for forming printed characters on a record medium, a carrier for said record medium, means for moving said carrier and printing means relative to one another in increments of distance along a line between a beginning-of-line position and an end-of-line position, means for moving said record medium substantially perpendicularly to said line, and printer control means for controlling said printer to form said characters responsively to corresponding coded character signals and to perform said functions responsively to corresponding coded function signals, said apparatus comprising in combination:

signal storage means for storing a plurality of said coded character and function signals;

means for applying a plurality of said coded character and function signals to the input of said storage means for storage therein;

means for coupling the output of said storage means to said printer control means so that said printer control means is responsive to coded character and function signals appearing at the output of said storage means; and

anticipatory margin adjust means, operative when said printing means and carrier are in a predetermined position on said line relative to one another intermediate said beginning-of-line position and said end-of-line position, for examining a predetermined plurality of those signals stored in the part of said storage means which would affect the operation of the printer during relative movement of said printing means and carrier between only said predetermined position and said end-of-line position, to determine if any of the examined signals correspond to any of selected ones of said coded character and function signals, said examining being completed prior to any response by said printer control means to any of said plurality of signals.

2. Apparatus according to claim **1** wherein said anticipatory margin adjust means includes means for inhibiting the performance of all said functions, other than those functions corresponding to said selected function signals, and for inhibiting the formation of any characters by said printer responsively to corresponding coded function and character signals stored in said storage means, said inhibiting means being responsive to determination by said margin adjust means that none of said selected coded function and character signals are included in said examined signals.

3. Apparatus according to claim **1** including a mass data recording medium, and further wherein said means for a plurality of said applying coded character and function signals to said storage means comprises means for playing out coded character and function signals recorded in said recording medium.

4. Apparatus according to claim **1** wherein said predetermined plurality of stored signals is between four and 10, inclusive.

5. Apparatus according to claim **1** wherein said predetermined plurality of stored signals is eight.

6. Apparatus according to claim **1** wherein said selected ones of said coded signals correspond to the following functions:

A. restoring the relative position of said carrier and printing means to a margin position opposite said end-of-line position and moving said record medium a predetermined distance substantially perpendicularly to said line;

B. providing relative motion between said carrier and printing means of at least one of said increments toward said end-of-line position; and

C. formation of a printed character representing a hyphen.

7. Apparatus according to claim **6** including means for forcing said printer to execute Function (A) immediately following the execution of either Function (B) or Function (C) if the first of said selected signals found during examination of said predetermined plurality of stored signals is a signal corresponding to either Function (B) or (C).

8. Apparatus according to claim **1** wherein said selected signals comprise signals representative of a carrier return function, a space and a hyphen.

9. Apparatus according to claim **1** wherein said anticipatory margin adjust means is operable to examine all of those signals stored in the part of the storage means which would affect the operation of the printer during movement of said printing means and carrier between said predetermined position and said end-of-line position.

10. Apparatus according to claim **1** wherein said signal storage means is a shift register, and further including;

recording apparatus having a mass data recording medium and reading means for reading coded character and function signals recorded in said mass data recording medium; and

means for transferring coded signals read by said reading means to said means for a plurality of said applying coded character and function signals to said storage means;

said anticipatory margin adjust means comprising register control means operative when said printing means and carrier are in said predetermined position for causing coded signals stored in said shift register to be circulated in said shift register without at the same time causing operation of said printing means;

sensing means for examining the coded signals stored in said shift register as said coded signals are being circulated and for determining if a selected number of the coded signals in said shift register which would affect operation of the printer during relative movement of said printing means and said carrier between said predetermined position and said end-of-line position correspond to any of selected ones of said coded character and function signals;

means for inhibiting operation of said printer; and

means for operating said inhibiting means in response to a determination by said sensing means that none of said selected character and function signals are included in said examined signals.

11. Apparatus in accordance with claim **10** further including means for terminating said circulation of coded signals when said circulating coded signals have been restored to register positions that said circulating coded signals occupied at the time said circulation was initiated.

12. Apparatus according to claim **10** wherein said margin adjust means comprises means operative if said examined signals include one of said selected signals for causing said printer to respond to at least those examined signals which were examined before said one selected signal.

13. Apparatus according to claim **10** wherein said register control means is operative to cause the signals stored in said shift register to undergo a single complete circulation cycle relative to said shift register.

14. Apparatus for processing data in conjunction with formation of characters and performance of selected functions by a printer having a printing means for forming printed characters on a record medium, a carrier for said record medium, means for moving said carrier and printing means relative to one another in increments of distance along a line to an end-of-line po-

sition, means for moving said record medium substantially perpendicularly to said line, and means for controlling said printer to form said characters responsively to corresponding coded character signals and to perform said functions responsively to corresponding coded function signals, said apparatus comprising in combination:

a shift register comprising *n* cells each adapted to store one of said coded character and function signals, *n* being an integer, said shift register having an input and an output;

first selectively operable means for applying a predetermined sequence of coded signals to the input of said shift register;

second selectively operable means for applying coded signals appearing at the output of said shift register to said means for controlling said printer, and also to the input of said shift register;

third selectively operable means for indexing coded signals stored in said shift register one cell position for each coded signal applied by said first selectively operable means to said shift register input or applied by said second selectively operable means to said means for controlling said printer;

means for terminating operation of said first selectively operable means when all of the coded signals in said predetermined sequence have been applied to the input of said shift register;

means for inhibiting operation of said first selectively operable means during operation of said second selectively operable means; and

anticipatory margin adjusting means operable only if said second and third selectively operable means have been rendered operative and then only when said printing means and said carrier are in a predetermined position on said line relative to one another and to said end-of-line position, for examining a predetermined number of those coded signals stored in that part of said shift register which would affect operation of the printer during relative movement of said printing means and said carrier between said predetermined position and said end-of-line position and for determining if any of the examined signals correspond to any one of a selected group of said coded character and function signals.

15. Apparatus according to claim **14** including:

another inhibiting means for inhibiting the performance of any of said functions and the formation of any of said characters by said printer responsively to corresponding coded signals stored in said shift register, said another inhibiting means being responsive to a determination by said margin adjusting means that none of the signals in said selected group are included in said examined signals.

16. Apparatus according to claim **15** wherein said margin adjusting means includes:

means operative when said printing means and carrier are in said predetermined position for indexing coded signals stored in said shift register *n* cell positions with the coded signals appearing at the output of said shift register being circulated back to the input of said shift register;

means for examining said predetermined number of those coded signals stored in said shift register during circulation thereof which would affect operation of the printer during relative movement of said printing means and said carrier between said predetermined and end-of-line positions, and for determining if any of said examined signals correspond to any one of said selected group of said coded character and function signals;

means for producing a margin control signal in response to a determination by said examining means that none of the signals in said selected group are included in said examined signals; and

means for operating said another inhibiting means in response to said margin control signal.

17. Apparatus according to claim **16** wherein said margin adjusting means further includes:

a counter for counting successive one-cell indexing of coded signals stored in said shift register, said counter being operative to produce an output signal when said counter has counted a number of indices not exceeding the number of said increments between said predetermined position and said end-of-line position, and means responsive to the output of said counter for inhibiting production of said margin control signal if none of the signals in said selected group are included in said examined signals in executing the number of indices required to generate said counter output signal.

18. Apparatus according to claim **17** wherein said counter is adjustable.

19. Apparatus for processing data in conjunction with formation of characters and performance of selected functions by a printer having a printing means for forming printed characters on a record medium, a carrier for said record medium, means for moving said carrier and printing means relative to one another in increments of distance along a line between a beginning-of-line position and an end-of-line position, means for moving said record medium substantially perpendicularly to said line, and control means for controlling said printer to form said characters responsively to corresponding coded character signals and to perform said functions responsively to corresponding coded function signals, said apparatus comprising in combination:

signal record playback means having an output;

signal storage means for storing a plurality of said coded character and function signals, said signal storage means including an input for receiving said coded character and function signals and an output;

means for coupling the output of said playback means to the input of said storage means;

means for coupling the output of said storage means to said control means so that said control means is responsive to output signals from said storage means; and

anticipatory margin adjusting means operative when said printing means and carrier are in a predetermined position on said line relative to one another intermediate said beginning-of-line position and said end-of-line position, for examining a predetermined plurality of those signals stored in the part of said storage means which would affect the operation of the printer during relative movement of said printing means and carrier only between said predetermined position and said end-of-line position, to determine if any of the examined signals correspond to any of selected ones of said coded function and character signals, said examining

being completed prior to any response by said control means to any of said plurality of signals.

20. Apparatus according to claim **19** wherein said anticipatory margin adjusting means includes means for inhibiting the performance of all said functions, other than those functions corresponding to said selected function signals, and for inhibiting the formation of any characters by said printer responsively to corresponding coded function and character signals stored in said storage means, said inhibiting means being responsive to a determination by said margin adjusting means that none of said selected function and character signals are included in said examined signals.

21. Apparatus for processing data in conjunction with formation of characters and performance of selected functions by a printer, said printer having means for forming printed characters on a record medium in a character-by-character and line-by-line format, and means for controlling said printer to form said characters and perform said functions responsively to corresponding coded character and function signals, said apparatus comprising in combination:

storage means comprising *n* cells, each capable of storing one of said coded character and function signals, *n* being an integer and said storage means having an input and an output;

means for applying to said input a plurality of said coded signals in a sequence that is predetermined as to content and order;

first control means for operating said storage means so that said coded signals are stored in said storage means in the sequence in which said coded signals are applied at said input;

second control means for operating said storage means so that coded signals stored therein appear at said output in the order in which said coded signals were stored;

means for applying coded signals appearing at said output to said means for controlling said printer;

signal sensing means for determining when said printer reaches a predetermined position short of an end-of-line printing position and before formation of any next character and the performance of any next function by said printer, whether any of a selected plurality of succeeding coded signals appearing at said output is a coded signal representative of a space, printer-return-to-left margin function or a hyphen; and

means for terminating operation of said printer at said predetermined position if a coded signal representative of a space, printer-return-to-left-margin function or a hyphen is not present among said selected plurality of succeeding coded signals appearing at said output, said selected plurality not exceeding the number of increments of printer movement in moving from said predetermined position to said end-of-line position.

22. Apparatus according to claim **21** wherein said storage means is a shift register.

23. Apparatus according to claim **21** wherein said signal sensing means comprises means, operative when said printer reaches said predetermined position, for examining those signals stored in said storage means which affect operation of said printer between said predetermined position and said end-of-line printing position,

means for determining if any one of a selected number of coded character and function signals is among the signals examined by said sensing means,

means for preventing application of coded signals to said means for controlling said printer during the time that signals stored in said storage means are being examined, and

means for inhibiting operation of said second control means only if none of said selected signals is among said examined signals.

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UNITED STATES PATENT OFFICE

CERTIFICATE OF CORRECTION

PATENT NO. : 3,895,704
DATED : July 22, 1975
INVENTOR(S) : RICHARD C. NORRIS

It is certified that error appears in the above-identified patent and that said Letters Patent are hereby corrected as shown below:

Column 51, line 41 delete "means for a plurality of said applying coded character"and substitute therefor --means for applying a plurality of said coded character.--

Column 52, line 22, delete"applying coded character and function signals to" and substitute therefor --applying a plurality of said coded character and function signals to--.

Signed and Sealed this

thirtieth Day of *September 1975*

[SEAL]

Attest:

RUTH C. MASON
Attesting Officer

C. MARSHALL DANN
Commissioner of Patents and Trademarks