(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
9 December 2004 (09.12.2004)

PCT

(10) International Publication Number
WO 2004/107406 A2

(51) International Patent Classification[7]: H01L

(21) International Application Number:
PCT/US2004/016304

(22) International Filing Date: 24 May 2004 (24.05.2004)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
60/472,970 23 May 2003 (23.05.2003) US

(71) Applicant *(for all designated States except US)*: **BOARD OF REGENTS, THE UNIVERSITY OF TEXAS SYSTEM** [US/US]; 201 West 7th Street, Austin, TX 78701 (US).

(72) Inventors; and
(75) Inventors/Applicants *(for US only)*: **DUPUIS, Russell, D.** [US/—]. **CHOWDHURY, Uttiya.**

(74) Agent: **MEYERTONS, Eric, B.**; Meyertons, Hood, Kivlin, Kowert & Goetzel, P.C., P.O. Box 398, Austin, TX 78767-0398 (US).

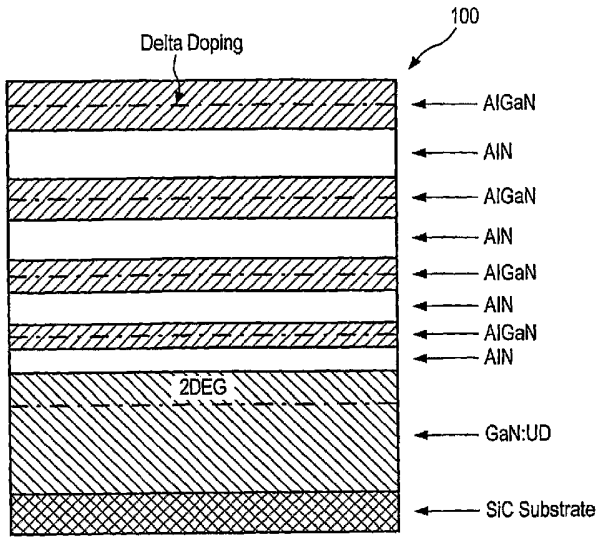
(81) Designated States *(unless otherwise indicated, for every kind of national protection available)*: AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BW, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NA, NI, NO, NZ, OM, PG, PH, PL, PT, RO, RU, SC, SD, SE, SG, SK, SL, SY, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, YU, ZA, ZM, ZW.

(84) Designated States *(unless otherwise indicated, for every kind of regional protection available)*: ARIPO (BW, GH, GM, KE, LS, MW, MZ, NA, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HU, IE, IT, LU, MC, NL, PL, PT, RO, SE, SI, SK, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Published:
— *without international search report and to be republished upon receipt of that report*

[Continued on next page]

(54) Title: SEMICONDUCTOR ELECTRONIC DEVICES AND METHODS



(57) Abstract: Embodiments disclosed herein include electronic device designs based upon electronic properties of Group III-N materials and quantum-mechanical effects of specialized heterostructures. Such electronic device designs may include, for example, heterojunction field-effect transistors (HFETs) and high-electron-mobility transistors (HEMTs). The design concepts permit high power, high-frequency, and high-temperature operation of advanced electronic circuits, including devices for radar, collision-avoidance systems, and wireless communications. Designs disclosed may include one or more AlN layers and/or one or more SMASH superlattice barriers combined with one or more *n*-type delta-doped regions. Alternately, in certain embodiments, one or more AlN layers and one or more SMASH superlattice barriers may be combined without the *n*-type delta-doped regions.

WO 2004/107406 A2

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

SEMICONDUCTOR ELECTRONIC DEVICES AND METHODS

BACKGROUND OF THE INVENTION

1. Field of the Invention

Embodiments disclosed herein generally relate to semiconductor devices. More particularly, embodiments relate to transistors having certain desired properties and methods of manufacturing such transistors.

2. Description of the Relevant Art

During the past few years, there has been interest in the use of wide-bandgap semiconductors, e.g., SiC and GaN, for applications in high-power and high-temperature electronic devices (e.g., *p-i-n* rectifiers, heterojunction bipolar transistors (HBTs), heterojunction field-effect transistors (HFETs), and Schottky barriers). For some applications, GaN devices are predicted to out-perform Si and SiC devices for power applications. Consequently, Group III-nitride materials are receiving attention for high-power electronic applications owing to their promising material properties. While there have recently been demonstrations of Group III-V nitride-based HFETs, to date, power devices performing at or near the theoretical limits for GaN do not appear to have been reported.

It is believed that microwave power devices based on GaAs have almost reached their power limits, whereas the needs for higher microwave power densities are increasing. One of the possibilities for improving power performance at X-band and higher frequencies is to use new material systems. Group III-nitride materials may be attractive for high-power and high-temperature devices because of their intrinsic properties: large energy bandgap, high breakdown voltage, and high peak electron velocity. Microwave power devices such as AlGaN/GaN HEMTs have demonstrated impressive output power density, greater than those of GaAs. For microwave power high electron mobility transistors (HEMTs), a high current gain cut off frequency along with a high saturation current may be desirable. A high drain current of 1,500 mA/mm with a transconductance of 300 mS/mm has been reported with a classic modulation-doped HEMT structure.

SUMMARY OF THE INVENTION

AlGaN/GaN HFETs may be candidates for future applications in high power, high-frequency, high power, and high-temperature electronics (e.g., BMD-class X-band radar systems) because of the fundamental characteristics of Group III-nitride materials. For example, in certain embodiments, a transistor having desired performance characteristics may include one or more AlN layers and/or one or more SMASH superlattice barriers combined with one or more *n*-type delta-doped regions. Alternately, in certain embodiments, one or more AlN and one or more SMASH superlattice barriers may be combined without the *n*-type delta-doped regions.

BRIEF DESCRIPTION OF THE DRAWINGS

Other objects and advantages of the invention will become apparent upon reading the following detailed description and upon reference to the accompanying drawings in which:

Fig. 1a: depicts a schematic diagram of an energy-band diagram for a SMASH in the InAlP/InGaP materials system, according to an embodiment;

Fig. 1b: depicts a schematic diagram of an energy-band diagram for multiple-quantum barrier in the InAlP/InGaP materials system, according to an embodiment;

Fig. 2a: depicts a schematic diagram of a SMASH barrier HFET structure showing superlattice charge layers with an AlN barrier, according to an embodiment;

Fig. 2b: depicts a schematic expanded view of the conduction band structure of an AlN/Al*x*Ga1-*x*N SMASH barrier for enhanced carrier confinement in the channel, according to an embodiment;

Fig. 3: depicts a diagram of drain current to drain voltage for a D^2B^2 AlGaN/AlN/GaN HFET, according to one embodiment;

Fig. 4: depicts a diagram transconductance to gate voltage for a D^2B^2 AlGaN/AlN/GaN HFET, according to one embodiment;

Fig. 5: depicts a diagram of drain current to drain voltage for a D^2B^2 AlGaN/AlN/GaN HFET, according to one embodiment;

Fig. 6: depicts a diagram of current gain to frequency for a D^2B^2 AlGaN/AlN/GaN HFET, according to one embodiment;

Fig. 7: depicts a diagram of minimum noise and associated gain to frequency for a D^2B^2 AlGaN/AlN/GaN HFET, according to one embodiment;

Fig. 8: depicts a diagram of drain current to drain voltage for a D^2B^2 AlGaN/AlN/GaN HFET, according to one embodiment;

Fig. 9: depicts a diagram of drain current and g_m to gate voltage for a D^2B^2 AlGaN/AlN/GaN HFET, according to one embodiment;

Fig. 10: depicts a diagram frequency response for a D^2B^2 AlGaN/AlN/GaN HFET, according to one embodiment;

Fig. 11: depicts a diagram of drain current to drain voltage for a D^2B^2 AlGaN/AlN/GaN HFET, according to one embodiment;

Fig. 12: depicts a diagram of drain current and g_m to gate voltage for a D^2B^2 AlGaN/AlN/GaN HFET, according to one embodiment;

Fig. 13: depicts a HFET with AlN barrier and delta-doped charge layer, according to an embodiment;

Fig. 14: depicts a HFET with AlN/GaN superlattice charge and buffer layer, according to an embodiment; and

Fig. 15: depicts a HFET with SMASH barrier layer, according to an embodiment.

While the invention is susceptible to various modifications and alternative forms, specific embodiments thereof are shown by way of example in the drawings and will herein be described in detail. It should be understood, however, that the drawing and detailed description thereto are not intended to limit the invention to the particular form disclosed, but on the contrary, the intention is to cover all modifications, equivalents and alternatives falling within the spirit and scope of the present invention as defined by the appended claims.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

In an embodiment, AlGaN/GaN heterojunction field-effect transistors (HFETs) may be used in high-power, high-frequency, and high-temperature electronics, because of the fundamental characteristics of Group III-nitride materials. Improved high-power HFET performance has been recently achieved and a power density of 10.7 W/mm at 10 GHz has been demonstrated. For high-power device applications, a high drain-source current, I_{DS}, along with a high transconductance and a large source-drain breakdown voltage may be desirable.

In an embodiment, a large source-drain current, I_{DS}, may be achieved if the sheet charge density, n_s, the carrier mobility, μ_n, and the saturation drift velocity, v_s, in the channel have relatively large values. Currently, a large source-drain current may be achieved by using undoped or modulation-doped AlGaN/GaN structures. Another method of achieving a large source-drain current may include increasing the aluminum mole fraction (and therefore, the bandgap) in an AlGaN barrier. Although, increasing the Al mole fraction in the AlGaN cap layer may lead to higher n_s, it may also lead to a decrease in μ_n. As a result, $n_s\mu_n$ product improvement may be limited.

Large source-drain current devices may be referred to as "high-electron mobility transistors" or HEMTs. Recently, the use of a binary barrier of AlN was reported to increase the low-field electron mobility, μ_n, and n_s in the channel, yielding an $n_s\ \mu_n$ product of 2.28×10^{16} V-s. However, the FET device performance (e.g., I_{DSmax} and g_m) did not appear to be improved compared to the performance achieved by a "standard" modulation-doped HFET.

Embodiments disclosed herein include delta-doped heterostructure FET designs. Such designs may include the use of one or more AlN barriers. Additionally, one or more superlattice barriers may be included in delta-doped heterostructure FET designs disclosed herein. One or more AlN and/or one or more superlattice barriers may be combined with one or more *n*-type delta-doped regions. Alternately, in certain embodiments, one or more AlN and one or more superlattice barriers may be combined without the *n*-type delta-doped regions. In embodiments that include *n*-type delta-doped regions, the *n*-type delta-doped regions may improve the current carrying capabilities of the HFET. In certain embodiments, n-type delta-doped regions have the additional benefits of reduced gate leakage, low noise, high g_m, and capability of sustaining a large voltage across the drain source region (large V_{DS}) prior to breakdown of the device. The structures described above may demonstrate relatively high $n_s\ \mu_n$ product, relatively large drain currents, relatively high values of extrinsic transconductance, relatively low noise figures at 17GHz, and/or transconductance values close to the state-of-the-art.

An superlattice heterostructure includes a series of alternating layers of smaller-bandgap "quantum well layer" and larger-bandgap "barrier layers." Quantum mechanics predicts that an electron has a non-zero reflection probability from a barrier lower than the energy of the electron. With appropriate design of the barriers and wells, the reflected wave may be made to interfere destructively with the incident electron wave. A propagation matrix is calculated for each interface that calculates the ratio of incident wave, reflected wave and transmitted wave. For a multi-period heterostructure, these propagation matrices are multiplied together yielding the effective propagation matrix for the superlattice. Such an superlattice structure effectively increases the heterojunction barrier while reducing the lattice mismatch and alloy scattering.

In one embodiment, the super lattice structure may be improved by growing a specially designed superlattice heterobarrier that has a non-periodic structure. An example of one such barrier with a special increased electron reflectivity design we have developed is called a "strain-modulated aperiodic superlattice heterobarrier" (SMASH™) and will be described in further detail below.

Embodiments disclosed herein include methods to improve performance of Group III-N HFET devices in terms of power, frequency response, noise and stability. Specifically, a number of HFET device structures are disclosed. For example, a first HFET device structure including delta-doped AlGaN/AlN/GaN HFETs using an ultra-thin AlN binary superlattice barrier layer is depicted in FIG. 2A. Other examples of HFET device structures include delta-doped and undoped strain-modulated aperiodic superlattice heterobarrier (SMASH) electron donor and confinement structures.

In an embodiment, a specially designed SMASH barrier may be used in an HFET device to improve carrier confinement and to reduce the leakage current for high-power devices. Such SMASH barriers may include quantum-mechanically designed barriers, which reflect electrons back into the channel. Such SMASH barriers may further provide a high carrier density from the combined effects of the piezoelectric and polarization charges and the carriers provided by delta doping. As used herein a SMASH barrier generally refers to a barrier in which successive well layers generally have an increasing band gap in the conduction band energy diagram.

In a strain-modulated aperiodic superlattice heterobarrier, successive well layers have an increasing band gap in the conduction band energy diagram for the SMASH as shown in FIG 1A for the InAlP/InGaP/GAAs system. A schematic drawing of the conduction band energy of a conventional multiple quantum barrier structure is shown in FIG. 1B. For the InAlP/InGaP/GaAs system, this corresponds to an increasing amount of strain in the consecutive wells of the superlattice. If a single quantum well is sandwich between a pair of SMASHs, the tendency of the electrons to thermalize into the well will be enhanced significantly because of the decreasing potential of the superlattice well layers towards the single quantum well. Once confined in the quantum well, the thermionic emission of the electrons will be greatly reduced due to the increased electron reflectivity of the SMASH. Therefore, the SMASH enhances the collection and confinement of the carriers. These arguments are confirmed both by theoretical calculations and by experimental observations.

A schematic diagram of an HFET device including a SMASH barrier is depicted in Fig. 2A, and generally referenced by numeral 100. HFET device 100 includes superlattice charge layers and at least one AlN barrier. As used herein a superlattice structure refers to a stack of repeating alternate layers.

The HFET device is formed on a substrate. Suitable substrates for the formation of an HFET include, but are not limited to c-plane (0001) Al_2O_3 (sapphire), 4H-SiC, 6H-SiC, thick AlN/sapphire, bulk GaN, AlN substrates, etc. While (0001) sapphire may be used for GaN growth because of its availability and relatively low cost, the lattice and thermal expansion coefficients are quite different from those of the Group III-N materials. It is believed that SiC has better thermal and lattice match to the Group III-N compounds, particularly to AlN, yet the crystalline quality of 6H- and 4H-SiC substrates is still not as high as sapphire. Furthermore, the surface roughness and subsurface damage for "typical" commercial SiC substrates are believed to be inferior to that of sapphire. While the cost of 2.0 in. diameter semi-insulating 4H-SiC substrates on the "open market" may be about forty times that of a 2.0 in. diameter sapphire substrate, the performance advantages of electronic devices fabricated from heteroepitaxial GaN/SiC films are documented.

In forming a device as disclosed herein, the quality of Group III-N epitaxial layers may be directly related to the quality and lattice constant of the substrate on which the Group III-N material is grown. For the growth of Group III-N epitaxial layers on sapphire or SiC substrates for high-power devices, low-pressure metalorganic chemical vapor deposition (MOCVD) or molecular-beam epitaxy (MBE) may be employed. For example, in an embodiment, GaN epitaxial layers may be grown in an EMCORE D125 reactor at pressures of ~200 Torr. In another embodiment, a Thomas Swan Close Coupled Showerhead (CCS) MOCVD reactor system with a seven wafer capacity may be used. Other reactor systems may also be suitably used to grow such structures. AlGaN layers may be grown in the same MOCVD reactor at ~50 Torr in order to avoid adduct formation as much as possible. Device structures may be grown in a H_2 ambient using adduct-purified trimethylgallium (TMGa) and trimethylaluminum (TMAl) as metal alkyl sources, and NH_3 as the nitrogen source. Silane (SiH_4) and bis(cyclopentadienyl)-magnesium (Cp_2Mg) may be employed as *n*-type and *p*-type dopants, respectively. Other

metalorganic, hydride and dopant sources may also be used, as are known in the art. A two-temperature growth process may be employed with a low-temperature thin AlN buffer layer (BL) for SiC substrates, and with high-temperature (HT) layers grown for the device active region. The MOCVD growth of GaN on SiC may begin with a ~100nm high temperature (*Tg*~1050 °C) AlN buffer layer, although various "graded AlGaN" conducting buffer layers have been developed for the growth of optoelectronic devices on SiC. In embodiments disclosed herein, it may be desirable to grow these layers without creating cracks in the epitaxial structure (e.g., by the use of various types of stress-relieving buffer layer structures).

In FIG. 2A, an undoped GaN layer is formed on a substrate of SiC. Undoped GaN layer may be formed from trimethyl gallium and ammonia in a MOCVD reactor at about 1050 °C.

A superlattice structure may be formed on top of the undoped GaN layer. In one embodiment, a SMASH superlattice structure is formed that includes alternating layers of undoped AlN and n-type doped AlGaN layers, as depicted in FIG. 2A. In FIG. 2A, superlattice includes 8 layers of alternating AlN and AlGaN layers. AlN layers are undoped and are formed by an epitaxial growth process. The AlGaN layer is then formed on top of the AlN process, with doping of the AlGaN layer occurring by introducing SiH_4 during into the reactor during the growth process. The layers are designed to create a superlattice heterobarrier that has a non-periodic structure. Fig. 2B depicts a schematic representation of the conduction band structure of HFET device 100.

Delta-doped binary-barrier (D^2B^2) HFET structures, and SMASH-FETs, may have several significant features. In an embodiment, a basic D^2B^2 HFET structure incorporates a binary AlN barrier and a delta-doped charge layer in the AlGaN near this AlN barrier. Such a structure may allow electrons to tunnel through this barrier and to enhance the free charge in the channel. Such structures may also reduce alloy scattering at the AlN-GaN interface as compared to an AlGaN-GaN interface.

AlGaN/GaN HFETs having a gate length of 0.2-0.5μm have been fabricated. Using the D^2B^2 structure, improved n_s x mobility product has been measured for electrons in the channel of an AlGaN/GaN HEMT. For example, in one experiment using a D^2B^2 AlGaN/GaN HFET structure, including a binary AlN barrier and an AlGaN delta-doped charge layer, a two-dimensional electron gas having a carrier mobility of μ_n = 1,058 cm2/V-s and a sheet carrier density of $n_s = 2.35\times10^{13}$ cm^{-2} at room temperature were obtained, resulting in a $n_s\,\mu_n$ product of 2.49×10^{16} /V-s. In experiments, AlGaN/AlN/GaN HFET devices with 0.15 μm gate lengths exhibited maximum current densities as high as I_{DSmax} = 1.8 A/mm at V_G = +1 V. FIG. 3 depicts a plot of I_{DS} vs. V_{DS} for an L_G=0.15 μm D^2B^2 AlGaN/AlN/GaN HFET. FIG. 4 depicts a plot of Transconductance vs. Gate Voltage for an L_G=0.15 μm D^2B^2 AlGaN/AlN/GaN HFET. FIG. 4 shows that such devices may exhibited peak transconductance of up to g_m = 350 mS/mm. FIG. 5 shows a plot of I_{DS} vs. V_{DS} for an L_G=0.25 μm D^2B^2 AlGaN/AlN/GaN HFET. FIG. 5 shows that AlGaN/AlN/GaN HFET devices with 0.25 μm gate lengths exhibited g_m = 240mS/mm. FIG. 6 depicts frequency response data for an L_G=0.25 μm D^2B^2 AlGaN/AlN/GaN HFET showing a current gain (h_{21}) and unilateral figure of merit (U) and indicating f_T = 50 GHz and f_{max} = 130 GHz.

L_G= 0.25 μm devices have demonstrated a record low-noise power for this gate length, as demonstrated in FIG. 7. FIG. 7 depicts the minimum noise figure and associated gain vs. frequency for V_{DS} = 10 V and 15V. The noise characteristics of these devices have been measured to be about 1.6 dB at 10 GHz, an exceptionally low value. Noise characterization was performed for the frequency range of 2-18 GHz to determine Γ_{opt}, the noise resistance (R_n), the minimum noise figure (F_{min}), and the associated gain (G_n). For L_G = 0.25μm D^2B^2 HFETs, a state-of-the-art

minimum noise figure of F_{min}=0.93 dB with 7 dB of associated gain was obtained at 17 GHz and at 10 GHz, the noise figure of the D^2B^2 HFET was 1.1 dB with 10 dB associated gain. These results indicate that the D^2B^2 structure may be compatible with high current densities, as well as with high-frequency and low-noise performance desired for *X*-band BMD-class receivers.

D^2B^2 devices having gate lengths of between about $L_G = 0.15\mu m$ and about $0.5\mu m$ have been formed. The devices may approximate short-gate lengths (e.g., for high-frequency applications) and longer-gate lengths (e.g., for high power devices). The formed devices have been used to evaluate the performance of the materials used to form the devices. In experiments, AlGaN/AlN/GaN HFET. FIG. 8 depicts a plot of I_{DS} vs. V_{DS} for an L_G=0.5 μm D^2B^2 AlGaN/AlN/GaN HFET. As shown in FIG. 8, devices with 0.5 μm gate lengths exhibited maximum current densities as high as $I_{DSmax} = 1.5$ A/mm at $V_{DS} = 9$ V. FIG. 9 depicts a plot of I_{DS} and g_m vs. V_G for an L_G=0.5 μm D^2B^2 AlGaN/AlN/GaN HFET. As shown in FIG. 9, the I_{DS}-V_G curves are nearly linear, corresponding to a large, relatively flat g_m vs. V_G curve. The peak I_{Dsmax} =1.4A/mm and g_m exceeds 230 mS/mm. It is believed that these values are record numbers for the performance of AlGaN/GaN HFETs with L_G approximately 0.5 μm (e.g., in the range of about 0.3 to 0.7μm). FIG. 10 shows the frequency response data for an $L_G = 0.5$ μm D^2B^2 AlGaN/AlN/GaN HFET indicating $f_T = 20$ GHz and f_{max} = about 75 GHz.

FIG. 12 depicts a plot of I_{DS} vs. V_{DS} for an L_G=0.15 μm D^2B^2 AlGaN/AlN/GaN HFET after metalization. As shown in FIG. 12, devices with 0.15 μm gate lengths exhibited maximum current densities as high as $I_{DSmax} > 1.8$ A/mm at $V_{DS} = 9$ V. Figs 12 and 13, the $L_G = 0.15$ μm devices exhibit even higher values of I_{DSmax} greater than 1.8 A/mm and g_m values as high as 330 mS/mm. It is believed that these values are record numbers for the performance of AlGaN/GaN HFETs with L_G approximately 0.15 μm. FIG. 13 depicts a plot of I_{DS} and g_m vs. V_G for an L_G=0.15 μm D^2B^2 AlGaN/AlN/GaN HFET after metalization. As shown in FIG. 13, the I_{DS}-V_G curves at V_{DS} are nearly linear, corresponding to a large, relatively flat g_m vs. V_G curve. The peak I_{Dsmax} >1.8A/mm and g_m exceeds 330 mS/mm.

Some known designs for high-power Group III-N gallium-nitride-based FETs employ a single AlGaN barrier layer to confine the electrons to the channel. This channel carries the current when the device is "ON." At high currents, high-energy charge carriers may be injected into this barrier reducing the current in the channel, lowering the effective mobility, and/or reducing the effect of the gate voltage on the current flow. In certain embodiments disclosed herein, the effective energy barrier may be increased by a significant amount due to quantum-mechanical reflection of carriers. Such reflections may enhance the performance of the device by maintaining the charge in the channel even for the high-current situations. Reflection may also improve the high-frequency performance. Certain embodiments may include both a superlattice and delta doping, which may provide more free charge carriers (electrons) to the channel than a conventional doped or undoped AlGaN charge layer.

An additional embodiment of an HFET design is represented schematically in FIG. 13. FIG. 13 depicts an embodiment of an HFET that includes an AlN barrier and delta-doped charge layer. While FIG. 13 depicts a SiC substrate, it should be understood that the HFET depicted in FIG. 13 may be formed on any other type of substrate as described previously. The process of forming an HFET as depicted in FIG. 13 includes forming a buffer layer of AlN on the substrate. As shown the buffer layer may be about 100 nm in thickness. Next a Si doped GaN layer is formed, the GaN layer may be doped with SiH_4 during epitaxial growth of the layer. A binary AlN and delta-doped AlGaN layer is then formed on top of the doped GaN layer. In one embodiment, the AlN barrier is a thin (< about 5 nm) layer. The doped AlGaN layer is formed on top of the barrier layer. In one embodiment, the doped AlGaN

layer has a composition of $Al_xGa_{1-x}N$ where x is about 0.2 to about 0.3. The AlGaN layer may be about 20 to 30 nm thick.

An additional embodiment of an HFET design is represented schematically in FIG. 14. FIG. 14 depicts an embodiment of an HFET that includes an AlN/GaN superlattice charge and buffer layer. While FIG. 14 depicts a SiC substrate, it should be understood that the HFET depicted in FIG. 14 may be formed on any other type of substrate as described previously. The process of forming an HFET as depicted in FIG. 14 includes forming a buffer layer of AlN on the substrate. As shown the buffer layer may be about 100 nm in thickness. An AlN/GaN superlattice buffer layer is formed. The superlattice buffer layer includes alternate layers of undoped AlN and GaN. Each of the layers may be about 2 nm or less in thickness. Next a Si doped GaN layer is formed, the GaN layer may be doped with SiH_4 during epitaxial growth of the layer. An AlN/GaN superlattice charge layer is formed on top of the doped GaN layer. The superlattice buffer layer includes alternate layers of undoped AlN and n-type doped GaN. Each of the layers may be about 2 nm or less in thickness.

An additional embodiment of an HFET design is represented schematically in FIG. 15. FIG. 15 depicts an embodiment of an HFET that includes an AlN barrier and delta-doped charge layer. While FIG. 15 depicts a SiC substrate, it should be understood that the HFET depicted in FIG. 15 may be formed on any other type of substrate as described previously. The process of forming an HFET as depicted in FIG. 5 includes forming a buffer layer of AlN on the substrate. As shown the buffer layer may be about 100 nm in thickness. Next a thin GaN layer is formed. A thin (< 5 nm) AlN barrier layer may be formed on the GaN layer. A superlattice structure may be formed on top of the undoped GaN layer. In one embodiment, a SMASH superlattice structure is formed that includes alternating layers of undoped AlN and n-type doped AlGaN layers. Doping of the AlGaN layer occurring by introducing SiH_4 during into the reactor during the growth process. The layers are designed to create a superlattice heterobarrier that has a non-periodic structure.

The HFET device performance, particularly for high-power operation, depends on many factors, including the source and drain Ohmic contact resistance. Generally, this contact is placed upon the "top" of the AlGaN "charge layer." In some embodiments, the AlGaN layer has been selectively removed to provide a more direct contact. For n-type GaN:Si and AlGaN:Si layers, both Ti/Al/Pt/Au and Ti/Ag/Au systems may be used to form contacts. In one embodiment, an n-type Ti/Al/Pt/Au contact scheme reproducibly shows the lowest TLM specific contact resistance using a 850C/30s anneal. These n-type Ohmic contacts have a specific contact resistance to n-type GaN:Si (n-$2x10^{18}$ cm) of $Rc<1x10^{-6}$Q-cm^2. Ohmic contact resistance to undoped AlGaN (typical of the electron barrier in HFETs) is generally higher. Recently, we have identified an new Ohmic contact scheme employing vanadium-based contacts for n-type AlGaN films which may improve Ohmic contacts to high Al-composition $Al_xGal_{1-x}N$ films with specific contact resistances as low as $4x10^{-5}$ Ohm-cm^2 for x = about 0.60 films.

SiN_x may be used as an amorphous dielectric insulator to improve the leakage characteristics and stability of the Gate for AlGaN/GaN HFETs. This film may be deposited immediately after the growth of the AlGaN charge layer in the MOCVD reactor. This "in-situ" passivation and Gate layer may provide a stable, low-leakage dielectric film to stabilize the surface charges due to the "free AlGaN" surface. It is widely known that GaN films "dissociate" during the "cool-down" process when the wafer is exposed to elevated temperatures in an H_2 + NH_3 environment. AlGaN also degrades in the same way, albeit at a somewhat reduced rate. This process may be especially rapid near a screw or edge dislocation. A stable, amorphous SiN_x film may be grown directly on the AlGaN layer-this will stabilize the AlGaN surface and inhibit the increase in leakage currents and Gate breakdown under high-stress

operating conditions. The gate metal may be deposited upon this thin SiN_x layer, creating an insulated gate structure. The in-situ SiN_X layer may be capped with an additional plasma-enhanced chemical vapor deposition (PECVD) SiN_X film in the regions between the Gate and the Source and the Gate and the Drain to improve the stability of the surfaces in these regions as well. The in-situ-deposited SiN_X film may reduce the leakage contributions from these areas as well.

Cl-based inductively coupled plasma (ICP) etching may be used for the device isolation processing. This is a relatively low-damage etching process. Alternatively, wet etching with KOH solutions is known to improve the leakage current density for *p-i-n* diodes and may be used for device isolation etching of HFETs as well. The stability of the mesa surfaces may play a role in the operation of the device under high-power conditions.

The commonly used gate metal for an HFET is Ni/Au because it is convenient and is compatible with submicron processing. Other gate metals may be used including W or WSi.

EXAMPLE

An unpassivated delta-doped, binary barrier (D^2B^2) HFET device with 0.15 μm-gate length was formed. The $Al_xGa_{1-x}N$/GaN ($x \approx 0.2, 1.0$) heterostructures of this work were grown by low-pressure metalorganic chemical vapor deposition (MOCVD) in an EMCORE TurboDisc D125 UTM high-speed rotating-disk reactor on 2.0 in. diameter 4H semi-insulating SiC substrates. The GaN epitaxial layer is grown at pressures of about 200 Torr and the AlGaN epitaxial layers are grown at about 50 Torr in a hydrogen ambient using adduct-purified trimethyl gallium (TMGa), trimethylaluminum (TMAl), and ammonia (NH_3). Silane (SiH_4) was used for the *n*-type dopant. The growth process begins with a high-temperature (about 1070 °C) AlN buffer layer, 100 nm in thickness. The subsequent device layers are grown at about 1050 °C, beginning with 3 μm of undoped GaN. On top of this is a 1 nm AlN barrier layer, followed by a 30 nm layer of $Al_xGa_{1-x}N$ (x is about 0.2). The delta doping occurs after 5nm of growth of this last layer, with an expected Si dopant concentration > 1×10^{19} cm^{-3} (as measured by secondary ion mass spectroscopy (SIMS) analysis on similarly doped structures). Room-temperature Hall-effect measurements yield an electron mobility of 1,066 cm^2/V-s and a sheet carrier density of 2.30×10^{13} cm^{-2}, resulting in a large $n_s\mu$ product of 2.45×10^{16} /V-s. This is a large improvement over a similar structure without the barrier layer and delta doping: Hall results were 1,308 cm^2/V-s, 1.18×10^{13} cm^{-2}, and 1.54×10^{16} /V-s, for mobility, sheet charge, and $n_s\mu$ product, respectively. Variable-temperature Hall-effect measurements were also performed over the temperature range from 77 K to 290 K. The sheet carrier density remained fairly constant over the measured temperature range, while the mobility steadily increased for lower temperatures, indicating that the 2DEG dominated the electrical transport characteristics.

D^2B^2 HFET devices were then fabricated from the epitaxial heterostructures. Using chlorine as the active species, a dry etch to a depth of 250 nm was performed for device isolation. A metallization scheme consisting of Ti/Al/Ti/Au was deposited by a conventional lift-off process and rapid thermal annealed at 950°C to obtain Ohmic contacts. From standard TLM measurements, the contact resistance was calculated to range from 0.68 to 0.87 Ohms-mm. The Ni/Au Schottky-barrier T-gate was defined by electron-beam lithography with a tri-layer resist structure (5.5% PMMA/ 8.5% P(MMA-MAA)/4% PMMA). HFET devices with gate lengths of 0.5 μm and 0.15 μm have been fabricated to investigate power device performance and high-frequency performance, respectively. The standard device has two parallel gate fingers, with a gate width of 75 μm. No passivation has been used for the devices reported here.

WHAT IS CLAIMED IS:

1. A field-effect transistor comprising:
a substrate;
an undoped GaN layer formed on the substrate; and
a superlattice structure formed on the undoped GaN layer, wherein the superlattice structure comprises alternating layers of a barrier layer of AlN and a doped layer of AlGaN.

2. The transistor of claim 1, wherein the substrate comprises SiC.

3. The transistor of claim 1, wherein the substrate comprises sapphire.

4. The transistor of claim 1, further comprising an AlN buffer layer disposed between the substrate and the first layer.

5. The transistor of claim 1, wherein the doped AlGaN layer is an n-type doped layer.

6. The transistor of claim 1, wherein the doped layer AlGaN layer is an n-type doped layer, and wherein the doping comprises Si.

7. The transistor of claim 1, wherein the doped layer comprises $Al_xGa_{1-x}N$, where x is from 0.2 to about 0.3.

8. The transistor of claim 1, wherein the superlattice structure comprises a strain-modulated aperiodic superlattice heterobarrier.

9. A method of making a field-effect transistor comprising:
forming an undoped GaN layer on a substrate;
forming a superlattice structure on the undoped GaN layer, wherein the superlattice structure comprises alternating layers of a barrier layer of AlN and a doped layer of AlGaN.

10. The method of claim 9, wherein the substrate comprises SiC.

11. The method of claim 9, wherein the substrate comprises sapphire.

12. The method of claim 9, further comprising forming an AlN layer between the substrate and the GaN layer.

13. The method of claim 9, wherein the doped AlGaN layer is an n-type doped layer.

14. The method of claim 9, wherein the doped layer AlGaN layer is an n-type doped layer, and wherein the doping comprises Si.

15. The method of claim 9, wherein the doped layer comprises $Al_xGa_{1-x}N$, where x is from 0.2 to about 0.3.

16. The method of claim 9, wherein the superlattice structure is formed as a strain-modulated aperiodic superlattice heterobarrier.

17. A field-effect transistor comprising:
a substrate;
a doped GaN layer formed on the substrate;
an AlN barrier layer formed on the doped GaN layer; and
a doped layer of AlGaN formed on the AlN barrier layer.

18. The transistor of claim 17, wherein the substrate comprises SiC.

19. The transistor of claim 17, wherein the substrate comprises sapphire.

20. The transistor of claim 17, further comprising an AlN buffer layer disposed between the substrate and the first layer.

21. The transistor of claim 17, wherein the doped AlGaN layer is an n-type doped layer.

22. The transistor of claim 17, wherein the doped layer AlGaN layer is an n-type doped layer, and wherein the doping comprises Si.

23. The transistor of claim 17, wherein the doped layer comprises $Al_xGa_{1-x}N$, where x is from 0.2 to about 0.3.

24. A method of making a field-effect transistor comprising:
forming a doped GaN layer on a substrate;
forming an AlN barrier layer on the doped GaN layer; and
forming a doped layer of AlGaN on the AlN barrier layer.

25. The method of claim 24, wherein the substrate comprises SiC.

26. The method of claim 24, wherein the substrate comprises sapphire.

27. The method of claim 24, further comprising forming an AlN layer between the substrate and the GaN layer.

28. The method of claim 24, wherein the doped AlGaN layer is an n-type doped layer.

29. The method of claim 24, wherein the doped layer AlGaN layer is an n-type doped layer, and wherein the doping comprises Si.

30. The method of claim 24, wherein the doped layer comprises $Al_xGa_{1-x}N$, where x is from 0.2 to about 0.3.

31. A field-effect transistor comprising:
a substrate;
a first superlattice structure, wherein the first superlattice structure comprises alternating layers of AlN and GaN;
a doped GaN layer formed on the first superlattice structure; and
a second superlattice structure formed on the doped GaN layer, wherein the second superlattice structure comprises alternating layers of a barrier layer of AlN and doped AlGaN.

32. The transistor of claim 31, wherein the substrate comprises SiC.

33. The transistor of claim 31, wherein the substrate comprises sapphire.

34. The transistor of claim 31, further comprising an AlN buffer layer disposed between the substrate and the first superlattice structure.

35. The transistor of claim 31, wherein the doped AlGaN layer is an n-type doped layer.

36. The transistor of claim 31, wherein the doped layer AlGaN layer is an n-type doped layer, and wherein the doping comprises Si.

37. The transistor of claim 31, wherein the doped layer comprises $Al_xGa_{1-x}N$, where x is from 0.2 to about 0.3.

38. A method of making a field-effect transistor comprising:
forming a first superlattice structure on a substrate, wherein the first superlattice structure comprises alternating layers of AlN and GaN;
forming a doped GaN layer on the first superlattice structure; and
forming a second superlattice structure on the doped GaN layer, wherein the second superlattice structure comprises alternating layers of a barrier layer of AlN and doped AlGaN.

39. The method of claim 38, wherein the substrate comprises SiC.

40. The method of claim 38, wherein the substrate comprises sapphire.

41. The method of claim 38, further comprising forming an AlN layer between the substrate and the first superlattice structure.

42. The method of claim 38, wherein the doped AlGaN layer is an n-type doped layer.

43. The method of claim 38, wherein the doped layer AlGaN layer is an n-type doped layer, and wherein the doping comprises Si.

44. The method of claim 38, wherein the doped layer comprises $Al_xGa_{1-x}N$, where x is from 0.2 to about 0.3.

45. A transistor comprising a plurality of layers on a substrate, wherein a portion of the layers comprise combinations of nitrogen with one or more elements selected from group III of the periodic table to form a strain-modulated aperiodic superlattice heterobarrier, and wherein one or more of the layers comprises an AlN barrier layer.

46. The transistor of claim 45 further comprising at least one delta doped region in at least one of the layers.

47. A method of forming a transistor comprising:
providing a substrate; and
depositing a plurality of layers on the substrate, wherein a portion of the layers comprise combinations of nitrogen with one or more elements selected from group III of the periodic table to form a strain-modulated aperiodic superlattice heterobarrier, and wherein one or more of the layers comprises an AlN barrier layer.

48. The method of claim 47, further comprising, delta-doping at least one of the layers.

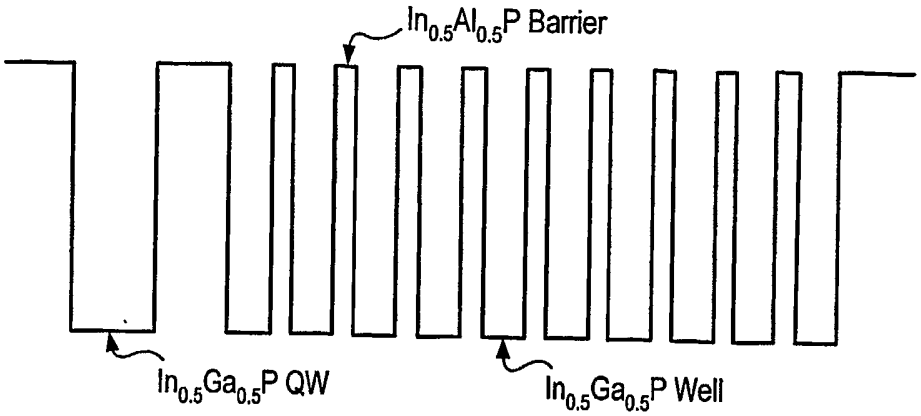

$In_{0.5}Al_{0.5}P$ Barrier
$In_{0.5}Ga_{0.5}P$ QW
$In_{0.5}Ga_{0.5}P$ Well

Fig. 1A

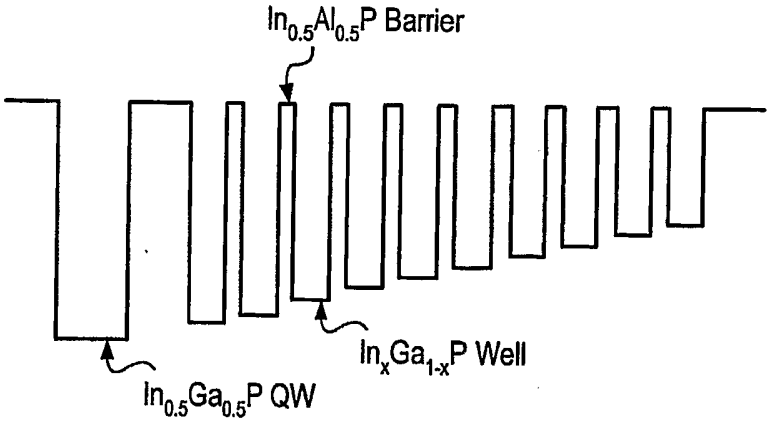

$In_{0.5}Al_{0.5}P$ Barrier
$In_xGa_{1-x}P$ Well
$In_{0.5}Ga_{0.5}P$ QW

Fig. 1B

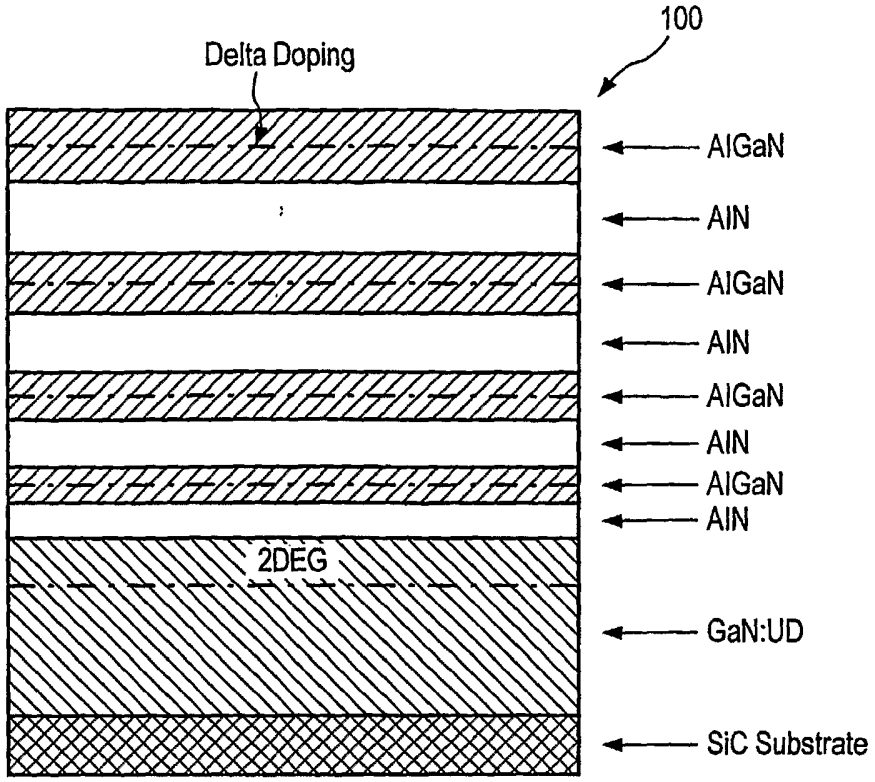

100
Delta Doping
AlGaN
AlN
AlGaN
AlN
AlGaN
AlN
AlGaN
AlN
2DEG
GaN:UD
SiC Substrate

Fig. 2A

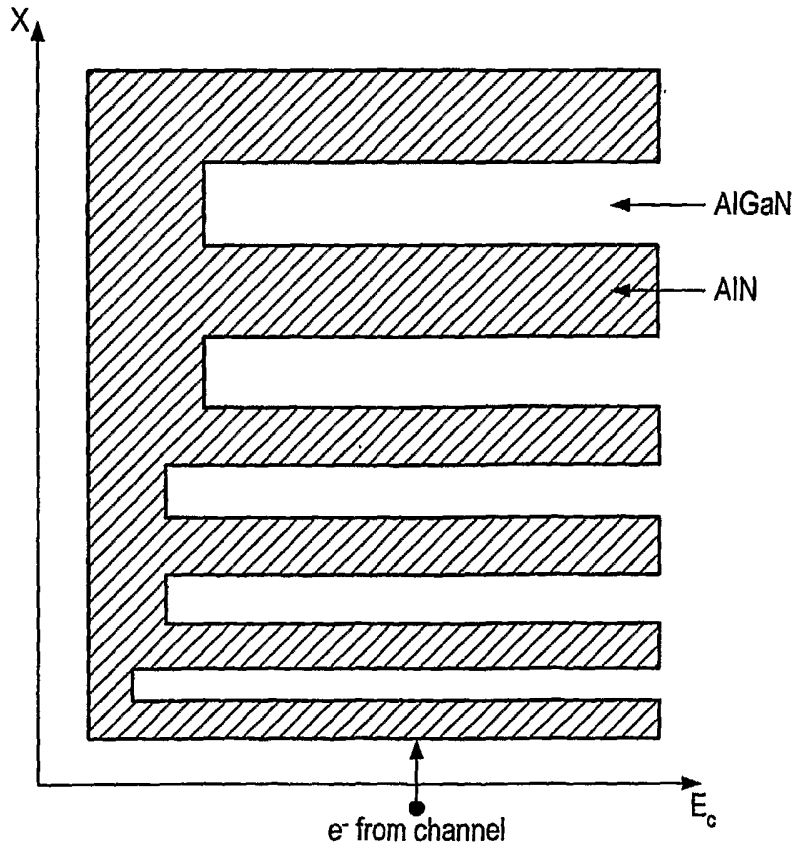

X
AlGaN
AlN
E_c
e⁻ from channel

Fig. 2B

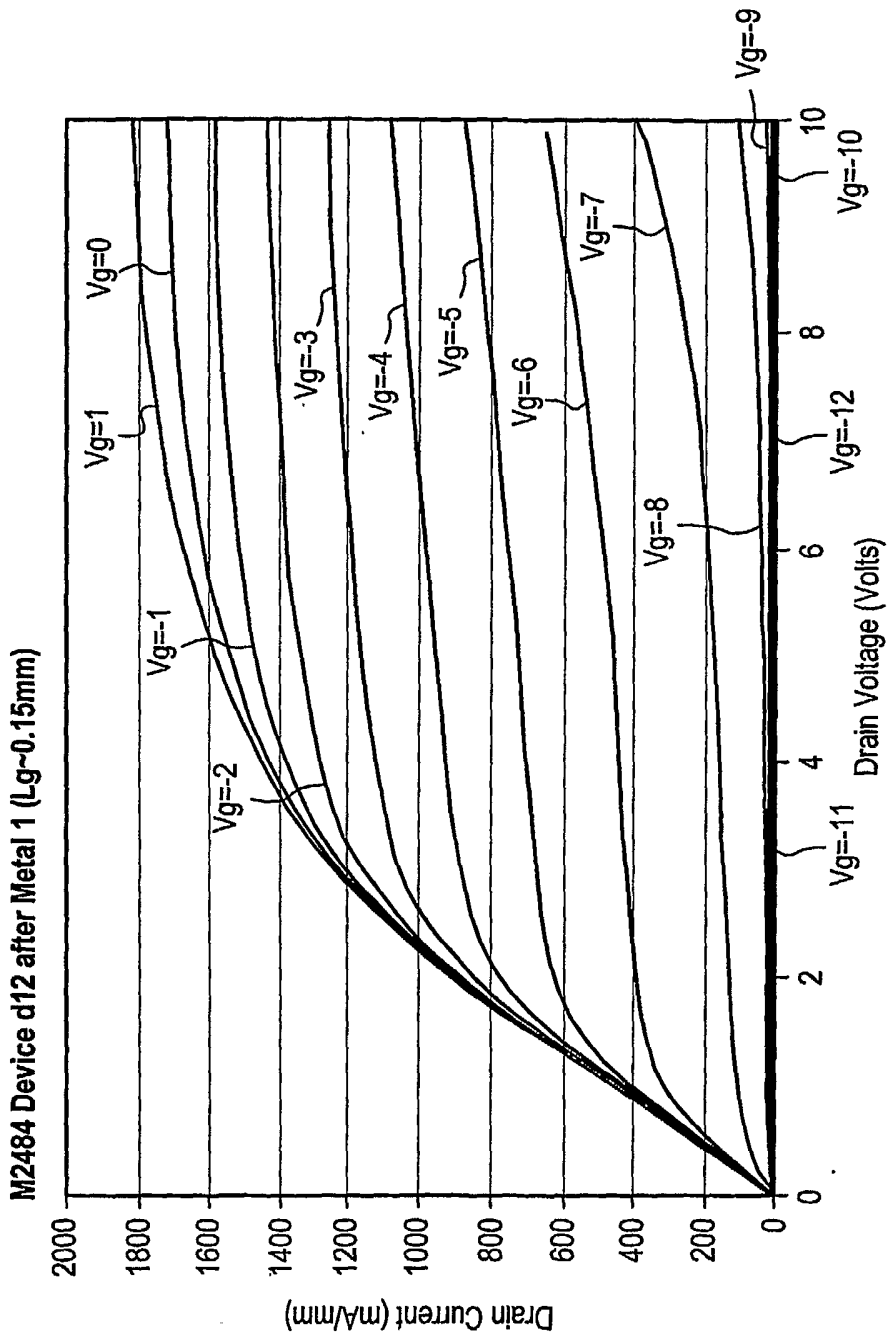

M2484 Device d12 after Metal 1 (Lg~0.15mm)
Drain Current (mA/mm)
Drain Voltage (Volts)
Vg=1
Vg=0
Vg=-1
Vg=-2
Vg=-3
Vg=-4
Vg=-5
Vg=-6
Vg=-7
Vg=-8
Vg=-9
Vg=-10
Vg=-11
Vg=-12
2000
1800
1600
1400
1200
1000
800
600
400
200
0
0
2
4
6
8
10

Fig. 3

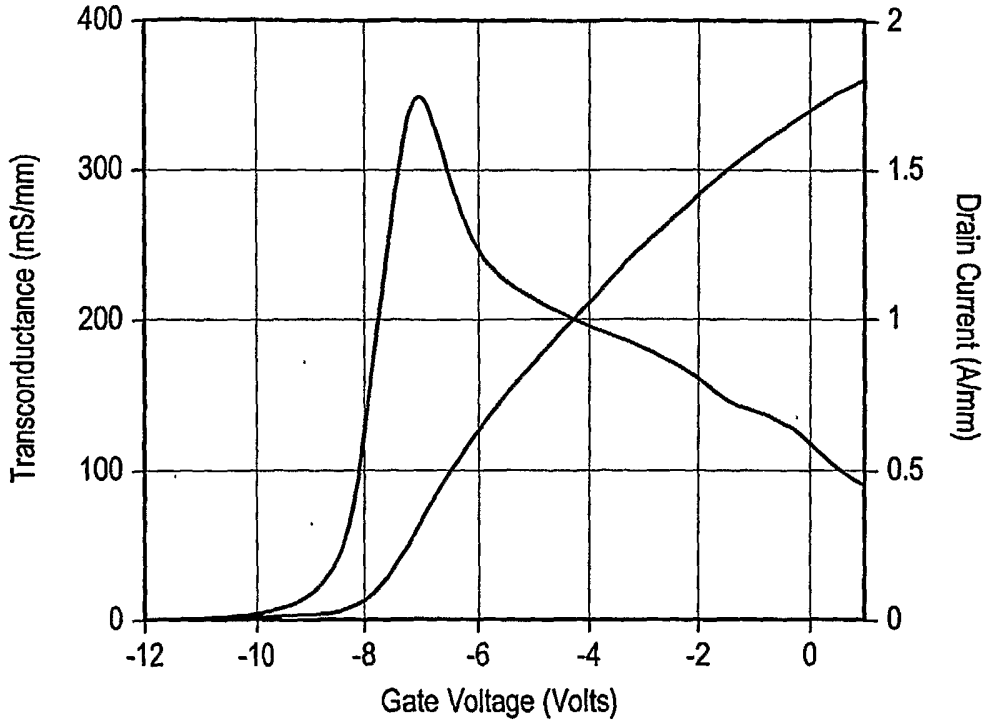

400
300
200
100
0
2
1.5
1
0.5
0
-12
-10
-8
-6
-4
-2
0
Transconductance (mS/mm)
Drain Current (A/mm)
Gate Voltage (Volts)

Fig. 4

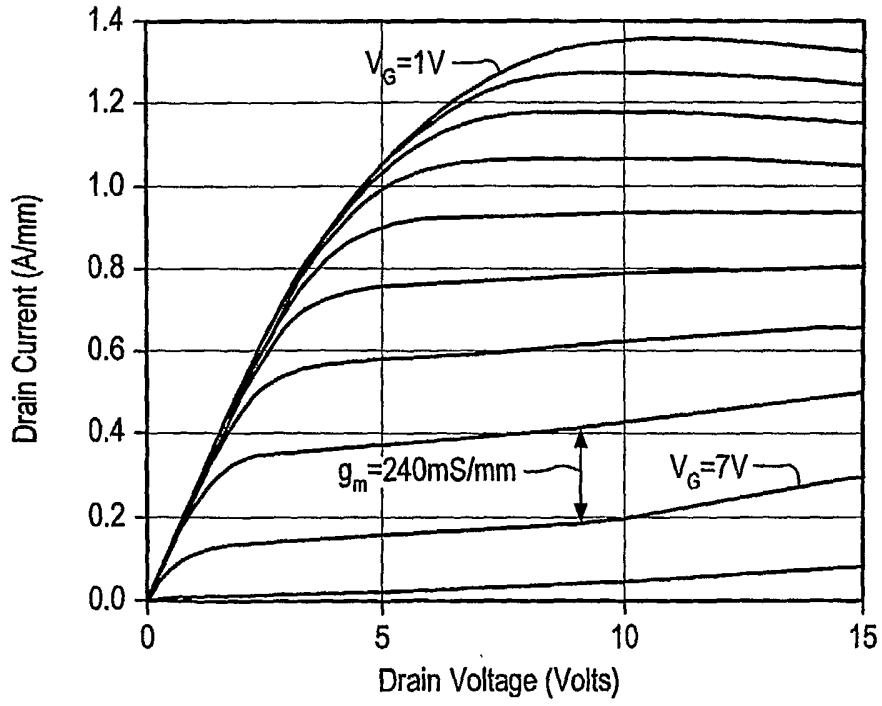

1.4
1.2
1.0
0.8
0.6
0.4
0.2
0.0
0
5
10
15
V_G=1V
g_m=240mS/mm
V_G=7V
Drain Current (A/mm)
Drain Voltage (Volts)

Fig. 5

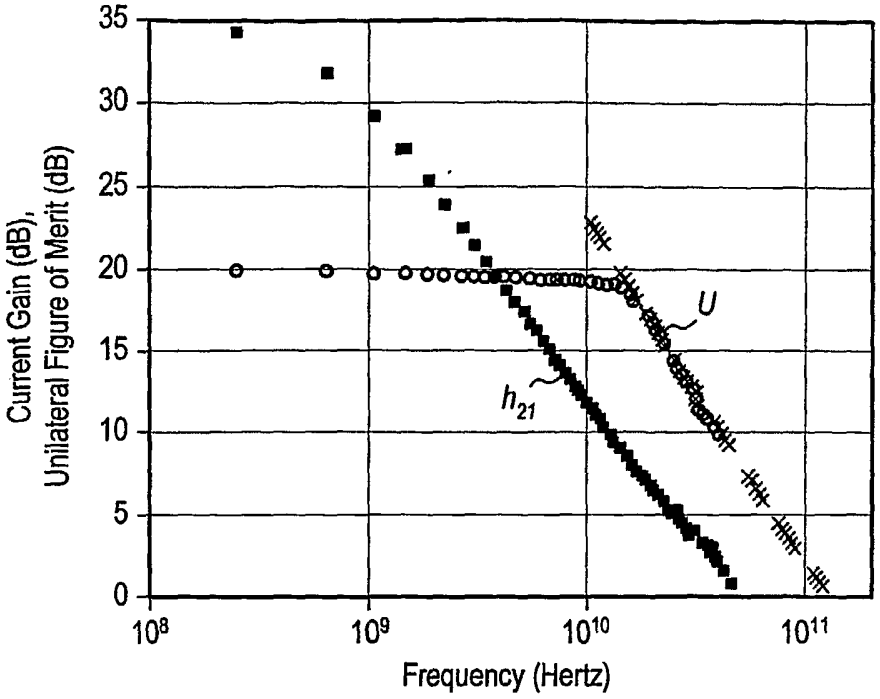

Current Gain (dB),
Unilateral Figure of Merit (dB)
35
30
25
20
15
10
5
0
10^8
10^9
10^{10}
10^{11}
Frequency (Hertz)
U
h_{21}

Fig. 6

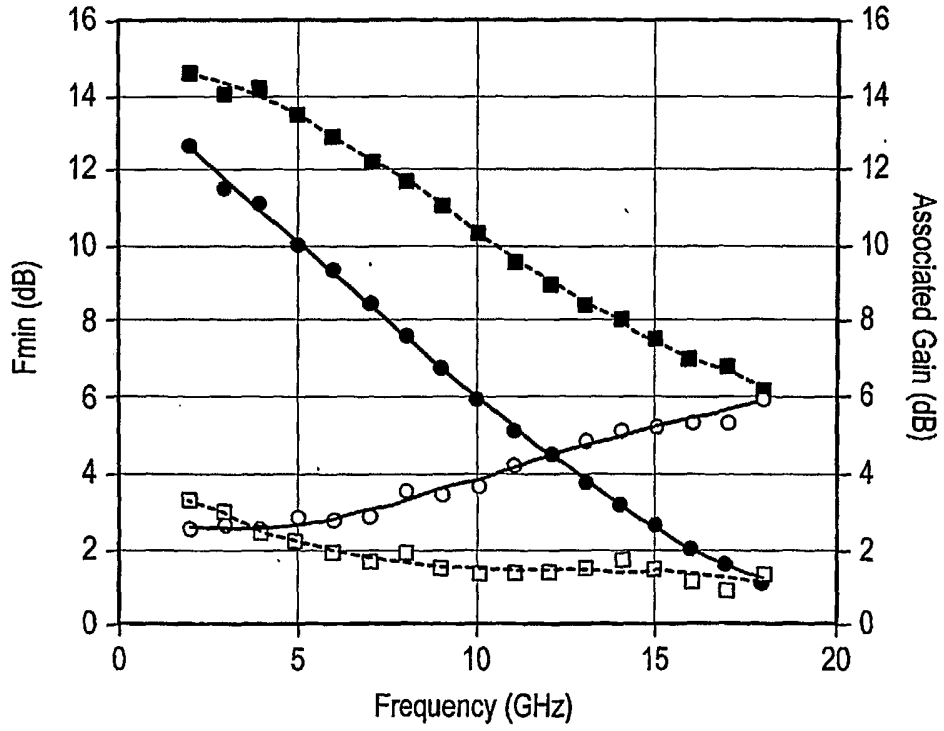

Fmin (dB)
Associated Gain (dB)
16
14
12
10
8
6
4
2
0
0
5
10
15
20
Frequency (GHz)

Fig. 7

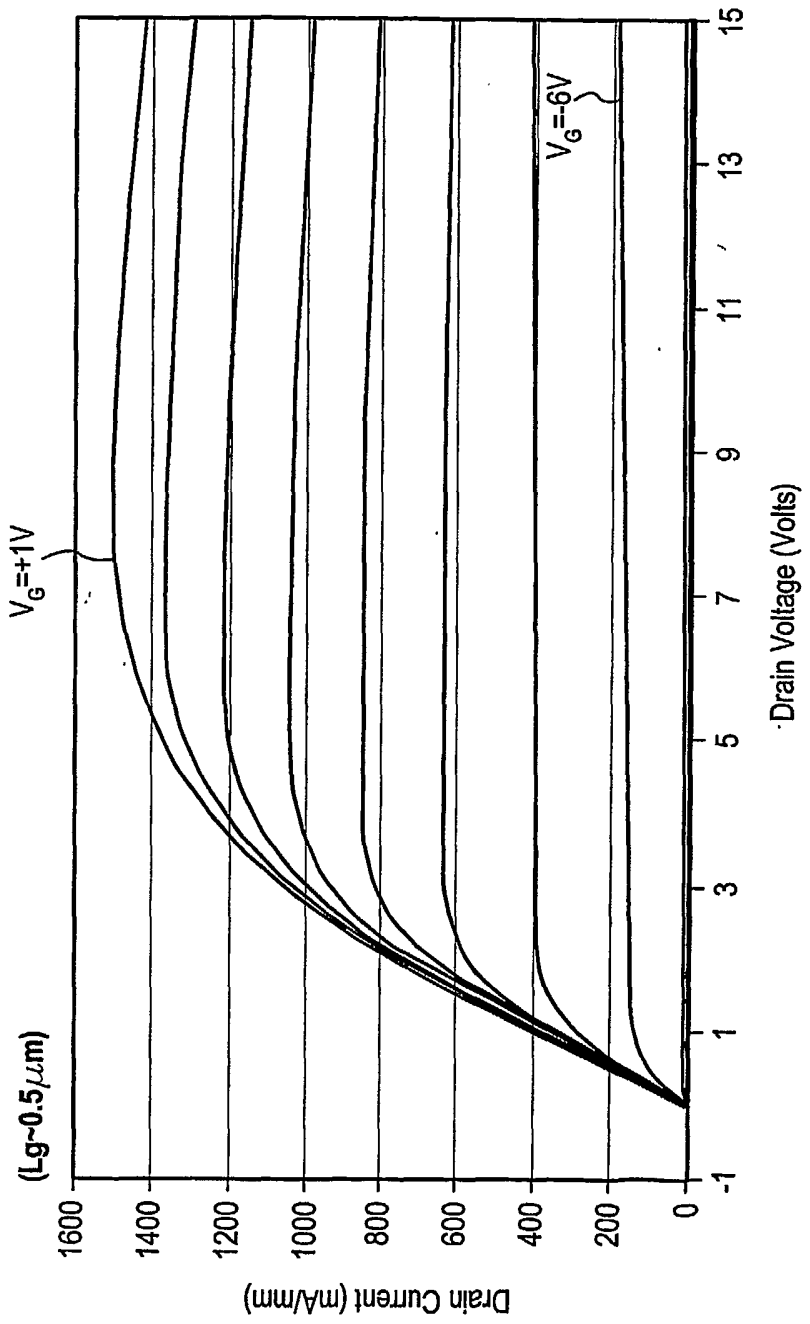

(Lg~0.5μm)
V_G=+1V
V_G=-6V
Drain Current (mA/mm)
1600
1400
1200
1000
800
600
400
200
0
-1
1
3
5
7
9
11
13
15
Drain Voltage (Volts)

Fig. 8

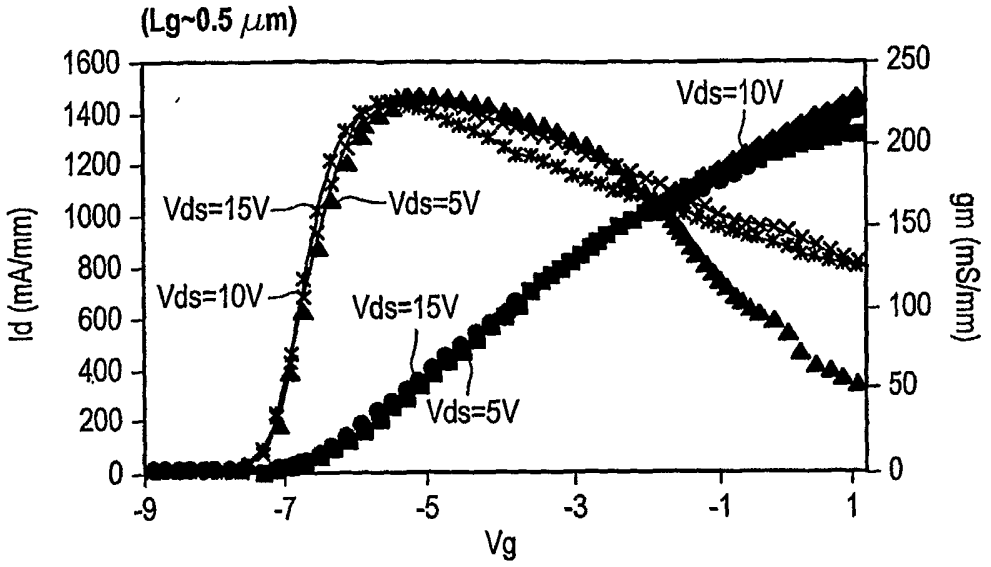

(Lg~0.5 μm)
Id (mA/mm)
gm (mS/mm)
Vg
Vds=10V
Vds=15V
Vds=5V
Vds=10V
Vds=15V
Vds=5V
1600
1400
1200
1000
800
600
400
200
0
250
200
150
100
50
0
-9
-7
-5
-3
-1
1

Fig. 9

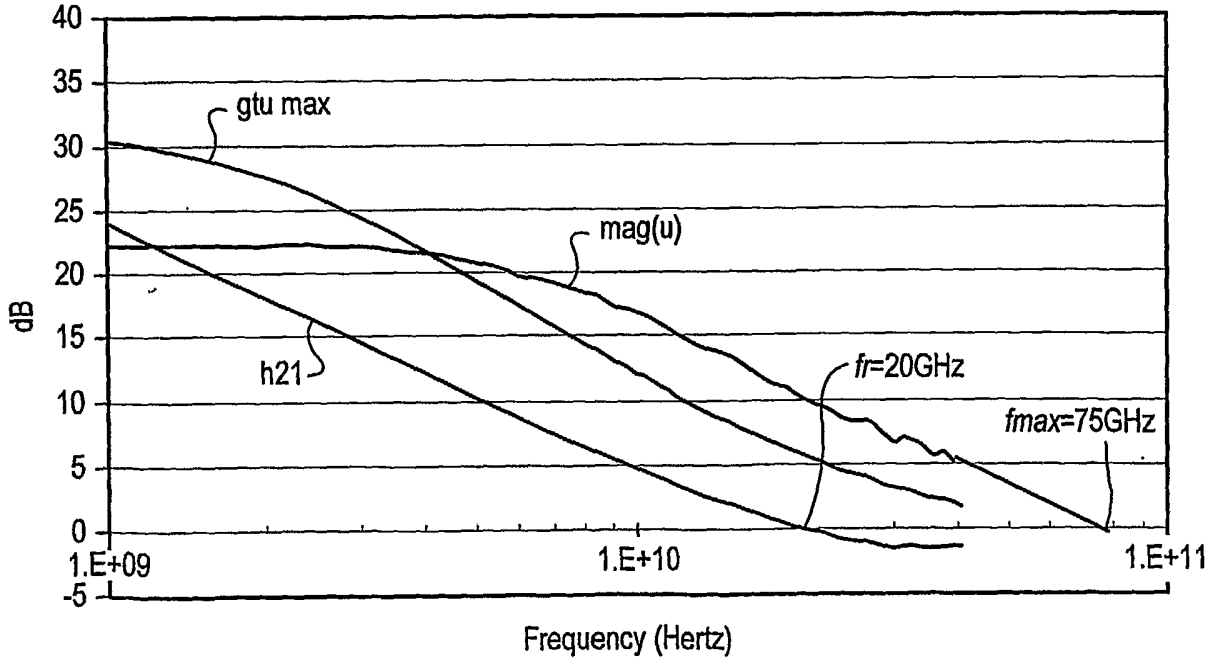

dB
Frequency (Hertz)
gtu max
mag(u)
h21
fr=20GHz
fmax=75GHz
40
35
30
25
20
15
10
5
0
-5
1.E+09
1.E+10
1.E+11

Fig. 10

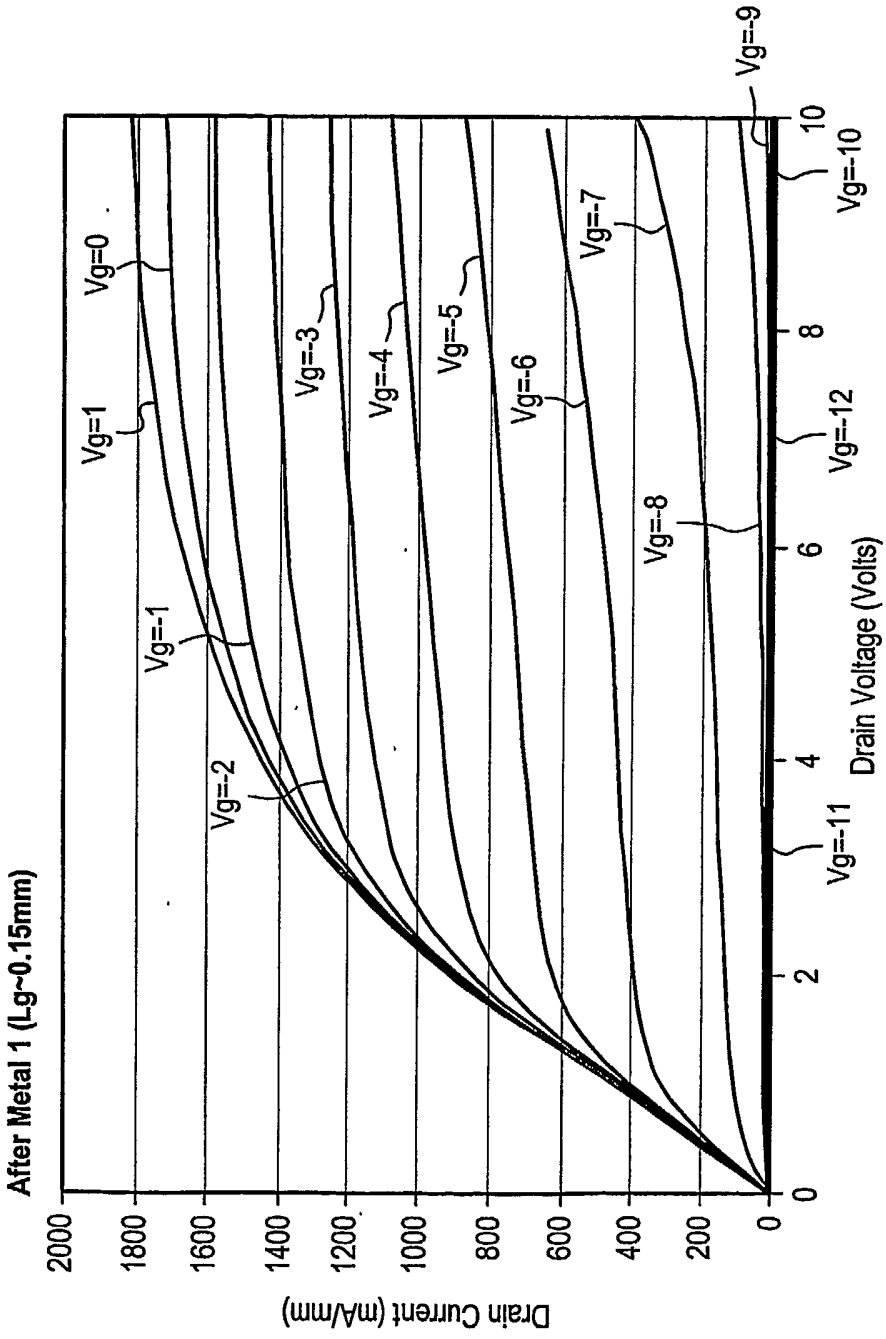

After Metal 1 (Lg~0.15mm)
Drain Current (mA/mm)
Drain Voltage (Volts)
Vg=1
Vg=0
Vg=-1
Vg=-2
Vg=-3
Vg=-4
Vg=-5
Vg=-6
Vg=-7
Vg=-8
Vg=-9
Vg=-10
Vg=-11
Vg=-12
0
200
400
600
800
1000
1200
1400
1600
1800
2000
0
2
4
6
8
10

Fig. 11

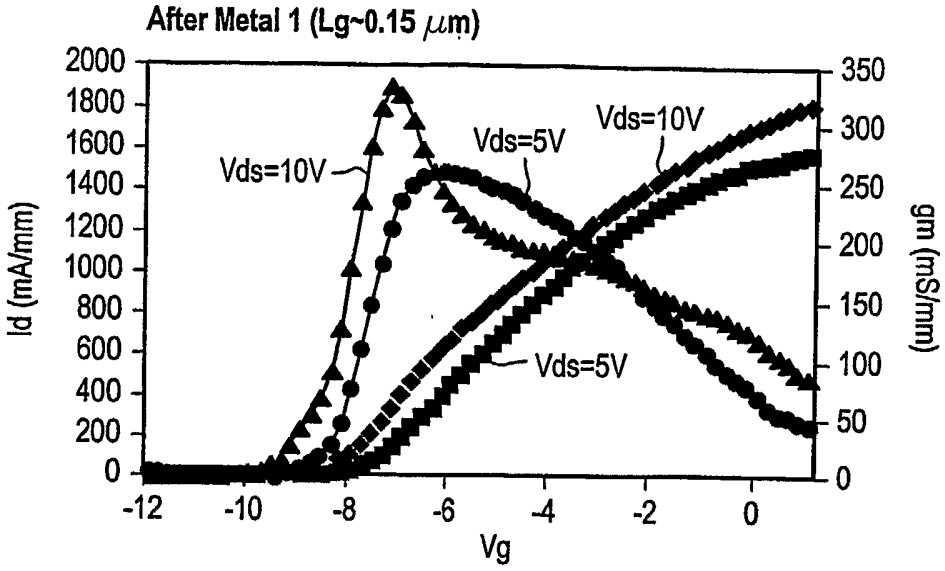

After Metal 1 (Lg~0.15 μm)
Id (mA/mm)
gm (mS/mm)
Vg
Vds=10V
Vds=5V
Vds=10V
Vds=5V
2000
1800
1600
1400
1200
1000
800
600
400
200
0
350
300
250
200
150
100
50
0
-12
-10
-8
-6
-4
-2
0

Fig. 12

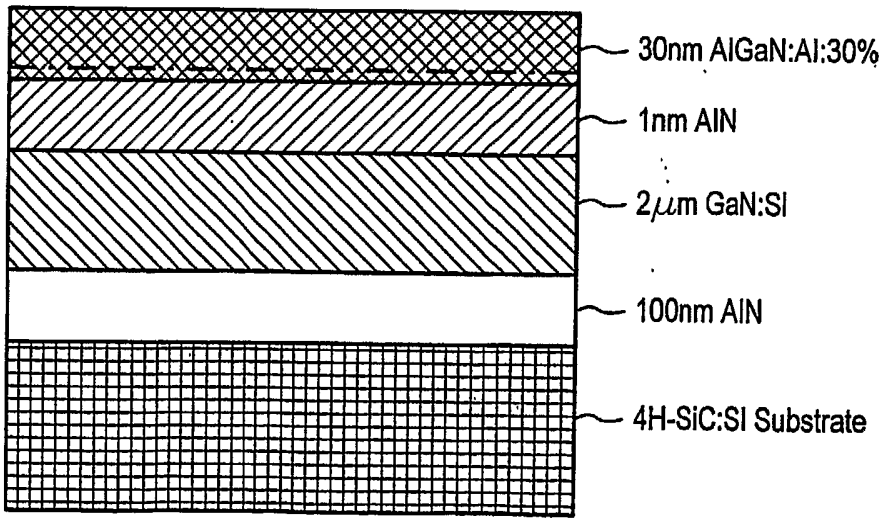

30nm AlGaN:Al:30%
1nm AlN
2μm GaN:SI
100nm AlN
4H-SiC:SI Substrate

Fig. 13

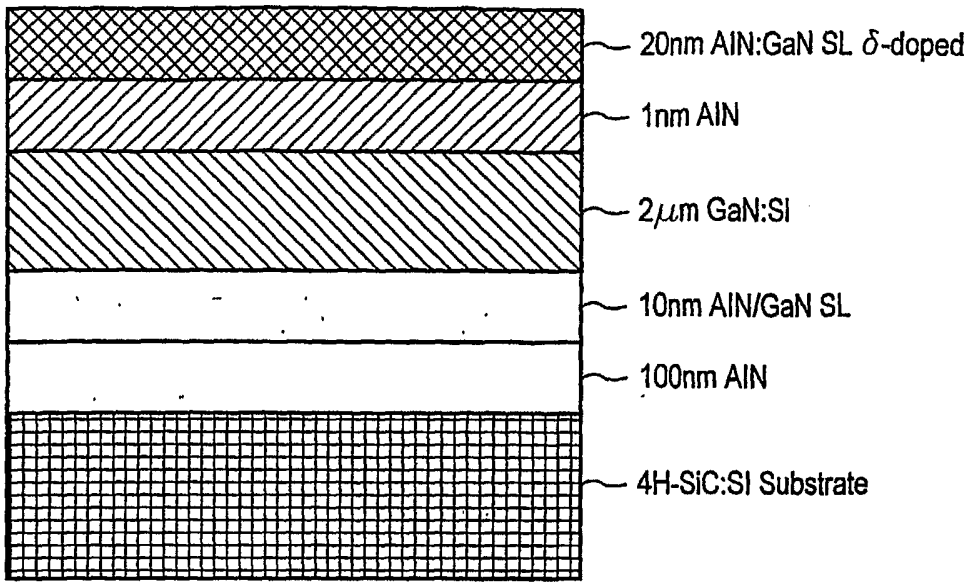

20nm AlN:GaN SL δ-doped
1nm AlN
2μm GaN:SI
10nm AlN/GaN SL
100nm AlN
4H-SiC:SI Substrate

Fig. 14

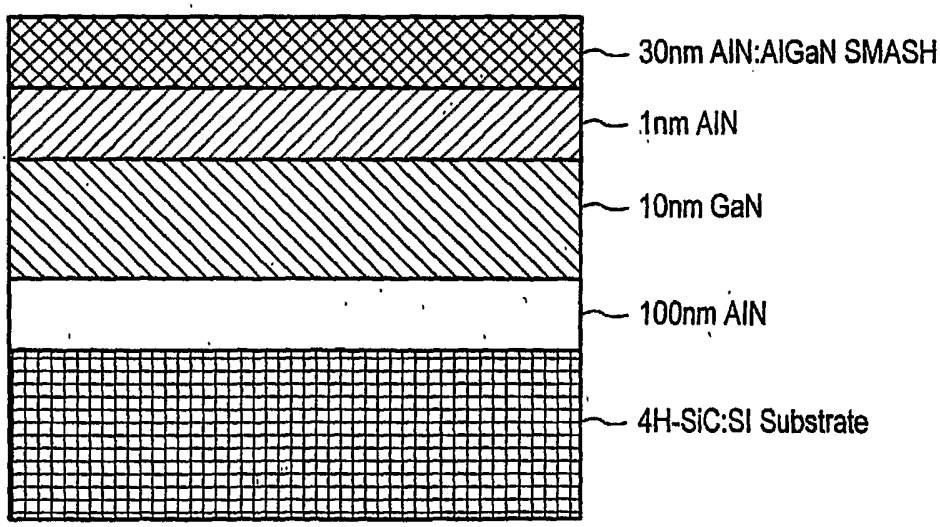

30nm AlN:AlGaN SMASH
1nm AlN
10nm GaN
100nm AlN
4H-SiC:SI Substrate

Fig. 15