

COATED SUBSTRATE FOR USE IN SENSORS

[0001] This application claims the benefit of priority under 35 U.S.C. § 119 of U.S. Provisional Application Serial No. 62/106894 filed on January 23, 2015 the content of which is relied upon and incorporated herein by reference in its entirety.

BACKGROUND

Field

[0002] The disclosure relates to a coated substrate for use in a sensor, and more particularly to a coated substrate for use in a capacitive fingerprint sensor embedded in a cover assembly of an electronic device.

Background

[0003] There is an increasing demand to incorporate sensor elements, such as fingerprint sensors, into electronic devices having touchscreens, such as cellular phones, tablets, and notebooks. Sensor elements can be convenient and useful for consumers. For example, fingerprint sensors are advantageous because they add an extra layer of security beyond password protection so that if your device is stolen, the thief cannot gain access to your personal information stored in the device without your fingerprint.

[0004] Many electronic devices having touchscreens have a protective cover made of glass. The challenge with incorporating sensor elements, such as fingerprint sensors, into such devices is that if the sensor element is placed under the cover glass, then the sensitivity and resolution of the sensor is not adequate if the cover glass is too thick. A need exists to embed sensor elements within the protective cover glass so that the thickness of the cover glass does not affect the sensitivity of the sensor element while ensuring a surface of the sensor element that is part of an outer surface of the electronic device has a coating stack that protects the surface against damage from electrostatic discharge, has scratch and impact resistant, and meet aesthetic requirements, such as color.

SUMMARY

[0005] Disclosed herein is a coated substrate for use in a sensor, a sensor including the coated substrate, and an electronic device including the sensor having the coated substrate.

[0006] In some embodiments, a coated substrate for use in a sensor includes a substrate having a first surface, a second surface opposing the first surface, at least one via hole extending from the first surface to the second surface, and a rigidity of greater than $0.03 \text{ Pa} \cdot \text{m}^3$; a metal layer disposed on the first surface of the substrate; an electrostatic discharge protection layer disposed on the metal layer having a dielectric breakdown voltage greater than $200 \text{ V}/\mu\text{m}$; and an outermost layer disposed on the electrostatic discharge protection layer providing scratch resistance and impact resistance.

BRIEF DESCRIPTION OF THE DRAWINGS

[0007] Fig.1 is a top plan view of an exemplary electronic device having a cover assembly with an embedded sensor substrate.

[0008] Fig. 2 is an exemplary cross section of the sensor substrate.

[0009] Fig. 3 is a first exemplary coating stack.

[0010] Fig. 4 is a second exemplary coating stack.

[0011] FIG. 5 is a plot of wavelength in nm vs. % reflection for glass samples having a white ink coating with a silicon layer of 5 nm, 10 nm, 20 nm, 30 nm, 40 nm, and 50 nm.

[0012] FIG. 6 is a plot of wavelength in nm vs. % reflection for bare glass samples having a silicon layer of 5 nm, 10 nm, 20 nm, 30 nm, 40 nm, and 50 nm.

DETAILED DESCRIPTION

[0013] Reference will now be made in detail to the present preferred embodiment(s), an example(s) of which is/are illustrated in the accompanying drawings. Whenever possible, the same reference numerals will be used throughout the drawings to refer to the same or like parts.

[0014] Incorporating sensor elements into electronic devices having touchscreens with a protective glass cover poses some challenges. For example, the sensor element is typically positioned under the protective glass in order to protect the sensor element from damage. However, this reduces the sensitivity and resolution of the sensor element. Also, in some instances, if the glass covering the sensor element is too thick, then the sensor element will

not operate properly. A solution to the above problem is to embed a sensor element within a cover glass such that a substrate of the sensor element is flush with an outer surface of the cover glass as discussed in U.S. Appl. No. 61/953,019, filed March 14, 2014 and U.S. Appl. No. 62/036,320, filed August 12, 2014, each of which is hereby incorporated by reference in its entirety. When the sensor substrate is part of the outer surface of the electronic device, it is vulnerable to damage from electrostatic discharge, as well as damage to scratches and impacts with foreign objects. A solution for protecting the surface of the sensor substrate is to apply a coating stack that will provide protection from electrostatic discharge damage and provide scratch and impact resistance. The coating stack can also address aesthetic requirements, such as color specifications.

[0015] FIG. 1 illustrates an exemplary embodiment of an electronic device 10 having a cover assembly 12 with a sensor substrate 14 embedded in an opening of a cover substrate 16. In some embodiments, cover substrate 16 can be glass, ceramic, glass-ceramic, or sapphire.

[0016] FIG. 2 illustrates a cross-section view of sensor substrate 14 having a first surface 18 and an opposing second surface 20. It is noted that the figures are not to scale. First surface 18 of sensor substrate 14 faces can be positioned so that it faces the exterior of electronic device 10 and second surface 20 of sensor element can be positioned so that it faces the interior of electronic device 10. Sensor substrate 14 can have an array of via holes 22 extending from first surface 18 to second surface 20. Vias 22 can be filled with a conductive material to provide a conductive path from first surface 18 of sensor substrate 14 to second surface 20 of sensor substrate 14. In some embodiments, a metal distribution layer 24 is applied to first surface 18 of sensor substrate 14 using conventional techniques and contacts the conductive material in via holes 22. In some embodiments, a coating stack 26 can be deposited over metal distribution layer 24. In some embodiments, a circuitry assembly or integrated circuit can be attached to second surface 20 of sensor substrate 14. The integrated circuit and sensor substrate assembly can act as a sensor element, including but not limited to, a fingerprint sensor (for example, a capacitive fingerprint sensor), a thermometer, a pulse oximeter, a pressure sensor, or an optics-based sensor.

[0017] Sensor substrate 30 can be a suitable insulative material, including, but not limited to glass, ceramic, glass ceramic, silicon, or a polymeric material. In some embodiments,

sensor substrate is sufficiently rigid to support coating stack 26. Rigidity (D) is defined by the equation:

$$D = ((2/3) * E * h^3) / (1 - n^2) \quad (1)$$

wherein E is the elastic modulus, h is the thickness of the substrate, and n is Poisson's ratio. In some embodiments, sensor substrate 30 can have a rigidity greater than 0.03 Pa*m³.

[0018] As shown in FIG. 2, coating stack 26 can include an intermediate layer 28 disposed on metal layer 24 and a top layer 30 disposed on intermediate layer 28. As used herein, the term "dispose" includes coating, depositing and/or forming a material onto a surface using any known method in the art. The phrase "disposed on" includes the instance of forming a material onto a surface such that the material is in direct contact with the surface and also includes the instance where the material is formed on a surface, with one or more intervening material(s) between the disposed material and the surface. In some embodiments, there can be an adhesion promotion layer between metal layer 24 and intermediate layer 28 and/or between intermediate layer 28 and top layer 30. Each of intermediate layer 28 and top layer 30 can be a single layer or can have a plurality of sublayers.

[0019] Intermediate layer 28 can function as an electrostatic discharge (ESD) layer to protect the electronics underneath it (e.g., the integrated circuit/circuitry assembly). In some embodiments, intermediate layer 28 provides ESD protection by having a dielectric breakdown voltage greater than 200 V/μm. In some embodiments, intermediate layer 28 also provides cushioning to top layer 30 to balance minimizing tensile stresses to top layer 30 and bi-axial flexural stresses to top layer 30 when top layer 30 is subjected to an impact load such as being dropped on a rough surface. In some embodiments, an elastic modulus of intermediate layer 28 affects the tensile stresses and bi-axial flexural stress to top layer 30. The bi-axial flexural stress decreases as the elastic modulus of intermediate layer 28 increases and the tensile stress increases as the elastic modulus of intermediate layer 28 increases. In some embodiments, intermediate layer 28 can have an elastic modulus in a range from about 50 MPa to about 500 MPa. Such an elastic modulus balances minimizing the tensile stresses and bi-axial flexural stresses to top layer 30 when the top layer has a tensile strength of at least 300 MPa. In some embodiments, intermediate layer 28 can have a thickness in a range from about 10 μm to about 100 μm. In some embodiments top layer 30 provides scratch and impact resistance. In some embodiments, top layer 30 has a thickness less than 2 μm.

[0020] In some embodiments, the materials for the layers of coating stack 26 are chosen with a goal of minimizing the overall thickness of coating stack 26 while still achieving adequate electrostatic discharge protection, and impact and scratch resistance. The sensitivity of the sensor is measured by the signal-to-noise ratio (SNR) and SNR is dependent on the thickness of the coating stack as the SNR decreases approximately 0.7 dB per micrometer of coating stack 26. In some embodiments, the SNR is greater than 20 dB. In some embodiments, coating stack 26 has an apparent thickness. As used herein, the term apparent thickness means how thick the coating stack 26 appears to be rather than how thick coating stack 26 actually is in part as a result of the refractive properties of coating stack 26. In some embodiments, the apparent thickness is less than the actual thickness. In some embodiments, coating stack 26 has an apparent thickness less than 20 μm . In some embodiments, the higher the dielectric constant of the electrostatic discharge protection layer the lower the apparent thickness.

[0021] FIG. 3 illustrates an exemplary coating stack 26'. Coating stack 26' includes an ESD protection layer 32 as intermediate layer 28' disposed on metal layer 24. Top coat 30' includes a color layer 34 disposed on ESD protection layer 32 and a hard coat 36 disposed on color layer 34.

[0022] ESD protection layer 32 can be a colored organic resin based ink, for example a white ink having the breakdown voltage, elastic modulus, and thickness properties discussed above. The ink can be applied using conventional techniques such as by screen printing. The ink can be a thermally or ultraviolet light curable ink.

[0023] Top coat 30' can have the thickness properties discussed above. In some embodiments, color layer 34 is a grey-based color. In such instances, color layer 34 can include one or more layers of a metal or metal oxide that provides the grey color and acts as a neutral density filter. Suitable materials include, but not limited to aluminum, silver, gold, and a copper-nickel alloy. In some embodiments, color layer 34 is not a grey-based color. In such instances, color layer 34 can include one or more layers of material that provide the non-grey-based color that act as an interference filter. The interference filter can include one or more layers of silicon. When an interference filter or neutral density filter is used, the filter minimizes reflection such that light passing through the filter is scattered and reflected back in all directions to minimize reflection of light, and thereby minimizes the ability of top coat 30' to act like a mirror. The filters can have a thickness of up to about 100 nm. The one or

more layers of color layer 34 can be deposited using conventional techniques, for example sputtering. Hard coat 36 can include a silicon oxide (SiO_2) layer, a silicon nitride (Si_3N_4) layer or both. The silicon oxide and/or silicon nitride layer can be deposited using conventional techniques, for example plasma enhanced chemical vapor deposition. In one embodiment hard coat 36 can be multilayer with a layer of silicon nitride disposed between two layers of silicon oxide. Each of the sublayers can have a thickness of about 100 nm.

[0024] FIG. 4 illustrates another exemplary coating stack 26''. Intermediate layer 28'' can include an ESD protection layer 38 disposed on metal layer 24 and a color layer 40 disposed on ESD protection layer 38. Top coat 30'' can include a hard coat 42. In this embodiment, top layer 30'' does not include a color layer because the color layer is incorporated in intermediate layer 28''.

[0025] ESD protection layer 38 can be an organic polymeric material having the breakdown voltage, elastic modulus, and thickness properties discussed above. Suitable polymeric materials can include a polyimide based material, an acrylate based material, or a fluorinated material. International Pub. No. WO2010/099254, which is hereby incorporated by reference in its entirety, discloses suitable materials for ESD protection layer 38. In some embodiments, the organic polymeric material of ESD protection layer 38 can be filled with inorganic particles including, but not limited to, titanium oxide. Suitable materials for the inorganic particles can include materials having a dielectric constant greater than about 50. In some embodiments, the size of the inorganic particles can be chosen in order to maximize diffusing the reflection of light. Color layer 40 can be a black ink. The ink can be applied using conventional techniques such as by screen printing. The ink can be a thermally or ultraviolet light curable ink. The ink can be applied so that color layer 40 has a thickness of about 6 μm .

[0026] Hard coat 42 can be the same as hard coat 36 described above. Hard coat 42 can include a silicon oxide (SiO_2) layer, a silicon nitride (Si_3N_4) layer or both. The silicon oxide and/or silicon nitride layer can be deposited using conventional techniques, for example plasma enhanced chemical vapor deposition. In one embodiment hard coat 42 can be multilayer with a layer of silicon nitride disposed between two layers of silicon oxide. Each of the sublayers can have a thickness of about 100 nm.

Examples

Example 1

[0027] The following experiment was performed to compare the reflection and color for a coating stack. Samples of Eagle XG[®] glass substrates available from Corning Incorporated were provided and cleaned with isopropyl alcohol and blown dry. A white ink was then screen printed on the cleaned glass substrates. After coating the white ink, the substrate was placed in a conventional oven and the white ink film was thermally cured at 250°C for approximately 30 minutes. After curing, the film thickness was approximately 10 μm as determined by a step height profile measured using a P16 surface profiler. Next a silicon layer was coated on top of the white ink film using a KDG sputtering system. Some samples had a 5 nm silicon layer deposited thereon and other samples had a 30 nm silicon layer deposited. The parameters for sputtering included room temperature, a pressure of 10 mtorr with 40 sccm argon and the plasma DC power of 1,000W. The deposition rate was about 5 nm per scan. Next a series of silicon oxide and silicon nitride layers were deposited on the silicon layer using a STS plasma-enhanced chemical vapor deposition to a thickness of 100 nm per layer. The silicon oxide and silicon nitride layers were deposited at a temperature of 200 °C using the following deposition parameters shown in Table 1 below to produce a first layer of silicon oxide having a thickness of 100 nm, a layer of silicon nitride having a thickness of 100 nm, and a layer of silicon oxide having a thickness of 100 nm.

Table 1

	He (sccm)	SiH4 (sccm)	N2O (sccm)	NH3 (sccm)	N2 (sccm)	Power (W)	P (mtorr)
SiO2	1000	10	1000			50	1100
Si3N4		20		100	2000	300	1000

[0028] The reflection and color after various stages of the process (prior to coating, after coating the white ink, after coating the first silicon oxide layer, and after coating the second silicon oxide layer) was measured. The % reflection was measured at 550 nm using a F10 spectrometer. The values are shown below in Table 2.

Table 2

	5nm Si				30nm Si			
Coating	Rx % @ 550nm	L*	a*	b*	Rx % @ 550nm	L*	a*	b*
Bare EXG	14.02	44.23	0.035	0.59	55.25	79.21	0.96	2.18
White-ink coated	1.5	12.61	1.67	4.03	1.5	12.61	1.67	4.03
100nm SiOx over coat	2.4	2.03	0.64	0.27	4.4	25.13	1.76	2.67
100nmSiOx/100nmSiNx/100nmSiOx over coat	1.1	7.89	-7.75	-7.84	9.6	33.25	-1.9	18.09

[0029] The results in Table 2 show that reflectance and color values change with the addition of each layer. Also, the presence of the thicker silicon layer increases the reflectance and color values after applying the silicon oxide and silicon nitride layers.

Example 2

[0030] A first set of Eagle XG[®] glass substrates available from Corning Incorporated were provided with a 10 μ m thick white ink as described in Example 1 above and then a silicon layer having a thickness of 5 nm, 10 nm, 20 nm, 30 nm, 40 nm, or 50 nm was deposited thereon in the manner described in Example 1. A second set of Eagle XG[®] glass substrates had a silicon layer having a thickness of 5 nm, 10 nm, 20 nm, 30 nm, 40 nm, or 50 nm deposited thereon in the manner described in Example 1. The reflectance of each sample was measured with a F10 Spectrometer over a range from 400 nm to 1000 nm. FIG. 5 is a plot of wavelength in nm vs. % reflection for each of the white coated samples (5 nm, 10 nm, 20 nm, 30 nm, 40 nm, and 50 nm silicon layer). As can be seen in FIG. 5, the reflection gradually increases as the wavelength increases for each silicon layer thickness. FIG. 6 is a plot of wavelength in nm vs. % reflection for each of the samples without the white ink coating (5 nm, 10 nm, 20 nm, 30 nm, 40 nm, and 50 nm silicon layer). As can be seen in FIG. 6, the reflection stays substantially the same as the wavelength increases for each silicon layer thickness.

[0031] It will be apparent to those skilled in the art that various modifications and variations can be made without departing from the spirit or scope of the invention.

What is claimed is:

1. A coated substrate for a sensor, comprising
a substrate comprising a first surface, a second surface opposing the first surface, at least one via hole extending from the first surface to the second surface, and a rigidity of greater than $0.03 \text{ Pa} \cdot \text{m}^3$;
a metal layer disposed on the first surface of the substrate;
an electrostatic discharge protection layer disposed on the metal layer having a dielectric breakdown voltage greater than $200 \text{ V}/\mu\text{m}$; and
an outermost layer disposed on the electrostatic discharge protection layer providing scratch resistance and impact resistance.
2. The coated substrate of claim 1, further comprising a color layer disposed between the electrostatic discharge layer and the outermost layer.
3. The coated substrate of claim 2, wherein the color layer is a filter.
4. The coated substrate of claim 3, wherein the combined thickness of the outermost layer and the color layer is less than $2 \mu\text{m}$.
5. The coated substrate of claim 2, wherein the color layer is a black ink.
6. The coated substrate of any one of claims 1-5, wherein the electrostatic discharge protection layer has an elastic modulus in a range from 50 MPa to 500 MPa.
7. The coated substrate of any one of claims 1-6, wherein the electrostatic discharge protection layer comprises a colored organic based ink.
8. The coated substrate of claim 7, wherein the colored organic based ink is white.
9. The coated substrate of any one of claims 1-8, wherein the electrostatic discharge protection layer comprises a polymeric resin filled with inorganic particles.
10. The coated substrate of claim 9, wherein the inorganic particles have a dielectric constant greater than 50.

11. The coated substrate of any one of claims 1-10, wherein the outermost layer is a silicon oxide/nitride layer.
12. The coated substrate of any one of claims 1-11, wherein the outermost layer has a tensile stress of at least 300 MPa.
13. A sensor comprising:
 - the coated substrate of any one of claims 1-12; and
 - a circuit assembly connected to the second surface.
14. The sensor of claim 13, wherein the sensor is a fingerprint sensor.
15. The sensor of claim 14, wherein the fingerprint sensor is a capacitive fingerprint sensor.
16. An electronic device comprising:
 - a cover assembly having an opening; and
 - the sensor of claim 13 disposed in the opening such that the outermost layer faces an exterior of the electronic device.

FIG. 1

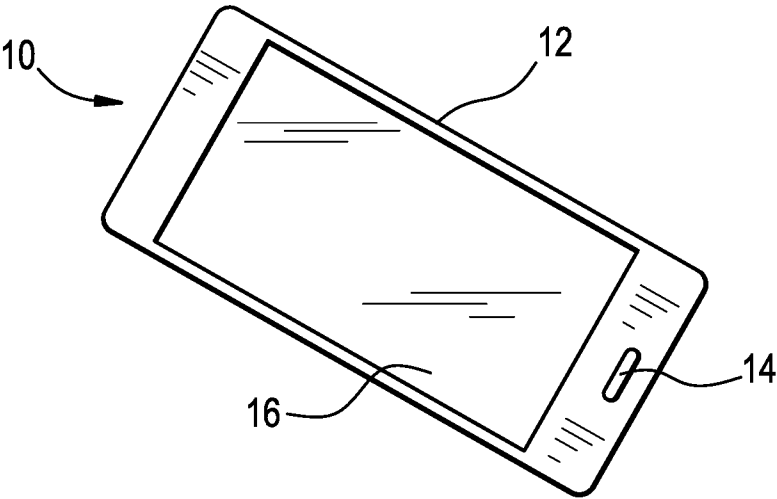


FIG. 2

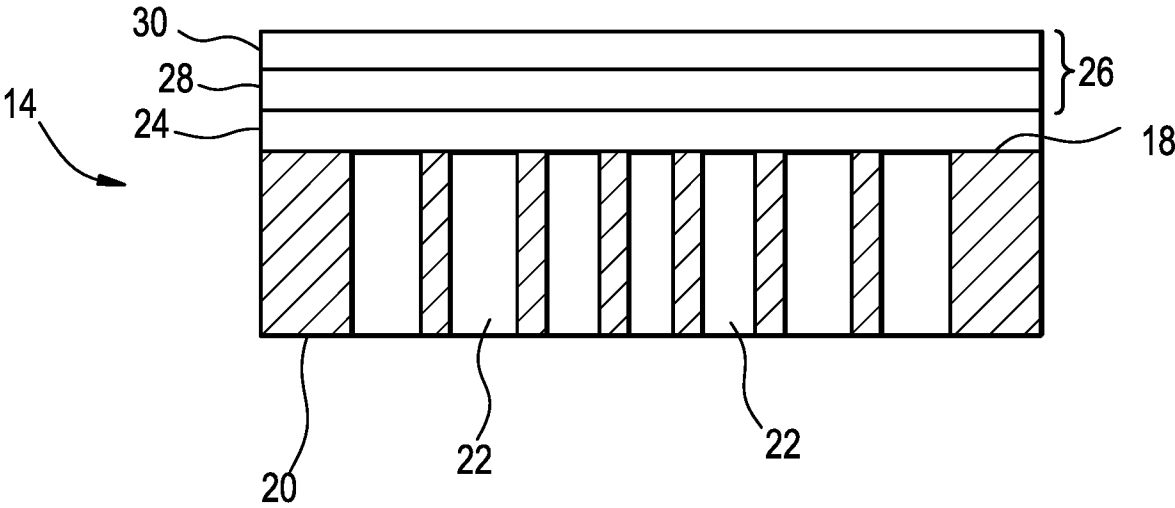


FIG. 3

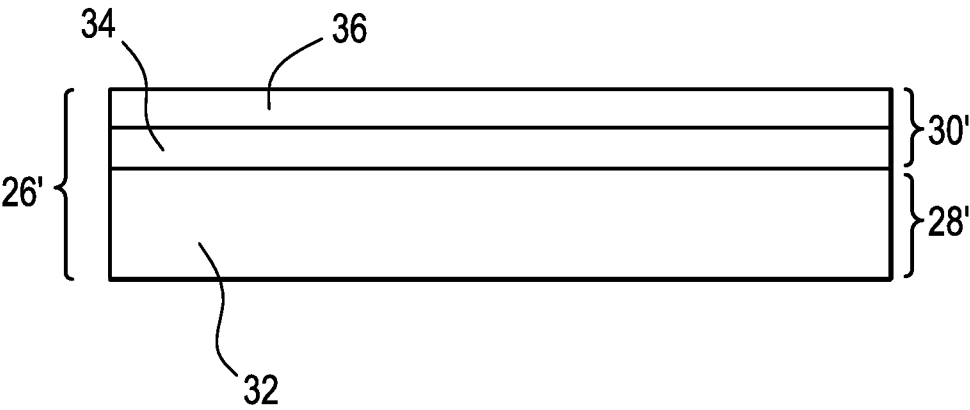
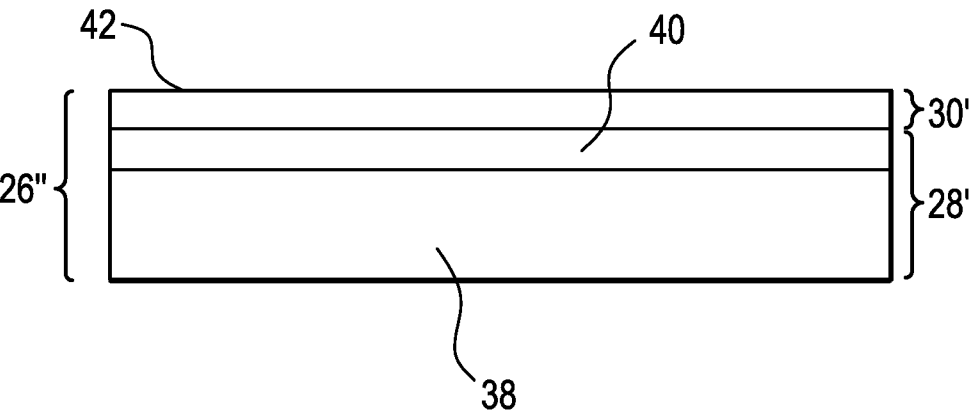


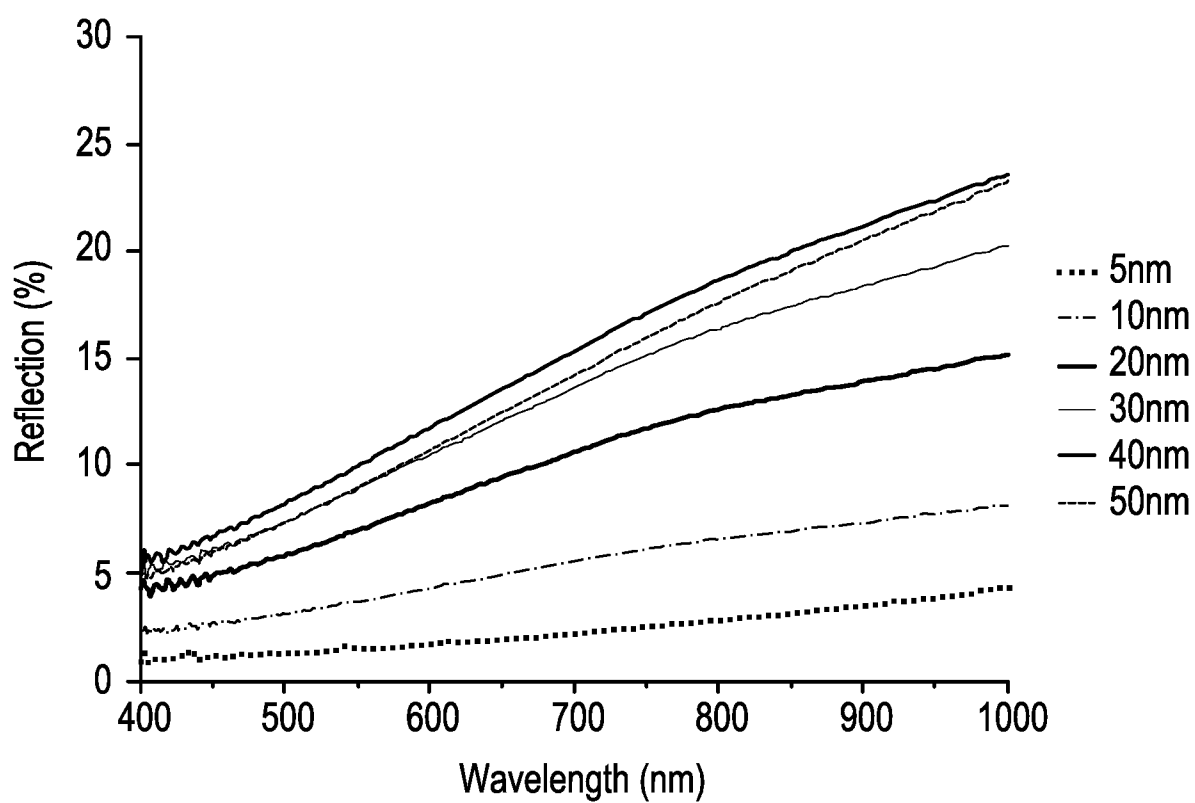
FIG. 4



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FIG. 5

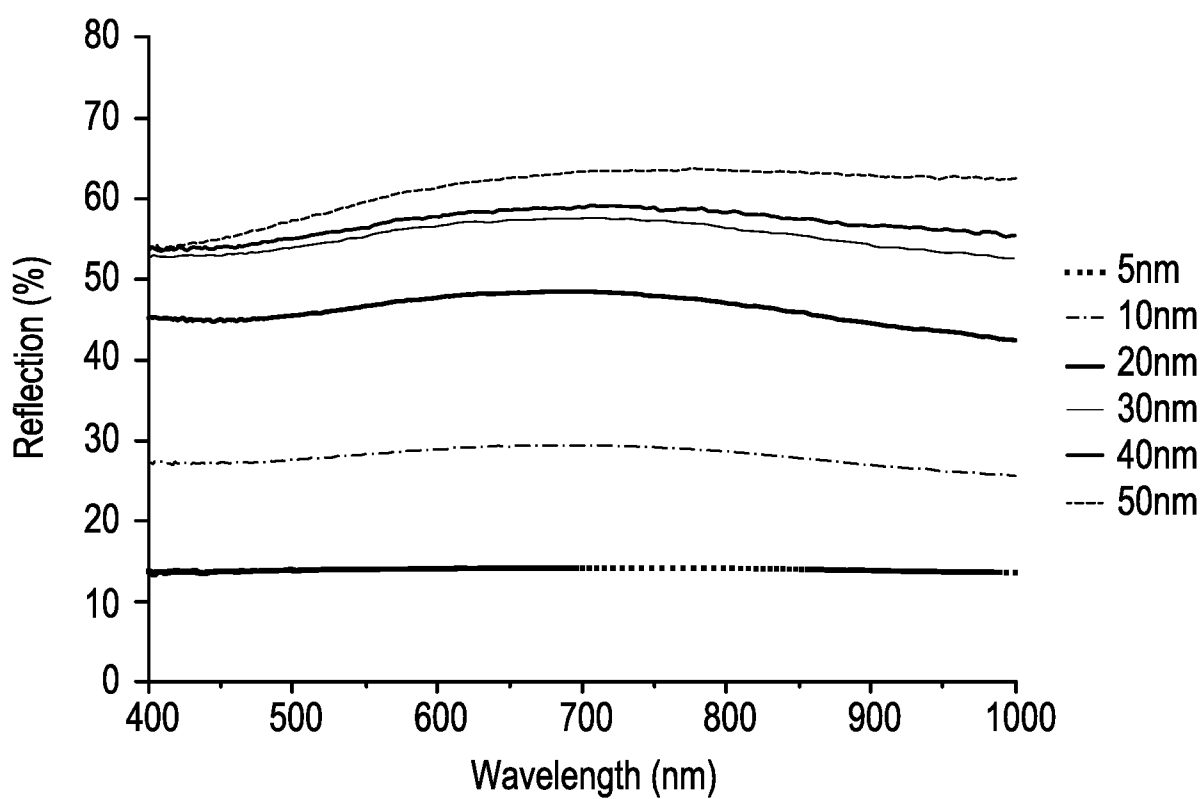
Reflection vs. Si thickness on white coated EXG



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FIG. 6

Reflection vs. Si thickness on bare EXG



INTERNATIONAL SEARCH REPORT

International application No
PCT/US2016/014209A. CLASSIFICATION OF SUBJECT MATTER
INV. G06K9/00
ADD.

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
G06K

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

EPO-Internal, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US 2003/161512 A1 (MATHIASSEN SVEIN [NO] ET AL) 28 August 2003 (2003-08-28) abstract paragraph [0015] paragraph [0024] - paragraph [0035] figure 1	1-16
Y	WO 2010/023323 A1 (IDEX ASA [NO]; BREDHOLT GEIR IVAR [NO]; BERNSTEIN RALPH W [NO]; CHRIST) 4 March 2010 (2010-03-04) abstract page 6, line 18 - line 35 figure 5 ----- -/--	1-16



Further documents are listed in the continuation of Box C.



See patent family annex.

* Special categories of cited documents :

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"E" earlier application or patent but published on or after the international filing date

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"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

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"&" document member of the same patent family

Date of the actual completion of the international search

8 April 2016

Date of mailing of the international search report

26/04/2016

Name and mailing address of the ISA/

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INTERNATIONAL SEARCH REPORT

International application No
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C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT		
Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US 2010/215968 A1 (FIELDS LENWOOD L [US] ET AL) 26 August 2010 (2010-08-26) abstract paragraph [0030] - paragraph [0032] paragraph [0037] paragraph [0048] - paragraph [0051] -----	1-16
Y	KR 101 451 222 B1 (DREAMTECH CO LTD [KR]) 16 October 2014 (2014-10-16) abstract paragraph [0097] - paragraph [0105] figure 12 -----	2-5

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No

PCT/US2016/014209

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 2003161512	A1	28-08-2003	AT 384306 T 15-02-2008
		AU 6442901 A 02-01-2002	
		CY 1107257 T1 21-11-2012	
		DE 60132460 T2 15-01-2009	
		DK 1303828 T3 19-05-2008	
		EP 1303828 A2 23-04-2003	
		ES 2299488 T3 01-06-2008	
		JP 4708671 B2 22-06-2011	
		JP 2003536085 A 02-12-2003	
		NO 20003004 A 10-12-2001	
		PT 1303828 E 25-03-2008	
		US 2003161512 A1 28-08-2003	
		US 2008002867 A1 03-01-2008	
		WO 0199035 A2 27-12-2001	
WO 2010023323	A1	04-03-2010	CN 102138147 A 27-07-2011
		EP 2332095 A1 15-06-2011	
		JP 5593317 B2 24-09-2014	
		JP 2012501484 A 19-01-2012	
		KR 20110063643 A 13-06-2011	
		US 2011182488 A1 28-07-2011	
		WO 2010023323 A1 04-03-2010	
US 2010215968	A1	26-08-2010	CN 102414231 A 11-04-2012
		EP 2401309 A2 04-01-2012	
		JP 5763553 B2 12-08-2015	
		JP 2012519224 A 23-08-2012	
		TW 201041916 A 01-12-2010	
		TW 201509968 A 16-03-2015	
		US 2010215968 A1 26-08-2010	
		US 2012037400 A1 16-02-2012	
		WO 2010099254 A2 02-09-2010	
KR 101451222	B1	16-10-2014	NONE