

(19) World Intellectual Property  
Organization  
International Bureau



(43) International Publication Date  
23 June 2005 (23.06.2005)

PCT

(10) International Publication Number  
**WO 2005/057631 A2**

(51) International Patent Classification<sup>7</sup>: **H01L 21/00**

(21) International Application Number:  
PCT/US2004/039970

(22) International Filing Date:  
30 November 2004 (30.11.2004)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:  
10/725,850 2 December 2003 (02.12.2003) US

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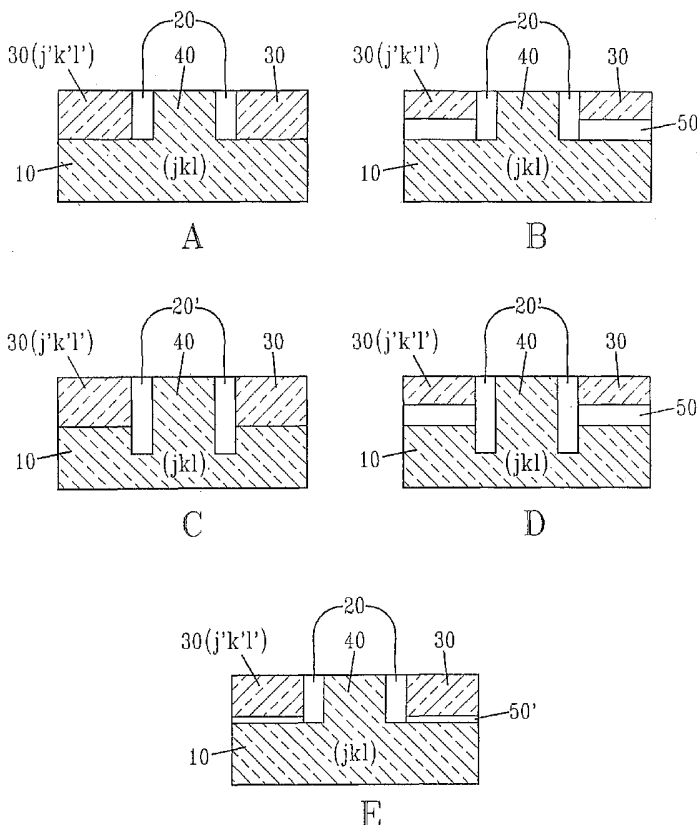
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(81) Designated States (unless otherwise indicated, for every kind of national protection available): AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BW, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NA, NI, NO, NZ, OM, PG, PH, PL, PT, RO, RU, SC, SD, SE, SG, SK, SL, SY, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, YU, ZA, ZM, ZW.

(84) Designated States (unless otherwise indicated, for every kind of regional protection available): ARIPO (BW, GH,

[Continued on next page]

(54) Title: PLANAR SUBSTRATE WITH SELECTED SEMICONDUCTOR CRYSTAL ORIENTATIONS FORMED BY LOCALIZED AMORPHIZATION AND RECRYSTALLIZATION OF STACKED TEMPLATE LAYERS



(57) Abstract: A method utilizing localized amorphization and recrystallization of stacked template layers is provided for making a planar substrate having semiconductor layers of different crystallographic orientations. Also provided are hybrid-orientation semiconductor substrate structures built with the methods of the invention, as well as such structures integrated with various CMOS circuits comprising at least two semiconductor devices disposed on different surface orientations for enhanced device performance.



GM, KE, LS, MW, MZ, NA, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HU, IE, IS, IT, LU, MC, NL, PL, PT, RO, SE, SI, SK, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

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- *as to applicant's entitlement to apply for and be granted a patent (Rule 4.17(ii)) for the following designations* AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BW, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NA, NI, NO, NZ, OM, PG, PH, PL, PT, RO, RU, SC, SD, SE, SG, SK, SL, SY, TJ, TM, TN, TR, TT, TZ, UA, UG, UZ, VC, VN, YU, ZA, ZM,

ZW, ARIPO patent (BW, GH, GM, KE, LS, MW, MZ, NA, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HU, IE, IS, IT, LU, MC, NL, PL, PT, RO, SE, SI, SK, TR), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG)

- *as to the applicant's entitlement to claim the priority of the earlier application (Rule 4.17(iii)) for all designations*

**Published:**

- *without international search report and to be republished upon receipt of that report*

*For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.*

PLANAR SUBSTRATE WITH SELECTED SEMICONDUCTOR CRYSTAL  
ORIENTATIONS FORMED BY LOCALIZED AMORPHIZATION AND  
RECRYSTALLIZATION OF STACKED TEMPLATE LAYERS

DESCRIPTION

Field of the Invention

[0001] The present invention relates to high-performance complementary metal oxide semiconductor (CMOS) circuits in which carrier mobility is enhanced by utilizing different semiconductor surface orientations for p-type field effect transistors (FETs) and n-type FETs. More particularly, the present invention relates to methods for fabricating planar substrate structures with different surface crystal orientations, and to the hybrid-orientation substrate structures produced by such methods.

Background of the Invention

[0002] The CMOS circuits of current semiconductor technology comprise n-type FETs (nFETs), which utilize electron carriers for their operation, and p-type FETs (pFETs), which utilize hole carriers for their operation. CMOS circuits are typically fabricated on semiconductor wafers having a single crystal orientation. In particular, most of today's semiconductor devices are built on Si having a (100) surface orientation.

[0003] It is known that electrons have a high mobility in Si with a (100) surface orientation and that holes have high mobility in Si with a (110) surface orientation. In fact, hole mobility can be about 2 to 4 times higher on a 110-oriented Si wafer than on a standard 100-oriented Si wafer. It would therefore be desirable to create a hybrid-orientation substrate comprising 100-oriented Si (where nFETs would be formed) and 110-oriented Si (where pFETs would be formed).

**[0004]** Planar hybrid substrate structures with different surface orientations have been described previously (see, for example, co-assigned U.S. Application Serial No. 10/696,634, filed October 29, 2003, and co-assigned U.S. Application Serial No. 10/250,241, filed June 17, 2003).

**[0005]** FIGS. 1A-1E show, in cross section view, some prior art examples of planar hybrid-orientation semiconductor substrate structures comprising bulk semiconductor substrate 10, dielectric trench isolation regions 20, semiconductor regions 30 with a first surface orientation (e.g., j'k'l'), and semiconductor region 40 with a second surface orientation (e.g., jkl). In the structure of FIG. 1A, semiconductor regions 30 and 40 are both directly on bulk substrate 10, with semiconductor region 40 and bulk substrate 10 having the same orientation. The structure of FIG. 1B differs from that of FIG. 1A only in that semiconductor regions 30 are on buried oxide (BOX) layer 50 instead of directly on bulk substrate 10. The structures of FIGS. 1C-1E differ from those of FIGS. 1A-1B by the thickness of BOX layers 50 and 50' and by the depth of trench isolation structures 20 and 20'.

**[0006]** FIGS. 2A-2B show, in cross section view, previous examples of how integrated CMOS circuits comprising at least one pFET on a (110) crystallographic plane of Si and at least one nFET on a (100) crystallographic plane of Si may be advantageously disposed on the hybrid-orientation substrate structure of FIG. 1B. In FIG. 2A, a bulk Si substrate 120 with 100 orientation has regions 130 of 110-oriented Si on BOX layer 140, and regions 150 of regrown 100-oriented Si on bulk substrate 120. pFET devices 170 are disposed on 110-oriented regions 130 and nFET devices 180 are disposed on 100-oriented regions 150. In FIG. 2B, a bulk Si substrate 180 with 110 orientation has regions 190 of 100-oriented Si on a BOX layer 140 and regions 200 of regrown 110-oriented Si on bulk substrate 180. pFET devices 210 are disposed on 110-oriented regions 180 and nFET devices 220 are disposed on 100-oriented regions 190.

[0007] FIGS. 3A-3I show, in cross section view, the steps of a prior art method used to form the structure of FIG. 1B. Specifically, FIG. 3A shows the starting Si substrate 250, and FIG. 3B shows substrate 250 after formation of BOX layer 260 and silicon-on-insulator (SiOI) device layer 270. Si substrate 250 may be 110- (or 100-) oriented, and SiOI device layer 270 would be 100- (or 110-) oriented. SiOI layer 270 may be formed by bonding or other methods. After depositing protective dielectric (preferably  $\text{SiN}_x$ ) layer 280 to form the structure of FIG. 3C, SiOI device layer 270 and BOX layer 260 are removed in selected areas to form openings 290 extending to Si substrate 250, as shown in FIG. 3D. Openings 290 are lined with a dielectric (preferably  $\text{SiN}_x$ ) which is then etched to form sidewall spacers 300, as shown in FIG. 3E. Next, epitaxial Si 310 is selectively grown in openings 290 to produce the structure of FIG. 3F, which is planarized back to form the structure of FIG. 3G. Protective dielectric 280 is then removed by a process such as polishing to form the structure of FIG. 3H with coplanar, differently oriented Si device layers 310 (on bulk Si substrate 250) and 320 (on BOX layer 260). FIG. 3I shows the completed substrate structure after shallow trench isolation areas 330 have been formed in the structure of FIG. 3H.

[0008] However, for many applications, it would be desirable to have *both* of the differently oriented Si regions on a BOX. Such structures are possible, but not easy, to produce by variations of the method of FIGS. 3A-3I. For example, the structure of FIG. 4 may be produced by replacing Si substrate 250 in FIG. 3A with a SiOI substrate 400 comprising substrate 410, BOX layer 420, and Si layer 430 to produce differently oriented single crystal regions 320 with a first orientation and 440 with a second orientation matching that of semiconductor layer 430. However, the use of two BOX layers adds extra complexity to the process and produces structures where one of the hybrid orientations is significantly thicker than the other (a disadvantage when both layers need to be thin). In addition, selective epitaxial Si growth can be tricky; defects are likely to nucleate on the sides of sidewall spacers 300 (shown in FIGS. 3E-3F), especially when openings 290 are small (e.g., less than 500 nm in diameter).

[0009] In view of the above, it would be desirable to have simpler and better methods (i.e., those that do not require epitaxial regrowth) to form planar hybrid-orientation semiconductor substrate structures, especially planar hybrid-orientation semiconductor-on-insulator (SOI) substrate structures wherein the differently oriented semiconductors are disposed on a common BOX layer.

[0010] In addition, it would be desirable to have integrated electrical circuits on such planar hybrid-orientation SOI substrates wherein the electrical circuits comprise pFETs on a (110) crystallographic plane and nFETs on a (100) crystallographic plane.

#### Summary of the Invention

[0011] It is therefore an object of the present invention to provide a planar hybrid-orientation SOI substrate structure with a surface comprising at least two clearly defined single-crystal semiconductor regions with different surface orientations, wherein the differently oriented semiconductor regions are disposed on a common BOX layer. The term "clearly defined" is used herein to denote that the surface regions of a given surface orientation are macroscopic and not merely single grains of polycrystalline Si.

[0012] It is a related object of the present invention to provide methods for fabricating such a planar hybrid-orientation semiconductor substrate structure.

[0013] It is a further object of the present invention to provide methods for fabricating similar hybrid-orientation semiconductor substrate structures on a variety of support layers.

[0014] It is yet another object of the present invention to provide integrated circuits (ICs) on the hybrid-orientation substrates of the present invention, wherein the ICs comprise pFETs on a (110) crystallographic plane and nFETs on a (100) crystallographic plane.

[0015] In accordance with the above listed and other objects, new methods are provided for forming a variety of planar hybrid-orientation semiconductor substrate structures. Common to all methods are three basic steps, by which the orientation of selected semiconductor regions may be changed from an original orientation to a desired orientation:

[0016] forming a bilayer template layer stack comprising a first, lower single crystal semiconductor layer (or substrate) having a first orientation and a second, upper (typically bonded) single crystal semiconductor layer having a second orientation different from the first;

[0017] amorphizing one of the layers of the bilayer template stack in selected areas (by ion implantation through a mask, for example) to form localized amorphized regions; and

[0018] recrystallizing the localized amorphized regions using the non-amorphized layer of the stack as a template, thereby changing the orientation in the localized amorphized regions from an original orientation to a desired orientation.

[0019] To minimize the possibility of lateral templating, the sides of the regions selected for amorphization and templated recrystallization would typically be isolated from adjacent crystalline regions, for example, by trenches. The trenches may be formed and filled before amorphization, formed and filled between amorphization and recrystallization, or formed after amorphization and filled after recrystallization.

[0020] In one embodiment of the present invention, the basic steps above are incorporated into a method for forming a planar hybrid-orientation SiOI substrate structure. A 100-oriented Si substrate is used for the first, lower layer of the bilayer template stack and a 110-oriented Si layer for the second, upper layer of the bilayer template stack. The uppermost portion of the template stack is amorphized in selected

areas to a depth that ends in the underlying 100-oriented Si substrate. The amorphized Si regions are then recrystallized into 100-oriented Si, using the underlying 100-oriented Si as a template. Following these steps of patterned amorphization and recrystallization, which leave surface regions of 100-oriented Si in the treated areas and surface regions of 110-oriented Si in the untreated areas, a buried oxide (BOX) layer is formed by oxygen implantation and annealing (e.g., a "Separation by Implantation of Oxygen" or SIMOX process).

**[0021]** In another embodiment of the present invention, the basic steps above are incorporated into a another method to form a planar hybrid-orientation SiOI substrate structure. In this method, a 110-oriented SiOI layer on a BOX layer is used for the first, lower layer of a bilayer template stack, and a 100-oriented Si layer is used for the second, upper layer of a bilayer template stack. The lowermost portion of the bilayer template stack is then amorphized in selected areas from the BOX layer up to a depth ending in the upper template layer. The amorphized Si regions are then recrystallized into 100-orientated Si, using the upper 100-oriented Si layer as a template. The uppermost portion of the bilayer template is then removed by a process such as polishing to leave coplanar surface regions of 110-oriented Si (in the untreated areas) and 100-oriented Si (in the treated areas).

**[0022]** The basic steps of the present invention can be easily adapted in whole or in part to form planar hybrid-orientation semiconductor structures on different substrates (e.g., bulk, thin or thick BOX, insulating or high resistivity substrates), or to form planar hybrid-orientation semiconductor substrate structures having three or more surface orientations.

**[0023]** Yet another aspect of the present invention provides integrated circuits on the planar hybrid-orientation semiconductor substrates of this invention, wherein the integrated circuits comprise pFETs on a (110) crystallographic plane and nFETs on a (100) crystallographic plane.



### Brief Description of the Drawings

[0024] These and other features, aspects, and advantages will be more readily apparent and better understood from the following detailed description of the invention, in which:

[0025] FIGS. 1A-1E show, in cross section view, some examples of prior art planar hybrid-orientation semiconductor substrate structures, wherein the first of two semiconductor orientations is disposed directly on a bulk semiconductor substrate and the second of two semiconductor orientations is disposed either on the substrate (FIGS. 1A and 1C), partially insulated from the substrate by a thin BOX layer (FIG. 1E), or fully insulated from the substrate by a thick BOX layer (FIGS. 1B and 1D);

[0026] FIGS. 2A-2B show, in cross section view, prior art examples of how the hybrid-orientation substrate structure of FIG. 1B might form the basis of integrated circuits comprising at least one pFET on a 110-oriented single crystal Si region and at least one nFET on a 100-oriented single crystal Si region;

[0027] FIGS. 3A-3I show, in cross section view, the steps of the basic prior art method used to form the structures of FIGS. 1A-1E, illustrated for the case of FIG. 1B;

[0028] FIG. 4 shows, in cross section view, a prior art example of a planar hybrid-orientation semiconductor substrate structure wherein both of two differently oriented single crystal Si regions are disposed on buried insulator layers;

[0029] FIGS. 5A-5B show, in cross section view, two preferred SOI embodiments of the hybrid-orientation substrates of the present invention;

[0030] FIG. 6 shows, in cross section view, how a hybrid-orientation substrate structure of the present invention can be used to form the basis of an integrated circuit

comprising at least one pFET on a (110) Si crystallographic plane and at least one nFET on a (100) Si crystallographic plane.

[0031] FIGS. 7A-7G show, in cross section view, the basic steps underlying the methods of the present invention, illustrated for the case of upper layer amorphization and lower layer templating;

[0032] FIGS. 8A-8G show, in cross section view, a first preferred method to produce the structure of FIG. 5A of the present invention;

[0033] FIG. 9A-9F show, in cross section view, a second preferred method to produce the structure of FIG. 5B of the present invention; and

[0034] FIGS. 10A-10I show, in cross section view, different embodiments of the hybrid-orientation substrates that may be produced by the methods of the present invention.

#### Detailed Description of the Invention

[0035] The present invention, which provides planar hybrid-orientation SOI substrate structures and methods of fabricating the same, will now be described in greater detail by referring to the drawings that accompany the present application.

[0036] FIGS. 5A-5B show, in cross section view, two preferred embodiments of hybrid-orientation substrates that can be fabricated by the methods of the present invention. Hybrid-orientation substrate 450 of FIG. 5A and hybrid-orientation substrate 460 of FIG. 5B both comprise first single crystal semiconductor regions 470 with a first orientation, and second single crystal semiconductor regions 480 with a second orientation different from the first orientation. Semiconductor regions 470 and 480 have approximately the same thickness and are disposed on the same BOX layer 490. The

term “BOX” denotes a buried oxide region. Although this terminology is specifically used here, the present invention is not limited to merely buried oxides. Instead, various insulating layers can be used; the various insulating layers are described in greater detail hereinbelow.

[0037] Semiconductor regions 470 and 480 are separated by dielectric trench isolation regions 500, which are shown as having the same depth and stopping on BOX layer 490. However, in some embodiments of the present invention, trench isolation regions 500 may be shallower (so as not to reach BOX layer 490), deeper (so as to extend past BOX layer 490), or of non-equal depths, as desired. The structures of FIGS. 5A and 5B differ from each other only in the particulars of substrates 510 and 520. Substrate 510 in FIG. 5A is a semiconductor having an epitaxial relationship to single crystal semiconductor region 480, whereas substrate 520 in FIG. 5B has no particular restrictions other than being compatible with whatever subsequent processing it will be subjected to.

[0038] The hybrid-orientation substrate structures of FIGS. 5A-5B may be incorporated as the substrates for integrated circuits comprising at least one pFET on a (110) crystallographic plane and at least one nFET on a (100) crystallographic plane. FIG. 6 illustrates an exemplary integrated circuit on a Si version of the hybrid-orientation substrate structure of FIG. 5B, in cross section view. Substrate 520 has single crystal 110-oriented Si regions 530 and single crystal 100-oriented Si regions 540, separated by isolation regions 500 on BOX layer 490. pFET devices 170 are disposed on 110-oriented regions 530 and nFET devices 180 are disposed on 100-oriented regions 540. For clarity, dopings are not shown.

[0039] The FETs shown in FIG. 6 can be fabricated on the structure shown in FIG. 5A using techniques that are well known to those skilled in the art. In some embodiments, the 110 and 100 crystal orientations of layers 540 and 530 are reversed. In that embodiment, the pFET devices 170 would still be fabricated atop the 110-

oriented regions and the nFET devices 180 would be fabricated atop the 100-oriented surface.

**[0040]** The present invention also provides new methods for forming planar hybrid-orientation semiconductor substrate structures. Common to all methods are three basic steps, by which the orientation of selected semiconductor regions may be changed from an original orientation to a desired orientation:

**[0041]** forming a bilayer template layer stack comprising a first, lower single crystal semiconductor layer (or substrate) having a first orientation and a second, upper (typically bonded) single crystal semiconductor layer having a second orientation different from the first;

**[0042]** amorphizing one of the layers of the bilayer template stack in selected areas (by ion implantation through a mask, for example) to form localized amorphized regions; and

**[0043]** recrystallizing the localized amorphized regions using the non-amorphized layer of the stack as a template, thereby changing the orientation in the localized amorphized regions from an original orientation to a desired orientation.

**[0044]** These steps are illustrated in FIGS. 7A-7D for the case of upper layer amorphization and bottom layer templating. Although this embodiment is shown, the present invention also contemplates methods in which the bottom layer is amorphized and recrystallization is templated from the top layer.

**[0045]** FIG. 7A shows initial SOI substrate 580 comprising base substrate 520, BOX layer 490, and single crystal SOI layer 590 with a first orientation. SOI layer 590 may be formed by bonding or by any other method known to the art. FIG. 7B shows bilayer template stack 600 comprising SOI layer 590 as a lower template layer with a first

orientation and single crystal semiconductor layer 610 as an upper template layer with a second orientation different from the first orientation. Layer 610 would typically be formed by bonding. FIG. 7C shows the structure of FIG. 7B after ion bombardment 620 in selected areas creates localized amorphized regions 630. Localized amorphized regions 630 extend from the top surface of upper template layer 610 down to interface 640, located within lower template layer 590. Selected area ion bombardment 620 would typically be effected by blanket ion bombardment in combination with a patterned mask. FIG. 7D shows the structure of FIG. 7C after localized amorphized regions 630 have been recrystallized (starting at interface 640, using lower layer 590 as a template) to form single crystal semiconductor region 650. Non-amorphized upper template layer regions 610' (with the second crystal orientation) and recrystallized region 650 (with the first crystal orientation) now comprise planar hybrid-orientation substrate 650 with surface A-B comprising at least two clearly defined single-crystal semiconductor regions with different surface orientations.

[0046] To minimize the possibility of lateral templating, the sides of the region(s) 630 selected for amorphization and templated recrystallization would typically be at least partially isolated from adjacent crystalline regions, for example, by trenches. The trenches may be formed and filled before amorphization, formed and filled between amorphization and recrystallization, or formed after amorphization and filled after recrystallization. Trench formation would typically be effected by a process such as reactive ion etching (RIE) through a mask.

[0047] FIGS. 7E-7G show examples of three geometries for isolation trenches. In FIG. 7E, isolation trenches 660 extend through the upper template layer, but do not extend past the amorphization depth. In this case, some templating from side interfaces 670 may occur. In FIG. 7F, isolation trenches 680 extend past the amorphization depth, but not all the way to BOX layer 490, and in FIG. 7G, isolation trenches 690 extend all the way to BOX layer 490. However, isolation trenches may not be necessary if the recrystallization rate of the desired crystal orientation is much faster than

recrystallization templated from competing undesired crystal orientations. For example, the recrystallization rates of Si-implant-amorphized single crystal Si samples has been reported to be three times faster for 100-oriented Si than for 110-oriented Si [see, for example, L. Csepregi et al., J. Appl. Phys. 49 3096 (1978)].

**[0048]** The fact that different semiconductor orientations can differ in their recrystallization rates should also be considered when designing the template layer stacks and process flows. The layer of a bilayer template stack having the slower-growing orientation would preferably be the one that is amorphized, whereas the layer with the faster-growing orientation would preferably be the one from which the recrystallization is templated.

**[0049]** In one embodiment of the invention, shown in FIGS. 8A-8G, the basic steps of FIGS. 7A-7D are incorporated into a method for forming a planar hybrid-orientation SiOI substrate structure similar to structure 450 of FIG. 5A. For simplicity, isolation trenches are not shown. FIG. 8A shows 100-oriented Si substrate 700 comprising the first, lower layer of the template stack; FIG. 8B shows the substrate 700 after addition of 110-oriented Si layer 710 comprising the second, upper layer of the template stack. Layer 710 would typically be formed by bonding.

**[0050]** FIG. 8C shows the structure of FIG. 8B being subjected to ion bombardment 720 in selected areas to create the structure of FIG. 8D with localized amorphized regions 730 extending from the top surface of template layer 710 to a depth ending in substrate 700. FIG. 8E shows the structure of FIG. 8D after localized amorphized regions 730 have been recrystallized (using 100-oriented Si substrate 700 as a template) to form single crystal 100-oriented Si region(s) 740. Non-amorphized 110-oriented Si regions 710' and recrystallized 100-oriented Si region(s) 740 now comprise bulk planar hybrid-orientation substrate 750 with surface A-B comprising at least two clearly defined single-crystal semiconductor regions with different surface orientations.

[0051] A SIMOX process is then used to create a BOX layer, as shown in FIGS. 8F-8G. FIG. 8F shows the structure of FIG. 8E being exposed to blanket oxygen ion implantation 760 used to create buried O-rich layer 770. O-rich layer 770 preferably contains the original interface between layers 700 and 710, and is converted into BOX layer 780 of FIG. 8G by the appropriate annealing steps.

[0052] In another embodiment of the present invention, shown in FIGS. 9A-9F, the basic steps of FIGS. 7A-7D are incorporated into yet another method to form a planar hybrid-orientation SiOI substrate structure similar to structure 460 of FIG. 5B. Specifically, FIG. 9A shows initial SiOI substrate 800 comprising base substrate 520, BOX layer 490, and 110-oriented single crystal Si layer 810. Si layer 810 may be formed by bonding or by any other method known to the art. FIG. 9B shows bilayer template stack 820 comprising 110-oriented Si layer 810 as a lower template layer and single crystal 100-oriented Si layer 830 as an upper template layer. Layer 830 would typically be formed by bonding. FIG. 9C shows the structure of FIG. 9B being subjected to ion bombardment 840 in selected areas to create the structure of FIG. 9D with buried localized amorphized regions 850. Localized amorphized regions 850 extend from BOX layer 490 through lower template layer 810 and partially into upper template layer 830. As mentioned above, the areas selected for amorphization and templated recrystallization would typically be isolated from adjacent crystalline regions by trenches (not shown) to minimize the possibility of lateral templating. FIG. 9E shows the structure of FIG. 9D after localized amorphized regions 850 have been recrystallized, using upper template layer 810 as a template, to form 100-oriented single crystal Si regions 860. Upper template layer 810 is then removed by a process such as polishing (or oxidation followed by wet etchback) to leave coplanar 110-oriented single-crystal Si regions 810' and 100-oriented single-crystal Si regions 860 disposed on common BOX layer 490.

[0053] It should be noted that the method of FIGS. 8A-8G may equally well be employed with the orientations of substrate 700 and upper template layer 710 reversed,

i.e., with substrate 700 comprising a 110-oriented Si wafer instead of a 100-oriented Si wafer, and upper template layer 710 comprising a single crystal layer of 100-oriented Si instead of a single crystal layer of 110-oriented Si. Likewise, the method of FIGS. 9A-9F may be employed with the orientations of lower template layer 810 and upper template layer 830 reversed, i.e., with lower template layer 810 being 100-oriented Si instead of 110-oriented Si and upper template layer 830 being 110-oriented Si instead of 100-oriented Si. More generally, the structures and methods of the present invention may be employed using semiconductors other than Si, as will be described in more detail below.

**[0054]** FIGS. 10A-10I show, in cross section view, different embodiments of the hybrid-orientation substrates that may be produced by the methods of the present invention. FIG. 10A shows "bulk" planar hybrid-orientation semiconductor substrate structure 900 comprising first single crystal semiconductor regions 910 with a first orientation, and second single crystal semiconductor regions 920 with a second orientation different from the first orientation, but identical to the orientation of substrate 930. Planar hybrid-orientation semiconductor substrate structure 940 of FIG. 10B is similar to structure 900 of FIG. 10A, but has trench isolation regions 950 separating single crystal semiconductor regions 910 and 920.

**[0055]** Planar hybrid-orientation semiconductor substrate structure 960 of FIG. 10C is similar to structure 900 of FIG. 10A. However, substrate 930 has been replaced with substrate 980, which may or not be epitaxially related to semiconductor region 920. Structure 960 also comprises BOX layer 970 under semiconductor regions 910 and 920, and residuals 990 of second semiconductor material with the second orientation remaining under first semiconductor regions 910. Planar hybrid-orientation semiconductor substrate structure 1000 of FIG. 10D is similar to structure 960 of FIG. 10C, except that semiconductor region 920 is epitaxially related to semiconductor substrate 930, and BOX layer 970 is located above interface 1010 between first single crystal semiconductor regions 910 and substrate 930.



**[0056]** Planar hybrid-orientation semiconductor substrate structures 1020 and 1030 of FIGS. 10E-10F are identical to structures 1000 and 940 of FIGS. 10A-10B, except that semiconductor substrate 930 has been replaced by insulating substrate 1040.

**[0057]** Planar hybrid-orientation semiconductor substrate structures 1050 and 1060 of FIGS. 10G-10H are similar to structure 960 of FIG. 10C, but have trench isolation regions 950. In structure 1050 of FIG. 10G, trench isolation regions 950 extend below interface 1070 between first single crystal semiconductor regions 910 and residuals 990, but do not reach BOX layer 970. In structure 1060 of FIG. 10H, trench isolation regions 950 extend to BOX layer 970.

**[0058]** Planar hybrid-orientation semiconductor substrate structure 1080 of FIG. 10I comprises three differently oriented single crystal semiconductor regions 910, 920, and 1090, separated by trench isolation regions 950 extending to BOX layer 970. Planar hybrid-orientation semiconductor substrate structures with three or more surface orientations may be produced by the localized amorphization and recrystallization methods of this invention by using a multilayer template stack instead of a bilayer template stack.

**[0059]** Structures like those of FIGS. 5A-5B and FIGS. 10A-10I may be produced by using various permutations of the basic steps of the invention with or without additional steps. For example, a planar hybrid-orientation structure resembling 460 of FIG. 5B may be produced from the structure of FIG. 10H by the additional steps of amorphizing residuals 990 of second semiconductor material 920 and recrystallizing the amorphized regions using single crystal region 910 as a template.

**[0060]** The semiconductor substrates and single crystal semiconductor regions of the present invention may be selected from a wide range of semiconductor materials. For example, substrates 510, 520, 700, 930 and 980, and differently oriented first and second semiconductor regions 470, 610', 910, and 480, 650, and 920 may be selected from the

group including Si, SiC, SiGe, SiGeC, Ge alloys, Ge, C, GaAs, InAs, InP as well as other III-V or II-VI compound semiconductors. Layered combinations or alloys of the aforementioned semiconductor materials (for example, Si layers on SiGe), with or without one or more dopants, are also contemplated herein. First and second semiconductor regions may be strained, unstrained, or a combination of strained and unstrained layers can be used. The crystallographic orientations would typically be selected from the group including (110), (111), and (100).

**[0061]** The thickness of first and second single crystal semiconductor regions 470, 610', 910, and 480, 650, and 920 is typically from about 1 to about 500 nm, with a thickness from about 10 to about 100 nm being more typical. The thickness of substrates 510, 520, 700, 930, and 980 would typically be between 5 and 1000  $\mu\text{m}$ , and most typically be about 600  $\mu\text{m}$ .

**[0062]** BOX layers and insulating substrates 1040 may be selected from a wide range of dielectric materials, including, but not limited to the group including  $\text{SiO}_2$ , crystalline  $\text{SiO}_2$ ,  $\text{SiO}_2$  containing nitrogen or other elements, silicon nitrides, metal oxides (e.g.,  $\text{Al}_2\text{O}_3$ ), insulating metal nitrides (e.g., AlN), highly thermally conductive materials such as crystalline diamond. BOX thicknesses may range from about 2 nm to about 500 nm, with preferable thicknesses typically being in the range from about 50 to about 150 nm.

**[0063]** Bonding methods for forming the template stack may include any methods known to those skilled in the art (see, for example, Q.Y. Tong et al. [in *Semiconductor Wafer Bonding: Science and Technology* (John Wiley, 1998)] and co-pending and co-assigned U.S. Application Serial No. 10/696,634, filed October 29, 2003, and co-pending and co-assigned U.S. Application Serial No. 10/250,241, filed June 17, 2003). The contents of each of the above mentioned co-assigned U.S. Applications are incorporated herein by reference.

[0064] Differently oriented semiconductor surfaces to be bonded are preferably hydrophobic (rather than hydrophilic) for the cleanest possible interfaces, since impurities in the amorphized regions will typically impede the progress of the recrystallization. However, very thin oxides at the bonded interface may be tolerable if the oxide can be made to assume a discontinuous, islanded morphology by suitable annealing (see, for example, P. McCann et al. ["An investigation into interfacial oxide in direct silicon bonding," 6th Int. Symp. on Semiconductor Wafer Bonding, San Francisco, Sept 2-7, 2001]). Wafer separation/removal after bonding may be accomplished by grinding or etching the wafer away (preferably making use of an etch stop layer), or by making use of a mechanically weak interface layer created at earlier steps in processing. Examples of mechanically weak interface layers include porous Si (see, for example, Epitaxial Layer Transfer (ELTRAN) described by K. Sakaguchi et al. in Solid State Technology, June 2000] and ion-implanted H-containing bubbles (see, for example, Smart Cut process, described in U.S. Patent No. 5,374,564 by M. Bruel, which issued December 20, 1994, and U.S. Patent No. 5,882,987 by K.V. Srikrishnan, which issued March 16, 1999).

[0065] Amorphization would typically be effected by ion implantation. The optimum ion implantation conditions will depend on the materials of the template layers, the thickness of the template layers, and position (upper or lower) of the stack layer being amorphized. Any ion species known to those skilled in the art may be used, including but not limited to: Si, Ge, Ar, C, O, N, H, He, Kr, Xe, P, B, As, etc. Ions for the amorphization are preferably Si or Ge. Lighter ions such as H and He are typically less effective at amorphization. Ion implantation may be performed at temperatures ranging from cryogenic to several hundred °C above nominal room temperature. By "nominal room temperature" it is meant a temperature from about 20° to about 40°C. Regions not being amorphized would typically be protected from ion implantation by a patterned mask (for example, patterned photoresist for a room temperature implantation process). Implants may be performed with or without "screen oxide" layers and may be performed with multiple implants at different energies if a sufficiently uniformly

amorphized region cannot be easily achieved with a single implant. The required implant dose depends on the implanting species, the semiconductor being implanted, and the thickness of the layer needing to be amorphized. Si implanted at cryogenic temperatures at 50, 100, 150, and 200 keV with a total dose of  $6 \times 10^{15}/\text{cm}^2$  was found to be sufficient to amorphize the top 400 nm of 100-oriented and 110-oriented Si (see, for example, L. Csepregi et al.). However, much lower doses (for example,  $5 \times 10^{14}/\text{cm}^2$  at 40 keV) can amorphize Si when the implanted ion is Ge and surface region to be amorphized is thinner than 50-100 nm.

[0066] Recrystallization of localized amorphous regions 630, 730, and 850 is typically effected by annealing at temperatures from about 200° to about 1300°C, preferably from about 400° to about 900°C, and more preferably from about 400° and 600°C, for a time period sufficient to bring about the desired recrystallization. This time period will depend on the orientation of the template layer, on the thickness of the amorphized region to be recrystallized, on the presence of implanted and other impurities in the amorphized layer, and possibly on the sharpness of the interface between the implanted and unimplanted regions. Annealing may be performed in a furnace or by rapid thermal annealing. In other embodiments, annealing may be performed using a laser anneal or a spike anneal. The annealing ambient would typically be selected from the group of gases including N<sub>2</sub>, Ar, He, H<sub>2</sub> and mixtures of these gases.

[0067] When a buried insulating is created in the structure following the recrystallizing step, any conventional ion implant step and annealing step that can be used in forming a buried insulating layer can be employed. For example, any conventional SIMOX process can be used in producing a buried oxide layer in the structures shown in FIGS. 8F-8G.

[0068] Several embodiments of the present invention, together with modifications thereof, have been described in detail herein and illustrated in the accompanying

drawings, it will be evident that various further modifications are possible without departing from the scope of the invention. In particular, it should be emphasized that while most of the substrate structures, circuits, and methods of this invention have been illustrated for the case of a small number of single crystal regions having two different orientations, the invention applies equally well to methods for providing and structures comprising large pluralities of such single crystal regions. Furthermore, the hybrid-orientation substrates of the invention may incorporate additional overlayers (such as epitaxially grown semiconductors or additional bonded layers), removal or etchback of certain surface features (for example, recessing one or more of the single crystal semiconductor regions or trench isolations), and/or specialized doping profiles, if such substrate features are desired for the subsequently fabricated devices. Nothing in the above specification is intended to limit the invention more narrowly than the appended claims. The examples given are intended only to be illustrative rather than exclusive.

## CLAIMS

Having thus described our invention in detail, what we claim as new and desire to secure by the Letters Patent is:

1. A planar hybrid-orientation semiconductor-on-insulator (SOI) substrate structure comprising:

at least two clearly defined single crystal semiconductor regions with different surface orientations, said at least two clearly defined single crystal semiconductor regions disposed on a common buried insulating layer, said common buried insulating layer disposed on a substrate.

2. The planar hybrid-orientation SOI substrate structure of Claim 1 further comprising at least one isolation region separating said at least two clearly defined single crystal semiconductor regions from each other.

3. The planar hybrid-orientation SOI substrate structure of Claim 2 wherein said at least one isolation region is a trench isolation region.

4. The planar hybrid-orientation SOI substrate structure of Claim 2 wherein said at least one isolation region extends down to at least an upper surface of the common buried insulating layer.

5. The planar hybrid-orientation SOI substrate structure of Claim 2 wherein said at least one isolation region does not extend down to said common buried insulating layer.

6. The planar hybrid-orientation SOI substrate structure of Claim 1 wherein said at least two clearly defined single crystal semiconductor regions comprise the same or different semiconductor materials.

7. The planar hybrid-orientation SOI substrate structure of Claim 6 wherein said semiconductor materials are selected from the group consisting of Si, SiC, SiGe, SiGeC, Ge alloys, Ge, C, GaAs, InAs, InP, layered combinations or alloys thereof, and other III-V or II-VI compound semiconductors.

8. The planar hybrid-orientation SOI substrate structure of Claim 1 wherein said at least two clearly defined single crystal semiconductor regions with different surface orientations both comprise a Si-containing semiconductor material.

9. The planar hybrid-orientation SOI substrate structure of Claim 1 wherein said at least two clearly defined single crystal semiconductor regions are each comprised of strained, unstrained or a combination of strained and unstrained semiconductor materials.

10. The planar hybrid-orientation SOI substrate structure of Claim 1 wherein said different surface orientations are selected from the group consisting of (110), (111) and (100).

11. The planar hybrid-orientation SOI substrate structure of Claim 8 wherein said different surface orientations are selected from the group consisting of (110), (111) and (100).

12. The planar hybrid-orientation SOI substrate structure of Claim 11 wherein said first Si-containing semiconductor region has a (100) crystal orientation and said second Si-containing semiconductor region has a (110) crystal orientation.

13. The planar hybrid-orientation SOI substrate structure of Claim 12 further comprising at least one nFET device and at least one pFET device, wherein said at least one nFET device is located on said (100) crystal orientation and said at least pFET device is located on said (110) crystal orientation.

14. The planar hybrid-orientation SOI substrate structure of Claim 1 further comprising at least one nFET device and at least one pFET device, wherein said at least one nFET device is located on a crystal orientation that is optimal for said device said at least pFET device is located on a crystal orientation that is optimal for said device.

15. The planar hybrid-orientation SOI substrate structure of Claim 1 wherein said buried insulating layer is a dielectric material selected from the group consisting of SiO<sub>2</sub>, crystalline SiO<sub>2</sub>, SiO<sub>2</sub> containing nitrogen, silicon nitride, metal oxides, metal nitrides, and highly thermally conductive materials.

16. The planar hybrid-orientation SOI substrate structure of Claim 15 wherein said dielectric material is SiO<sub>2</sub> or crystalline SiO<sub>2</sub>.

17. The planar hybrid-orientation SOI substrate structure of Claim 1 wherein said substrate is a semiconductor material selected from the group consisting of Si, SiC, SiGe, SiGeC, Ge alloys, Ge, C, GaAs, InAs, InP, layered combinations or alloys thereof, and other III-V or II-VI compound semiconductors.



18. The planar hybrid-orientation SOI substrate structure of Claim 1 wherein said substrate has an epitaxial relationship to at least one of said single crystal semiconductor regions.

19. The planar hybrid-orientation SOI substrate structure of Claim 1 wherein said at least two clearly defined single crystal semiconductor regions comprise three single crystal semiconductor regions of different crystal orientation that are separated by isolation regions.

20. The planar-hybrid-orientation SOI substrate structure of Claim 19 further comprising at least one nFET device and at least one pFET device, wherein said at least one nFET device is located on a crystal orientation that is optimal for said device said at least pFET device is located on a crystal orientation that is optimal for said device.

21. The planar-hybrid-orientation SOI substrate structure of Claim 1 wherein at least one of said at least two clearly defined single crystal regions comprises an upper semiconductor disposed on a lower, residual semiconductor, said upper and lower semiconductors having different surface orientations, said residual semiconductor in direct contact with said common buried insulating layer.

22. The planar-hybrid-orientation SOI substrate structure of Claim 21 further comprising at least one nFET device and at least one pFET device, wherein said at least one nFET device is located on a crystal orientation that is optimal for said device said at least pFET device is located on a crystal orientation that is optimal for said device.

23. The planar hybrid-orientation SOI substrate structure of Claim 21 further comprising at least one isolation region separating said at least two clearly defined single

crystal semiconductor regions from each other, wherein said at least one isolation region extends down at least to said common buried insulating layer.

24. The planar hybrid-orientation SOI substrate structure of Claim 21 further comprising at least one isolation region separating said at least two clearly defined single crystal semiconductor regions from each other, wherein said at least one isolation region does not extend down to said common buried insulating layer.

25. The planar hybrid-orientation SOI substrate structure of Claim 1 wherein said substrate is an insulator.

26. The planar hybrid-orientation SOI substrate structure of Claim 8 wherein at least one of said at least two clearly defined single crystal Si-containing semiconductor regions comprises an upper Si-containing semiconductor disposed on a lower, residual Si-containing semiconductor, said upper and lower semiconductors having different surface orientations, said residual semiconductor in direct contact with said common buried oxide layer.

27. The planar hybrid-orientation SOI substrate structure of Claim 26 wherein said different surface orientations are selected from the group consisting of (110), (111) and (100).

28. The planar hybrid-orientation SOI substrate structure of Claim 27 wherein first Si-containing semiconductor region has a (100) crystal orientation and said second Si-containing semiconductor region has a (110) crystal orientation.

29. The planar hybrid-orientation SOI substrate structure of Claim 28 further comprising at least one nFET device and at least one pFET device, wherein said at least one nFET device is located on said (100) crystal orientation and said at least pFET device is located on said (110) crystal orientation.

30. The planar hybrid-orientation SOI substrate structure of Claim 26 further comprising at least one nFET device and at least one pFET device, wherein said at least one nFET device is located on a crystal orientation that is optimal for said device said at least pFET device is located on a crystal orientation that is optimal for said device.

31. The planar hybrid-orientation SOI substrate structure of Claim 26 further comprising at least one isolation region separating said at least two clearly defined single crystal Si-containing semiconductor regions from each other.

32. The planar hybrid-orientation SOI substrate structure of Claim 31 wherein said at least one isolation region is a trench isolation region.

33. The planar hybrid-orientation SOI substrate structure of Claim 31 wherein said at least one isolation region extends down to at least an upper surface of the common buried insulating layer.

34. The planar hybrid-orientation SOI substrate structure of Claim 31 wherein said at least one isolation region does not extend to said common buried oxide layer.

35. A method of forming a planar hybrid-orientation substrate comprising the steps of

forming a bilayer template layer stack comprising a first, lower single crystal semiconductor layer having a first orientation and a second, upper single crystal semiconductor layer having a second orientation different from the first;

amorphizing one of the semiconductor layers of the bilayer template stack in selected areas to form localized amorphized regions; and

recrystallizing the localized amorphized regions using a non-amorphized semiconductor layer of the stack as a template, thereby changing the orientation in the localized amorphized regions from an original orientation to a desired orientation.

36. The method of Claim 35 wherein said first, lower single crystal semiconductor layer is disposed on the insulating layer of an SOI substrate.

37. The method of Claim 35 wherein said first, lower single crystal semiconductor layer comprises a single crystal semiconductor substrate.

38. The method of Claim 35 wherein said second, upper single crystal semiconductor layer is formed atop the first, lower single crystal semiconductor by bonding.

39. The method of Claim 35 wherein said localized amorphized region is formed predominately within the second, upper single crystal semiconductor layer.

40. The method of Claim 35 wherein said localized amorphized region is formed predominately within the first, lower single crystal semiconductor layer.

41. The method of Claim 36 wherein said localized amorphized region is formed predominately within the first, lower single crystal semiconductor layer, and further including the step of removing said top layer after recrystallization, by a process such as chemical mechanical polishing.

42. The method of Claim 35 further comprising forming at least one trench isolation region to separate said areas selected for amorphization from those not selected for amorphization, said at least one trench isolation being formed prior to amorphizing, between amorphizing and recrystallizing, or partially after amorphizing and partially after recrystallizing.

43. The method of Claim 35 wherein said first, lower single crystal semiconductor and layer said second, upper single crystal semiconductor layer are composed of the same or different semiconductor material selected from the group consisting of Si, SiC, SiGe, SiGeC, Ge alloys, Ge, C, GaAs, InAs, InP, layered combinations or alloys thereof, and other III-V or II-VI compound semiconductors.

44. The method of Claim 35 wherein said first, lower single crystal semiconductor layer and said second, upper single crystal semiconductor layer are both composed of a Si-containing semiconductor material.

45. The method of Claim 35 wherein said first, lower single crystal semiconductor layer and said second, upper single crystal semiconductor layer are composed of strained, unstrained or a combination of strained and unstrained semiconductor materials.

46. The method of Claim 35 wherein said first, lower single crystal semiconductor layer and said second, upper single crystal semiconductor layer have different surface orientations selected from (110), (111) and (100).

47. The method of Claim 35 further comprising forming at least one nFET device and at least one pFET device, wherein said at least one nFET device is located on a crystal orientation that is optimal for said device said at least pFET device is located on a crystal orientation that is optimal for said device.

48. The method of Claim 37 further comprising forming a buried insulating layer after said recrystallizing step.

49. The method of Claim 48 wherein said buried insulating layer is formed by a separation-by-ion implantation of oxygen (SIMOX) process.

50. The method of Claim 35 wherein said amorphizing is accomplished by ion implantation.

51. The method of Claim 50 wherein said ion implantation comprises an ion selected from the group consisting of Si, Ge, Ar, C, O, N, H, He, Kr, Xe, P, B and As.

52. The method of Claim 50 wherein said ion implantation comprising an ion selected from the group consisting of Si and Ge.

53. The method of Claim 50 wherein said ion implantation is performed using a patterned mask.

54. The method of Claim 35 wherein said recrystallizing is performed at a temperature from about 200°C to about 1300°C

55. The method of Claim 35 wherein said recrystallizing is performed in a gas selected from the groups consisting of N<sub>2</sub>, Ar, He, H<sub>2</sub> and mixtures thereof.

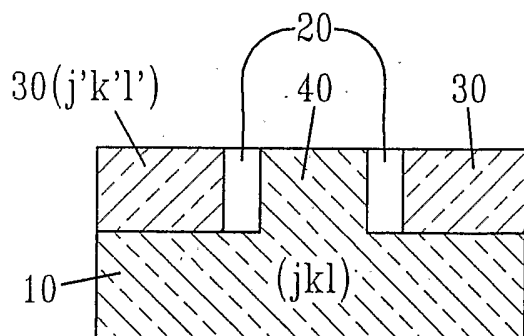


FIG. 1A  
Prior Art

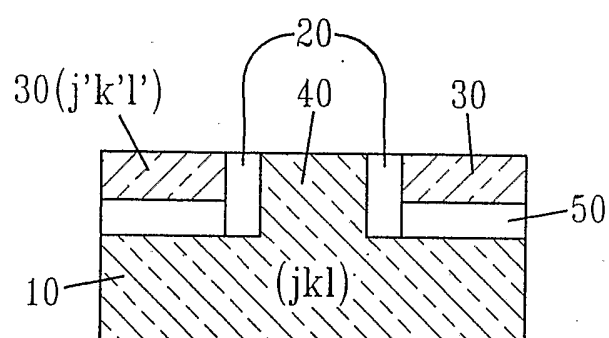


FIG. 1B  
Prior Art

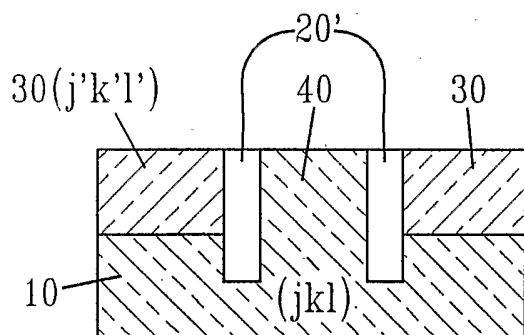


FIG. 1C  
Prior Art

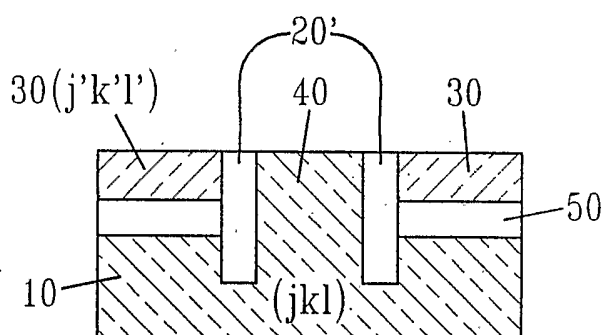


FIG. 1D  
Prior Art

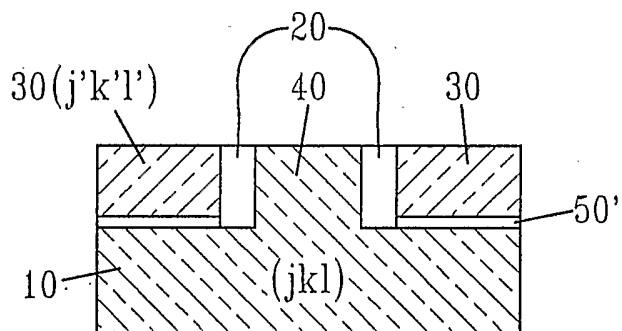


FIG. 1E  
Prior Art



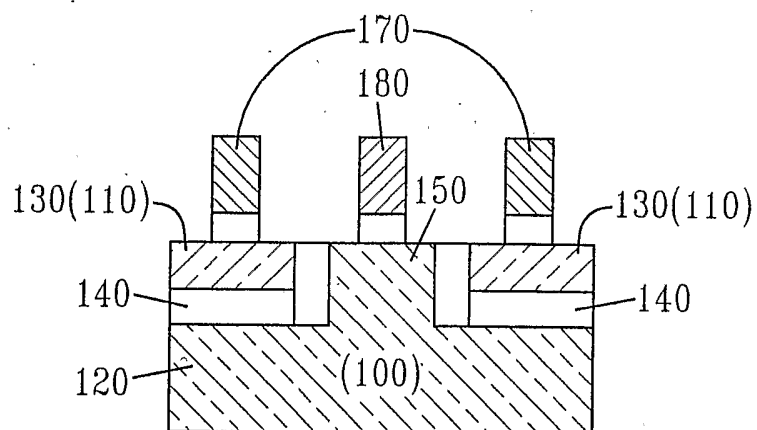


FIG. 2A  
Prior Art

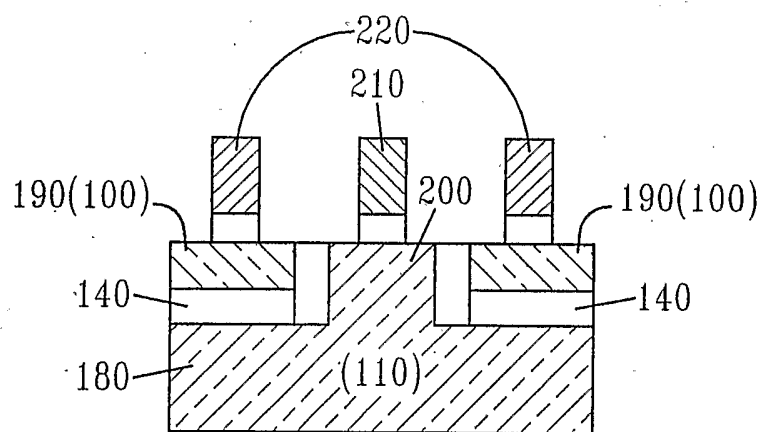


FIG. 2B  
Prior Art

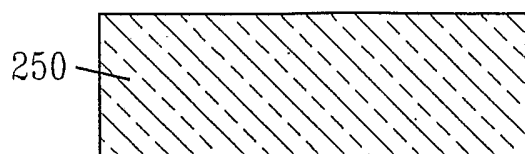


FIG. 3A  
Prior Art

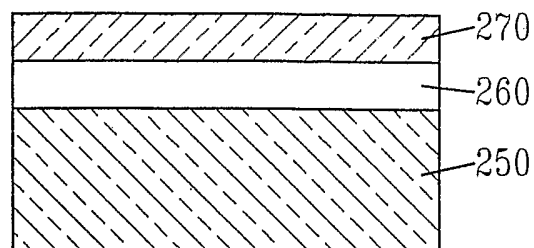


FIG. 3B  
Prior Art

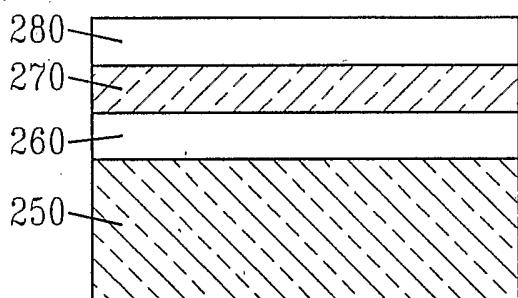


FIG. 3C  
Prior Art

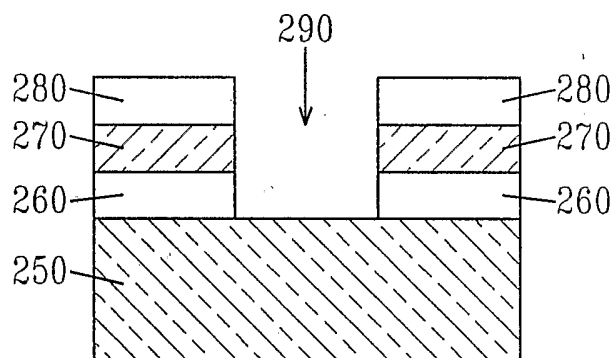


FIG. 3D  
Prior Art

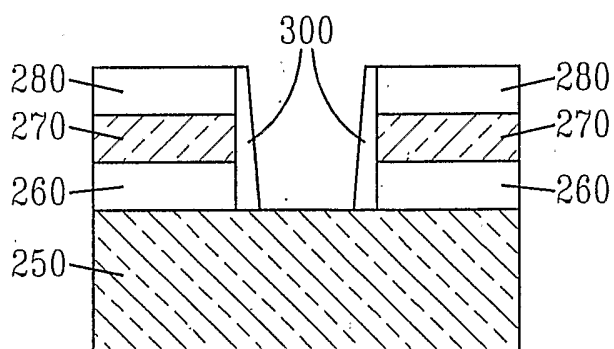


FIG. 3E  
Prior Art

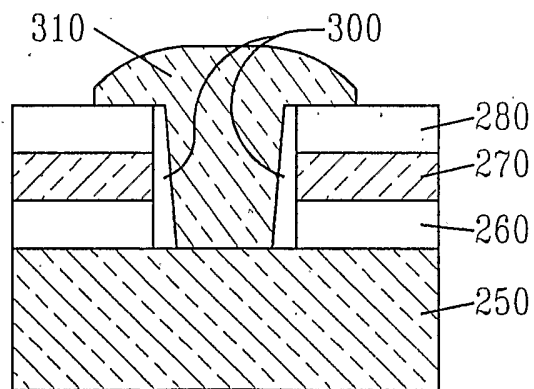


FIG. 3F  
Prior Art

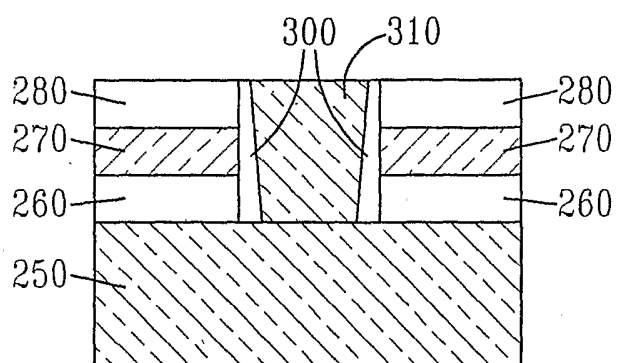


FIG. 3G  
Prior Art

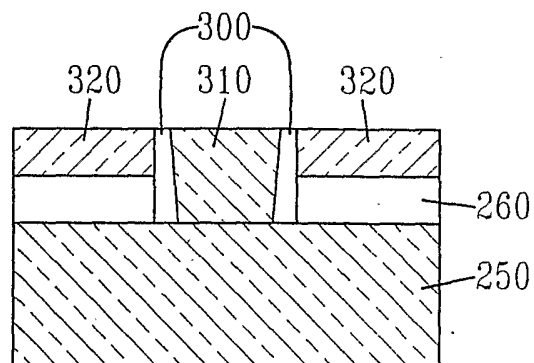


FIG. 3H  
Prior Art

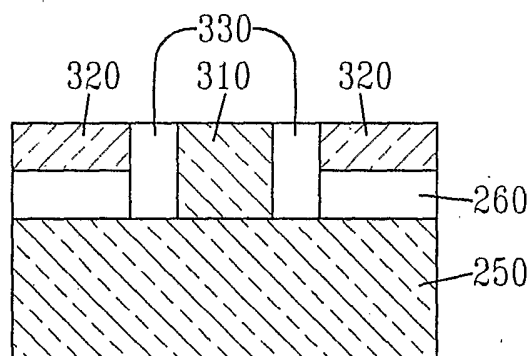


FIG. 3I  
Prior Art

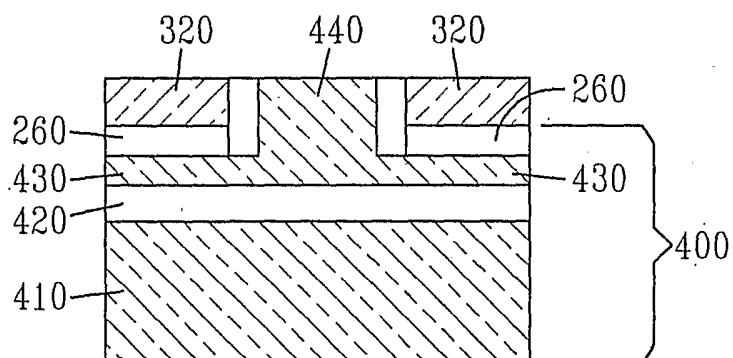


FIG. 4  
Prior Art

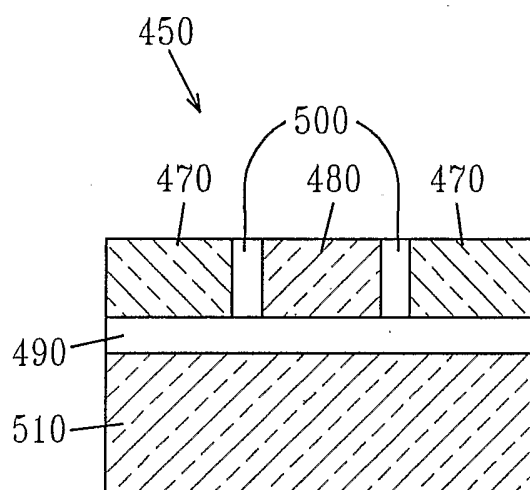


FIG. 5A

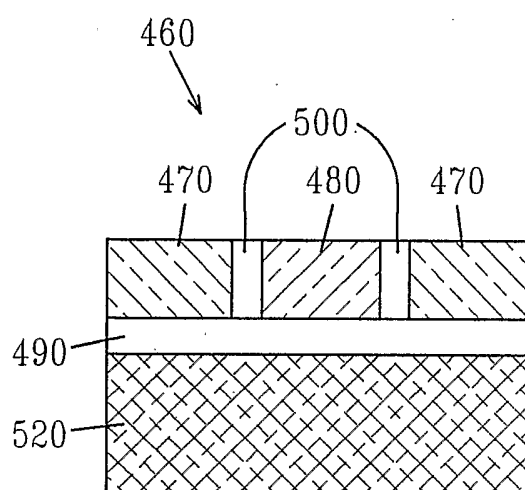


FIG. 5B

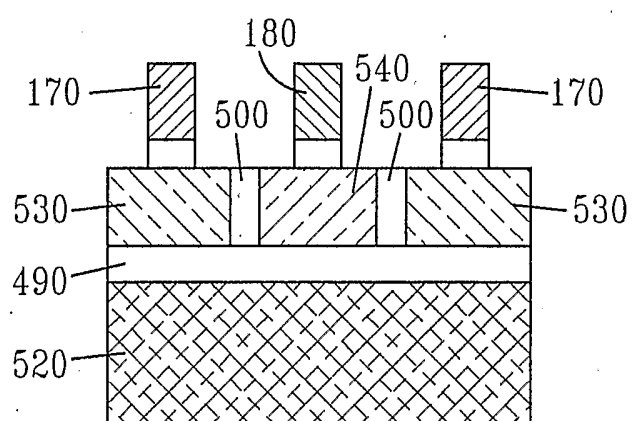


FIG. 6

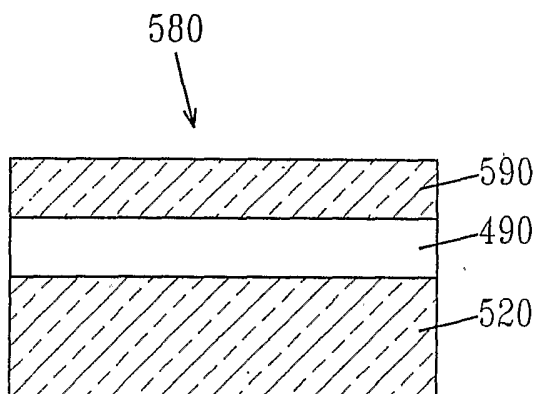


FIG. 7A

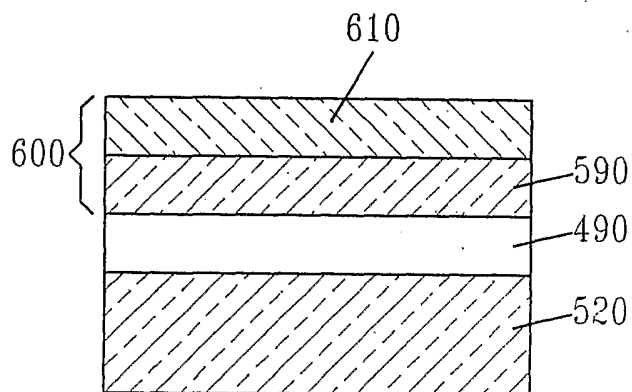


FIG. 7B

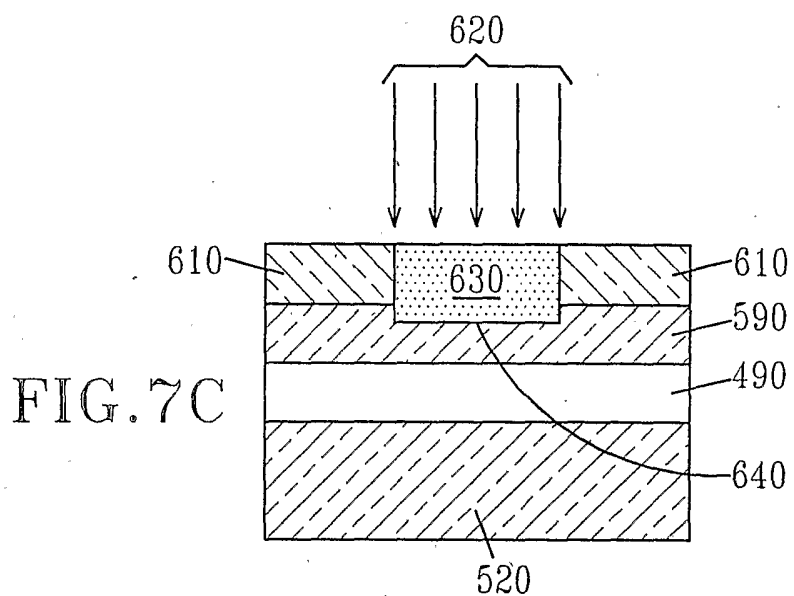


FIG. 7C

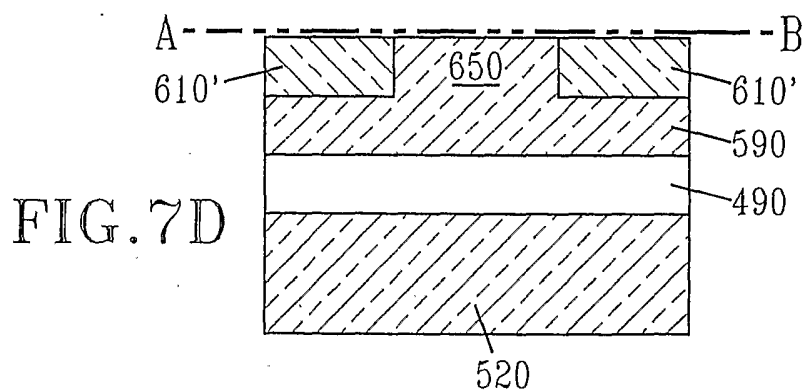


FIG. 7D

FIG. 7E

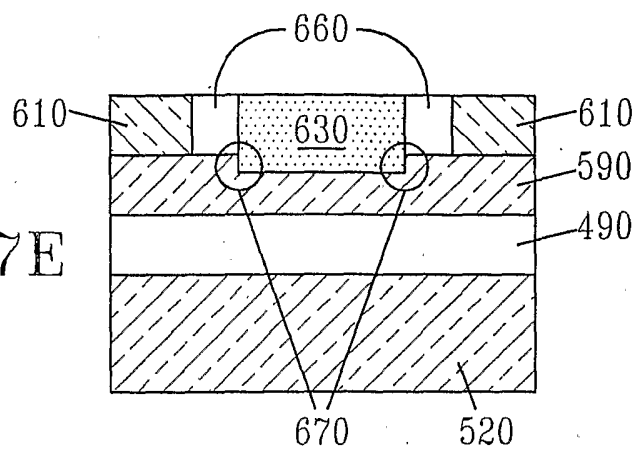


FIG. 7F

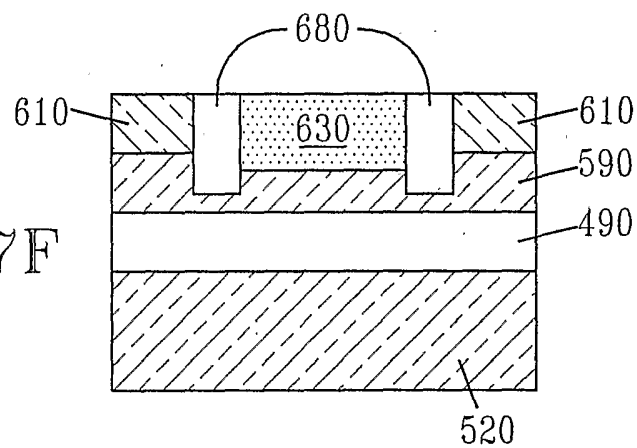
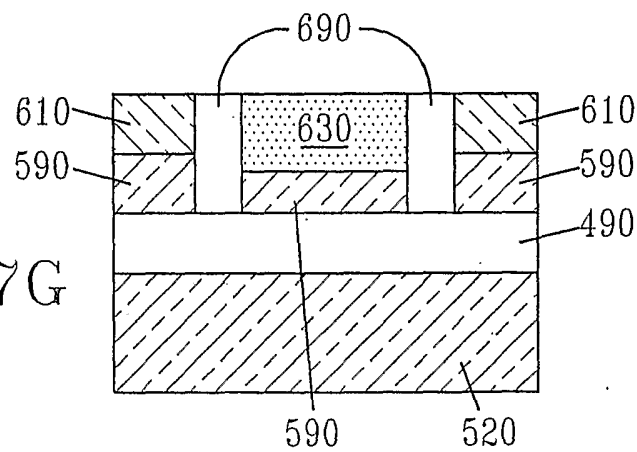


FIG. 7G



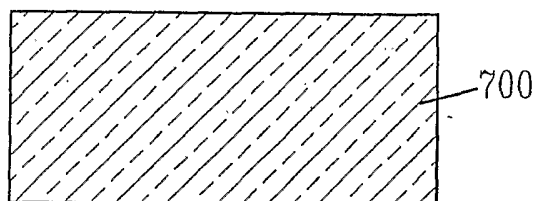


FIG. 8A

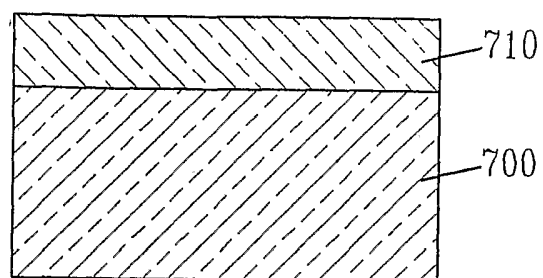


FIG. 8B

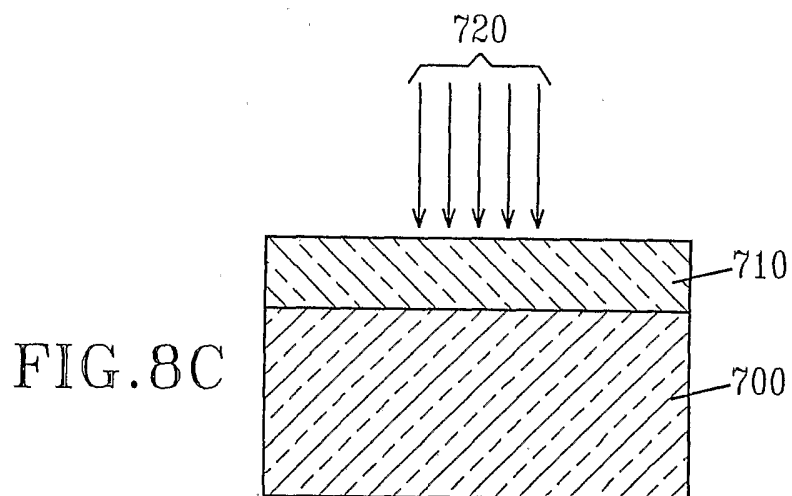


FIG. 8C

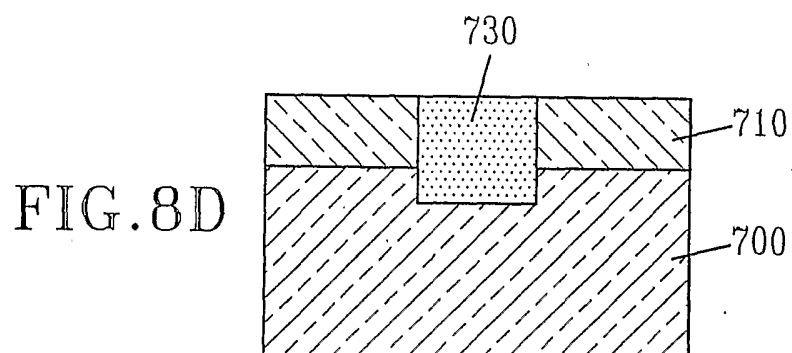
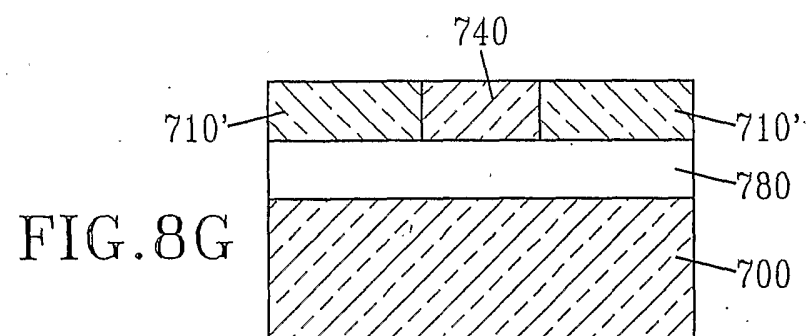
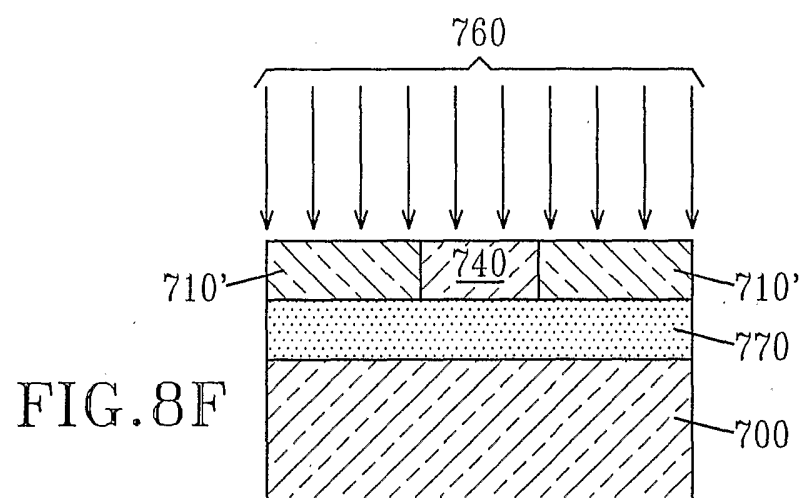
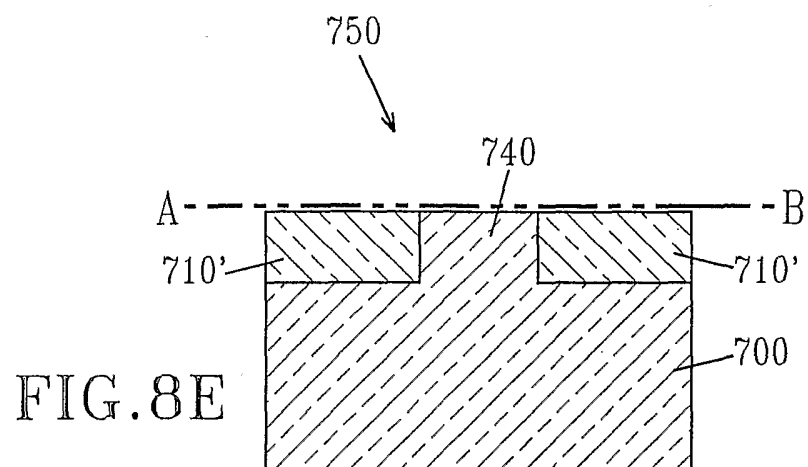


FIG. 8D





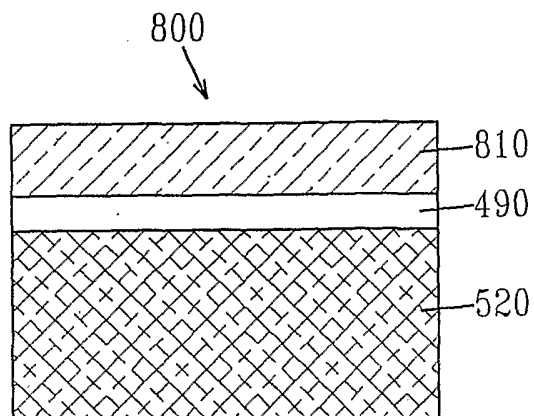


FIG. 9A

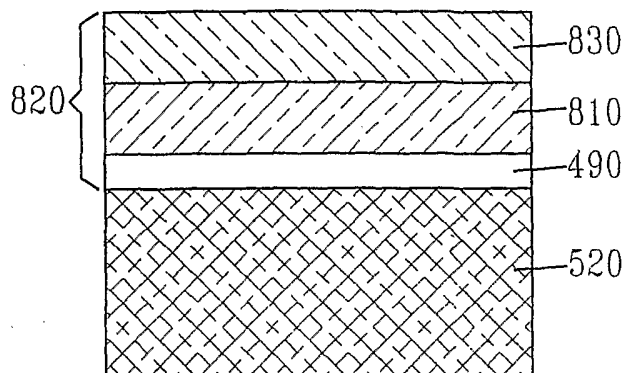


FIG. 9B

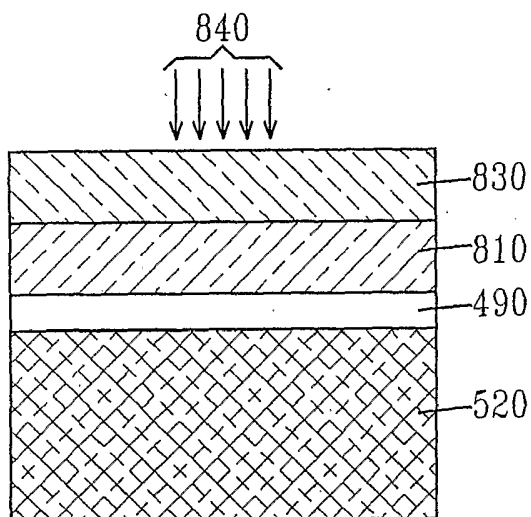


FIG. 9C

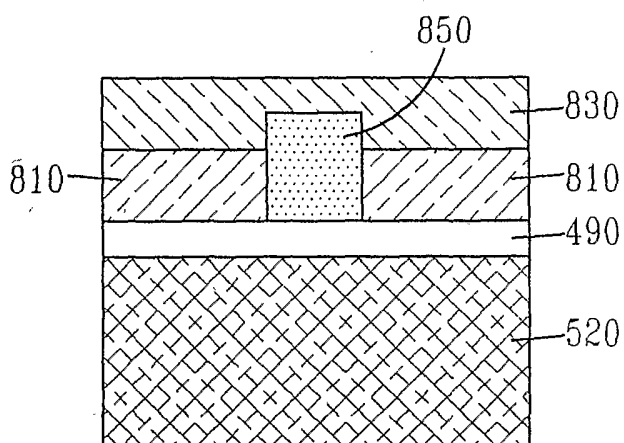


FIG. 9D

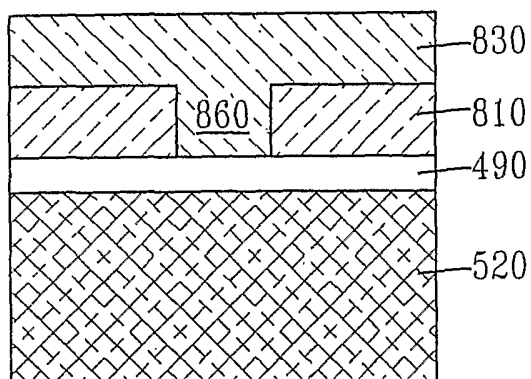


FIG. 9E

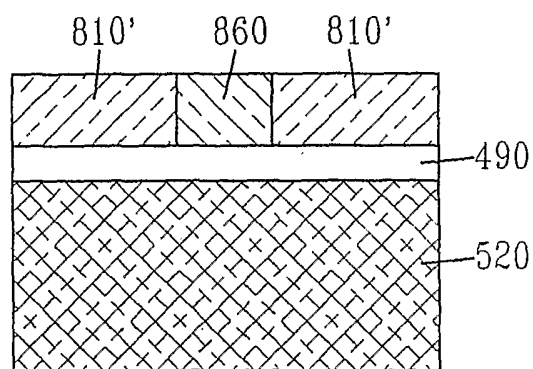


FIG. 9F

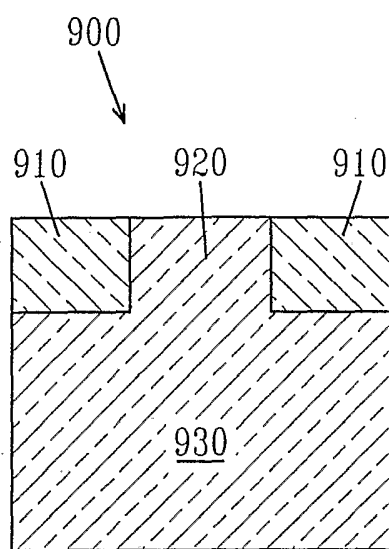


FIG. 10A

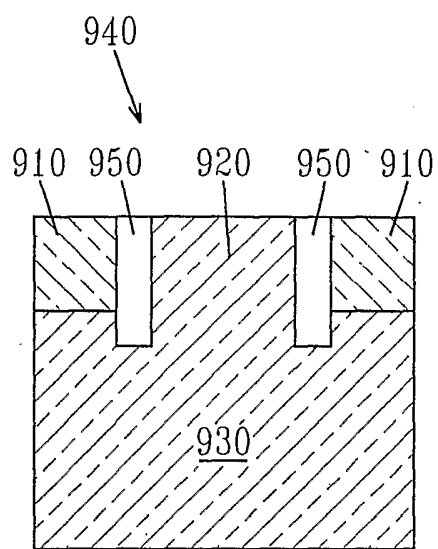


FIG. 10B

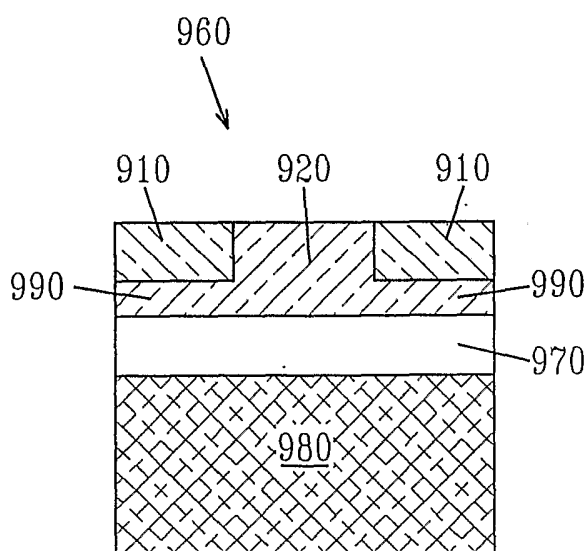


FIG. 10C

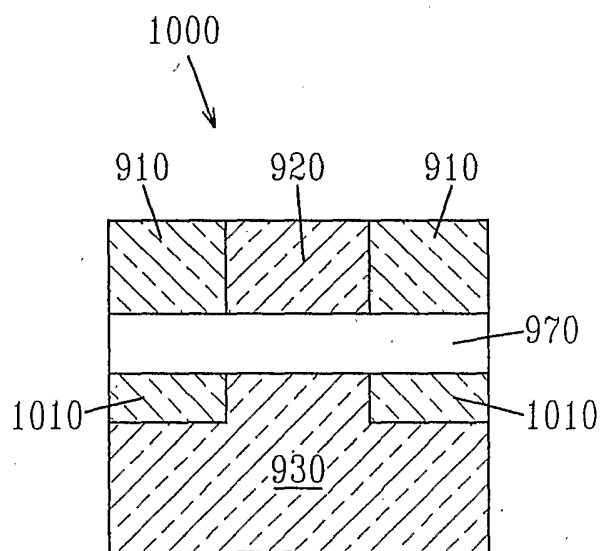


FIG. 10D

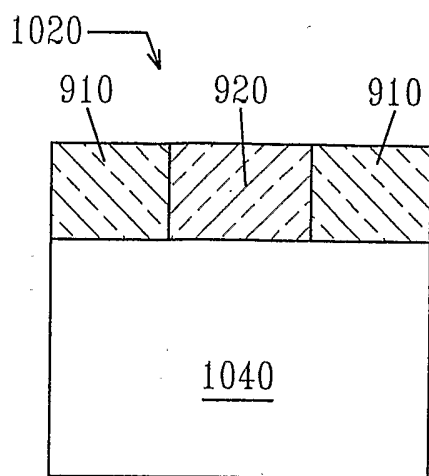


FIG. 10E

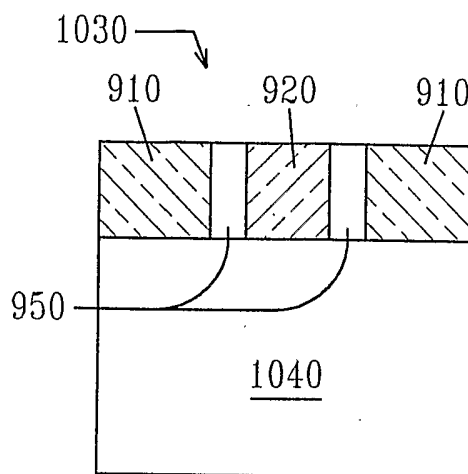


FIG. 10F

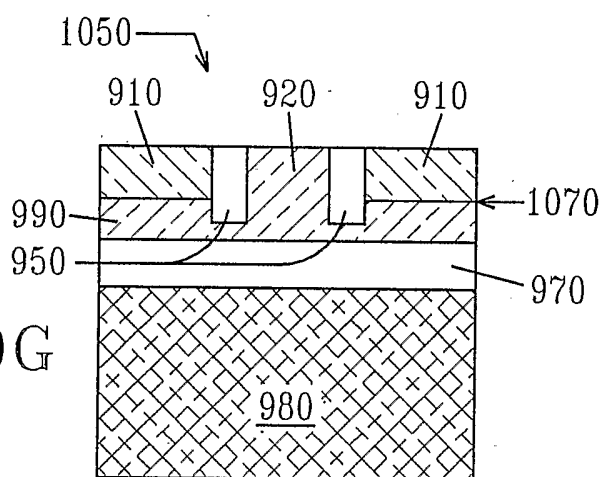


FIG. 10G

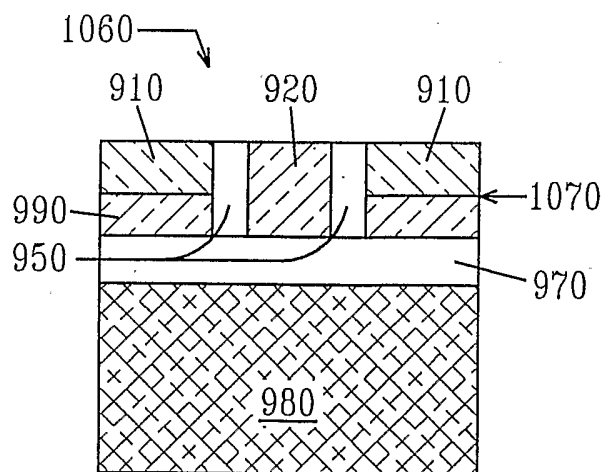


FIG. 10H

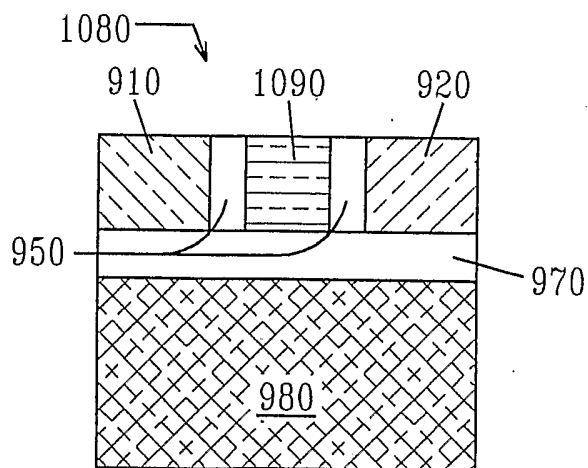


FIG. 10I