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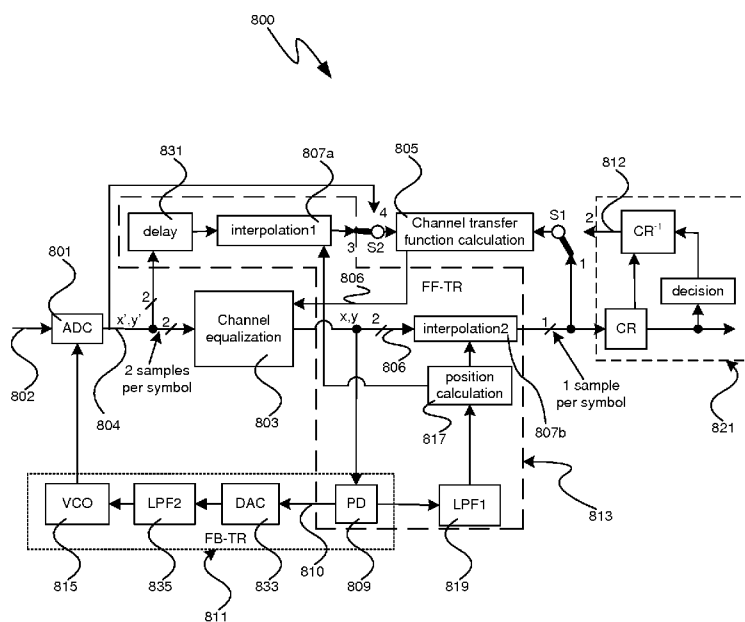


Fig. 8

(57) Abstract: The invention relates to a coherent optical receiver (800), comprising: analog-to-digital conversion means (801) configured for sampling an analog coherent optical signal (802) into a digital coherent optical signal (804); channel equalization means (803) configured for equalizing the digital coherent optical signal (804); channel transfer function calculation means (801) configured for calculating a channel transfer function (808) based on the digital coherent optical signal (804) and the equalized digital coherent optical signal (801) interpolated by interpolation means (807a, 807b) and configured for adjusting the channel equalization means (803) based on the calculated channel transfer function (808); phase detection means (809) configured for providing a timing error detection characteristic, TEDC, signal (810), based on the equalized digital coherent optical signal (806); feed-backward timing recovery means (811) configured for adjusting the sampling of the analog-to-digital conversion means (801) based on the TEDC signal (810) with respect to a frequency offset compensation criterion; and feed-forward timing recovery means (813) configured for adjusting the interpolation means (807a, 807b) with respect to a phase offset compensation criterion.

Coherent optical receiver

TECHNICAL FIELD

The present invention relates to a coherent optical receiver and a method for clock
5 recovery in a coherent optical receiver.

BACKGROUND

An important goal of long-haul optical fiber systems is to transmit the highest data
throughput over the longest distance without signal regeneration in optical-electrical-
10 optical regenerators. Given constraints on the bandwidth imposed by optical amplifiers
and ultimately by the fiber itself, it is important to maximize spectral efficiency. Most
current systems use binary modulation formats, such as on-off keying encoding one bit
per symbol.

Advanced modulation formats in combination with coherent receivers enable high capacity
15 and spectral efficiency. Polarization multiplexing, quadrature amplitude modulation and
coherent detection are seen as a winning combination for the next generation of high-
capacity optical transmission systems since they allow information encoding in all the
available degrees of freedom.

Commercial devices using QAM (quadrature amplitude modulation) constellation are
20 already available in 40 and 100 Gb/s optical transmission systems. The 16-QAM is likely a
candidate for 400 Gb/s optical transmission systems. A Block diagram of a coherent
optical receiver 100 is shown in Fig. 1. Since the digital signal is mapped into both
polarization a 90°hybrid 101 is used to mix the input signal 102 with the local oscillator
(LO) signal 104 that results in four output signals 106 (two signals per polarization). The
25 optical signal 102 is converted to an electrical signal via an optical front end (OFE) 103
consisting of photo diodes (single PIN or balanced) and a transimpedance amplifier (TIA).
As the signal power may vary over time, fast automatic gain control blocks 105
compensate for signal power variations. There are four automatic gain control (AGC)
blocks 105 that can also be an integral part of the OFE blocks 103. Often, due to
30 realization complexity, a pair of AGC blocks 105 is controlled by one control signal ($V_{X_{AGC}}$)

for X polarization and VY_{AGC} for Y polarization; see Fig. 1). However, four AGC blocks 105 can be controlled by 4 independent control voltages. Signals 108 after AGC blocks 105 are quantized by the use of analog-to-digital converters (ADCs) 107.

Four quantized digital data streams 110 are further processed in a digital signal processing (DSP) block 109 that is divided into two parts, a fast DSP hardware part 109a and a slow DSP software part 109b. In the DSP block 109, one compensates for chromatic dispersion (CD), polarization mode dispersion (PMD), polarization rotation, nonlinear effects, LO noise, LO frequency offset, etc. Estimation of slow processes (LO frequency offset, CD etc.) can be done in the software part 109b of the DSP circuit 109.

Basic DSP blocks 200 are presented in Fig. 2. After offset and gain correction 201 the four signals 202 are equalized for chromatic dispersion in frequency domain using two fast Fourier transformation (FFT) blocks 203. Frequency offset is removed in a frequency recovery block 205. Polarization tracking, PMD compensation and residual CD compensation are done in time domain using finite impulse response (FIR) filters 207 arranged in butterfly structure. Both residual frequency offset and carrier phase recovery are done in a carrier recovery block 209. When differential decoding is applied at the transmitter side, a differential decoder is used in a decoding and frame detection block 211. CD is efficiently compensated in FFT blocks 203. The compensation CD function is

$$CD^{-1}(DL) = \exp\left(-j\left(\frac{2\pi n f_s}{N}\right)^2 \frac{\lambda_0^2 DL}{4\pi c}\right)$$

where λ_0 is the signal wavelength, f_s is the sampling frequency, N is the FFT size, c is the speed of light, n is the tap number, L is fiber length, and D is dispersion coefficient.

Due to complexity reasons, only one FFT block 301 using complex input is applied to each polarization (Fig. 3). The inverse FFT (IFFT) 303 is identical to the FFT 301 although real and imaginary parts are swapped at input and output.

In digital communication systems, the heart of each receiver is a clock recovery circuit that extracts frequency and phase from incoming data and forces a local clock source to control the sampling rate and the sampling phase of the ADC. The second feature is not too important in over-sampled systems, as data processing blocks are less sensitive to the sampling phase. Several phase detectors (PD) have been proposed for digital systems. Some of them are frequently used in practical systems: The Mueller and Müller

phase detector is described in [K. H. Mueller and M. Muller, IEEE Transaction on Comm. 24, 516-531 (1976)]. The Alexander phase detector is described in [J. D. H. Alexander, Electron. Lett. 111, 541-542 (1975)]. The Gardner phase detector is described in [F. Gardner, IEEE Transaction on Comm. 34, 423-429 (1986)]. The Godard phase detector is described in [D. Godard, IEEE Transaction on Comm. 26, 517-523 (1978)]. It is common for all phase detectors that a timing error detector characteristic (PD output over symbol interval) is very similar to the sinusoidal function. One exception is the "bang-bang" phase detector of Alexander which TEDC also has sinusoidal shape in the presence of noise.

The Mueller and Müller PD works with one sample per symbol. Other PDs are used with two-fold oversampling.

The Gardner PD TEDC can be described for complex signals as:

$$TEDC(\tau) = E[real(x(kT - T/2 + \tau)(x^*(kT + \tau) - x^*(kT - T + \tau)))] \quad (1)$$

where T is symbol interval, x is input signal, τ is the sampling instant (between 0 and T), E is expectation operator, and $*$ denotes complex conjugate operation. The Godard PD can be easily translated in FFT domain as

$$TEDC(\tau) = E\left[imag\left(\sum_{k=0}^{N/2-1} X(k)X^*(N/2 + k)\right)\right] \quad (2)$$

where N is the FFT size (size of Fourier transform), and X is FFT of $x(kT/2 + \tau)$, $k=0,1,\dots,N-1$. The received signal is oversampled (two samples per symbol).

The Nyquist transmission based on Nyquist pulses is used to frequency limit the channel bandwidth. This enables better channel packaging and automatically higher spectral efficiency. The raised-cosine filter is an implementation of a low-pass Nyquist filter, i.e., one that has the property of vestigial symmetry. This means that its spectrum exhibits odd symmetry about $1/2T$, where T is the symbol-period of the communications system. Its frequency-domain description is given by:

$$H(f) = \begin{cases} T, & |f| \leq \frac{1-\beta}{2T} \\ \frac{T}{\beta} \left[1 + \cos \left(\frac{\pi T}{\beta} \left[|f| - \frac{1-\beta}{2T} \right] \right) \right], & \frac{1-\beta}{2T} < |f| \leq \frac{1+\beta}{2T} \\ 0, & \text{otherwise} \end{cases}$$

$$0 \leq \beta \leq 1 \quad (3)$$

and characterized by two values; β , the *roll-off factor*, and T , the sampling period. The impulse response of such a filter is given by:

$$h(t) = \text{sinc} \left(\frac{t}{T} \right) \frac{\cos \left(\frac{\pi \beta t}{T} \right)}{1 - \frac{\beta^2 t^2}{T^2}} \quad (4)$$

in terms of the normalized sinc function. The roll-off factor, β , is a measure of the *excess bandwidth* of the filter, i.e. the bandwidth occupied beyond the Nyquist bandwidth of $1/2T$.

Frequency 400a and impulse response 400b of the Nyquist filter are shown in Fig. 4. The minimum signal bandwidth is achieved for a roll-off factor equal to 0.

Decreasing the roll-off factor (ROF, β) destroys the clock tone quality. The TEDC becomes very small that generates large and uncontrolled jitter. The TEDC simulation results 500 of the Gardner PD for QPSK modulation format at $E_b/N_0=3\text{dB}$ show serious clock tone degradation for small ROF values as can be seen from Fig. 5. A sinusoidal TEDC becomes acceptable for ROF values greater than 0.3.

For the same case, more TEDC characteristics 600 (one per 512 symbols) were simulated for ROF=0. The results shown in Fig. 6 illustrate the clock recovery problem.

TEDCs are very small and desynchronized.

The solution 700 described by [T. T. Fang, IEEE Transaction on Comm. 1, 133-140 (1991)] uses 4th power operation in PAM systems to generate the clock tone at Baud rate as illustrated in Fig. 7. This approach uses specific pre-filter 701 and narrowband filter 703

to filter out the clock tone. It enables the clock extraction for small ROF value but fails for higher ROF values. The complete system 700 is realized in the analog domain where there is no any limitation in terms of sampling frequency and signal digitalizing before the clock extraction.

5

SUMMARY

It is the object of the invention to provide a technique for improved clock recovery in coherent optical receivers.

10 This object is achieved by the features of the independent claims. Further implementation forms are apparent from the dependent claims, the description and the figures.

A technique for improved clock recovery can be realized by using feed-forward and feed-backward clock recovery coupled by a phase detector providing a timing error detection characteristic (TDEC) signal for clock offset and phase offset compensation.

15 In order to describe the invention in detail, the following terms, abbreviations and notations will be used:

QAM: quadrature amplitude modulation,

QPSK: quadrature phase shift keying,

LO: local oscillator,

OFE: optical front end,

20 PIN: positive intrinsic negative,

AGC: automatic gain control,

ADC: analog-to-digital converter,

DSP: digital signal processing,

CD: chromatic dispersion,

25 PMD: polarization mode dispersion,

	FFT:	Fast Fourier Transform,
	FIR:	finite impulse response,
	PD:	phase detector,
	TEDC:	timing error detection characteristic,
5	ROF:	roll-off factor,
	TR:	timing recovery,
	FF-TR:	feed-forward timing recovery,
	FB-TR:	feed-backward timing recovery,
	CR:	clock recovery,
10	LPF:	low-pass filter,
	DAC:	digital-to-analog converter,
	VCO:	voltage controlled oscillator,
	UI:	unit interval,
	CDU:	clock distribution unit,
15	OFDM:	orthogonal frequency division multiplex.

According to a first aspect, the invention relates to a coherent optical receiver, comprising:
analog-to-digital conversion means configured for sampling an analog coherent optical
signal into a digital coherent optical signal; channel equalization means configured for
equalizing the digital coherent optical signal; channel transfer function calculation means
configured for calculating a channel transfer function based on the digital coherent optical
signal and the equalized digital coherent optical signal interpolated by interpolation means
and configured for adjusting the channel equalization means based on the calculated
channel transfer function; phase detection means configured for providing a timing error
detection characteristic, TEDC, signal, based on the equalized digital coherent optical

signal; feed-backward timing recovery means configured for adjusting the sampling of the analog-to-digital conversion means based on the TEDC signal with respect to a frequency offset compensation criterion; and feed-forward timing recovery means configured for adjusting the interpolation means with respect to a phase offset compensation criterion.

- 5 The coherent optical receiver provides clock extraction in Nyquist systems. By using the feed-forward and feed-backward timing recovery means, clock extraction can be enabled independently on the roll-off factor, ROF, β . The coherent optical receiver provides a timing signal for feed-back timing recovery by using the feed-backward timing recovery means. The coherent optical receiver enables feed-forward timing recovery tolerating
- 10 large and fast jitter by using the feed-forward timing recovery means. By using the interpolation means, the coherent optical receiver generates the quadrature component using the simplest linear interpolation that does not require four samples per each complex signal component which is easy to implement. The coherent optical receiver can be operated independently on modulation formats.
- 15 In a first possible implementation form of the coherent optical receiver according to the first aspect, the TEDC signal indicates a phase offset and a frequency offset of the analog coherent optical signal with respect to a local oscillator, the local oscillator controlling the sampling of the analog-to-digital conversion means.

By using the TEDC signal, phase offset and a frequency offset of the analog coherent

20 optical signal can be compensated.

In a second possible implementation form of the coherent optical receiver according to the first aspect as such or according to the first implementation form of the first aspect, the interpolation means comprises first interpolation means configured for interpolating the digital coherent optical signal and second interpolation means configured for interpolating

25 the equalized digital coherent optical signal.

In a third possible implementation form of the coherent optical receiver according to the second implementation form of the first aspect, the first interpolation means provides two output samples for two input samples; and the second interpolation means provides one output sample for two input samples.

30 When the first interpolation means provides two output samples for two input samples and the second interpolation means provides one output sample for two input samples,

interpolation can be correctly adjusted for precisely calculating the channel transfer function.

In a fourth possible implementation form of the coherent optical receiver according to the first aspect as such or according to any of the preceding implementation forms of the first aspect, the feed-forward timing recovery means comprises position calculation means
5 configured for calculating clock positions based on the TEDC signal.

By using the position calculation means, clock positions can be precisely adjusted with respect to phase offset compensation.

In a fifth possible implementation form of the coherent optical receiver according to the fourth implementation form of the first aspect, the interpolation means is configured to
10 provide samples of the digital coherent optical signal and the equalized digital coherent optical signal at the calculated clock positions.

When the interpolation means provides samples of the digital coherent optical signal and the equalized digital coherent optical signal at the calculated clock positions, the channel
15 equalization means can accurately equalize the digital coherent optical signal, thereby reducing the bit error rate.

In a sixth possible implementation form of the coherent optical receiver according to the fourth implementation form of the first aspect, the TEDC signal is filtered by an infinite impulse response, IIR, low-pass filter before being provided to the position calculation
20 means.

In a seventh possible implementation form of the coherent optical receiver according to the first aspect as such or according to any of the preceding implementation forms of the first aspect, the coherent optical receiver comprises: carrier recovery means configured to
25 recover a carrier signal of the analog coherent optical signal based on the equalized digital coherent optical signal.

By recovering the carrier signal, the coherent optical receiver is flexible for using the carrier signal or the digital coherent optical signal for detecting the channel transfer function.

In an eighth possible implementation form of the coherent optical receiver according to the seventh implementation form of the first aspect, the channel transfer function calculation
30

means is configured for calculating the channel transfer function based on the carrier signal.

Calculating the channel transfer function based on the carrier signal is easy to implement.

5 In a ninth possible implementation form of the coherent optical receiver according to the first aspect as such or according to any of the preceding implementation forms of the first aspect, the digital coherent optical signal comprises two samples per symbol.

Using a digital coherent optical signal comprising two samples per symbol improves the accuracy of the receiver.

10 In a tenth possible implementation form of the coherent optical receiver according to the ninth implementation form of the first aspect, the phase detection means is configured for providing the TEDC signal based on samples of two contiguous symbol intervals.

A TEDC signal based on samples of two contiguous symbol intervals can be easily calculated. A simple filter with one delay element can be applied for that calculation.

15 In an eleventh possible implementation form of the coherent optical receiver according to the first aspect as such or according to any of the preceding implementation forms of the first aspect, the coherent optical receiver is configured for receiving optical signals using Nyquist pulses, configured for receiving optical signals of any QAM or PSK modulation format and/or configured for receiving optical signals with signal bandwidth smaller than a minimum defined Nyquist bandwidth.

20 By receiving optical signals using Nyquist pulses, the performance of the receiver with respect to data rate is improved. The coherent optical receiver can be flexibly used for receiving any QAM or PSK modulation format.

25 According to a second aspect, the invention relates to a phase detector for a coherent optical receiver, wherein the phase detector is configured for providing a TEDC signal based on a digital coherent optical signal according to the following relations: $TEDC(\tau) = E(\text{real}\{[C(n-1)-C(n+1)]\text{conj}[C(n)]\})$, $C(n-1) = A(n-1)\text{conj}[\alpha+(1-\alpha)B(n-1)]$, $C(n) = B(n-1)\text{conj}[\alpha+(1-\alpha)A(n)]$, $C(n+1) = A(n)\text{conj}[\alpha+(1-\alpha)B(n)]$, where $A(n)$ and $B(n)$ describe samples of the digital coherent optical signal (804) within one symbol interval n , $E()$ denotes expectation value and $\text{conj}[]$ denotes conjugate complex operation.

Such a phase detector provides a linear TEDC signal having a strong clock tone and low jitter.

In a first possible implementation form of the phase detector according to the second aspect, the phase detector is configured for providing a linear TEDC signal, in particular
5 by applying the relations according to the second aspect to the digital coherent optical signal and a shifted version thereof.

Such phase detector can be easily implemented by using standard FIR filtering or IIR filtering.

According to a third aspect, the invention relates to a method for clock recovery in a
10 coherent optical receiver, the method comprising: sampling an analog coherent optical signal into a digital coherent optical signal; equalizing the digital coherent optical signal; calculating a channel transfer function based on interpolations of the digital coherent optical signal and the equalized digital coherent optical signal and adjusting the channel equalization means based on the calculated channel transfer function; providing a timing
15 error detection characteristic, TEDC, signal, based on the equalized digital coherent optical signal; adjusting the sampling of the analog-to-digital converter based on the TEDC signal with respect to a frequency offset compensation criterion; and adjusting the interpolations of the digital coherent optical signal and the equalized digital coherent optical signal with respect to a phase offset compensation criterion.

20 Such a method can be advantageously applied for clock extraction in Nyquist systems. By adjusting the sampling of the analog-to-digital converter based on the TEDC signal with respect to a frequency offset compensation criterion and by adjusting the interpolations of the digital coherent optical signal and the equalized digital coherent optical signal with respect to a phase offset compensation criterion, the clock extraction can be enabled
25 independently on the roll-off factor. The method thus provides a timing signal for feed-back timing recovery and enables feed-forward timing recovery tolerating large and fast jitter. By using the interpolations, the method is able to generate the quadrature component using the simplest linear interpolation that does not require four samples per each complex signal component which is easy to implement. The method therefore allows
30 operating a coherent optical receiver independently on modulation formats.

The methods, systems and devices described herein may be implemented as software in a Digital Signal Processor (DSP), in a micro-controller or in any other side-processor or as hardware circuit within an application specific integrated circuit (ASIC).

5 The invention can be implemented in digital electronic circuitry, or in computer hardware, firmware, software, or in combinations thereof, e.g. in available hardware of conventional mobile devices or in new hardware dedicated for processing the methods described herein.

BRIEF DESCRIPTION OF THE DRAWINGS

10 Further embodiments of the invention will be described with respect to the following figures, in which:

Fig. 1 shows a block diagram illustrating a conventional coherent optical receiver 100;

Fig. 2 shows a block diagram illustrating basic DSP blocks 200 of the coherent optical receiver 100 depicted in Fig. 1;

15 Fig. 3 shows a block diagram illustrating a CD compensation block 300 of the basic DSP blocks 200 depicted in Fig. 2;

Fig. 4 shows diagrams of frequency 400a and impulse response 400b of a conventional raised-cosine filter with various roll-off factors;

20 Fig. 5 shows a diagram illustrating QPSK Gardner timing error detection characteristics (TEDC) 500 for roll-off factors from 0 to 1 in steps of 0.1 for the raised-cosine filter depicted in Fig. 4;

Fig. 6 shows a diagram illustrating QPSK Gardner TEDCs 600 for a roll-off factor of 1 for the raised-cosine filter depicted in Fig. 4;

25 Fig. 7 shows a block diagram illustrating signal preprocessing of a 4th power low analog system 700 for clock tone extraction;

Fig. 8 shows a block diagram illustrating a coherent optical receiver 800 according to an implementation form;

Fig. 9 shows a diagram illustrating a TED characteristic 900 of a phase detector according to an implementation form;

Fig. 10 shows eye diagrams of real 1000a and imaginary 1000b parts of QPSK modulated signal;

- 5 Fig. 11a shows a block diagram of a phase detector 1100 with linear TEDC according to an implementation form;

Fig. 11b shows a block diagram of a low pass filter 1150 used in the phase detector 1100 depicted in Fig. 11a according to an implementation form;

- 10 Fig. 12 shows a TEDC diagram illustrating the linear TEDC 1200 of the phase detector 1100 depicted in Fig. 11 for a $ROF=0$ and $\alpha=0$;

Fig. 13 shows a block diagram of a phase detector 1300 with linear TEDC according to an implementation form;

Fig. 14 shows a block diagram of a phase detector 1400 with linear TEDC comprising a circuit for changing the sampling phase according to an implementation form;

- 15 Fig. 15a shows a diagram 1500a illustrating a parameter $W1$ for $ROF=0$ and $\alpha=0$ for the phase detector with linear TEDC depicted in Fig. 13;

Fig. 15b shows a diagram 1500b illustrating a parameter $gW2$ for $ROF=0$ and $\alpha=0$ for the phase detector with linear TEDC depicted in Fig. 13;

- 20 Fig. 15c shows a diagram 1500c illustrating TEDC for $ROF=0$ and $\alpha=0$ for the phase detector with linear TEDC depicted in Fig. 13;

Fig. 16 shows a diagram 1600 illustrating TEDC for 4QAM and $E_b/N_0=3\text{dB}$ for the phase detector with linear TEDC depicted in Fig. 13;

Fig. 17 shows a diagram 1700 illustrating TEDC for 16QAM and $E_b/N_0=6\text{dB}$ for the phase detector with linear TEDC depicted in Fig. 13;

- 25 Fig. 18 shows a diagram 1800 illustrating TEDCs for 64QAM and $E_b/N_0=10\text{dB}$ for the phase detector with linear TEDC depicted in Fig. 13;

Fig. 19 shows a diagram 1900 illustrating TEDCs for 4QAM and $E_b/N_0=3\text{dB}$ for the phase detector with linear TEDC depicted in Fig. 13;

Fig. 20 shows a diagram 2000 illustrating TEDCs for 16QAM and $E_b/N_0=6\text{dB}$ for the phase detector with linear TEDC depicted in Fig. 13;

- 5 Fig. 21 shows a diagram 2100 illustrating TEDCs for 64QAM and $E_b/N_0=10\text{dB}$ for the phase detector with linear TEDC depicted in Fig. 13;

Fig. 22 shows a block diagram of a transmitter circuit 2200 and a receiver circuit 2250 illustrating Nyquist super-channel clocking according to an implementation form;

- 10 Fig. 23 shows a block diagram illustrating a circuit 2300 comprising parallel implemented phase detectors according to an implementation form; and

Fig. 24 shows a schematic diagram illustrating a method 2400 for clock recovery in a coherent optical receiver according to an implementation form.

DETAILED DESCRIPTION OF EMBODIMENTS OF THE INVENTION

- 15 Fig. 1 shows a block diagram illustrating a conventional coherent optical receiver 100 as described above.

Fig. 2 shows a block diagram illustrating basic DSP blocks 200 of the coherent optical receiver 100 depicted in Fig. 1 as described above.

- 20 Fig. 3 shows a block diagram illustrating a CD compensation block 300 of the basic DSP blocks 200 depicted in Fig. 2 as described above.

Fig. 4 shows diagrams of frequency 400a and impulse response 400b of a conventional raised-cosine filter with various roll-off factors as described above.

- 25 Fig. 5 shows a diagram illustrating QPSK Gardner timing error detection characteristics (TEDC) 500 for roll-off factors from 0 to 1 in steps of 0.1 for the raised-cosine filter depicted in Fig. 4 as described above.

Fig. 6 shows a diagram illustrating QPSK Gardner TEDCs 600 for a roll-off factor of 1 for the raised-cosine filter depicted in Fig. 4 as described above.

Fig. 7 shows a block diagram illustrating signal preprocessing of a 4th power low analog system 700 for clock tone extraction as described above.

Fig. 8 shows a block diagram illustrating a coherent optical receiver 800 according to an implementation form.

- 5 The coherent optical receiver 800 comprises analog-to-digital conversion means 801, e.g. an analog-to-digital converter (ADC) configured for sampling an analog coherent optical signal 802 into a digital coherent optical signal 804. The coherent optical receiver 800 comprises channel equalization means 803 configured for equalizing the digital coherent optical signal 804. The coherent optical receiver 800 comprises channel transfer function calculation means, e.g. a channel transfer function calculator 805 configured for
- 10 calculating a channel transfer function 808 based on the digital coherent optical signal 804 and the equalized digital coherent optical signal 806 interpolated by interpolation means 807a, 807b and configured for adjusting the channel equalization means 803 based on the calculated channel transfer function 808. The digital coherent optical signal 804
- 15 passes a delay element 831 and first interpolation means, e.g. a first interpolator 807a before being provided to the channel transfer function calculation means 805. A switch S2 is used for switching the digital coherent optical signal 804 either directly or after having passed the delay element 831 and the first interpolator 807a to the channel transfer function calculation means 805.
- 20 The analog coherent optical signal 802 may correspond to the signal 108 described above with respect to Fig. 1. The analog-to-digital converter (ADC) 801 may correspond to the ADC 107 described above with respect to Fig. 1. The digital coherent optical signal 804 may correspond to the signal 110 described above with respect to Fig. 1.

- 25 The coherent optical receiver 800 comprises phase detection means 809, e.g. a phase detector as described below with respect to Figures 11, 13 and 14, configured for providing a timing error detection characteristic, TEDC, signal 810, based on the equalized digital coherent optical signal 806.

- 30 The coherent optical receiver 800 comprises feed-backward timing recovery means 811 configured for adjusting the sampling of the analog-to-digital conversion means 801 based on the TEDC signal 810 with respect to a frequency offset compensation criterion. The TEDC signal 810 passes a digital-to-analog converter 833 and a low pass filter 835 before being provided to a local oscillator of a voltage controlled oscillator 815. The voltage

controlled oscillator (VCO) 815 controls the adjusting of the sampling rate and sampling time of the analog-to-digital converter 801 such that a frequency offset between the digital coherent optical signal and the analog coherent optical signal is compensated.

5 The coherent optical receiver 800 comprises feed-forward timing recovery means 813 configured for adjusting the interpolation means 807a, 807b with respect to a phase offset compensation criterion. The TEDC signal 810 passes a low pass filter 819 before being provided to a position calculator 817 which uses the filtered TEDC signal to calculate adequate clock positions for the first interpolator 807a and for a second interpolator 807b. The second interpolator 807b interpolates the equalized digital coherent optical signal 806
10 and provides the interpolated equalized digital coherent optical signal to the channel transfer function calculator 805. The first interpolator 807a interpolates the digital coherent optical signal 804 delayed by the delay element 831 and provides the interpolated delayed digital coherent optical signal to the channel transfer function calculator 805. The channel transfer function calculator 805 calculates the channel transfer function based on the
15 interpolated equalized digital coherent optical signal and based on the interpolated delayed digital coherent optical signal. A switch S1 can be used to selectively provide a recovered carrier signal 812, recovered by a carrier recovery unit 821 or the interpolated equalized digital coherent optical signal, to the channel transfer function calculator 805.

20 The feed-forward (FF-) 813 and feed-backward (FB-) 811 timing recovery (TR) in coherent optical systems are presented in Fig. 8. The feed-backward timing recovery (FB-TR) 811 comprises a phase detector (PD) 809, a digital-analog converter (DAC) 833, a low-pass filter (LPF2) 835 and a voltage controlled oscillator (VCO) 815 as a local oscillator (LO). The feed-forward timing recovery (FF-TR) 813 comprises interpolation means 807a, 807b, the phase detector (PD) 809, a position calculation means 817, a low-pass filter (LPF1)
25 819 and a delay element 831. The ADC 801 normally delivers complex signals from both polarizations (x' and y' ; four data lines). In an implementation, the signal denoted as the digital coherent optical signal 804 is twice oversampled, although it is possible to work with less than 2 samples per symbol using polyphase filters. The channel equalizer 803 compensates for CD, PMD, nonlinear effects, etc. Channel transfer function consisting of
30 linear and nonlinear cascaded functions is estimated in the block "Channel transfer function calculation" 805. This block can use a training sequence to estimate the channel transfer function (switch S2 is in the position 4 and switch S1 in the neutral position).

After channel equalization the signal x and y , denoted as the equalized digital coherent optical signal 806 is used in the phase detector (PD) 809 that is shared with FF-TR 813 and FB-TR 811. The phase detector 809 outputs the signal (denoted as TEDC signal 810) that contains information about the clock parameters. The right clock signal has to be:

5

$$s(t) = \sin(2\pi f) \quad (5)$$

However, the Tx VCO and Rx VCO are not synchronized. The current clock signal is equal to

10

$$s(t) = A \sin(2\pi(f + \Delta f)t + \varphi) \quad (6)$$

The parameter A is practically irrelevant for clock extraction (only plays role in the design of timing recovery circuits; mostly influencing the reaction time of the recovery blocks. The clock offset Δf and phase offset φ are the negative effects that have to be compensated.

15

The FB-TR 811 is responsible for clock offset compensation via the feedback loop (small bandwidth loop). Since there is a large delay between the phase detector and ADC blocks 801 the FF-TR 813 is required to follow/compensate the fast sampling phase variations (not related to self-phase jitter).

20

The PD block 809 outputs the signal 810 that is proportional to the residual phase difference between the received data and Rx VCO clocks. This signal 810 is filtered (LPF2, 835) after the DAC block 833 and used for VCO 815 clock and phase adjustment. The FF-TR 813 filters the PD output 810 using IIR low-pass filter (LPF1, 819) in the digital domain. The filtered signal contains information about the correct clock position. This is used in a block for position calculation 817. Based on this position and samples after the channel equalizer 803 the interpolator 807b (Interpolation2; 2 samples in; one sample out) delivers samples at the correct sampling instances. The channel estimator 805 can work in either blind or decision directed mode and the data before the channel equalizer 803 are delayed 831 (shift register) and interpolated 807a (Interpolation1; 2 samples in; 2 samples out) as the data after channel equalization 803. This way, the data at the correct sampling phases are used for channel estimation 805.

30

Data after carrier recovery 821 also can be used for channel estimation 805 (switch S1 in position 2) to improve channel estimator 805 accuracy. The enhanced PD 809 works with complex (can also work with real signal) modulation formats. The received signal 806 is twice over-sampled (two samples per symbol). Samples within one symbol interval n are
 5 denoted by $A(n)$ and $B(n)$. Then, the TEDC signal 810 is calculated by using the equation

$$TEDC(\tau) = E \left(\text{real} \{ [C(n-1) - C(n+1)] \text{conj}[C(n)] \} \right) \quad (7)$$

where C values are derived as

$$\begin{aligned} C(n-1) &= A(n-1) \text{conj} [\alpha + (1-\alpha)B(n-1)] \\ C(n) &= B(n-1) \text{conj} [\alpha + (1-\alpha)A(n)] \\ C(n+1) &= A(n) \text{conj} [\alpha + (1-\alpha)B(n)] \end{aligned} \quad (8)$$

and E stands for expectation (averaging using low-pass filter in practical implementations). The TEDC signal 810 for $\alpha=0$ and $\text{ROF}=0$ has the sinusoidal shape with positive zero crossing indicating steady-state (sampling instant; see Fig. 9). Using
 15 imaginary part in equation (7) results in TEDC having the constant value over one unit interval (UI; symbol interval). Such a TEDC cannot be used directly for clock extraction. The conjugate operation in Eq. 7 can be avoided to improve performance in some specific transmission scenarios. In an implementation, the parameter α is used to improve clock performance for different modulation formats and pulse shapes and to additionally adjust
 20 the sampling phase.

In an implementation of the coherent optical receiver 800, the TEDC signal 810 indicates a phase offset and a frequency offset of the analog coherent optical signal 801 with respect to a local oscillator 815, wherein the local oscillator 815 is controlling the sampling of the analog-to-digital conversion means 801.

25 In an implementation of the coherent optical receiver 800, the interpolation means 807a, 807b comprises first interpolation means 807a configured for interpolating the digital coherent optical signal 804 and second interpolation means 807b configured for interpolating the equalized digital coherent optical signal 806.

In an implementation of the coherent optical receiver 800, the first interpolation means 807a provides two output samples for two input samples; and wherein the second interpolation means 807b provides one output sample for two input samples.

5 In an implementation of the coherent optical receiver 800, the feed-forward timing recovery means 813 comprises position calculation means 817 configured for calculating clock positions based on the TEDC signal 810.

In an implementation of the coherent optical receiver 800, the interpolation means 807a, 807b is configured to provide samples of the digital coherent optical signal 804 and the equalized digital coherent optical signal 806 at the calculated clock positions.

10 In an implementation of the coherent optical receiver 800, the TEDC signal 810 is filtered by an infinite impulse response, IIR, low-pass filter 819 before being provided to the position calculation means 817.

In an implementation, the coherent optical receiver 800 comprises carrier recovery means 821 configured to recover a carrier signal 812 of the analog coherent optical signal 802
15 based on the equalized digital coherent optical signal 806.

In an implementation of the coherent optical receiver 800, the channel transfer function calculation means 805 is configured for calculating the channel transfer function 808 based on the carrier signal 812.

20 In an implementation of the coherent optical receiver 800, the digital coherent optical signal 804 comprises two samples per symbol.

In an implementation of the coherent optical receiver 800, the phase detection means 809 is configured for providing the TEDC signal 810 based on samples of two contiguous symbol intervals.

25 In an implementation, the coherent optical receiver 800 is configured for receiving optical signals using Nyquist pulses, configured for receiving optical signals of any QAM or PSK modulation format and/or configured for receiving optical signals with signal bandwidth smaller than a minimum defined Nyquist bandwidth.

In an implementation of the coherent optical receiver 800, the phase detection means 809 is configured for providing a TEDC signal 810 based on a digital coherent optical signal
30 804 according to equations (7) and (8).

In an implementation of the coherent optical receiver 800, the phase detection means 809 is configured for providing a linear TEDC signal 810, in particular by applying the equations (7) and (8) to the digital coherent optical signal 804 and a shifted version thereof.

5 Fig. 9 shows a diagram illustrating a TED characteristic 900 of a phase detector according to an implementation form. The phase detector can be applied in a coherent optical receiver 800 as described above with respect to Fig. 8. By analyzing the TED characteristics 900 of Fig. 9 one can conclude that the phase detector generates the clock at 0.25UI. The VCO will be locked at this phase; rising zero TEDC crossing. However, the
10 clock should be at 0.5UI which is in the center of the diagram.

Fig. 10 shows eye diagrams of real 1000a and imaginary 1000b signals at the input of the phase detector depicted in Fig. 9. The eye diagrams show real and imaginary parts of QPSK signals. Comparing Fig. 9 and 10 one can conclude that the phase detector generates clock at 0.25UI, the VCO will be locked at this phase; rising zero TEDC
15 crossing, but the clock should be at 0.5UI, i.e. in the center of the eye.

Fig. 11a shows a block diagram of a phase detector 1100 with linear TEDC according to an implementation form. The phase detector 1100 can be applied in a coherent optical receiver 800 as described above with respect to Fig. 8.

The PD block is modified with respect to the phase detector shown in Figures 9 and 10 to
20 provide the correct sampling phase. The input signal 1102 is processed by two PDs 1101, 1103 (eq. 7 and 8). One part of the signal is interpolated at sampling instances shifted by UI/4 1105. This way the signal W_2 is generated that has sin shape and the W_1 signal that has cos shape. Using the block calculating angle function (*atan*) values 1107 (can be look-up table; LUT) from $-\pi$ to $+\pi$ and normalizing these values by 2π the output signal 1110
25 from this block 1107 takes values between -0.5 and +0.5. This value τ is directly used for interpolation. To achieve large tracking range the τ value can be processed by an unwrapping function.

Fig. 11b shows a block diagram of a low pass filter 1150 used in the phase detector 1100 depicted in Fig. 11a according to an implementation form. The LPF1 1150 is realized in
30 digital domain using IIR structure having transfer function:

$$H(z) = \frac{\beta}{1 - (1 - \beta)z^{-1}}; f_{3dB} \approx \beta f_c / 2\pi$$

where f_c is a frequency of the filter input digital signal. The interpolator for the second
 5 phase detector 1103 generating the sin function can be realized as the interpolators
 shown in Fig. 8. For example, a cubic interpolator using four samples may be used to
 interpolate the signal.

Fig. 12 shows a TEDC diagram illustrating the linear TEDC 1200 of the phase detector
 1100 depicted in Fig. 11 for a ROF=0 and $\alpha=0$. The linear TEDC is presented in Fig. 12.

10 This function is periodical with period equal to one UI. In an implementation, such a phase
 detector is applied in a coherent optical receiver 800 as described above with respect to
 Fig. 8.

Fig. 13 shows a block diagram of a phase detector 1300 with linear TEDC according to an
 implementation form. The phase detector 1300 can be applied in a coherent optical
 15 receiver 800 as described above with respect to Fig. 8.

Two adjacent samples 1302, 1304 are added 1301 and fed to the basic phase detectors
 1307, 1309 of the main PD 1300. The basic phase detectors 1307 and 1309 change the
 output signal powers and the signal W_2 has different maxima than the signal W_1 . It results
 in non-atan function. Using appropriate equations this power change can be accurately
 20 calculated. The signal W_2 is multiplied 1303 by a parameter g before entering to the
 lookup-table (LUT) 1305. This parameter is equal to:

$$g = \frac{1}{8} \sqrt{\frac{\pi}{2 + \pi}} \quad (9)$$

Fig. 14 shows a block diagram of a phase detector 1400 with linear TEDC comprising a
 25 circuit for changing the sampling phase according to an implementation form. The phase
 detector 1400 can be applied in a coherent optical receiver 800 as described above with
 respect to Fig. 8.

Sampling phase can be further adjusted using switch 1401 that can exchange W_1 and W_2
 function and their signs:

$$W_1' = a_1 W_m$$

$$W_2' = a_2 W_n$$

5 where a_1 and a_2 can be +1 or -1. W_m and W_n are W_1 or gW_2 and W_m is not equal to W_n .

Fig. 15a shows a diagram 1500a illustrating a parameter W_1 for ROF=0 and $\alpha=0$ for the phase detector with linear TEDC depicted in Fig. 13; Fig. 15b shows a diagram 1500b illustrating a parameter gW_2 for ROF=0 and $\alpha=0$ for the phase detector with linear TEDC depicted in Fig. 13 and Fig. 15c shows a diagram 1500c illustrating TEDC for ROF=0 and $\alpha=0$ for the phase detector with linear TEDC depicted in Fig. 13.

The signals W_1 and gW_2 are almost identical except of a shift by 90 degree that is wanted. It proves that the parameter g was appropriately calculated. The small difference between these two functions did not degrade the linearity of the TEDC function. As can be seen from Fig. 15c, the TEDC signal 1500c is linear and convenient for the use in the interpolators. The range of the *atan* function can be extended using an unwrapping function to cover a large jitter that is not limited to one UI. The phase shift can be defined as:

$$\tau_c(n) = \tau_c(n-1) + \Phi(n) + \Delta\Phi(n)$$

$$\Phi(n) = \tau(n) - \tau(n-1)$$

$$\Delta\Phi(n) = \begin{cases} 0 & , \quad -0.5 \leq \Phi(n) \leq 0.5 \\ -1 & , \quad \Phi(n) > 0.5 \\ +1 & , \quad \Phi(n) < -0.5 \end{cases}$$

The unwrapping function range depends on the available registers length. To avoid large phase fluctuations especially in the acquisition phase (clock frequency offset acquiring) this function can be limited to several symbols.

25 Fig. 16 shows a diagram 1600 illustrating TEDC for 4QAM and $E_b/N_0=3\text{dB}$ for the phase detector with linear TEDC depicted in Fig. 13; Fig. 17 shows a diagram 1700 illustrating TEDC for 16QAM and $E_b/N_0=6\text{dB}$ for the phase detector with linear TEDC depicted in Fig. 13; Fig. 18 shows a diagram 1800 illustrating TEDCs for 64QAM and $E_b/N_0=10\text{dB}$ for

the phase detector with linear TEDC depicted in Fig. 13; Fig. 19 shows a diagram 1900 illustrating TEDCs for 4QAM and $E_b/N_0=3\text{dB}$ for the phase detector with linear TEDC depicted in Fig. 13; Fig. 20 shows a diagram 2000 illustrating TEDCs for 16QAM and $E_b/N_0=6\text{dB}$ for the phase detector with linear TEDC depicted in Fig. 13 and Fig. 21 shows a diagram 2100 illustrating TEDCs for 64QAM and $E_b/N_0=10\text{dB}$ for the phase detector with linear TEDC depicted in Fig. 13.

Three modulation formats, 4, 16 and 64 QAM with ROF from 0 to 1 in step of 0.1 ($\alpha=0$) are simulated and TEDCs are presented. The signal power in all cases was normalized to 1. One can denote that the TEDC curves are almost independent on ROF values and modulation formats. Such a behavior is not achieved by any known PD. The E_b/N_0 values are selected at a bit error rate (BER) of 0.02 (20% soft FEC limit).

For all cases self and noise jitter performance for ROF=0 and $\alpha=0$ was investigated. Each TEDC curve is derived on 1024 symbols. 64 curves are shown in each figure. The amount of jitter can be estimated from the width of positive zero crossing area. In all cases the absolute peak-to-peak jitter did not cross 2% of UI (sampling period; unit interval). Based on publications and experience, such jitter performances are within acceptable limits.

Fig. 22 shows a block diagram of a transmitter circuit 2200 and a receiver circuit 2250 illustrating Nyquist super-channel clocking according to an implementation form.

The current trend in coherent optical communication is to increase spectral efficiency using higher modulation formats, both polarizations and dense channel packaging (OFDM, Nyquist, etc.). Therefore, a group of N transmitters Tx1, Tx2, TxN is integrated to save power, size and price. Instead of N VCOs the super-channel transmitter circuit 2200 shares one VCO 2201 to all transmitters Tx1, Tx2, TxN. It is realized as shown in Fig. 22. One VCO 2201 supplies the clock distribution unit (CDU, 2203) that clocks all N transmitters Tx1, Tx2, TxN.

As expected, the receiver side 2250 gains from channel integration. Instead of N only one PD 2251 is implemented to support clock extraction. One PD connected to data of the first receiver Rx1 (or any receiver Rx1, Rx2, RxN) extracts clock tone information that is later filtered by low-pass filter (LPF, 2253) and sent to VCO 2255. PD gain, LPF parameters and VCO gain control the timing performance (loop bandwidth, dumping, etc.).

Fig. 23 shows a block diagram illustrating a phase detector circuit 2300 comprising parallel implemented phase detectors according to an implementation form.

High symbol rates require parallel implementation of DSP algorithms including the clock extraction algorithm. Data are grouped in blocks of N symbols. When two-fold
5 oversampling is employed the total number of samples per block is $2N$. In Fig. 23, two samples within one symbol interval are denoted by a and b . This figure presents realization for $\alpha=0$. It is straightforward to modify the structure in case α different than 0 (see Eq. 8). The maximum number of PD outputs per data block is equal to N . The last output requires first two samples from next data block and is not included in Fig. 23. In
10 real applications, not all data must be processed by PDs. Usually, some portion of data are unused that might sacrifice clock performance. High modulation formats require higher signal-to-noise ratios, and the reducing number of data to be processed in the clock extraction engine does not significantly influence timing performance. PD outputs denoted by v are summed up in a summing unit 2301 providing a PD output signal 2302 which is
15 filtered by LPF1 as described above with respect to Fig. 8 to be used for interpolation. Also, the summed up (averaged signal) 2302 is DAC converted, e.g. by using the DAC 833 and used in the FB-TR 811 controlling VCO 815 frequency and phase. The VCO output clocks the ADC circuit 801 as described above with respect to Fig. 8. In an implementation, the phase detector circuit 2300 is applied as phase detector 809 in the
20 coherent optical receiver 800 as described above with respect to Fig. 8.

Fig. 24 shows a schematic diagram illustrating a method 2400 for clock recovery in a coherent optical receiver according to an implementation form.

The method 2400 comprises sampling 2401 an analog coherent optical signal into a digital coherent optical signal. The method 2400 comprises equalizing 2403 the digital
25 coherent optical signal. The method 2400 comprises calculating 2405 a channel transfer function based on interpolations of the digital coherent optical signal and the equalized digital coherent optical signal and adjusting the channel equalization means based on the calculated channel transfer function. The method 2400 comprises providing 2407 a timing error detection characteristic, TEDC, signal, based on the equalized digital coherent
30 optical signal. The method 2400 comprises adjusting 2409 the sampling of the analog-to-digital converter based on the TEDC signal with respect to a frequency offset compensation criterion. The method 2400 comprises adjusting 2411 the interpolations of

the digital coherent optical signal and the equalized digital coherent optical signal with respect to a phase offset compensation criterion.

From the foregoing, it will be apparent to those skilled in the art that a variety of methods, systems, computer programs on recording media, and the like, are provided.

- 5 The present disclosure also supports a computer program product including computer executable code or computer executable instructions that, when executed, causes at least one computer to execute the performing and computing steps described herein.

Many alternatives, modifications, and variations will be apparent to those skilled in the art in light of the above teachings. Of course, those skilled in the art readily recognize that
10 there are numerous applications of the invention beyond those described herein. While the present inventions has been described with reference to one or more particular embodiments, those skilled in the art recognize that many changes may be made thereto without departing from the scope of the present invention. It is therefore to be understood that within the scope of the appended claims and their equivalents, the inventions may be
15 practiced otherwise than as specifically described herein.

CLAIMS:

1. Coherent optical receiver (800), comprising:

analog-to-digital conversion means (801) configured for sampling an analog coherent optical signal (802) into a digital coherent optical signal (804);

5 channel equalization means (803) configured for equalizing the digital coherent optical signal (804);

channel transfer function calculation means (805) configured for calculating a channel transfer function (808) based on the digital coherent optical signal (804) and the equalized digital coherent optical signal (806) interpolated by interpolation means (807a, 807b) and configured for adjusting the channel equalization means (803) based on the
10 calculated channel transfer function (808);

phase detection means (809) configured for providing a timing error detection characteristic, TEDC, signal (810), based on the equalized digital coherent optical signal (806);

15 feed-backward timing recovery means (811) configured for adjusting the sampling of the analog-to-digital conversion means (801) based on the TEDC signal (810) with respect to a frequency offset compensation criterion; and

feed-forward timing recovery means (813) configured for adjusting the interpolation means (807a, 807b) with respect to a phase offset compensation criterion.

20 2. The coherent optical receiver (800) of claim 1, wherein the TEDC signal (810) indicates a phase offset and a frequency offset of the analog coherent optical signal (801) with respect to a local oscillator (815), the local oscillator (815) controlling the sampling of the analog-to-digital conversion means (801).

3. The coherent optical receiver (800) of claim 1 or claim 2, wherein the interpolation
25 means (807a, 807b) comprises first interpolation means (807a) configured for interpolating the digital coherent optical signal (804) and second interpolation means (807b) configured for interpolating the equalized digital coherent optical signal (806).

4. The coherent optical receiver (800) of claim 3, wherein the first interpolation means (807a) provides two output samples for two input samples; and wherein the second interpolation means (807b) provides one output sample for two input samples.
5. The coherent optical receiver (800) of one of the preceding claims, wherein the
5 feed-forward timing recovery means (813) comprises position calculation means (817) configured for calculating clock positions based on the TEDC signal (810).
6. The coherent optical receiver (800) of claim 5, wherein the interpolation means (807a, 807b) is configured to provide samples of the digital coherent optical signal (804) and the equalized digital coherent optical signal (806) at the calculated clock positions.
- 10 7. The coherent optical receiver (800) of claim 5, wherein the TEDC signal (810) is filtered by an infinite impulse response, IIR, low-pass filter (819) before being provided to the position calculation means (817).
8. The coherent optical receiver (800) of one of the preceding claims, comprising
15 carrier recovery means (821) configured to recover a carrier signal (812) of the analog coherent optical signal (802) based on the equalized digital coherent optical signal (806).
9. The coherent optical receiver (800) of claim 8, wherein the channel transfer function calculation means (805) is configured for calculating the channel transfer function (808) based on the carrier signal (812).
10. The coherent optical receiver (800) of one of the preceding claims, wherein the
20 digital coherent optical signal (804) comprises two samples per symbol.
11. The coherent optical receiver (800) of claim 10, wherein the phase detection means (809) is configured for providing the TEDC signal (810) based on samples of two contiguous symbol intervals.
12. The coherent optical receiver (800) of one of the preceding claims, configured for
25 receiving optical signals using Nyquist pulses, configured for receiving optical signals of any QAM or PSK modulation format and/or configured for receiving optical signals with signal bandwidth smaller than a minimum defined Nyquist bandwidth.
13. Phase detector (809, 1100, 1300, 1400) for a coherent optical receiver (800), wherein the phase detector is configured for providing a TEDC signal (810) based on a
30 digital coherent optical signal (804) according to the following relations:

$$\text{TEDC}(\tau) = E(\text{real}\{[C(n-1)-C(n+1)]\text{conj}[C(n)]\}),$$

$$C(n-1) = A(n-1)\text{conj}[\alpha+(1-\alpha)B(n-1)],$$

$$C(n) = B(n-1)\text{conj}[\alpha+(1-\alpha)A(n)],$$

$$C(n+1) = A(n)\text{conj}[\alpha+(1-\alpha)B(n)],$$

5 where $A(n)$ and $B(n)$ describe samples of the digital coherent optical signal (804) within one symbol interval n , $E()$ denotes expectation value and $\text{conj}[]$ denotes conjugate complex operation.

14. The phase detector (809, 1100, 1300, 1400) of claim 13, configured for providing a linear TEDC signal (810), in particular by applying the relations of claim 13 to the digital
10 coherent optical signal (804) and a shifted version thereof.

15. Method (2400) for clock recovery in a coherent optical receiver, the method (2400) comprising:

sampling (2401) an analog coherent optical signal into a digital coherent optical signal;

15 equalizing (2403) the digital coherent optical signal;

calculating (2405) a channel transfer function based on interpolations of the digital coherent optical signal and the equalized digital coherent optical signal and adjusting the channel equalization means based on the calculated channel transfer function;

providing (2407) a timing error detection characteristic, TEDC, signal, based on the
20 equalized digital coherent optical signal;

adjusting (2409) the sampling of the analog-to-digital converter based on the TEDC signal with respect to a frequency offset compensation criterion; and

adjusting (2411) the interpolations of the digital coherent optical signal and the equalized digital coherent optical signal with respect to a phase offset compensation
25 criterion.

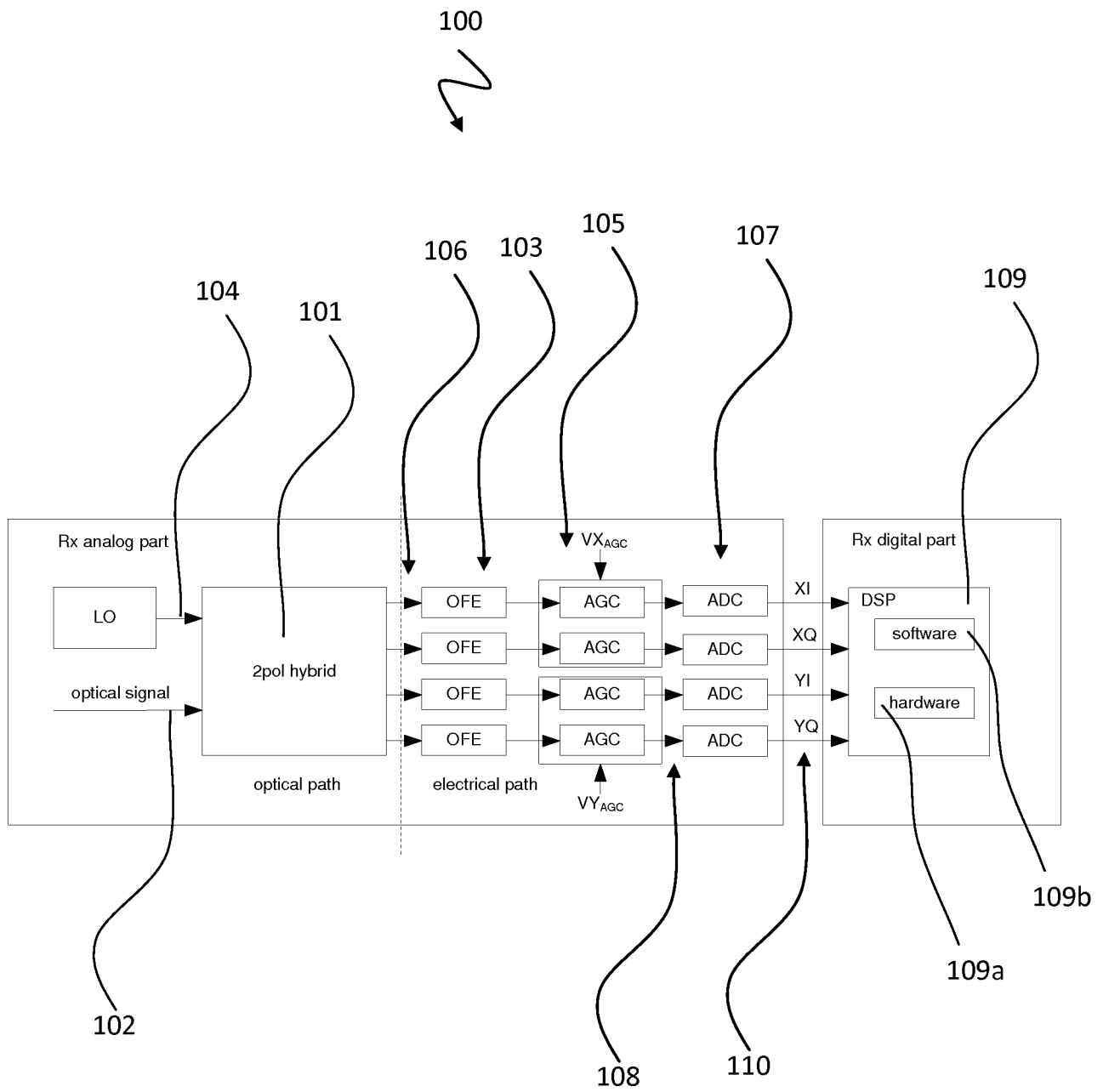


Fig. 1

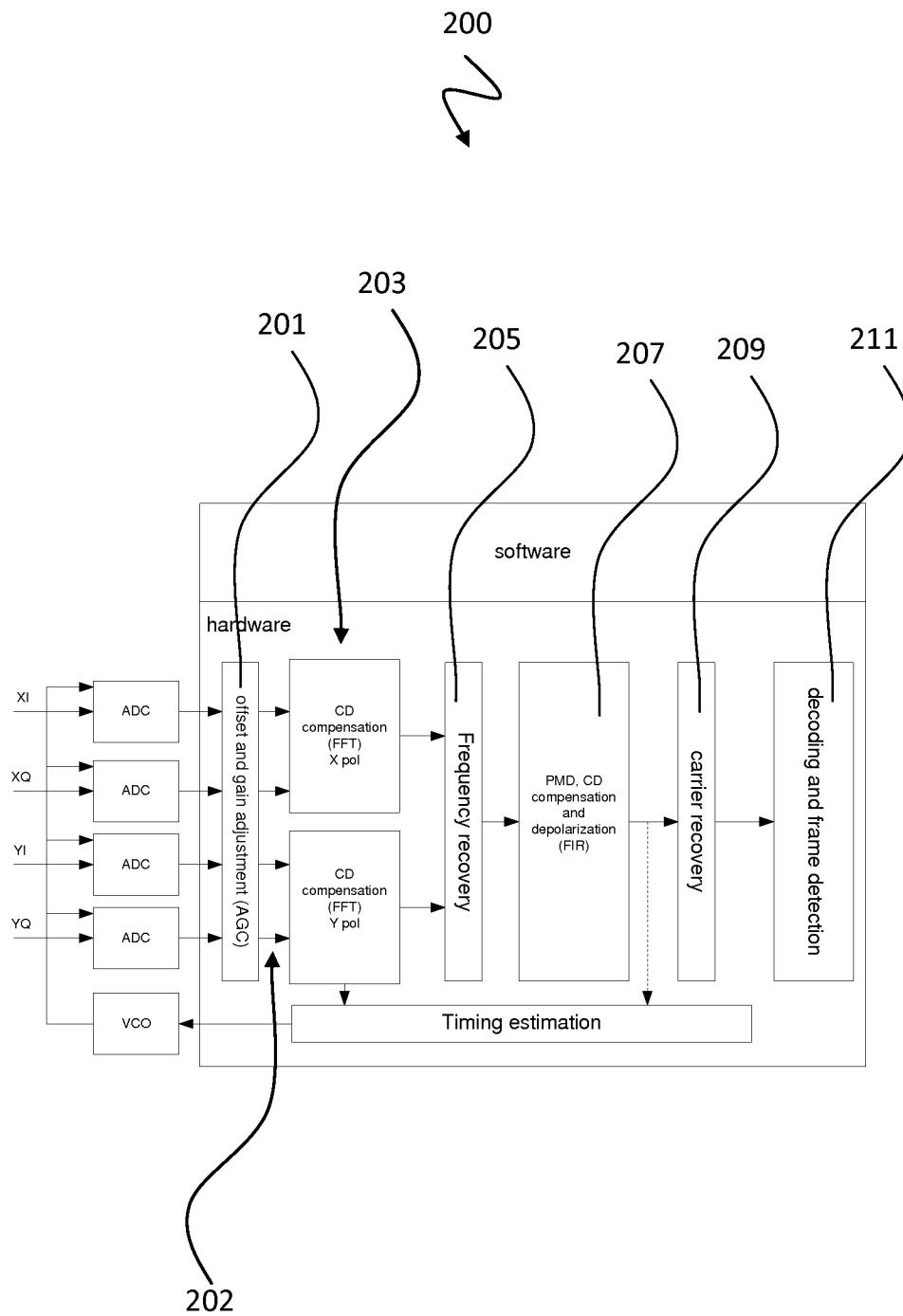


Fig. 2

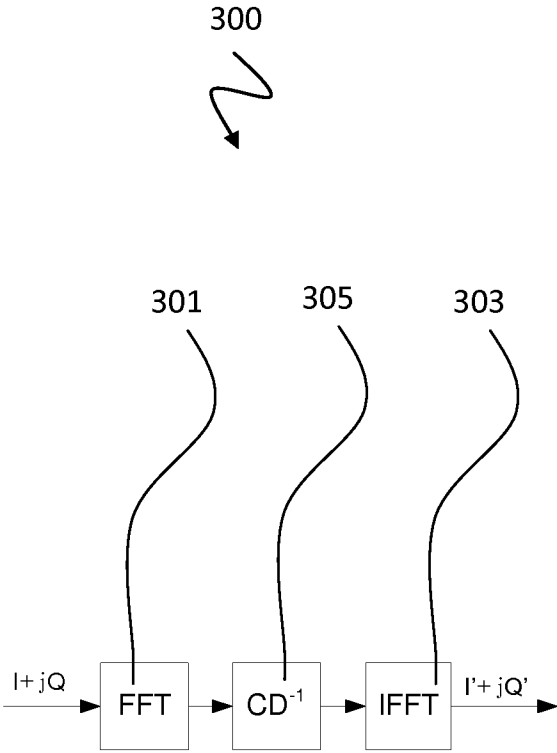


Fig. 3

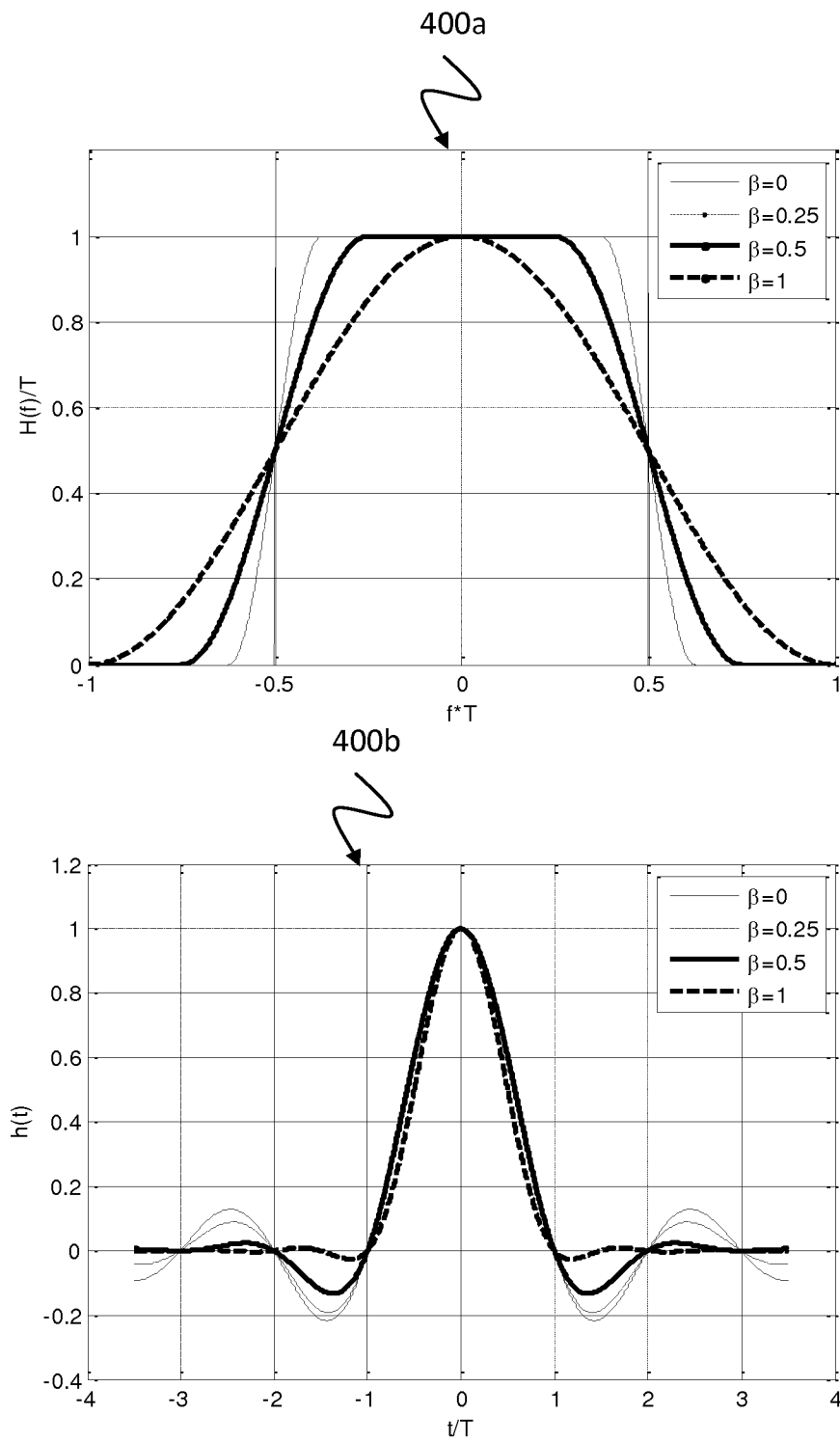


Fig. 4

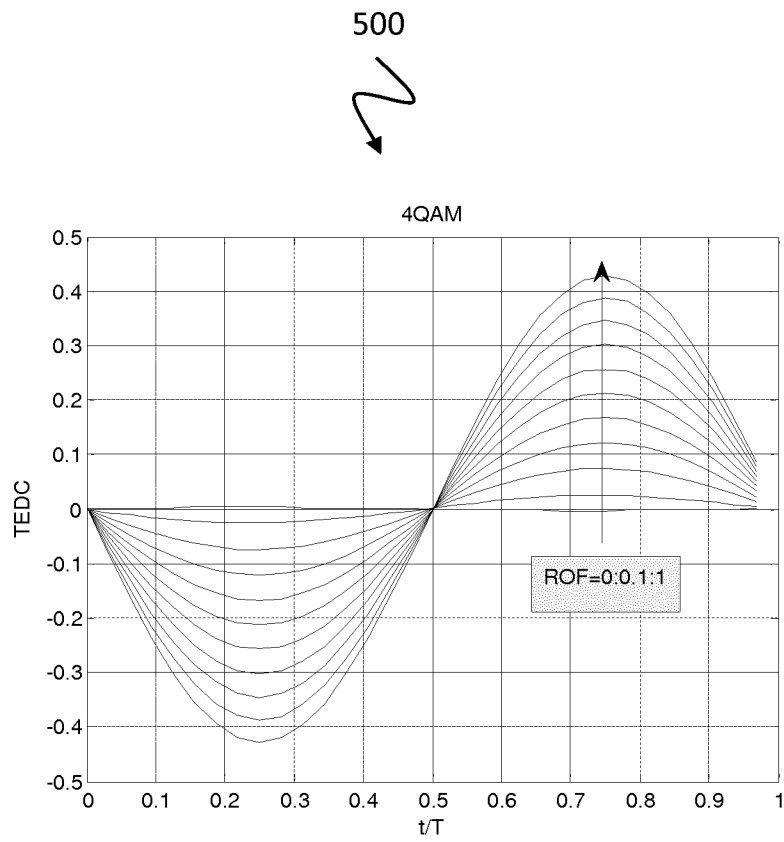


Fig. 5

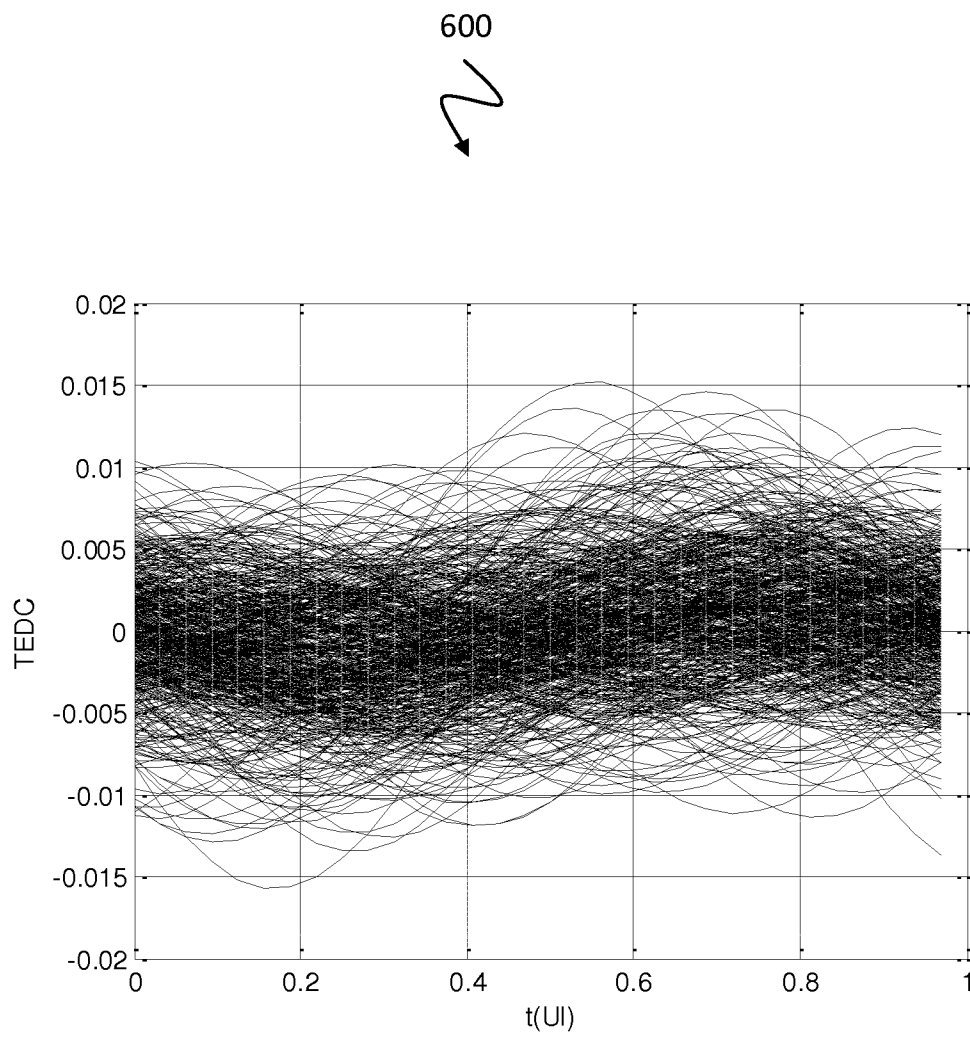


Fig. 6

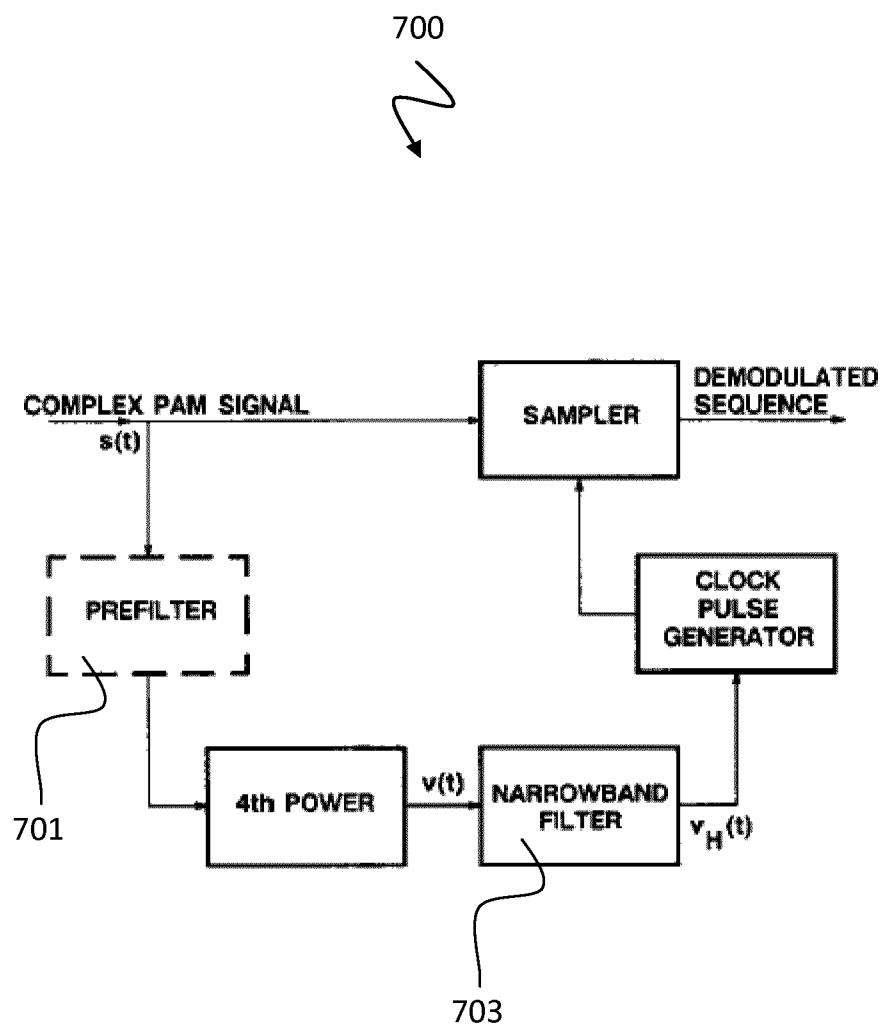


Fig. 7

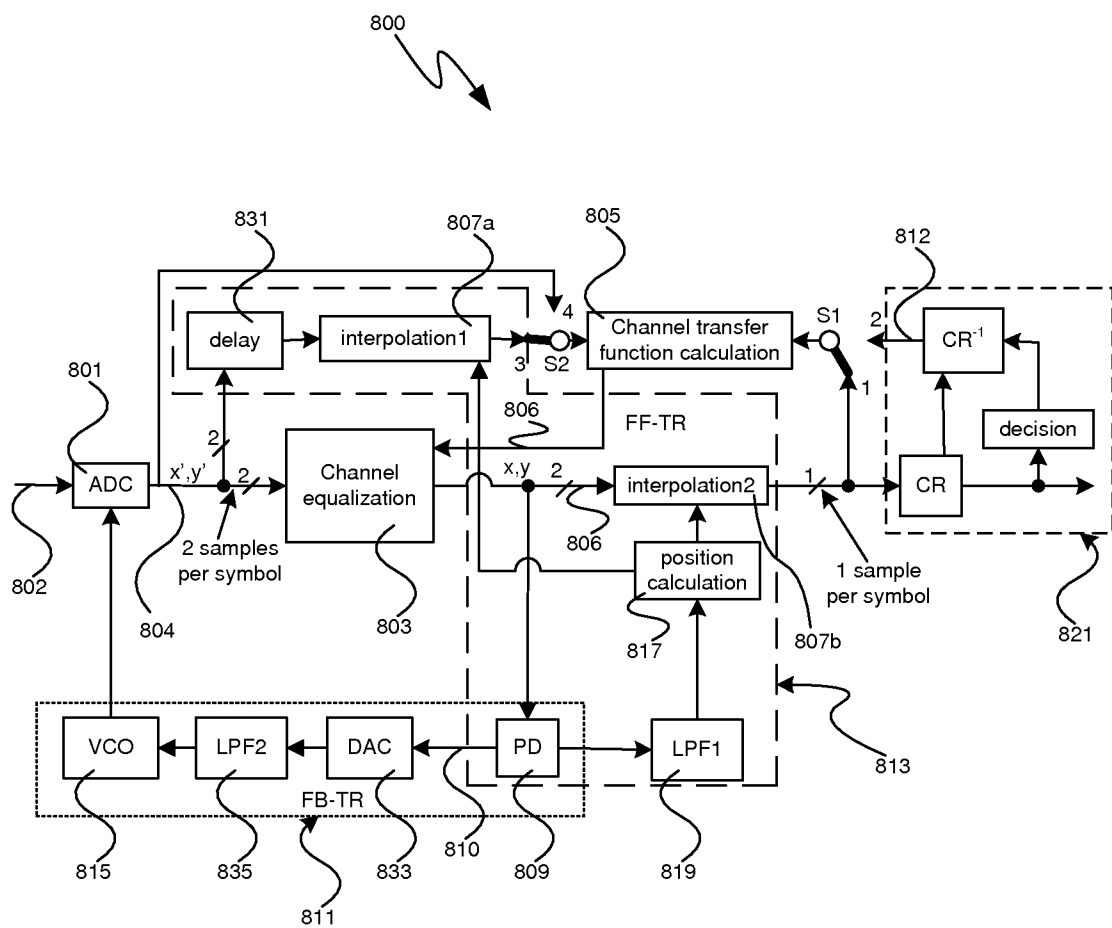


Fig. 8

900

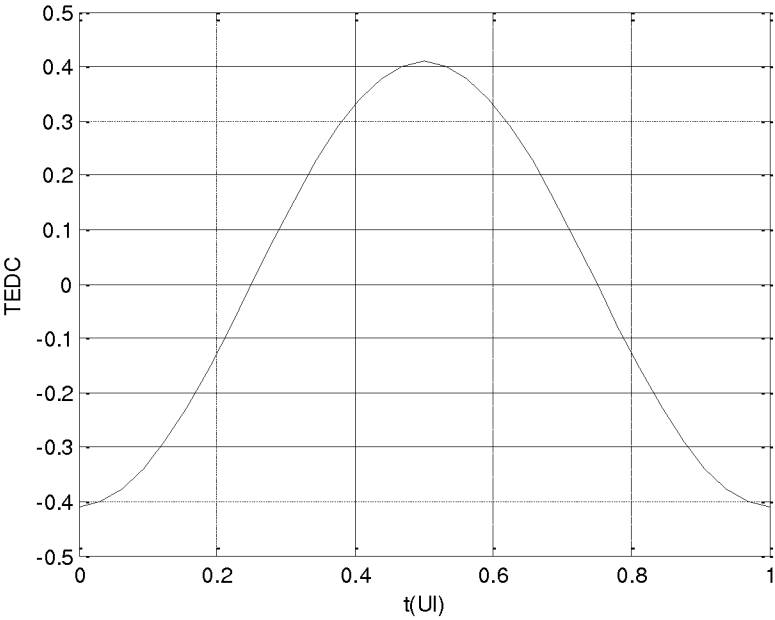


Fig. 9

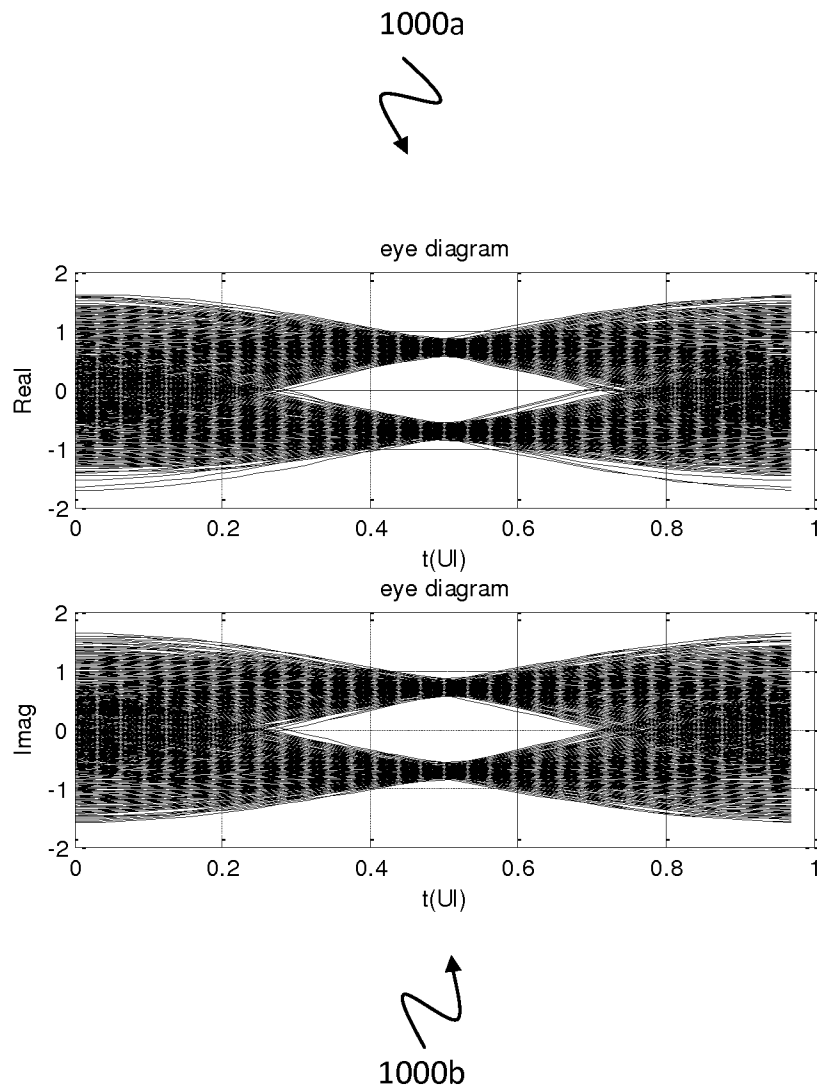


Fig. 10

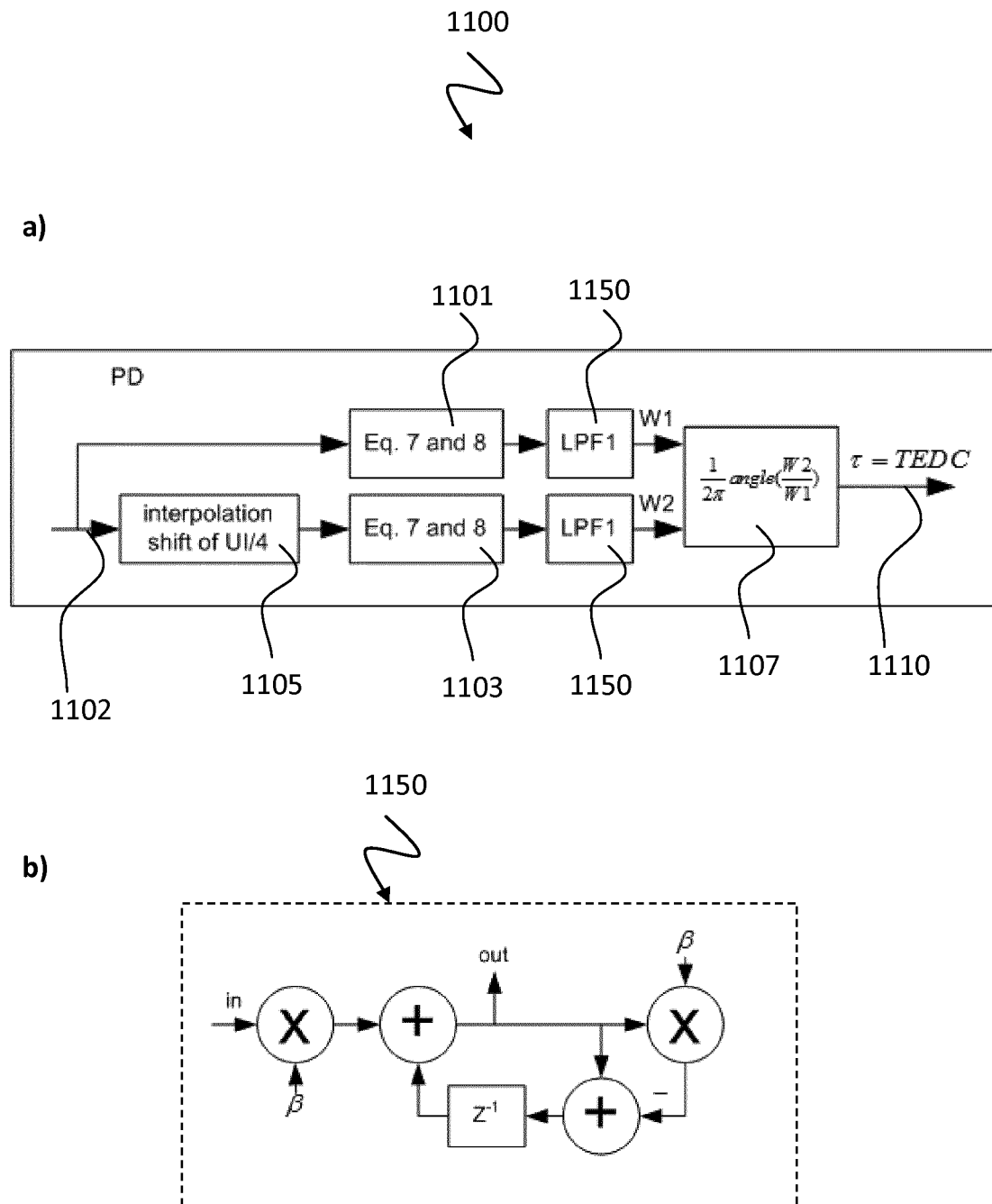


Fig. 11

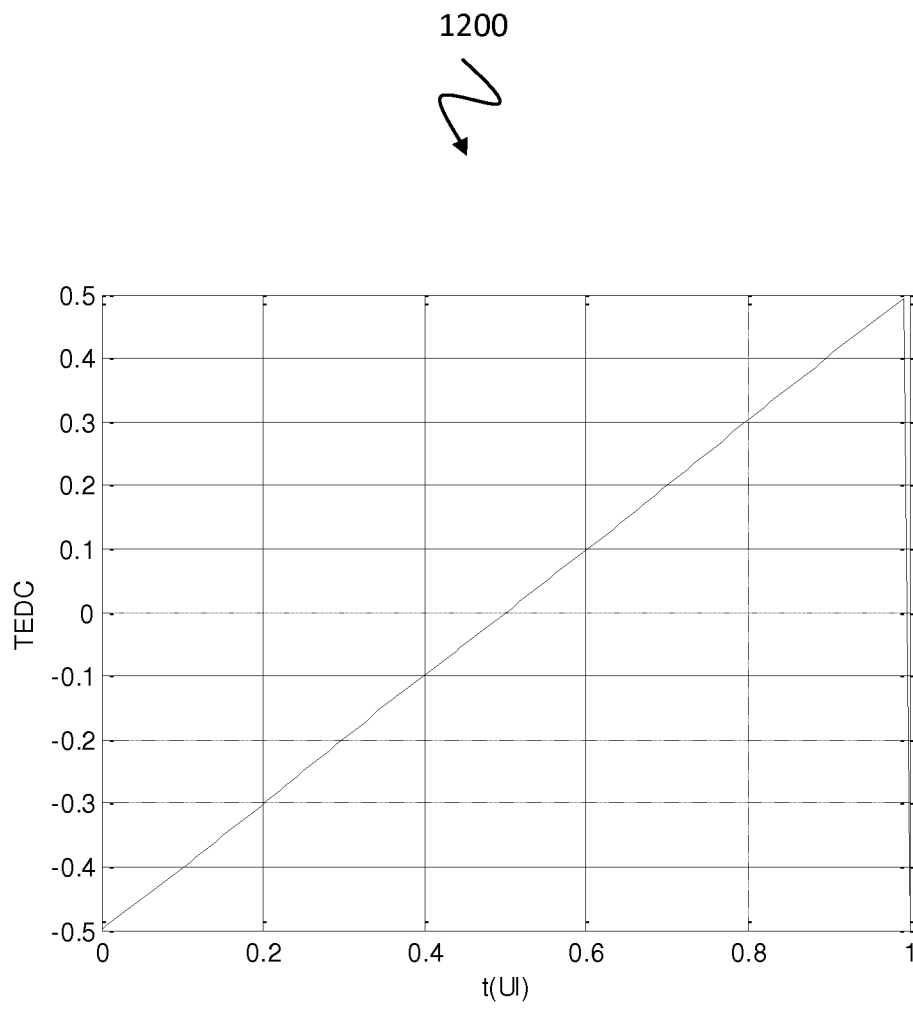


Fig. 12

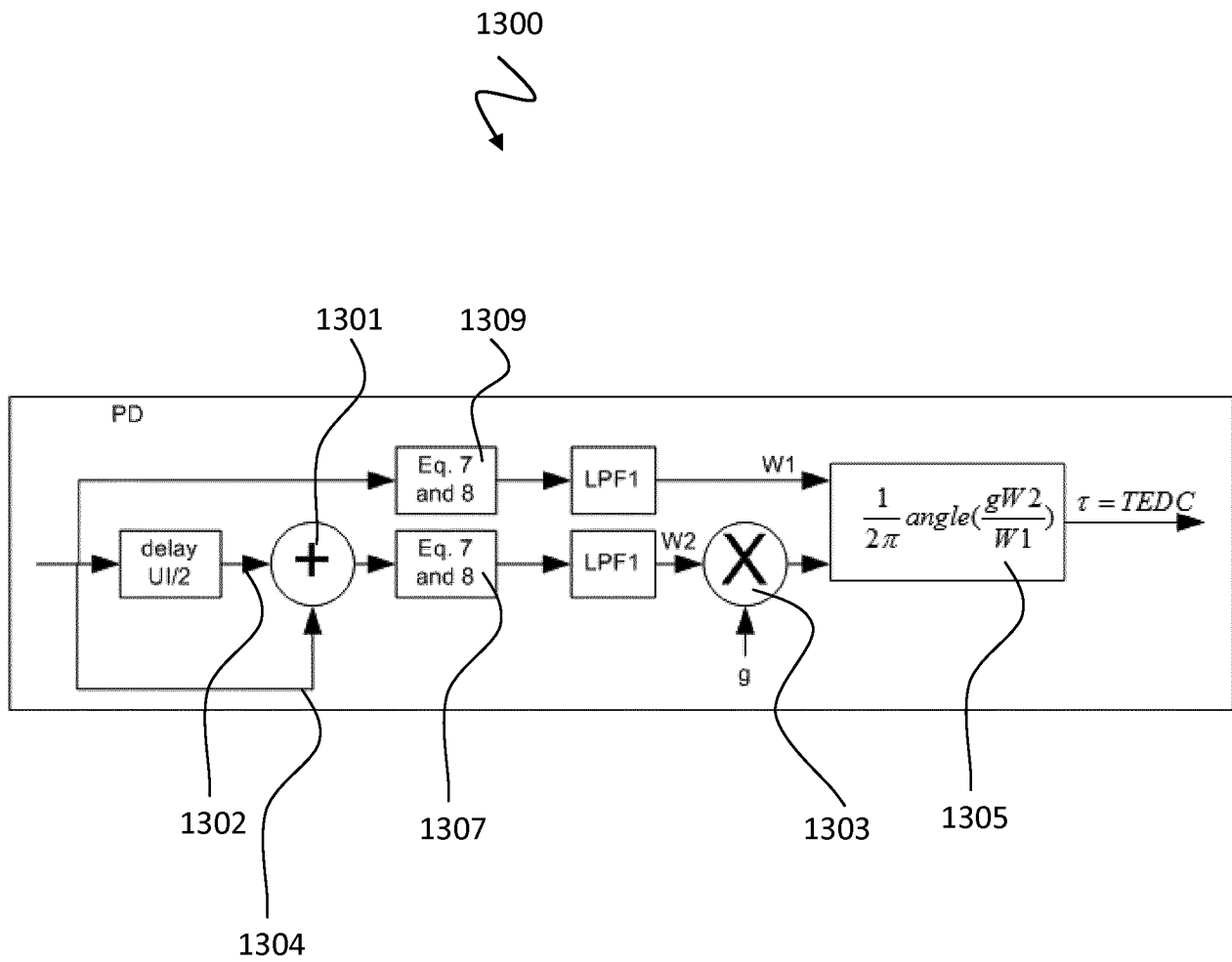


Fig. 13

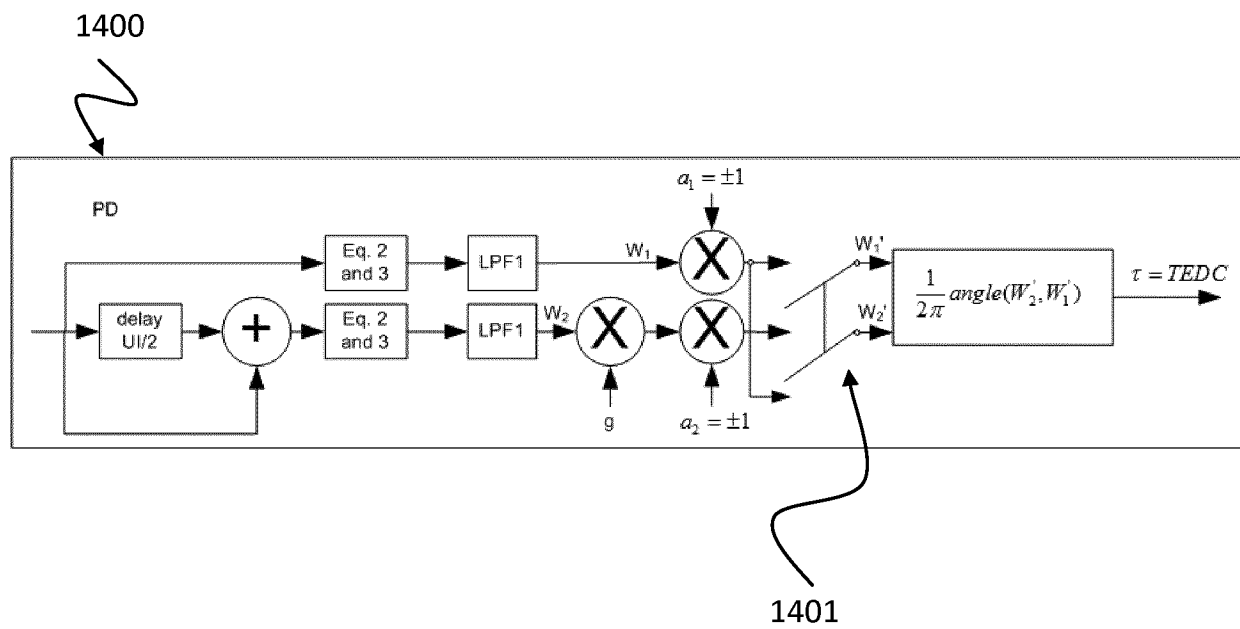


Fig. 14

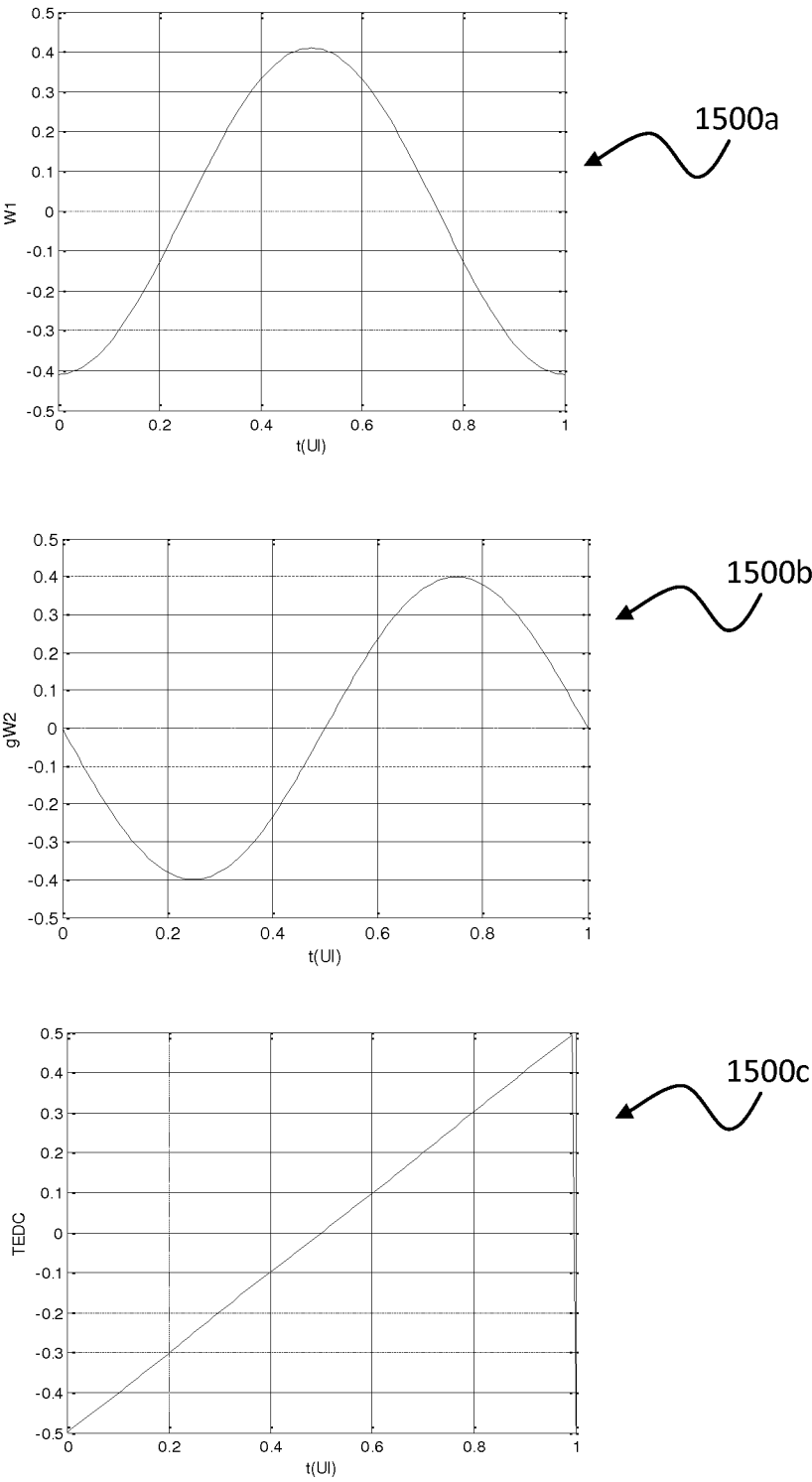


Fig. 15

1600

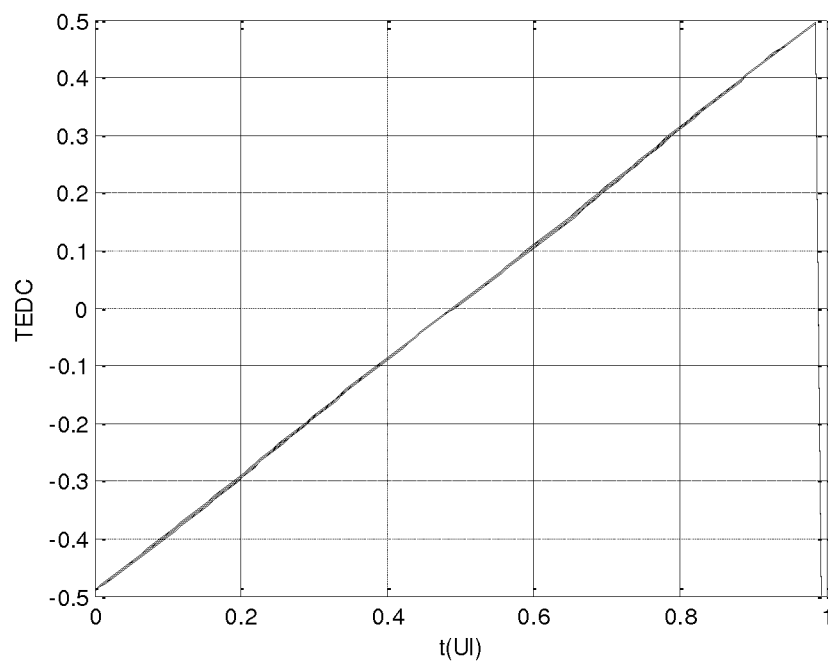


Fig. 16

1700

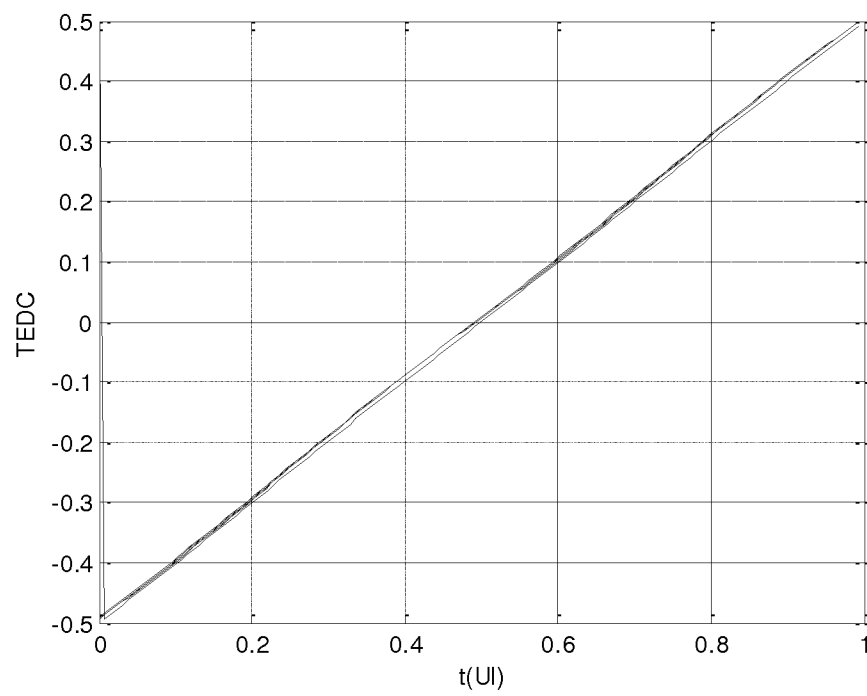


Fig. 17

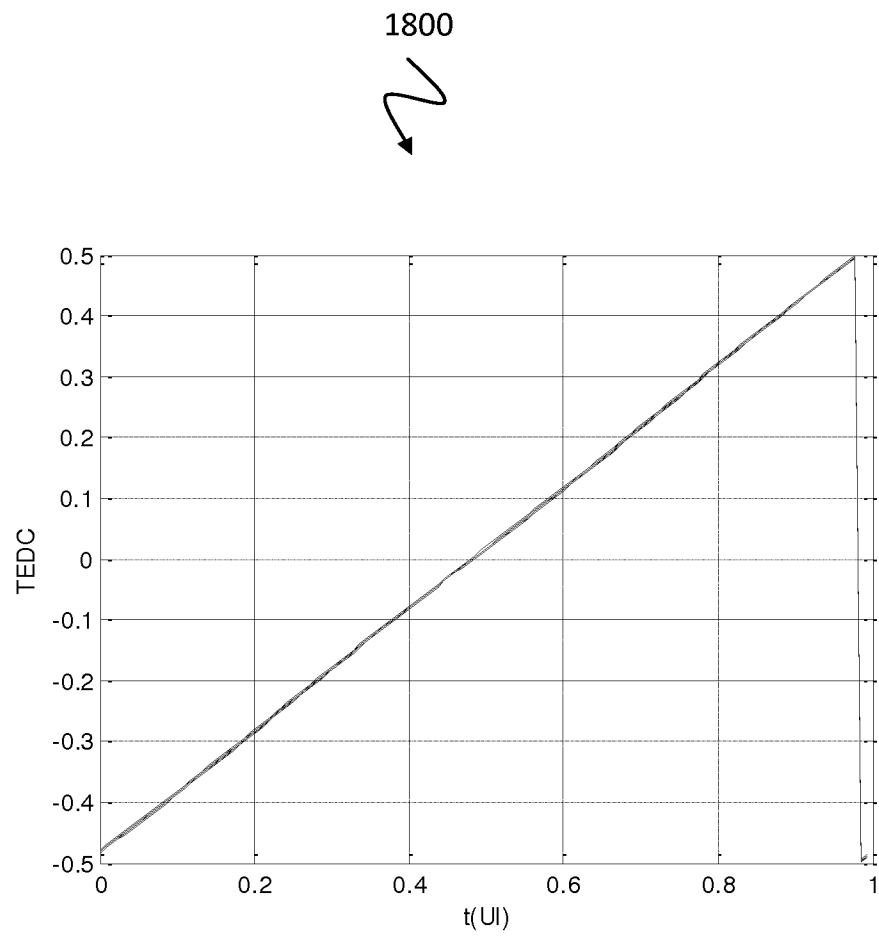


Fig. 18

1900

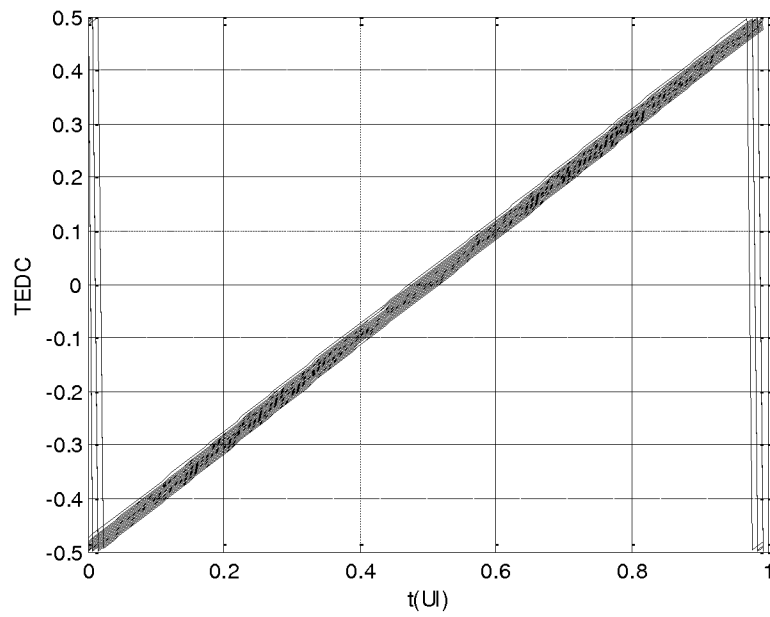


Fig. 19

2000

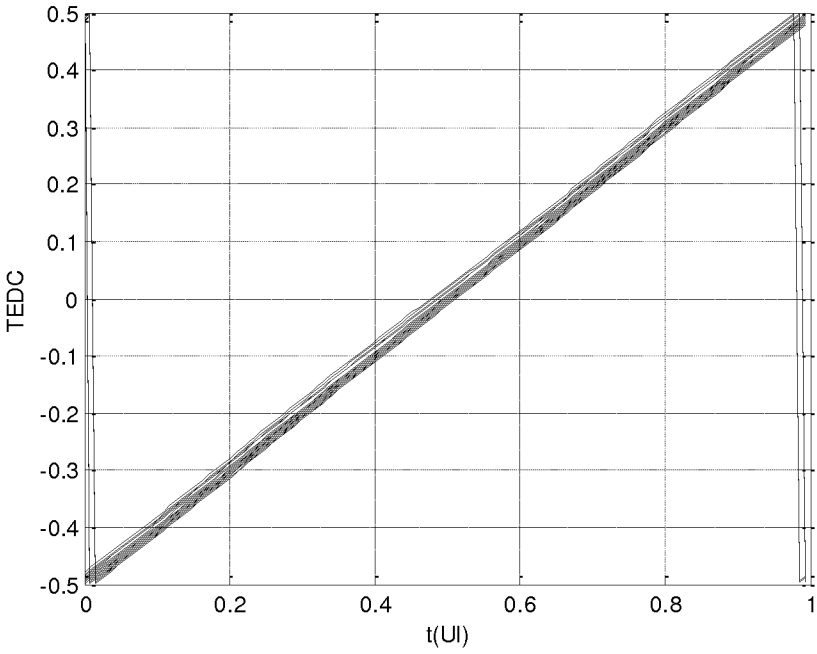


Fig. 20

2100

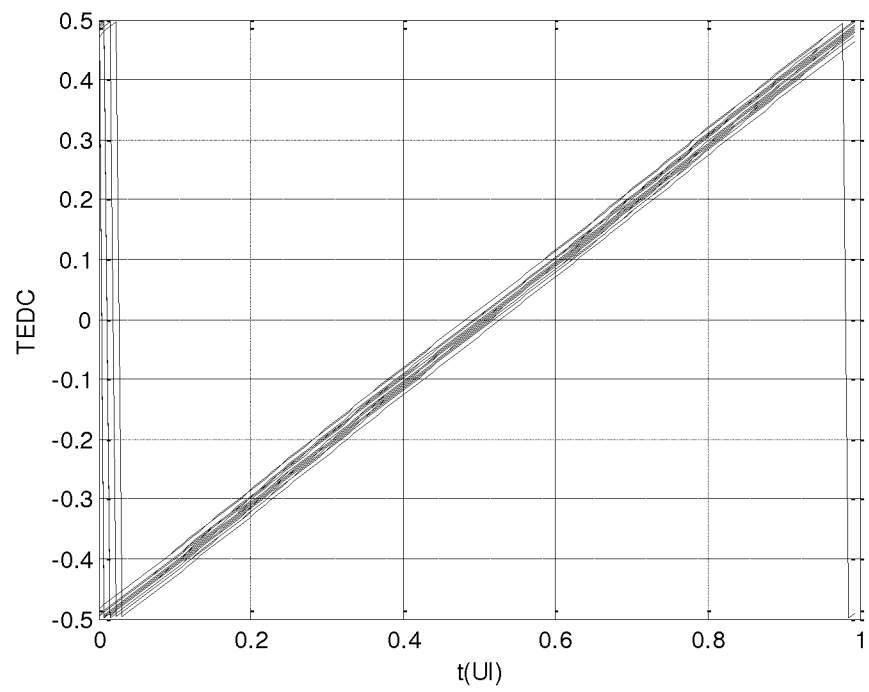


Fig. 21

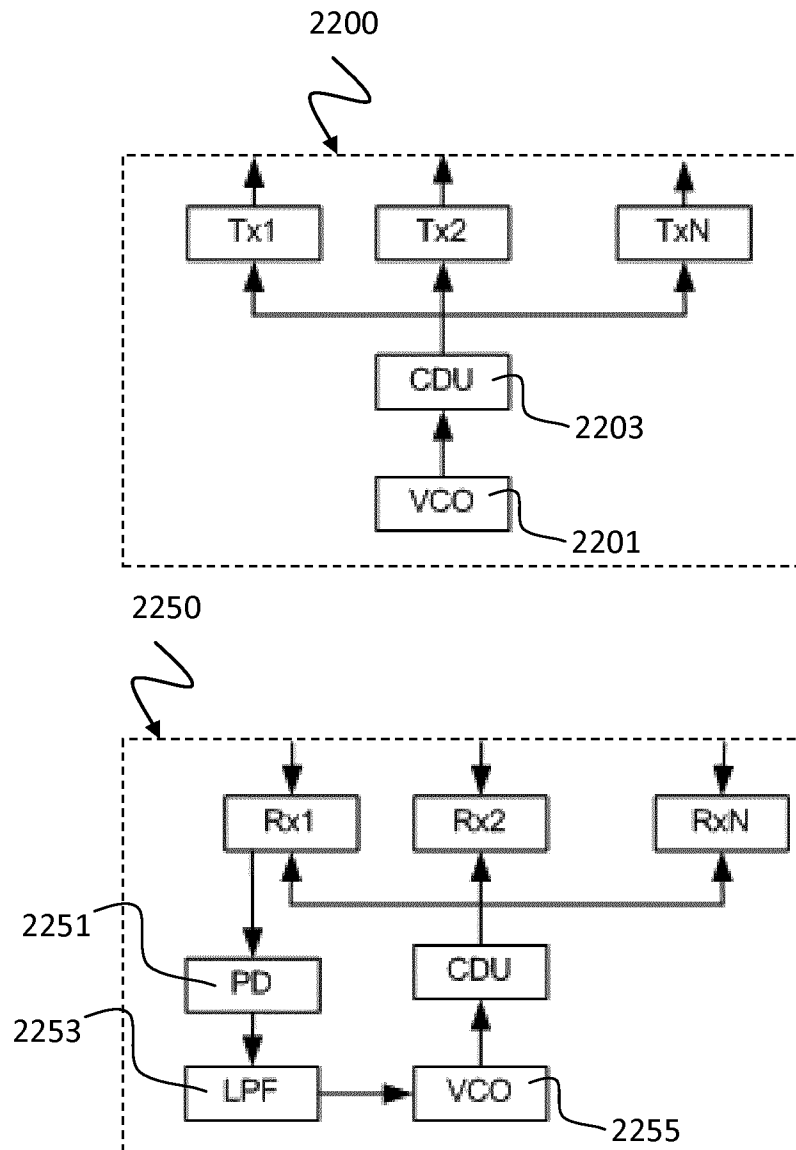


Fig. 22

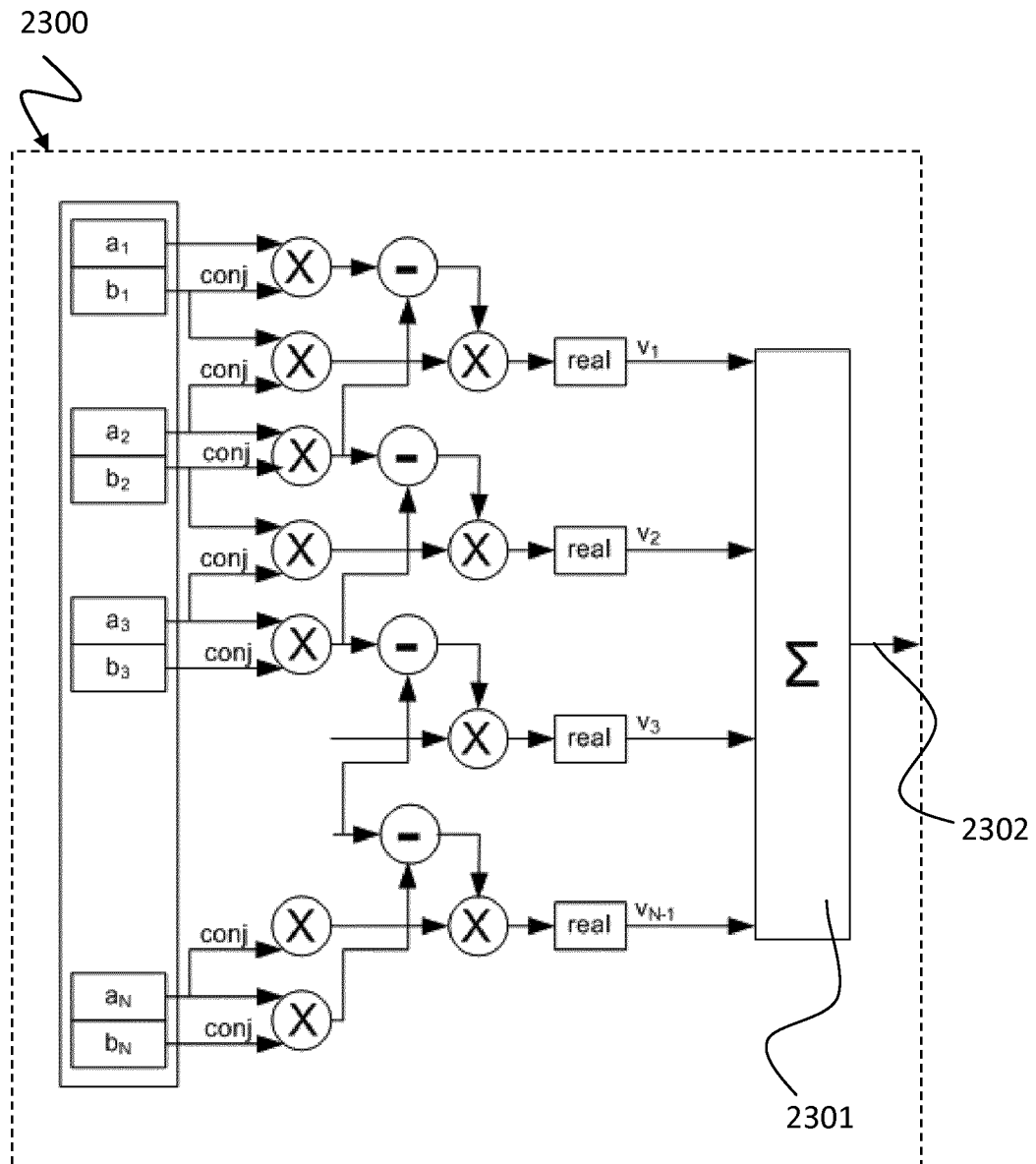


Fig. 23

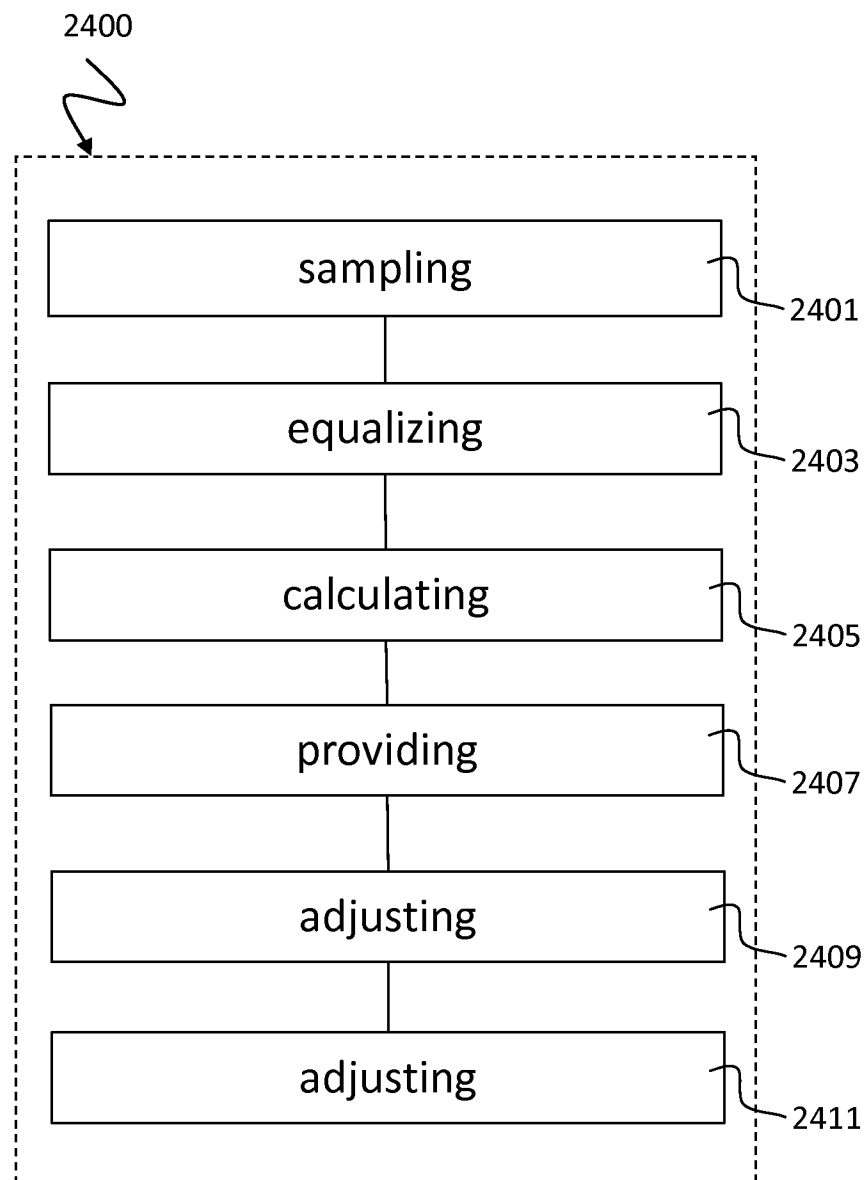


Fig. 24

INTERNATIONAL SEARCH REPORT

International application No

PCT/EP2013/061533

A. CLASSIFICATION OF SUBJECT MATTER

INV. H04L7/00 H04B10/61
ADD.

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

H04B H04L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

EPO-Internal, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	GB 2 472 082 A (COREOPTICS INC [US]) 26 January 2011 (2011-01-26) abstract page 1, line 1 - line 10 page 2, line 9 page 2, line 21 - line 23 page 3, line 2 - line 31 page 4, line 27 - page 5, line 8 page 6, line 1 - line 7 page 9, line 7 - line 34 page 10, line 19 - line 34 page 11, line 8 - line 9 page 9, line 27 - line 28 page 13, line 2 - line 25 page 15, line 14 - line 19 page 16, line 25 - line 27 figures 10,12 ----- -/-	1-12,15



Further documents are listed in the continuation of Box C.



See patent family annex.

* Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search

28 February 2014

Date of mailing of the international search report

05/06/2014

Name and mailing address of the ISA/

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Authorized officer

Marongiu, M

INTERNATIONAL SEARCH REPORT

International application No

PCT/EP2013/061533

C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2012/213510 A1 (STOJANOVIC NEBOJSA [DE]) 23 August 2012 (2012-08-23) paragraph [0002] paragraph [0010] - paragraph [0019] paragraph [0089] - paragraph [0093] paragraph [0098] - paragraph [0101] paragraph [0114] - paragraph [0116] figures 5,9 -----	1-12,15
A	THIAGO F PORTELA ET AL: "Novel Non-Data-Aided Clock Recovery Method for DP-QPSK Systems With CMA Equalizers", IEEE PHOTONICS TECHNOLOGY LETTERS, IEEE SERVICE CENTER, PISCATAWAY, NJ, US, vol. 24, no. 19, 1 October 2012 (2012-10-01), pages 1696-1699, XP011460853, ISSN: 1041-1135, DOI: 10.1109/LPT.2012.2212880 page 1696, column 1 - page 1698, column 1 abstract -----	1-12,15
A	MAXIM KUSCHNEROV ET AL: "DSP for Coherent Single-Carrier Receivers", JOURNAL OF LIGHTWAVE TECHNOLOGY, IEEE SERVICE CENTER, NEW YORK, NY, US, vol. PP, no. 16, 15 August 2009 (2009-08-15), pages 3614-3622, XP011262207, ISSN: 0733-8724 abstract page 3615, column 2 figures 2,3 -----	1-12,15
A	US 2010/164764 A1 (NAYAK RATNAKAR ARAVIND [US]) 1 July 2010 (2010-07-01) paragraph [0002] - paragraph [0003] paragraph [0007] - paragraph [0008] paragraph [0021] paragraph [0023] - paragraph [0025] paragraph [0031] - paragraph [0034] figures 2,4 -----	1-12,15

INTERNATIONAL SEARCH REPORT

International application No.
PCT/EP2013/061533

Box No. II Observations where certain claims were found unsearchable (Continuation of item 2 of first sheet)

This international search report has not been established in respect of certain claims under Article 17(2)(a) for the following reasons:

1. ☐ Claims Nos.:
because they relate to subject matter not required to be searched by this Authority, namely:
2. ☐ Claims Nos.:
because they relate to parts of the international application that do not comply with the prescribed requirements to such an extent that no meaningful international search can be carried out, specifically:
3. ☐ Claims Nos.:
because they are dependent claims and are not drafted in accordance with the second and third sentences of Rule 6.4(a).

Box No. III Observations where unity of invention is lacking (Continuation of item 3 of first sheet)

This International Searching Authority found multiple inventions in this international application, as follows:

see additional sheet

1. ☐ As all required additional search fees were timely paid by the applicant, this international search report covers all searchable claims.
2. ☐ As all searchable claims could be searched without effort justifying an additional fees, this Authority did not invite payment of additional fees.
3. ☐ As only some of the required additional search fees were timely paid by the applicant, this international search report covers only those claims for which fees were paid, specifically claims Nos.:
4. ☒ No required additional search fees were timely paid by the applicant. Consequently, this international search report is restricted to the invention first mentioned in the claims; it is covered by claims Nos.:

1-12, 15

Remark on Protest

- ☐ The additional search fees were accompanied by the applicant's protest and, where applicable, the payment of a protest fee.
- ☐ The additional search fees were accompanied by the applicant's protest but the applicable protest fee was not paid within the time limit specified in the invitation.
- ☐ No protest accompanied the payment of additional search fees.

FURTHER INFORMATION CONTINUED FROM PCT/ISA/ 210

This International Searching Authority found multiple (groups of) inventions in this international application, as follows:

1. claims: 1-12, 15

Coherent optical receiver with both feed-backward and feed-forward timing recovery means and corresponding method.

2. claims: 13, 14

Phase detector for providing a timing error detection characteristic according to the formula $TEDC(t) = E(\text{real}\{[C(n-1) - C(n+1)\text{conj}[C(n)]]\})$

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No

PCT/EP2013/061533

Patent document cited in search report		Publication date		Patent family member(s)		Publication date
GB 2472082	A	26-01-2011	CN	102577183 A		11-07-2012
			GB	2472082 A		26-01-2011
			US	2012121274 A1		17-05-2012
			WO	2011010259 A2		27-01-2011

US 2012213510	A1	23-08-2012	CA	2767975 A1		17-08-2012
			CN	102511135 A		20-06-2012
			EP	2502364 A1		26-09-2012
			US	2012213510 A1		23-08-2012
			WO	2012109793 A1		23-08-2012

US 2010164764	A1	01-07-2010	CN	101743690 A		16-06-2010
			EP	2191569 A1		02-06-2010
			JP	5173021 B2		27-03-2013
			JP	2011523277 A		04-08-2011
			KR	20110021701 A		04-03-2011
			TW	200949703 A		01-12-2009
			US	2010164764 A1		01-07-2010
			WO	2009142620 A1		26-11-2009
