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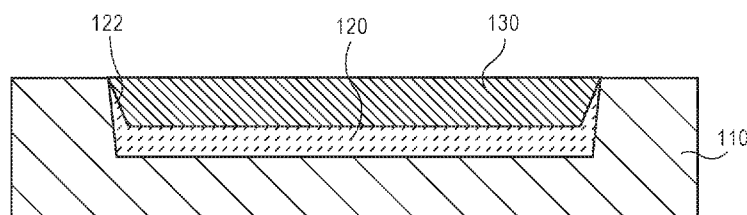


FIG. 1E

(57) Abstract: Embodiments of the invention include thin-film transistors and methods of making such devices with damascene processes. In an embodiment the thin-film transistor (TFT) device includes an interlayer dielectric (ILD) layer, where a trench is formed into the ILD layer. In an embodiment a TFT semiconductor layer formed in the trench, wherein extensions of the TFT semiconductor layer extend up sidewalls of the trench. In an embodiment, a capping layer formed over a top surface of the TFT semiconductor layer. Additional embodiments may include a source electrode and a drain electrode, where the source electrode and the drain electrode contact a surface of the TFT semiconductor layer, and a gate electrode separated from a surface of the TFT semiconductor layer by a gate dielectric layer.



## **DAMASCENE PATTERNING FOR THIN-FILM TRANSISTOR FABRICATION**

### **FIELD OF THE INVENTION**

Embodiments of the invention are in the field of semiconductor processing and, in particular, thin-film transistors and methods of forming such devices with damascene patterning processes.

### **BACKGROUND OF THE INVENTION**

Typically, thin-film transistors are fabricated by blanket depositing a layer of the thin-film transistor material. Thereafter, a photoresist layer is deposited over the thin-film transistor material layer and patterned. The pattern in the photoresist layer is then transferred to the thin-film transistor material layer using wet and/or dry etching processes in order to define the thin-film transistor.

As such, thin-film transistors require precise fabrication conditions in order to produce efficient and high performance devices. One particular fabrication condition that needs to be closely monitored is the temperature of the processing operations that are used to fabricate the thin-film transistor. For example, at elevated temperatures the elements of the thin-film transistor diffuse and disassociate with other materials. This alters the chemical composition of the thin-film transistor, and alters the performance of the thin-film transistor. Additionally, the thin-film transistor may be oxidized during etching and cleaning processes. Accordingly, the etchants used to pattern the semiconductor material for the thin film transistor are limited. Furthermore, etching processes used to pattern the interlayer dielectrics surrounding the thin-film transistor may inadvertently attack the film and result in undercutting. Accordingly, restrictions on dry and/or wet etches used to form the thin-film transistor and restrictions on the materials used for the surrounding dielectric materials limit the performance of the thin-film transistor.

### **BRIEF DESCRIPTION OF THE DRAWINGS**

Figure 1A is a cross-sectional illustration of an interlayer dielectric (ILD) in which a thin-film transistor (TFT) may be formed, according to an embodiment of the invention.

Figure 1B is a cross-sectional illustration of the device after the ILD that has been patterned to form a trench in which the TFT semiconductor layer may be deposited, according to an embodiment of the invention.

Figure 1C is a cross-sectional illustration of the device after the TFT semiconductor layer has been blanket deposited, according to an embodiment of the invention.

Figure 1D is a cross-sectional illustration of the device after a capping layer is deposited

over the TFT semiconductor layer, according to an embodiment of the invention.

Figure 1E is a cross-sectional illustration of the device after a polishing operation is implemented to planarize the material layers, according to an embodiment of the invention.

Figure 2A is a cross-sectional illustration of a device after a source and drain contact have  
5 been fabricated in a first ILD, according to an embodiment of the invention.

Figure 2B is a cross-sectional illustration of the device after a second ILD has been deposited over the first ILD, according to an embodiment of the invention.

Figure 2C is a cross-sectional illustration of the device after the second ILD has been patterned to form a trench in which the TFT semiconductor layer may be deposited, according to  
10 an embodiment of the invention.

Figure 2D is a cross-sectional illustration of the device after the TFT semiconductor layer and the gate dielectric layer have been deposited, according to an embodiment of the invention.

Figure 2E is a cross-sectional illustration of the device after a capping layer has been deposited over the gate dielectric layer, according to an embodiment of the invention.

Figure 2F is a cross-sectional illustration of the device after the material layers are planarized with a polishing operation, according to an embodiment of the invention.  
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Figure 2G is a cross-sectional illustration of the device after a third ILD is deposited over the second ILD, according to an embodiment of the invention.

Figure 2H is a cross-sectional illustration of the device after a gate trench is patterned through the third ILD and the capping layer, according to an embodiment of the invention.  
20

Figure 2I is a cross-sectional illustration of the device after the gate electrode is formed in the gate trench, according to an embodiment of the invention.

Figure 3A is a cross-sectional illustration of a first ILD with a gate electrode, according to an embodiment of the invention.

Figure 3B is a cross-sectional illustration of the device after a second ILD has been formed over the first ILD, according to an embodiment of the invention.  
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Figure 3C is a cross-sectional illustration of the device after a trench has been formed into the second ILD, according to an embodiment of the invention.

Figure 3D is a cross-sectional illustration of the device after a gate dielectric layer and a TFT semiconductor layer have been deposited in the trench, according to an embodiment of the invention.  
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Figure 3E is a cross-sectional illustration of the device after a capping layer has been deposited over the TFT layer, according to an embodiment of the invention.

Figure 3F is a cross-sectional illustration of the device after the layers have been planarized

with a polishing operation, according to an embodiment of the invention.

Figure 3G is a cross-sectional illustration of the device after source and drain openings are formed through the capping layer, according to an embodiment of the invention.

Figure 3H is a cross-sectional illustration of the device after the source and drain are  
5 formed in the source and drain openings, according to an embodiment of the invention.

Figure 4 is a cross-sectional illustration of a TFT that includes source, gate, and drain electrodes below the TFT, according to an embodiment of the invention.

Figure 5 is a cross-sectional illustration of a TFT that includes source, gate, and drain electrodes above the TFT, according to an embodiment of the invention.

10 Figure 6 is an interposer implementing one or more embodiments of the invention.

Figure 7 is a computing device built in accordance with an embodiment of the invention.

## DETAILED DESCRIPTION OF THE INVENTION

Described herein are systems that include thin-film transistors (TFTs) and methods of  
15 forming such devices with damascene processing operations. In the following description, various aspects of the illustrative implementations will be described using terms commonly employed by those skilled in the art to convey the substance of their work to others skilled in the art. However, it will be apparent to those skilled in the art that the present invention may be practiced with only some of the described aspects. For purposes of explanation, specific  
20 numbers, materials and configurations are set forth in order to provide a thorough understanding of the illustrative implementations. However, it will be apparent to one skilled in the art that the present invention may be practiced without the specific details. In other instances, well-known features are omitted or simplified in order not to obscure the illustrative implementations.

Various operations will be described as multiple discrete operations, in turn, in a manner  
25 that is most helpful in understanding the present invention, however, the order of description should not be construed to imply that these operations are necessarily order dependent. In particular, these operations need not be performed in the order of presentation.

As noted above, TFTs are currently fabricated with subtractive patterning processes, such as wet and/or dry etching processes. However, these operations limit the materials that may be  
30 used to form the TFT due to concerns such as diffusion of the TFT materials during high temperature operations and other negative etching effects (e.g., undercutting, oxidation, or the like). Accordingly, embodiments of the invention include TFTs that are fabricate with damascene processing operations. The use of a damascene processing operations allows for the dimensions of the TFT to be defined prior to the deposition of the TFT material. Accordingly,

damascene processes used to form the TFT semiconductor material and capping layer allow for increased flexibility in material choice for the interlayer dielectric (ILD). Accordingly, negative etching interactions and diffusion are not present in embodiments of the invention because all etching happens before the TFT semiconductor material is formed.

5 Referring now to Figures 1A-1E, a series of cross-sectional illustrations are shown that illustrate a generic process for forming the semiconductor layer of a TFT with a damascene process, according to an embodiment of the invention. In Figures 1A-1E the source, gate, and drain contacts are omitted for clarity, and in order to not obscure embodiments of the invention. However, embodiments that illustrate how the source, gate, and drain are fabricated in  
10 conjunction with the semiconductor layer are provided in greater detail below.

Referring now to Figure 1A, a cross-sectional illustration of an interlayer dielectric (ILD) 110 is shown, according to an embodiment of the invention. The ILD 110 may be a first layer of ILD formed on a support substrate (not shown), or it may be any subsequent ILD in a stack-up of multiple ILDs. According to an embodiment, the ILD 110 may have a thickness  $T_1$  that is greater  
15 than a thickness of a subsequently formed TFT semiconductor layer. For example, the ILD 110 may have a thickness  $T_1$  that is greater than approximately 5 nm. In an embodiment, the ILD 110 may have a thickness  $T_1$  that is greater than approximately 50 nm. In yet another embodiment, the ILD 110 may have a thickness  $T_1$  that is greater than approximately 100 nm. In an embodiment, the ILD 110 may be any suitable low-k dielectric material. For example, low-k  
20 dielectric materials may include, but are not limited to, silicon dioxide ( $\text{SiO}_2$ ), carbon doped oxide (CDO), silicon nitride, organic polymers such as perfluorocyclobutane or polytetrafluoroethylene, fluorosilicate glass (FSG), and organosilicates such as silsesquioxane, siloxane, or organosilicate glass. The ILD material may include pores or air gaps to further reduce their dielectric constant.

25 Referring now to Figure 1B, a cross-sectional illustration of the ILD 110 after a trench 112 is patterned in to the surface is shown, according to an embodiment of the invention. According to an embodiment, the trench 112 may be patterned with any suitable etching process. For example, the trench 112 may be patterned with typical wet and/or dry etching processes. In the illustrated embodiment, sidewalls 113 of the trench are illustrated as being slightly off axis  
30 from 90°. However, it is to be appreciated that the angle of the sidewalls with respect to the surface of the ILD 110 may be any angle, and is primarily determined by the etching processes that are used to form the trench 112.

According to an embodiment, the dimensions of the trench may be chosen in order to define a TFT that has a desired performance. For example, the trench 112 may have an opening

with a length  $L$  that is substantially similar to the desired length of the subsequently formed TFT. For example, the length  $L$  may be between approximately 20 nm and approximately 200 nm. However, it is to be appreciated that the length  $L$  may also be less than 20 nm or greater than 200 nm according to different embodiments of the invention. In an embodiment, the depth  $D$  of the trench 112 may be chosen so that it is greater than the desired thickness of the subsequently deposited TFT semiconductor layer. For example, the depth  $D$  of the trench 112 may be between approximately 10 nm and approximately 100 nm. However, it is to be appreciated that the depth  $D$  may also be less than 10 nm or greater than 100 nm according to different embodiments of the invention.

Referring now to Figure 1C, a cross-sectional illustration of the device after a TFT semiconductor layer 120 is blanket deposited is shown, according to an embodiment of the invention. In an embodiment, the TFT semiconductor material may be any suitable semiconductor material used for thin film transistors. In one embodiment, the TFT semiconductor layer 120 may be one or more of InGaZnO, alpha-Ge, alpha-Si, ZnO, and polymer/organic semiconductors. In an embodiment, the TFT semiconductor layer 120 is deposited to a thickness  $T_2$  that is desired for the thickness of the TFT film in the final TFT device. In an embodiment, the thickness  $T_2$  may be between approximately 5 nm and approximately 50 nm. However, it is to be appreciated that the thickness  $T_2$  may also be less than 5 nm or greater than 50 nm according to different embodiments of the invention.

According to an embodiment the thickness of the TFT semiconductor layer 120 may be precisely controlled by using deposition process such as atomic layer deposition (ALD). Such deposition processes may be considered conformal deposition processes. As such, embodiments may include extensions 122 of the TFT semiconductor layer 120 that extend up along the wall 113 of the trench 112. In an embodiment, at least a portion of the extensions 122 may remain in the final TFT device, as will be shown below.

Referring now to Figure 1D, a cross-sectional illustration of the device after a capping layer 130 is formed over the TFT semiconductor layer 120 is shown, according to an embodiment of the invention. In an embodiment, the capping layer 130 may be any suitable non-conductive material that can be used to fill the remaining portions of the trench 112 in order to hermetically seal the TFT semiconductor layer 120 formed in the trench 112. For example, the capping layer 130 may be a dielectric material, such as SiN. In an embodiment, the SiN capping layer may be doped with any suitable dopants, such as carbon, oxygen, or the like. According to an embodiment, the capping layer may be deposited with any suitable deposition processes, such as chemical vapor deposition (CVD), plasma enhanced CVD (PECVD), or the like.

Referring now to Figure 1E, a cross-sectional illustration of the device after a polishing process has been implemented is shown, according to an embodiment of the invention. In an embodiment, the polishing process may recess the portions of the capping layer 130 and the TFT semiconductor layer 120 that are formed above the trench 112. In an embodiment, a portion of the ILD 110 may also be recessed. As a result of the polishing process, a top surface of the capping layer 133 may be substantially coplanar with a top surface of the ILD 110.

In an embodiment, the polishing process may be a chemical mechanical polishing (CMP) process. It is to be appreciated that substantially no oxidation of the TFT semiconductor layer 120 occurs during the polishing process since the capping layer protects the TFT semiconductor layer 120 during the polishing operation. Accordingly, the resulting device includes a TFT semiconductor layer 120 that is formed with the proper dimensions without suffering from oxidation, diffusion, or other etching effects such as those described above.

Referring now to Figure 2A-2I, a series of cross-sectional illustrations are shown that illustrate a generic process for forming a TFT where the semiconductor layer of a TFT is formed with a damascene process, according to an embodiment of the invention. In Figures 2A-2I, the source and drain electrodes are formed below the TFT semiconductor layer, and the gate electrode is formed above the TFT semiconductor layer.

Referring now to Figure 2A, a cross-sectional illustration of a first ILD 210 with a source electrode 241 and a drain electrode 242 is shown, according to an embodiment of the invention. In an embodiment, the first ILD 210 may be a first layer of ILD formed on a support substrate (not shown), or it may be any subsequent ILD in a stack-up of multiple ILDs. In an embodiment, the source electrode 241 and the drain electrode 242 may be formed with any suitable processes known in the art. For example, the source electrode 241 and the drain electrode 242 may be formed with subtractive processes or damascene processes. In an embodiment, the source electrode 241 and the drain electrode 242 may be conductive materials, such as copper.

Referring now to Figure 2B, a cross-sectional illustration of the device after a second ILD 214 is formed over the first ILD 210 is shown, according to an embodiment. In an embodiment, the second ILD 214 may have a thickness  $T_1$  that is greater than a thickness of a subsequently formed TFT semiconductor layer. For example, the second ILD 214 may have a thickness  $T_1$  that is greater than approximately 5 nm. In an embodiment, the second ILD 214 may have a thickness  $T_1$  that is greater than approximately 50 nm. In yet another embodiment, the second ILD 214 may have a thickness  $T_1$  that is greater than approximately 100 nm. In an embodiment, the second ILD 214 may be any suitable dielectric material.

Referring now to Figure 2C a cross-sectional illustration of the device after a trench 212

is patterned in to the surface is shown, according to an embodiment of the invention. According to an embodiment, the trench 212 may be patterned with any suitable etching process. For example, the trench 212 may be patterned with typical wet and/or dry etching processes. In the illustrated embodiment, sidewalls 213 of the trench are illustrated as being slightly off axis from 90°. However, it is to be appreciated that the angle of the sidewalls with respect to the surface of the second ILD 214 may be any angle, and is primarily determined by the etching processes that are used to form the trench 212.

According to an embodiment, the dimensions of the trench may be chosen in order to define a TFT that has a desired performance. For example, the trench 212 may have an opening with a length L that is substantially similar to the desired length of the subsequently formed TFT. For example, the length L may be between approximately 20 nm and approximately 200 nm. However, it is to be appreciated that the length L may also be less than 20 nm or greater than 200 nm according to different embodiments of the invention. In an embodiment, the trench 214 may be formed entirely through the second ILD 214 in order to expose the source electrode 241 and the drain electrode 242.

Referring now to Figure 2D, a cross-sectional illustration of the device after the TFT semiconductor layer 220 and a gate dielectric layer 250 are formed is shown, according to an embodiment of the invention. In an embodiment, the TFT semiconductor layer may be deposited in the trench 212 such that it is in direct contact with the source electrode 241 and the drain electrode 242. In an embodiment, the TFT semiconductor material may be any suitable semiconductor material used for thin film transistors. In one embodiment, the TFT semiconductor layer 220 may be one or more of InGaZnO, alpha-Ge, alpha-Si, ZnO, and polymer/organic semiconductors. In an embodiment, the TFT semiconductor layer 220 is deposited to a thickness  $T_2$  that is desired for the thickness of the TFT film in the final TFT device. In an embodiment, the thickness  $T_2$  may be between approximately 5 nm and approximately 50 nm. However, it is to be appreciated that the thickness  $T_2$  may also be less than 5 nm or greater than 50 nm according to different embodiments of the invention.

According to an embodiment the thickness of the TFT semiconductor layer 220 may be precisely controlled by using deposition process such as ALD. Such deposition processes may be considered conformal deposition processes. As such, embodiments may include extensions 222 of the TFT semiconductor layer 220 that extend up along the wall 213 of the trench 212. In an embodiment, at least a portion of the extensions 222 may remain in the final TFT device, as will be shown below.

In an embodiment, the gate dielectric layer 250 may be any suitable high-K dielectric

material. In an embodiment, the gate dielectric layer 250 may include one layer or a stack of layers. The high-k dielectric material may include elements such as hafnium, silicon, oxygen, titanium, tantalum, lanthanum, aluminum, zirconium, barium, strontium, yttrium, lead, scandium, niobium, and zinc. Examples of high-k materials that may be used in the gate

5 dielectric layer include, but are not limited to, hafnium oxide, hafnium silicon oxide, lanthanum oxide, lanthanum aluminum oxide, zirconium oxide, zirconium silicon oxide, tantalum oxide, titanium oxide, barium strontium titanium oxide, barium titanium oxide, strontium titanium oxide, yttrium oxide, aluminum oxide, lead scandium tantalum oxide, and lead zinc niobate. In an embodiment, the gate dielectric layer 250 may be blanket deposited over the TFT  
10 semiconductor layer. For example, the gate dielectric layer may be deposited with CVD, PECVD, or the like.

Referring now to Figure 2E, a cross-sectional illustration of the device after a capping layer 230 is formed over the gate dielectric layer 250 is shown, according to an embodiment of the invention. In an embodiment, the capping layer 230 may be any suitable non-conductive  
15 material that can be used to fill the remaining portions of the trench 212 in order to hermetically seal the TFT semiconductor layer 220 formed in the trench 212. For example, the capping layer 130 may be a dielectric material, such as SiN. In an embodiment, the SiN capping layer may be doped with any suitable dopants, such as carbon, oxygen, or the like. According to an embodiment, the capping layer may be deposited with any suitable deposition processes, such as  
20 CVD, PECVD, or the like.

Referring now to Figure 2F, a cross-sectional illustration of the device after a polishing process has been implemented is shown, according to an embodiment of the invention. In an embodiment, the polishing process may recess the portions of the capping layer 230, the gate dielectric layer 250, and the TFT semiconductor layer 220 that are formed above the trench 212.

25 In an embodiment, a portion of the second ILD 214 may also be recessed. As a result of the polishing process, a top surface of the capping layer 233 may be substantially coplanar with a top surface of the second ILD 214.

In an embodiment, the polishing process may be a CMP process. It is to be appreciated that substantially no oxidation of the TFT semiconductor layer 220 occurs during the polishing  
30 process since the capping layer 230 and the gate dielectric 250 protects the TFT semiconductor layer 120 during the polishing operation. Accordingly, the resulting device includes a TFT semiconductor layer 220 that is formed with the proper dimensions without suffering from oxidation, diffusion, or other etching effects such as those described above.

Referring now to Figure 2G, a cross-sectional illustration of the device after a third

dielectric layer 216 is formed over the second dielectric layer 214 is shown, according to an embodiment of the invention. According to an embodiment, the third dielectric layer 216 may be any suitable dielectric material. For example, the selection of the dielectric material is not limited by processing conditions that may negatively affect the TFT semiconductor layer 220.

5 Referring now to Figure 2H, a cross-sectional illustration of the device after a gate trench 272 is formed through the third dielectric layer 216 and the capping layer 230 is shown, according to an embodiment of the invention. According to an embodiment, the gate trench 272 may be formed with any patterning process, such as wet and/or dry etching. In an embodiment, the gate trench 272 exposes the gate dielectric layer 250. Furthermore, it is to be appreciated that  
10 the presence of the gate dielectric layer 250 provides protection to the TFT semiconductor layer 220 from the etching process.

Referring now to Figure 2I, a cross-sectional illustration of the device after the gate electrode 270 is formed is shown, according to an embodiment of the invention. In an embodiment, the gate electrode 270 may be any suitable conductive material. In some  
15 embodiments, the gate electrode 270 may consist of a stack of two or more metal layers, where one or more metal layers are workfunction metal layers and at least one metal layer is a fill metal layer. For example, metals that may be used for the gate electrode 270 include, but are not limited to, ruthenium, palladium, platinum, cobalt, nickel, and conductive metal oxides, e.g., ruthenium oxide, hafnium, zirconium, titanium, tantalum, aluminum, alloys of these metals, and  
20 carbides of these metals such as hafnium carbide, zirconium carbide, titanium carbide, tantalum carbide, and aluminum carbide. In an embodiment the gate electrode may be deposited with any suitable deposition process, such as CVD, PECVD, sputtering, or the like. In an embodiment, the gate electrode 272 may also be formed with a replacement metal gate process, as is known in the art. In such an embodiment, the gate trench 272 may be filled with a polysilicon material that is  
25 subsequently removed and replaced with one or more conductive metals.

Referring now to Figure 3A-3H, a series of cross-sectional illustrations are shown that illustrate a process for forming a TFT where the semiconductor layer of a TFT is formed with a damascene process, according to an embodiment of the invention. In Figures 3A-3H, the source and drain electrodes are formed above the TFT semiconductor layer, and the gate electrode is  
30 formed below the TFT semiconductor layer.

Referring now to Figure 3A, a cross-sectional illustration of a first ILD 310 with a gate electrode 370 is shown, according to an embodiment of the invention. In an embodiment, the first ILD 310 may be a first layer of ILD formed on a support substrate (not shown), or it may be any subsequent ILD in a stack-up of multiple ILDs. In an embodiment, the gate electrode 370

may be formed with any suitable processes known in the art. For example, the gate electrode 370 may be formed with subtractive processes or damascene processes. In an embodiment, the gate electrode 370 may be conductive materials, such as those described above.

Referring now to Figure 3B, a cross-sectional illustration of the device after a second IL  
5 314 is formed over the first ILD 310 is shown, according to an embodiment. In an embodiment, the second ILD 314 may have a thickness  $T_1$  that is greater than a thickness of a subsequently formed TFT semiconductor layer. For example, the second ILD 314 may have a thickness  $T_1$  that is greater than approximately 5 nm. In an embodiment, the second ILD 314 may have a thickness  $T_1$  that is greater than approximately 50 nm. In yet another embodiment, the second ILD 314  
10 may have a thickness  $T_1$  that is greater than approximately 100 nm. In an embodiment, the second ILD 314 may be any suitable dielectric material.

Referring now to Figure 3C a cross-sectional illustration of the device after a trench 312 is patterned in to the surface is shown, according to an embodiment of the invention. According to an embodiment, the trench 312 may be patterned with any suitable etching process. For  
15 example, the trench 312 may be patterned with typical wet and/or dry etching processes. In the illustrated embodiment, sidewalls 313 of the trench are illustrated as being slightly off axis from 90°. However, it is to be appreciated that the angle of the sidewalls with respect to the surface of the second ILD 314 may be any angle, and is primarily determined by the etching processes that are used to form the trench 312.

According to an embodiment, the dimensions of the trench may be chosen in order to  
20 define a TFT that has a desired performance. For example, the trench 312 may have an opening with a length  $L$  that is substantially similar to the desired length of the subsequently formed TFT. For example, the length  $L$  may be between approximately 20 nm and approximately 200 nm. However, it is to be appreciated that the length  $L$  may also be less than 20 nm or greater than 200  
25 nm according to different embodiments of the invention. In an embodiment, the trench 314 may be formed entirely through the second ILD 314 in order to expose the gate electrode 370.

Referring now to Figure 3D, a cross-sectional illustration of the device after a gate  
dielectric layer 350 and the TFT semiconductor layer 320 and are formed is shown, according to an embodiment of the invention. In an embodiment, the gate dielectric layer 350 may be  
30 deposited first so that it is formed over a top surface of the gate electrode 350. In an embodiment, the gate dielectric layer 350 may be any suitable high-K dielectric material, such as those described above. In an embodiment, the gate dielectric layer 350 may be blanket deposited over the TFT semiconductor layer. For example, the gate dielectric layer may be deposited with CVD, PECVD, or the like.

In an embodiment, the TFT semiconductor layer may be deposited in the trench 312 such that it is formed over the top surface of the gate dielectric layer 350. In an embodiment, the TFT semiconductor material may be any suitable semiconductor material used for thin film transistors. In one embodiment, the TFT semiconductor layer 320 may be one or more of

5 InGaZnO, alpha-Ge, alpha-Si, ZnO, and polymer/organic semiconductors. In an embodiment, the TFT semiconductor layer 320 is deposited to a thickness  $T_2$  that is desired for the thickness of the TFT film in the final TFT device. In an embodiment, the thickness  $T_2$  may be between approximately 5 nm and approximately 50 nm. However, it is to be appreciated that the thickness  $T_2$  may also be less than 5 nm or greater than 50 nm according to different embodiments of the

10 invention.

According to an embodiment, the thickness of the TFT semiconductor layer 320 may be precisely controlled by using deposition process such as atomic layer deposition (ALD). Such deposition processes may be considered conformal deposition processes. As such, embodiments may include extensions 322 of the TFT semiconductor layer 320 that extend up along the wall

15 313 of the trench 312. In an embodiment, at least a portion of the extensions 322 may remain in the final TFT device, as will be shown below.

Referring now to Figure 3E, a cross-sectional illustration of the device after a capping layer 330 is formed over the gate dielectric layer 350 is shown, according to an embodiment of the invention. In an embodiment, the capping layer 330 may be any suitable non-conductive

20 material that can be used to fill the remaining portions of the trench 312 in order to hermetically seal the TFT semiconductor layer 320 formed in the trench 312. For example, the capping layer 330 may be a dielectric material, such as SiN. In an embodiment, the SiN capping layer may be doped with any suitable dopants, such as carbon, oxygen, or the like. According to an embodiment, the capping layer may be deposited with any suitable deposition processes, such as

25 CVD, PECVD, or the like.

Referring now to Figure 3F, a cross-sectional illustration of the device after a polishing process has been implemented is shown, according to an embodiment of the invention. In an embodiment, the polishing process may recess the portions of the capping layer 330, the gate dielectric layer 350, and the TFT semiconductor layer 320 that are formed above the trench 312.

30 In an embodiment, a portion of the second ILD 314 may also be recessed. As a result of the polishing process, a top surface of the capping layer 333 may be substantially coplanar with a top surface of the second ILD 314.

In an embodiment, the polishing process may be a CMP process. It is to be appreciated that substantially no oxidation of the TFT semiconductor layer 320 occurs during the polishing

process since the capping layer 330 protects the TFT semiconductor layer 320 during the polishing operation. Accordingly, the resulting device includes a TFT semiconductor layer 320 that is formed with the proper dimensions without suffering from oxidation, diffusion, or other etching effects such as those described above.

5 Referring now to Figure 3G, a cross-sectional illustration of the device after a source and drain trenches 344,345 are formed through the capping layer 330 is shown, according to an embodiment of the invention. According to an embodiment, the source and drain trenches 344,345 may be formed with any patterning process, such as wet and/or dry etching. In an embodiment, the source and drain trenches 344,345 expose TFT semiconductor layer 320.

10 Referring now to Figure 3I, a cross-sectional illustration of the device after the source electrode 341 and the drain electrode 342 are formed is shown, according to an embodiment of the invention. In an embodiment, the source electrode 341 and the drain electrode 342 may be any suitable conductive material. For example, the gate electrode may be copper. In an embodiment the gate electrode may be deposited with any suitable deposition process, such as  
15 CVD, PECVD, sputtering, or the like.

It is to be appreciated that the above referenced TFT devices are just exemplary illustrations, and the use of damascene patterning to form the TFT semiconductor layer may be used to form many TFT devices with various configurations. Particularly, the TFT devices in Figures 2I and 3H include source/drain electrodes that are formed on opposite surfaces of the  
20 TFT semiconductor layer than the gate electrode. However, embodiments may also include TFT devices where the source, drain, and gate electrodes are formed over the same surface of the TFT semiconductor layer.

Referring now to Figure 4, a cross-sectional illustration of a TFT device where the source electrode 441, the drain electrode 442, and the gate electrode 470 are formed below the TFT  
25 semiconductor layer. As illustrated in Figure 4, the TFT device includes a TFT semiconductor layer 420 formed with a damascene process. Particularly, the indication that the TFT semiconductor layer 420 is formed with a damascene process is the presence of extensions 422 along the edge of the TFT semiconductor layer 420. In the illustrated embodiment, the source electrode 441 and the drain electrode 442 are in direct contact with a bottom surface of the TFT  
30 semiconductor layer 420, and the gate electrode 470 is separated from the bottom surface of the TFT semiconductor layer 520 by the gate dielectric 450. Furthermore, the processing, and materials for forming the TFT device in Figure 4 may be substantially similar to those described above, as those skilled in the art will recognize.

Referring now to Figure 5, a cross-sectional illustration of a TFT device where the

source electrode 541, the drain electrode 542, and the gate electrode 570 are formed above the TFT semiconductor layer 520. As illustrated in Figure 5, the TFT device includes a TFT semiconductor layer 520 formed with a damascene process. Particularly, the indication that the TFT semiconductor layer 520 is formed with a damascene process is the presence of extensions 522 along the edge of the TFT semiconductor layer 520. In the illustrated embodiment, the source electrode 541 and the drain electrode 542 are in direct contact with a top surface of the TFT semiconductor layer 520, and the gate electrode 570 is separated from the bottom surface of the TFT semiconductor layer 520 by the gate dielectric 550. Furthermore, the processing, and materials for forming the TFT device in Figure 5 may be substantially similar to those described above, as those skilled in the art will recognize.

Figure 6 illustrates an interposer 600 that includes one or more embodiments of the invention. The interposer 600 is an intervening substrate used to bridge a first substrate 602 to a second substrate 604. The first substrate 602 may be, for instance, an integrated circuit die. The second substrate 604 may be, for instance, a memory module, a computer motherboard, or another integrated circuit die. Generally, the purpose of an interposer 600 is to spread a connection to a wider pitch or to reroute a connection to a different connection. For example, an interposer 600 may couple an integrated circuit die to a ball grid array (BGA) 606 that can subsequently be coupled to the second substrate 604. In some embodiments, the first and second substrates 602/604 are attached to opposing sides of the interposer 600. In other embodiments, the first and second substrates 602/604 are attached to the same side of the interposer 600. And in further embodiments, three or more substrates are interconnected by way of the interposer 600.

The interposer 600 may be formed of an epoxy resin, a fiberglass-reinforced epoxy resin, a ceramic material, or a polymer material such as polyimide. In further implementations, the interposer may be formed of alternate rigid or flexible materials that may include the same materials described above for use in a semiconductor substrate, such as silicon, germanium, and other group III-V and group IV materials.

The interposer may include metal interconnects 608 and vias 610, including but not limited to through-silicon vias (TSVs) 612. The interposer 600 may further include embedded devices 614, including both passive and active devices. Such devices include, but are not limited to, capacitors, decoupling capacitors, resistors, inductors, fuses, diodes, transformers, sensors, and electrostatic discharge (ESD) devices. More complex devices such as radio-frequency (RF) devices, power amplifiers, power management devices, antennas, arrays, sensors, and MEMS devices may also be formed on the interposer 600.

In accordance with embodiments of the invention, apparatuses or processes disclosed herein may be used in the fabrication of interposer 600.

Figure 7 illustrates a computing device 700 in accordance with one embodiment of the invention. The computing device 700 may include a number of components. In one  
5 embodiment, these components are attached to one or more motherboards. In an alternate embodiment, these components are fabricated onto a single system-on-a-chip (SoC) die rather than a motherboard. The components in the computing device 700 include, but are not limited to, an integrated circuit die 702 and at least one communication chip 708. In some  
10 implementations the communication chip 708 is fabricated as part of the integrated circuit die 702. The integrated circuit die 702 may include a CPU 704 as well as on-die memory 706, often used as cache memory, that can be provided by technologies such as embedded DRAM (eDRAM) or spin-transfer torque memory (STTM or STTM-RAM).

Computing device 700 may include other components that may or may not be physically and electrically coupled to the motherboard or fabricated within an SoC die. These other  
15 components include, but are not limited to, volatile memory 710 (e.g., DRAM), non-volatile memory 712 (e.g., ROM or flash memory), a graphics processing unit 714 (GPU), a digital signal processor 716, a crypto processor 742 (a specialized processor that executes cryptographic algorithms within hardware), a chipset 720, an antenna 722, a display or a touchscreen display 724, a touchscreen controller 726, a battery 728 or other power source, a power amplifier (not  
20 shown), a global positioning system (GPS) device 728, a compass 730, a motion coprocessor or sensors 732 (that may include an accelerometer, a gyroscope, and a compass), a speaker 734, a camera 736, user input devices 738 (such as a keyboard, mouse, stylus, and touchpad), and a mass storage device 740 (such as hard disk drive, compact disk (CD), digital versatile disk (DVD), and so forth).

25 The communications chip 708 enables wireless communications for the transfer of data to and from the computing device 700. The term “wireless” and its derivatives may be used to describe circuits, devices, systems, methods, techniques, communications channels, etc., that may communicate data through the use of modulated electromagnetic radiation through a non-solid medium. The term does not imply that the associated devices do not contain any wires,  
30 although in some embodiments they might not. The communication chip 708 may implement any of a number of wireless standards or protocols, including but not limited to Wi-Fi (IEEE 802.11 family), WiMAX (IEEE 802.16 family), IEEE 802.20, long term evolution (LTE), Ev-DO, HSPA+, HSDPA+, HSUPA+, EDGE, GSM, GPRS, CDMA, TDMA, DECT, Bluetooth, derivatives thereof, as well as any other wireless protocols that are designated as 3G, 4G, 5G,

and beyond. The computing device 700 may include a plurality of communication chips 708. For instance, a first communication chip 708 may be dedicated to shorter range wireless communications such as Wi-Fi and Bluetooth and a second communication chip 708 may be dedicated to longer range wireless communications such as GPS, EDGE, GPRS, CDMA, WiMAX, LTE, Ev-DO, and others.

The processor 704 of the computing device 700 includes one or more devices, such as TFT devices formed with damascene processing operations, that are formed in accordance with embodiments of the invention. The term “processor” may refer to any device or portion of a device that processes electronic data from registers and/or memory to transform that electronic data into other electronic data that may be stored in registers and/or memory.

The communication chip 708 may also include one or more devices, such as TFT devices formed with damascene processing operations, that are formed in accordance with embodiments of the invention.

In further embodiments, another component housed within the computing device 700 may contain one or more devices, such as TFT devices formed with damascene processing operations, that are formed in accordance with implementations of the invention.

In various embodiments, the computing device 700 may be a laptop computer, a netbook computer, a notebook computer, an ultrabook computer, a smartphone, a tablet, a personal digital assistant (PDA), an ultra mobile PC, a mobile phone, a desktop computer, a server, a printer, a scanner, a monitor, a set-top box, an entertainment control unit, a digital camera, a portable music player, or a digital video recorder. In further implementations, the computing device 700 may be any other electronic device that processes data.

The above description of illustrated implementations of the invention, including what is described in the Abstract, is not intended to be exhaustive or to limit the invention to the precise forms disclosed. While specific implementations of, and examples for, the invention are described herein for illustrative purposes, various equivalent modifications are possible within the scope of the invention, as those skilled in the relevant art will recognize.

These modifications may be made to the invention in light of the above detailed description. The terms used in the following claims should not be construed to limit the invention to the specific implementations disclosed in the specification and the claims. Rather, the scope of the invention is to be determined entirely by the following claims, which are to be construed in accordance with established doctrines of claim interpretation.

Example 1: a thin-film transistor (TFT) device, comprising: an interlayer dielectric (ILD) layer, wherein a trench is formed into the ILD layer; a TFT semiconductor layer formed in the

trench, wherein extensions of the TFT semiconductor layer extend up sidewalls of the trench; a capping layer formed over a top surface of the TFT semiconductor layer; a source electrode and a drain electrode, wherein the source electrode and the drain electrode contact a surface of the TFT semiconductor layer; and a gate electrode separated from a surface of the TFT

5 semiconductor layer by a gate dielectric layer.

Example 2: the TFT device of Example 1, wherein a top surface of the capping layer is substantially coplanar with a top surface of the ILD layer.

Example 3: the TFT device of Example 1 or Example 2, wherein the gate electrode is separated from a top surface of the TFT semiconductor layer by the gate dielectric layer.

10 Example 4: the TFT device of Example 1, Example 2, or Example 3, wherein the source electrode and the drain electrode contact a bottom surface of the TFT semiconductor layer.

Example 5: the TFT device of Example 1, Example 2, Example 3, or Example 4, wherein the source electrode and the drain electrode contact the top surface of the TFT semiconductor layer.

15 Example 6: the TFT device of Example 1, Example 2, Example 3, Example 4, or Example 5, wherein the gate electrode is separated from a bottom surface of the TFT semiconductor layer by the gate dielectric layer.

Example 7: the TFT device of Example 1, Example 2, Example 3, Example 4, Example 5, or Example 6, wherein the source electrode and the drain electrode contact a top surface of the  
20 TFT semiconductor layer.

Example 8: the TFT device of Example 1, Example 2, Example 3, Example 4, Example 5, Example 6, or Example 7, wherein the source electrode and the drain electrode contact the bottom surface of the TFT semiconductor layer.

Example 9: the TFT device of Example 1, Example 2, Example 3, Example 4, Example  
25 5, Example 6, Example 7, or Example 8, wherein the gate dielectric layer is formed over a top surface of the TFT semiconductor layer, and wherein the cap layer is formed over a top surface of the TFT semiconductor layer.

Example 10: the TFT device of Example 1, Example 2, Example 3, Example 4, Example  
5, Example 6, Example 7, Example 8, or Example 9, wherein the gate dielectric layer is formed  
30 over the surface of the trench, and wherein the TFT semiconductor layer is formed over a top surface of the top surface of the gate dielectric layer.

Example 11: the TFT device of Example 1, Example 2, Example 3, Example 4, Example  
5, Example 6, Example 7, Example 8, Example 9, or Example 10, wherein sidewalls of the trench are not oriented 90° with respect to a top surface of the ILD layer.

Example 12: the TFT device of Example 1, Example 2, Example 3, Example 4, Example 5, Example 6, Example 7, Example 8, Example 9, Example 10, or Example 11, wherein the TFT semiconductor layer is one or more of InGaZnO, alpha-Ge, alpha-Si, ZnO, or polymer/organic semiconductors.

5        Example 13: a method of forming a thin-film transistor (TFT) device, comprising: forming an interlayer dielectric (ILD) layer; forming a trench into the ILD layer; depositing a TFT semiconductor material over the ILD layer with a conformal deposition process; depositing a capping material over a top surface of the TFT semiconductor material; and planarizing the device such that a top surface of the capping material is substantially coplanar with a top surface  
10    of the ILD layer.

Example 14: the method of Example 13, wherein the TFT semiconductor layer includes extensions formed along sidewalls of the trench in the ILD layer.

Example 15: the method of Example 13 or Example 14, further comprising: forming a source electrode and a drain electrode, wherein the source electrode and drain electrode contact a  
15    surface of the TFT semiconductor layer.

Example 16: the method of Example 13, Example 14, or Example 15, wherein forming the trench in the ILD layer exposes the surface of the source electrode and drain electrode.

Example 17: the method of Example 13, Example 14, Example 15, or Example 16, further comprising: forming a gate dielectric layer; and forming a gate electrode, wherein the  
20    gate electrode is separated from the TFT semiconductor layer by the gate dielectric layer.

Example 18: the method of Example 13, Example 14, Example 15, Example 16, or Example 17 wherein the gate dielectric layer is formed over a top surface of the TFT semiconductor layer.

Example 19: the method of Example 13, Example 14, Example 15, Example 16, Example  
25    17, or Example 18, wherein the gate dielectric layer is formed below a bottom surface of the TFT semiconductor layer.

Example 20: the method of Example 13, Example 14, Example 15, Example 16, Example 17, Example 18, or Example 19, wherein the gate electrode is formed with a damascene process.

Example 21: the method of Example 13, Example 14, Example 15, Example 16, Example  
30    17, Example 18, Example 19, or Example 20, wherein the gate electrode is formed with a replacement metal gate process.

Example 22: the method of Example 13, Example 14, Example 15, Example 16, Example 17, Example 18, Example 19, Example 20, or Example 21, wherein the TFT semiconductor layer in the trench is completely covered by the capping layer prior to the device being planarized.

Example 23: a thin-film transistor (TFT) device, comprising: an interlayer dielectric (ILD) layer, wherein a trench is formed into the ILD layer; a TFT semiconductor layer formed in the trench, wherein extensions of the TFT semiconductor layer extend up sidewalls of the trench; a capping layer formed over a top surface of the TFT semiconductor layer, wherein a top surface  
5 of the capping layer is substantially coplanar with a top surface of the ILD layer; a source electrode and a drain electrode, wherein the source electrode and the drain electrode contact a surface of the TFT semiconductor layer; and a gate electrode separated from a surface of the TFT semiconductor layer by a gate dielectric layer, wherein the gate electrode is formed over a surface of the TFT semiconductor layer that is opposite to the surface which the source electrode  
10 and the drain electrode contact.

Example 24: the TFT device of Example 23, wherein the source electrode and the drain electrode contact a bottom surface of the TFT semiconductor layer.

Example 25: the TFT device of Example 23 or Example 24, wherein the source electrode and the drain electrode contact a top surface of the TFT semiconductor layer.

15

**CLAIMS****What is claimed is:**

1. A thin-film transistor (TFT) device, comprising:
  - 5 an interlayer dielectric (ILD) layer, wherein a trench is formed into the ILD layer;  
a TFT semiconductor layer formed in the trench, wherein extensions of the TFT semiconductor layer extend up sidewalls of the trench;  
a capping layer formed over a top surface of the TFT semiconductor layer;  
a source electrode and a drain electrode, wherein the source electrode and the
  - 10 drain electrode contact a surface of the TFT semiconductor layer; and  
a gate electrode separated from a surface of the TFT semiconductor layer by a gate dielectric layer.
2. The TFT device of claim 1, wherein a top surface of the capping layer is substantially  
15 coplanar with a top surface of the ILD layer.
3. The TFT device of claim 1, wherein the gate electrode is separated from a top surface of the TFT semiconductor layer by the gate dielectric layer.
- 20 4. The TFT device of claim 3, wherein the source electrode and the drain electrode contact a bottom surface of the TFT semiconductor layer.
5. The TFT device of claim 3, wherein the source electrode and the drain electrode contact the top surface of the TFT semiconductor layer.
- 25 6. The TFT device of claim 1, wherein the gate electrode is separated from a bottom surface of the TFT semiconductor layer by the gate dielectric layer.

7. The TFT device of claim 6, wherein the source electrode and the drain electrode contact a top surface of the TFT semiconductor layer.
- 5 8. The TFT device of claim 6, wherein the source electrode and the drain electrode contact the bottom surface of the TFT semiconductor layer.
9. The TFT device of claim 1, wherein the gate dielectric layer is formed over a top surface of the TFT semiconductor layer, and wherein the cap layer is formed over a top surface of the TFT semiconductor layer.
- 10 10. The TFT device of claim 1, wherein the gate dielectric layer is formed over the surface of the trench, and wherein the TFT semiconductor layer is formed over a top surface of the top surface of the gate dielectric layer.
- 15 11. The TFT device of claim 1, wherein sidewalls of the trench are not oriented 90° with respect to a top surface of the ILD layer.
12. The TFT device of claim 1, wherein the TFT semiconductor layer is one or more of InGaZnO, alpha-Ge, alpha-Si, ZnO, and polymer/organic semiconductors.
- 20 13. A method of forming a thin-film transistor (TFT) device, comprising:  
forming an interlayer dielectric (ILD) layer;  
forming a trench into the ILD layer;  
25 depositing a TFT semiconductor material over the ILD layer with a conformal deposition process;  
depositing a capping material over a top surface of the TFT semiconductor

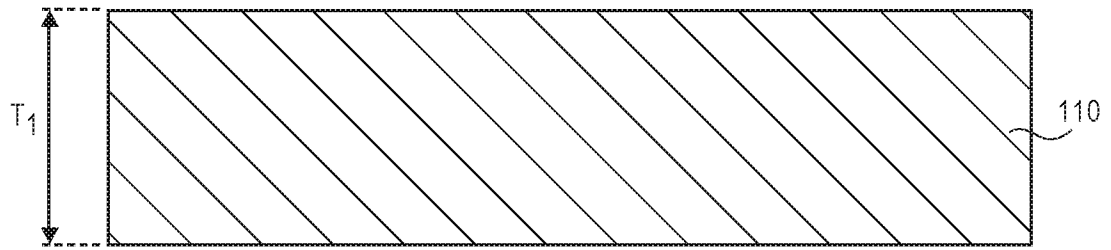
material; and

planarizing the device such that a top surface of the capping material is substantially coplanar with a top surface of the ILD layer.

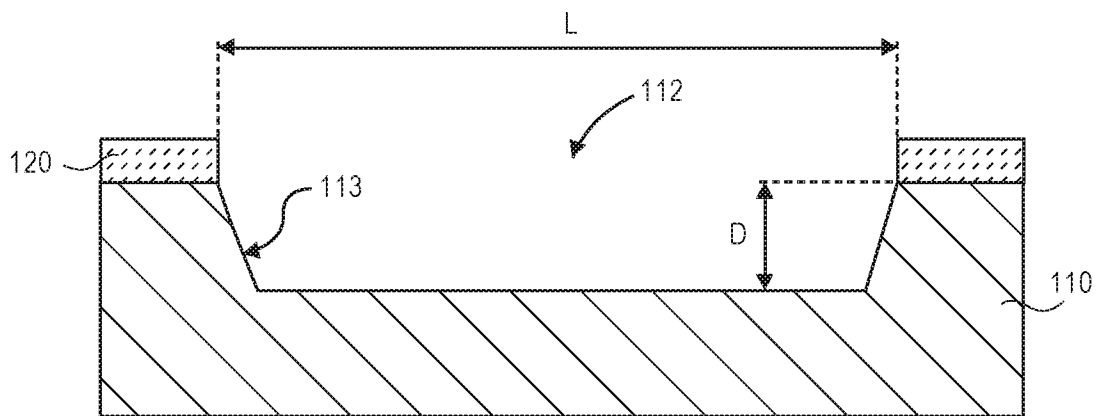
- 5     14.     The method of claim 13, wherein the TFT semiconductor layer includes extensions formed along sidewalls of the trench in the ILD layer.
15.     The method of claim 13, further comprising:  
forming a source electrode and a drain electrode, wherein the source electrode and  
10     drain electrode contact a surface of the TFT semiconductor layer.
16.     The method of claim 13, wherein forming the trench in the ILD layer exposes the surface of the source electrode and drain electrode.
- 15     17.     The method of claim 13, further comprising:  
forming a gate dielectric layer; and  
forming a gate electrode, wherein the gate electrode is separated from the TFT  
semiconductor layer by the gate dielectric layer.
- 20     18.     The method of claim 17, wherein the gate dielectric layer is formed over a top surface of the TFT semiconductor layer.
19.     The method of claim 17, wherein the gate dielectric layer is formed below a bottom  
surface of the TFT semiconductor layer.
- 25
20.     The method of claim 17, wherein the gate electrode is formed with a damascene process.

21. The method of claim 17, wherein the gate electrode is formed with a replacement metal gate process.
- 5 22. The method of claim 13, wherein the TFT semiconductor layer in the trench is completely covered by the capping layer prior to the device being planarized.
23. A thin-film transistor (TFT) device, comprising:
- 10 an interlayer dielectric (ILD) layer, wherein a trench is formed into the ILD layer;  
a TFT semiconductor layer formed in the trench, wherein extensions of the TFT semiconductor layer extend up sidewalls of the trench;  
a capping layer formed over a top surface of the TFT semiconductor layer, wherein a top surface of the capping layer is substantially coplanar with a top surface of the ILD layer;
- 15 a source electrode and a drain electrode, wherein the source electrode and the drain electrode contact a surface of the TFT semiconductor layer; and  
a gate electrode separated from a surface of the TFT semiconductor layer by a gate dielectric layer, wherein the gate electrode is formed over a surface of the TFT semiconductor layer that is opposite to the surface which the source electrode and the drain electrode contact.
- 20
24. The TFT device of claim 23, wherein the source electrode and the drain electrode contact a bottom surface of the TFT semiconductor layer.
- 25 25. The TFT device of claim 23, wherein the source electrode and the drain electrode contact a top surface of the TFT semiconductor layer.

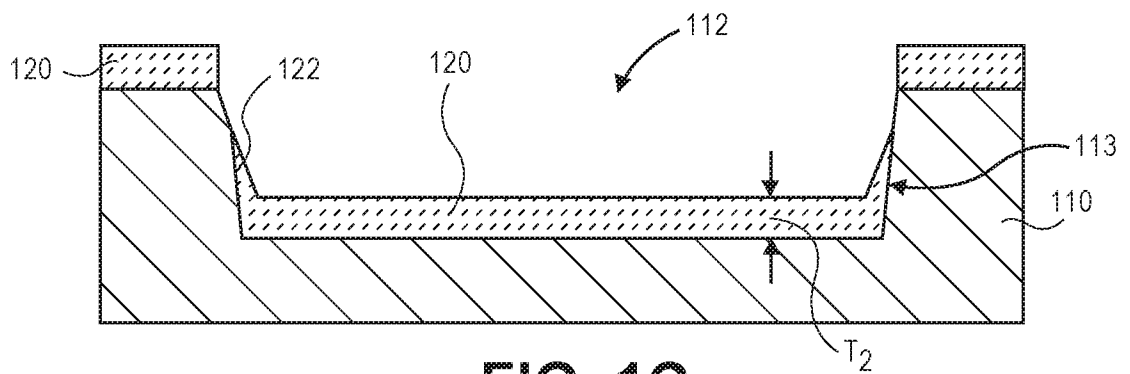
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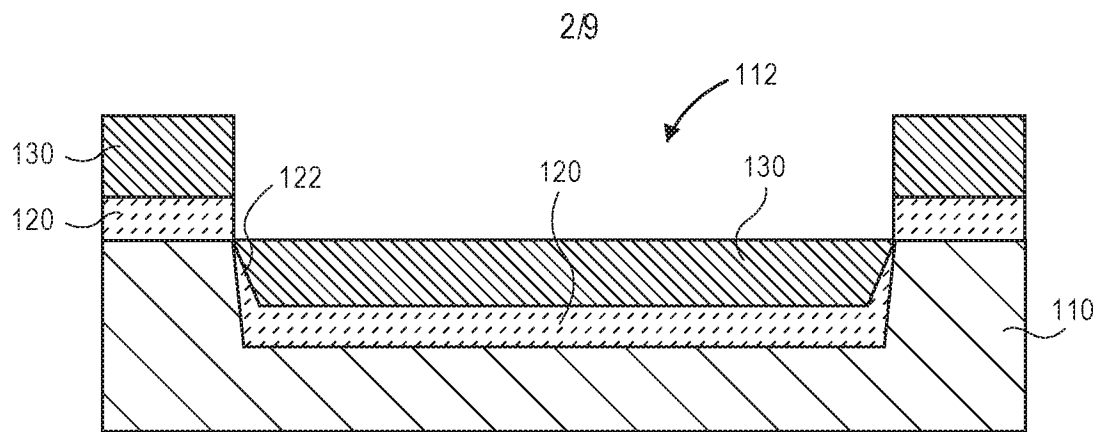
**FIG. 1A**



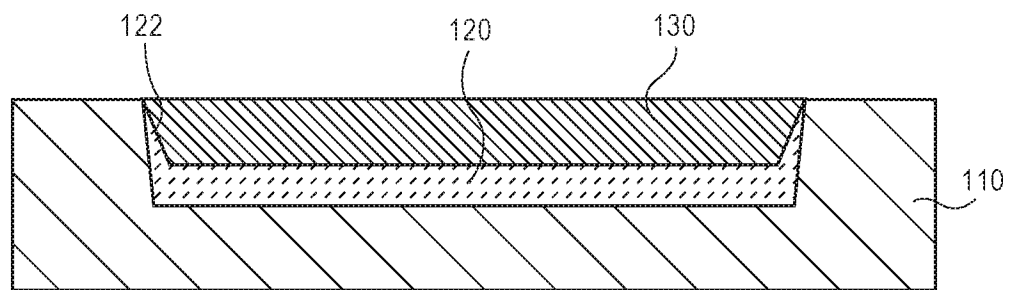
**FIG. 1B**



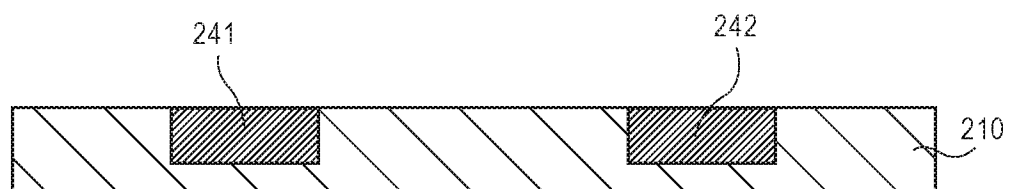
**FIG. 1C**



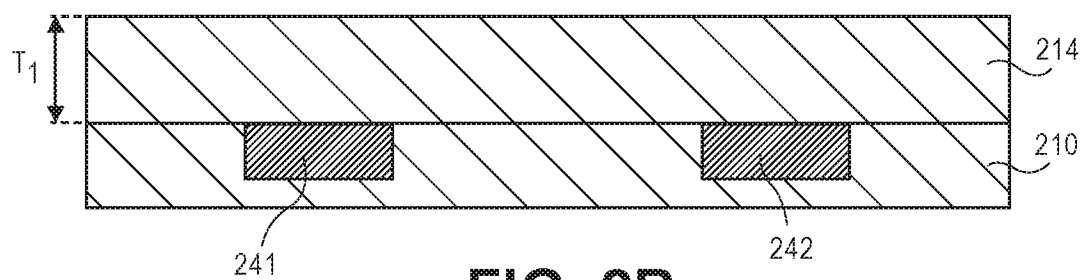
**FIG. 1D**



**FIG. 1E**



**FIG. 2A**



**FIG. 2B**

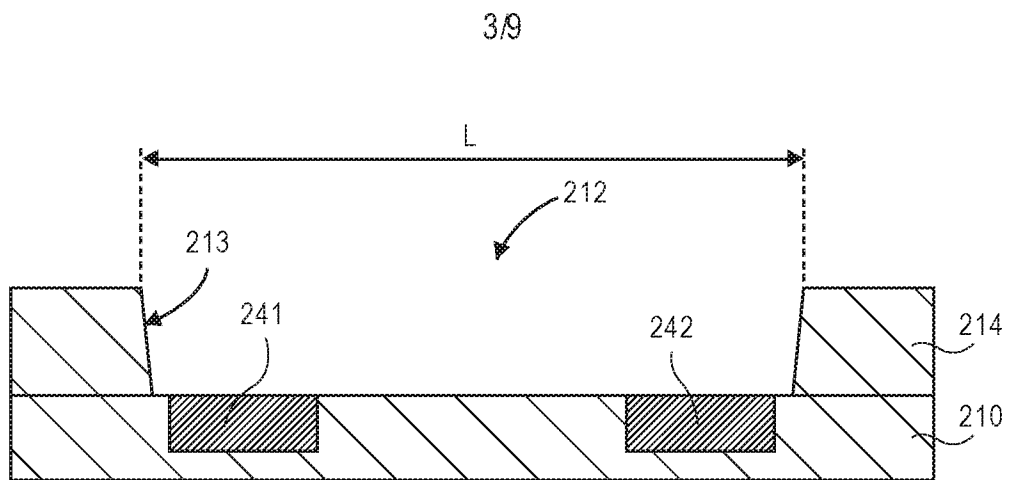


FIG. 2C

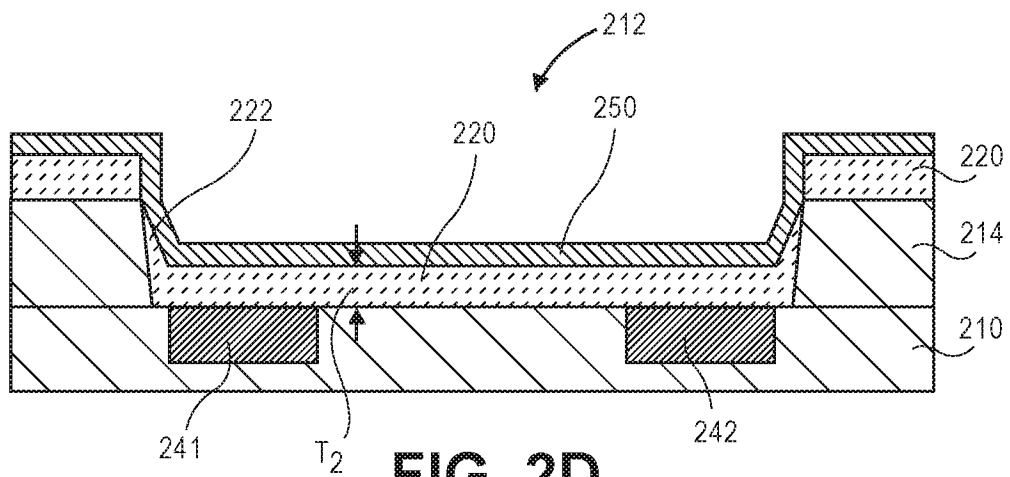


FIG. 2D

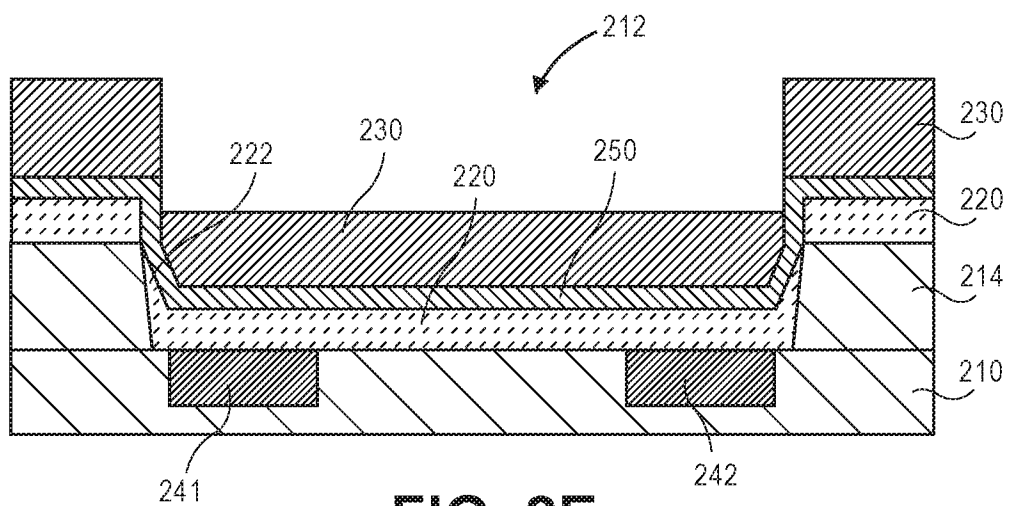
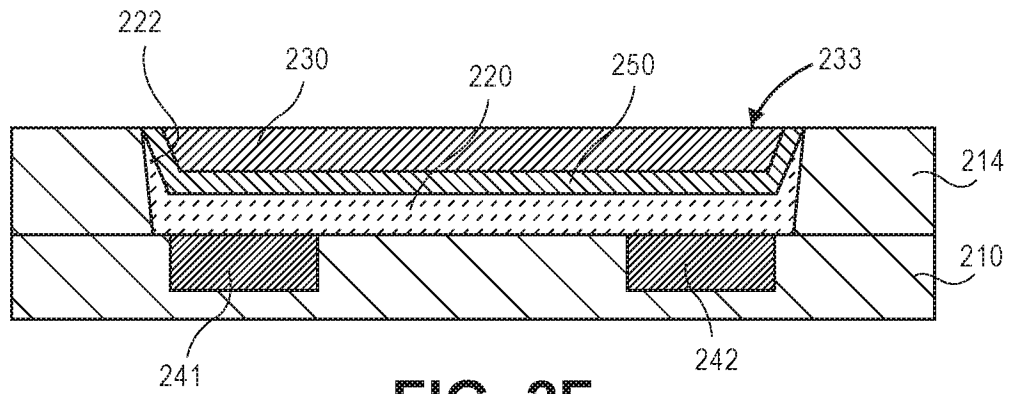
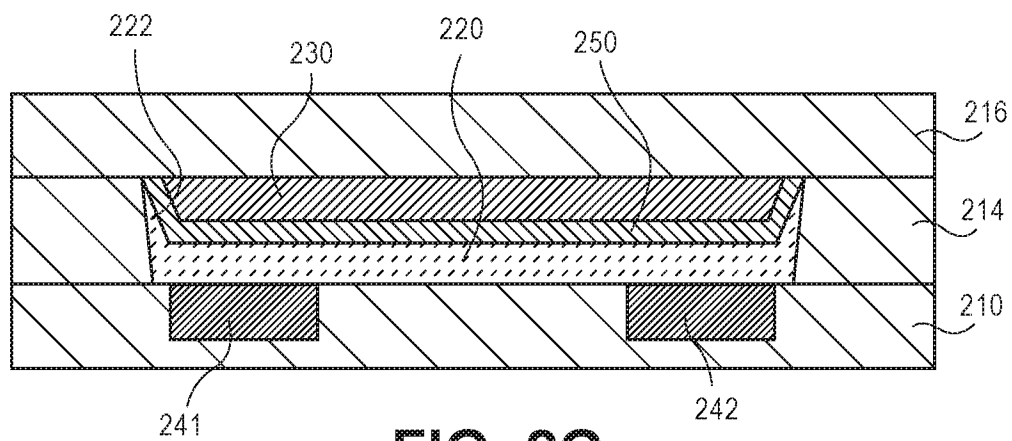


FIG. 2E

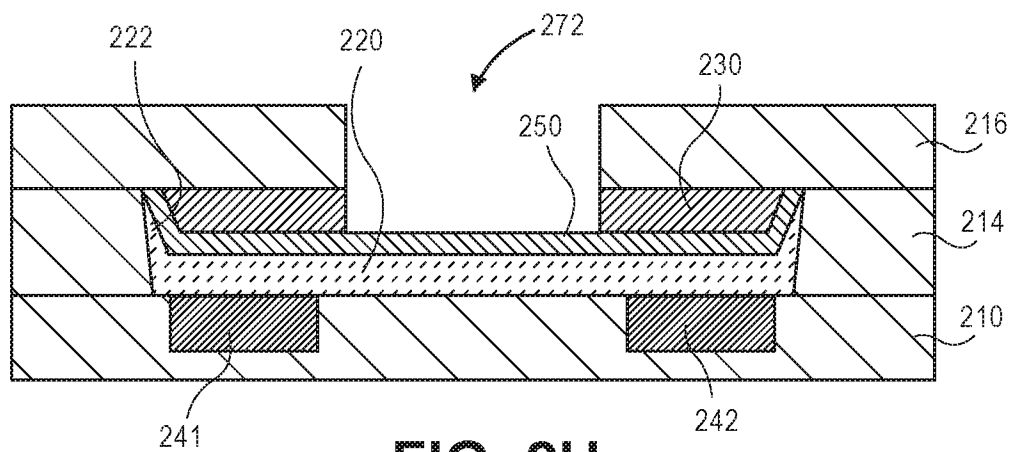
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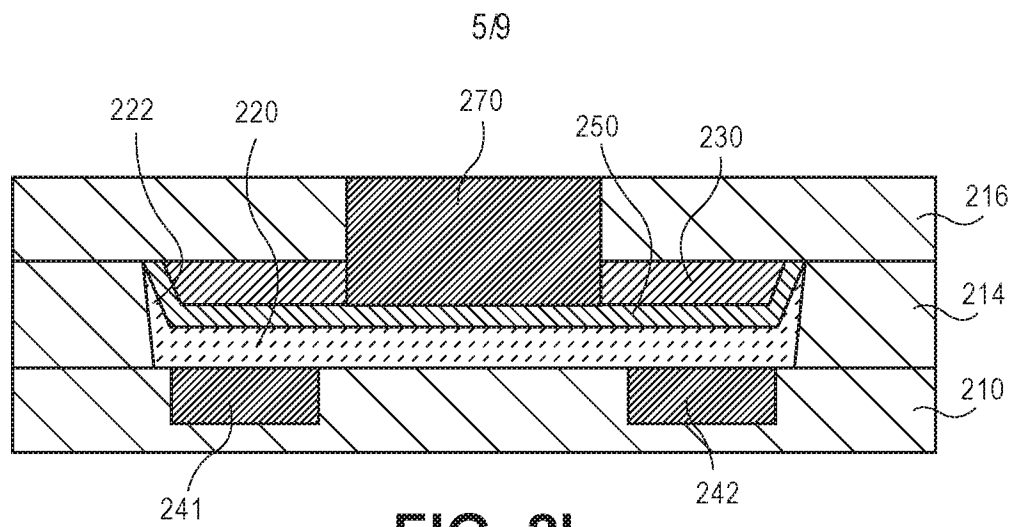
**FIG. 2F**



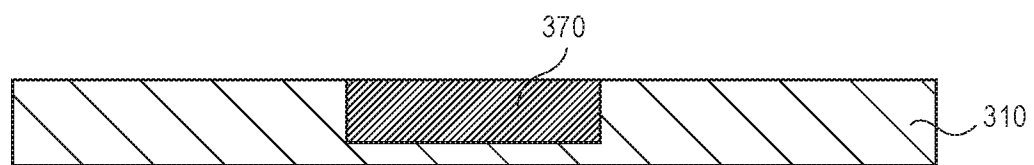
**FIG. 2G**



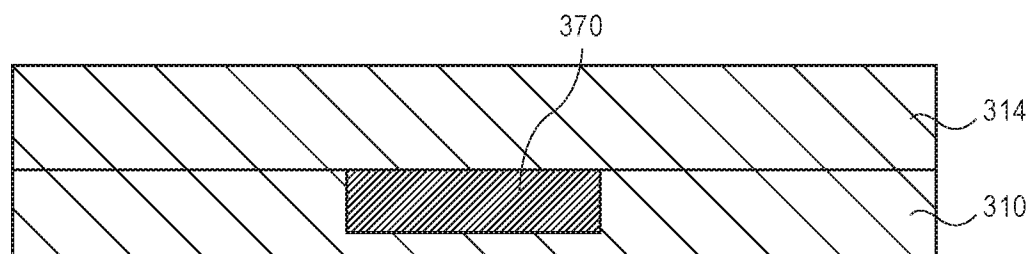
**FIG. 2H**



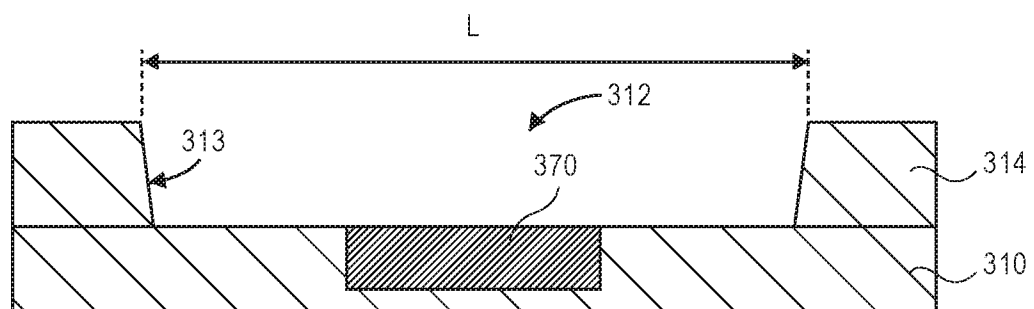
**FIG. 2I**



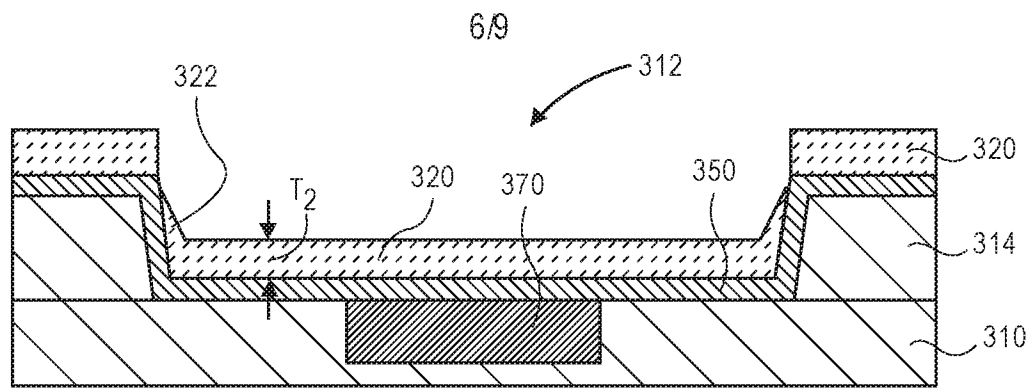
**FIG. 3A**



**FIG. 3B**



**FIG. 3C**



**FIG. 3D**

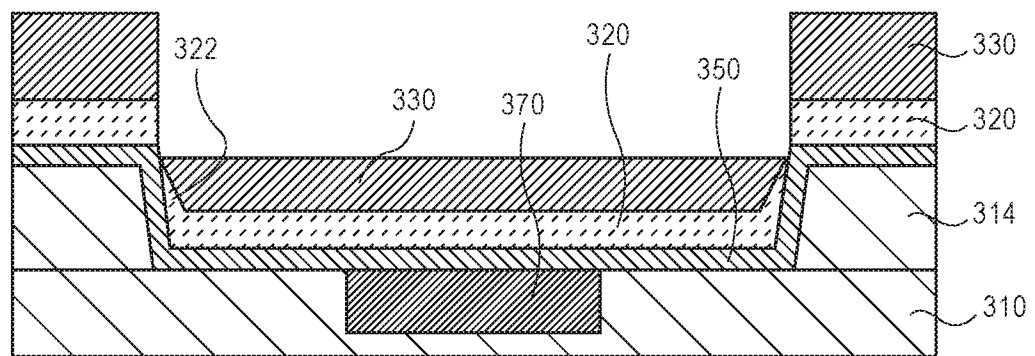
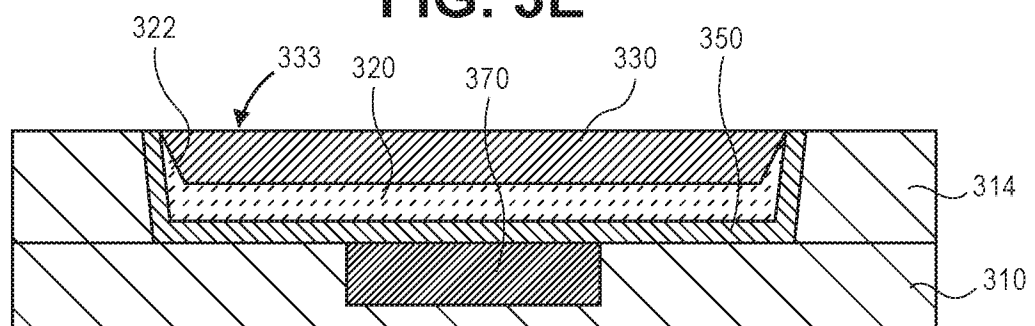


FIG. 3E



**FIG. 3F**

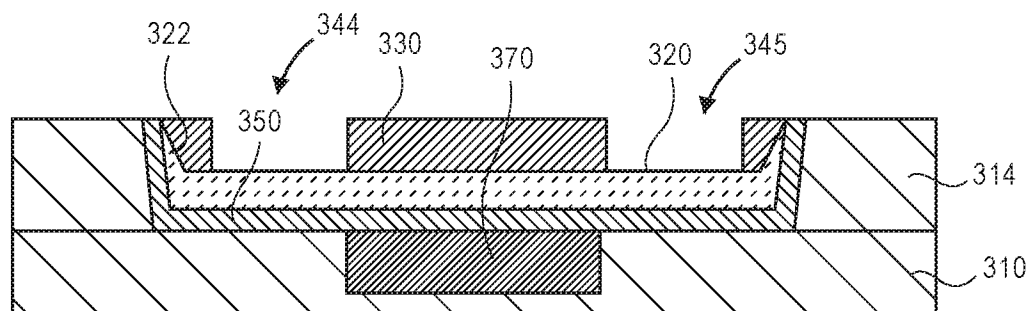
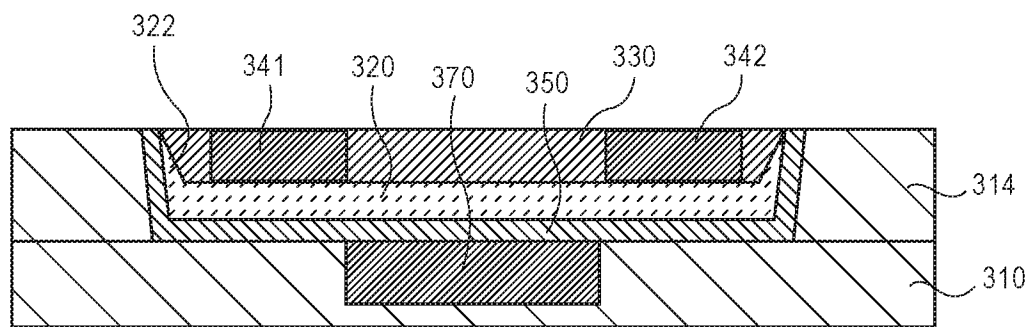
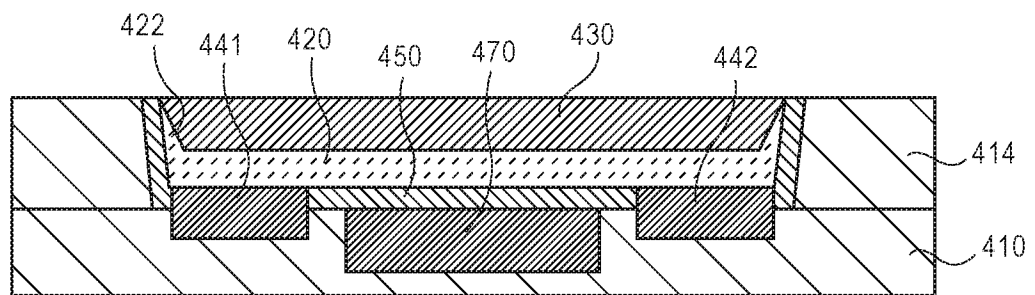


FIG. 3G

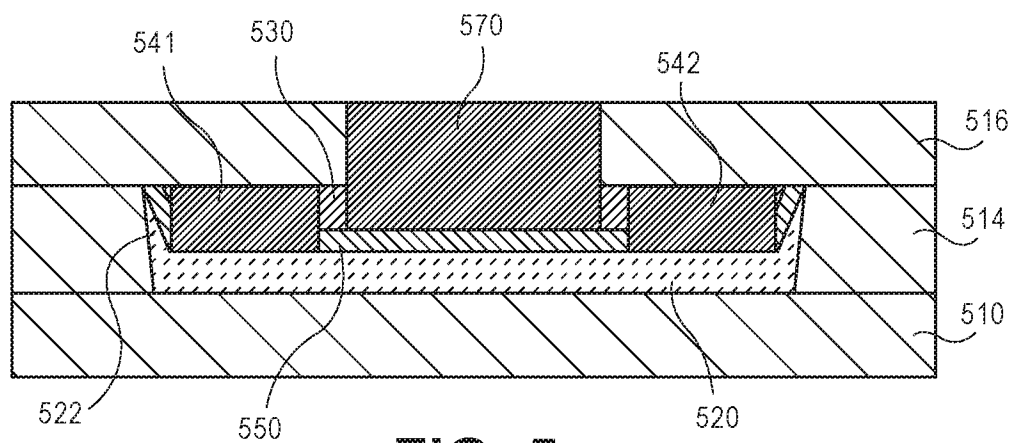
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**FIG. 3H**



**FIG. 4**



**FIG. 5**

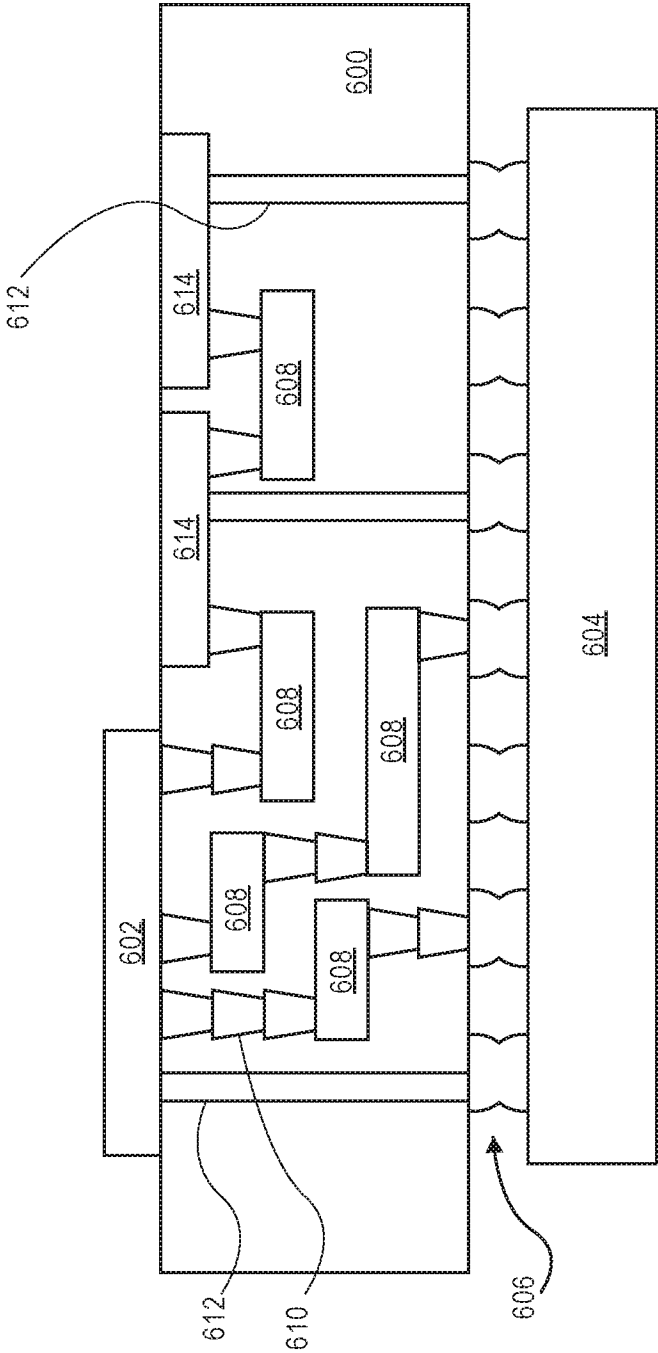
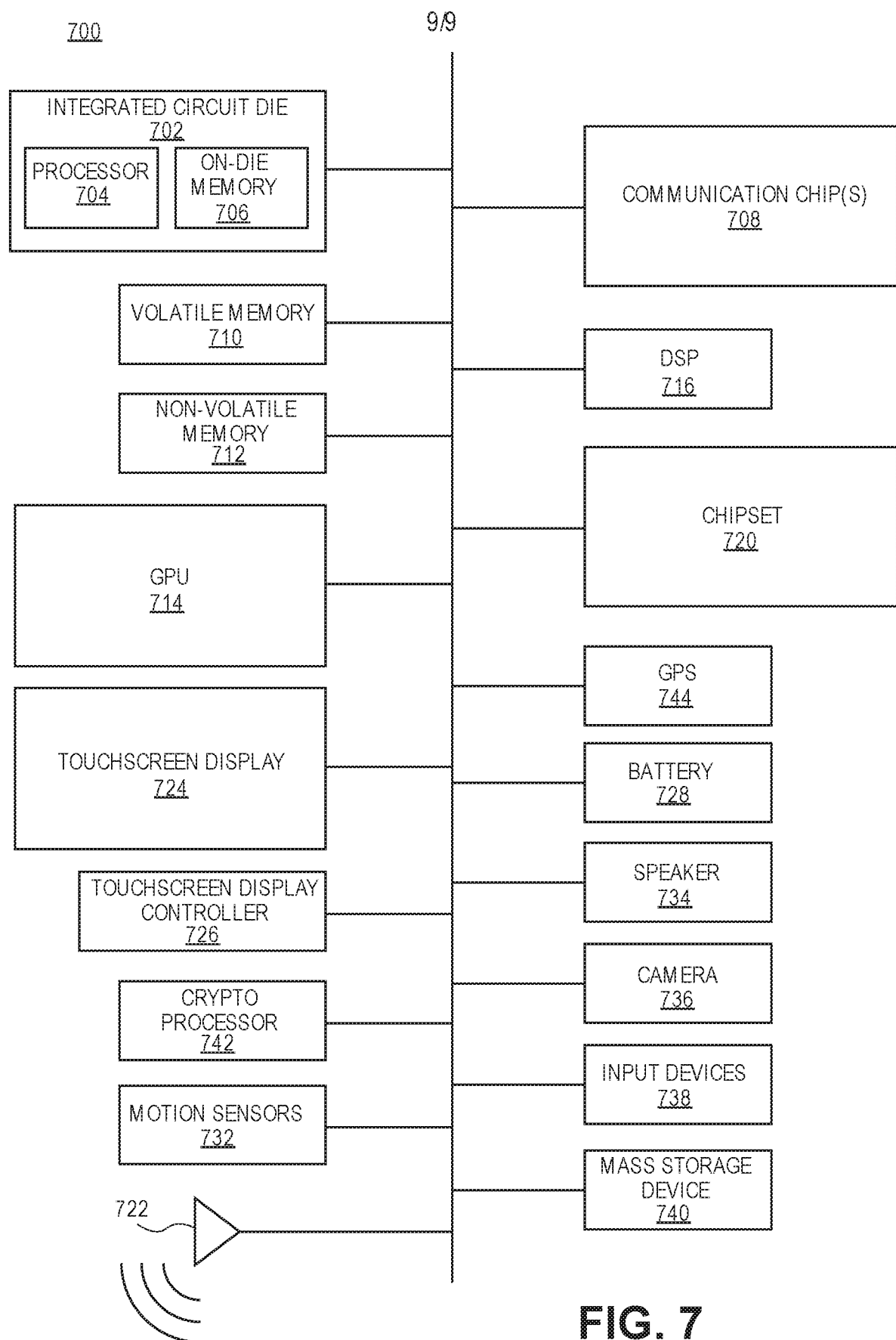


FIG. 6



**A. CLASSIFICATION OF SUBJECT MATTER****H01L 29/786(2006.01)i, H01L 21/768(2006.01)i**

According to International Patent Classification (IPC) or to both national classification and IPC

**B. FIELDS SEARCHED**

Minimum documentation searched (classification system followed by classification symbols)

H01L 29/786; H01L 21/336; H01L 29/72; H01L 21/82; H01L 21/768

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Korean utility models and applications for utility models

Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

eKOMPASS(KIPO internal) &amp; Keywords: TFT, interlayer dielectric, capping layer, gate electrode, source electrode, drain electrode, trench, planarize, coplanar

**C. DOCUMENTS CONSIDERED TO BE RELEVANT**

| Category* | Citation of document, with indication, where appropriate, of the relevant passages | Relevant to claim No. |
|-----------|------------------------------------------------------------------------------------|-----------------------|
| Y         | JP 3273989 B2 (NIPPON STEEL CORP.) 15 April 2002                                   | 1,3-12                |
| A         | See paragraphs [0027]-[0030], [0034] and figures 2(a)-2(f).                        | 2, 13-25              |
| Y         | US 6107662 A (KIM) 22 August 2000                                                  | 1,3-12                |
| A         | See column 3, lines 22-23 and figure 4A.                                           |                       |
| A         | JP 2008-060524 A (SHARP CORP.) 13 March 2008                                       | 1-25                  |
| A         | See paragraphs [0019]-[0022] and figure 5.                                         |                       |
| A         | JP 2013-131766 A (PLASTIC LOGIC LTD. et al.) 04 July 2013                          | 1-25                  |
| A         | See paragraphs [0072]-[0100] and figures 3(A)-4(B).                                |                       |
| A         | US 2009-0258462 A1 (KONEVECKI et al.) 15 October 2009                              | 1-25                  |
| A         | See claim 1 and figures 3d-3e.                                                     |                       |



Further documents are listed in the continuation of Box C.



See patent family annex.

\* Special categories of cited documents:

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

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