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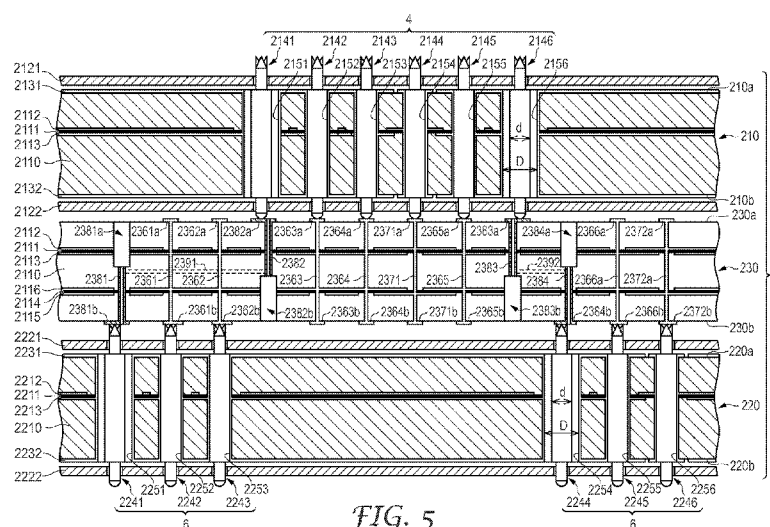


FIG. 5

(57) **Abstract:** The present invention relates to an IC device socket that enables the efficient use of conductive contact pins and enables them to be efficiently replaced. The IC device socket (100) includes a pin holder (1) that includes a first substrate (210), a second substrate (220), and a third substrate (230). The first substrate (210) includes a first pin (4) disposed to form a first arrangement pattern. The second substrate (220) includes a second pin (6) disposed to form a second arrangement pattern that is different from the first arrangement pattern. The third substrate (230) is disposed between the first and second substrates (210, 220), includes a plurality of conduction paths that electrically connect pins having the same function from among the first and second pins (4, 6), and the third substrate (230) is separated from at least one of the first and second substrates (210, 220).

IC DEVICE SOCKET

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Field of the Invention

The present invention relates to an IC device socket that retains connector pins used for electrically connecting each terminal of an electronic device such as a semiconductor integrated circuit (LSI) such as a processor, memory, or the like (hereafter referred to as an IC device) to a separate circuit board.

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Background

In recent years various IC devices are used. IC devices normally have a plurality of signal terminals for receiving various signals from the circuit board to operate the IC device, various signal terminals for transmitting the signals output from the IC device to the circuit board, a power supply terminal to supply electrical power to the IC device, and a ground terminal. Also, the interval (pitch) between the various terminals varies depending on the IC device. Therefore, in order to operate a plurality of types of IC device with different pitches between terminals using a single circuit board for operating the circuit board, for example, an inspection substrate for IC devices, it is necessary to electrically connect each of the terminals of the IC device with the corresponding terminals of the circuit board. In these cases an IC device socket having a plurality of connector pins arranged in alignment with the pitches between the various terminals is used.

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For example, Patent Document 1 discloses a board with variable terminal pitch. Patent Document 1 discloses "A plurality of socket terminal inserting holes 3 is provided in the center of a board body 1 of a board with variable terminal pitch in positions corresponding to the individual terminal pins 2a of a burn-in socket 2 on which a ball grid array (BGA) package has been mounted so that the socket terminal inserting holes 3 are connected to the individual terminal pins 2a, and a plurality of connecting pins 5 that connect with individual terminal connecting holes 4a is provided on the periphery of the board body 1 at positions corresponding to each terminal connecting hole 4a provided on a printed wiring board 4, and thereby interterminal connections between the burn-in socket 2 and printed wiring board 4 having mutually different terminal pitches are realized."

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Also, in connection with an IC device socket, Patent Document 2 discloses "The pitches of the electrodes 23 disposed on the rear side may be greater than the pitches of the electrodes 22 disposed on the top side."

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In addition, the IC device socket disclosed in Patent Document 3 has "a lower bracket 11, an upper bracket 20, an adjustment bracket 30, a cover 40, a lower oriented conduction sheet 50, a pad pitch conversion board 60, and an upper oriented conduction sheet 70". Also, Patent Document 3 discloses that

"semiconductor device side pads 81 or the like are arranged in grid form on the top surface and motherboard side pads are arranged in grid form on the bottom surface at approximately double the pitch of the semiconductor side pads. The motherboard pads are arranged at the pitch of the motherboard side pads of the pad pitch conversion board 60."

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Prior Art Documents

Patent Documents

Patent Document 1: Japanese Unexamined Patent Application Publication No. H11-67396

Patent Document 2: Japanese Unexamined Patent Application Publication No. 2000-82553

10 Patent Document 3: Japanese Unexamined Patent Application Publication No. 2007-80592

Summary

As a result of studying the conventional IC device sockets, the inventors found the following issues. Namely, in the conventional IC device socket, terminal (or pad) pitch conversion is carried out by a conversion member that integrates a contact portion wherein a plurality of connection pins (conductive contact pins) is disposed corresponding to the terminals of the IC device, and a contact portion wherein a plurality of connection pins (conductive contact pins) is disposed corresponding to the circuit board. In addition, the conductive contact pins are expensive, so normally connection pins whose reliability has reduced due to repeated use are replaced as needed. Therefore, when replacing the conductive contact pins in one contact portion, it is necessary to replace the whole conversion member, and the efficiency of the replacement operation is significantly reduced. Also, when replacing the whole conversion member, conductive contact pins that in reality do not need to be replaced must be replaced as a whole, so it was not possible to efficiently use the expensive conductive contact pins.

25 The present invention was devised to solve the problem as described above, and it is an object of the present invention to provide an IC device socket having a construction that enables the conductive contact pins to be efficiently used, and that enables efficient replacement of the conductive contact pins.

In order to solve the above task, the IC device socket according to the present invention includes a first substrate having a plurality of first conductive contact pins that extend through the interior thereof; a second substrate having a plurality of second conductive contact pins that extend through the interior thereof; and a third substrate that electrically connects pins having the same function from among the plurality of first conductive contact pins and the plurality of second conductive contact pins. In the first substrate, the plurality of first conductive contact pins is disposed to form a first arrangement pattern. In the second substrate, the plurality of second conductive contact pins is disposed to form a second arrangement pattern that is different from the first arrangement pattern, and each of the second conductive contact pins corresponds to one of the first conductive contact pins.. The third substrate is disposed between the first and second substrates, and has a plurality of conduction paths in the interior thereof.

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Each conduction path electrically connects one of the first conductive contact pins with the corresponding second conductive contact pin.

The third substrate may have a construction in which a dielectric layer and a pair of conductor layers that sandwich the dielectric layer from both the first substrate side and the second substrate side thereof is embedded within the third substrate (hereafter referred to as an ECM construction). In recent years, the signals handled by IC devices such as LSI and the like have higher frequencies associated with higher processing speeds, and the stable supply of power to these high frequency devices has become increasingly important. To stabilize the power supplied to an IC device, it is necessary to reduce the impedance between the ground and power supply, but it is possible to reduce the impedance by providing capacitance between the ground and power supply by the above construction.

Also, preferably the third substrate has a construction in which at least one of a strip line and a microstrip line are embedded within the third substrate. In this case, it is easy to control the signal impedance in the third substrate, as a part of the pin holder for a high frequency device. In the first and second substrates also, a construction that electrically isolates at least the conductive contact pins that form signal paths from the conductive members provided on the inside surface of the through holes in which they are inserted (hereafter referred to as a coaxial construction) may be adopted. In this construction also, it is easy to control the signal impedance, so the IC device socket according to the present invention is sufficiently compatible with the high frequency signals handled by the IC devices.

In particular, in the IC device socket according to the present invention, is separated from at least one of the first and second substrates. Therefore, the third substrate may be separate from the first and second substrates.

According to the present invention, the third substrate is disposed between the first substrate in which the first conductive contact pins are disposed so as to form the first arrangement pattern, and the second substrate in which the second conductive contact pins are disposed so as to form the second arrangement pattern which is different from the first arrangement pattern, the third substrate is separate from at least one of the first and second substrates, and the third substrate has a plurality of conduction paths that electrically connect pins having the same function from among the first and second conductive contact pins. As a result of this construction, it is possible to replace only the portions that need to be replaced, so the efficiency of use of the conductive contact pins and the efficiency of their replacement operation are dramatically improved.

Brief Description of the Drawings

FIG. 1 is a perspective view illustrating the construction of an embodiment of the IC device socket according to the present invention;

FIG. 2 illustrates the cross-sectional construction along the line I-I in the IC device socket illustrated in FIG. 1;

FIG. 3 is a plan view illustrating an example of a first arrangement pattern of first conductive contact pins disposed on a first substrate;

FIG. 4 is a plan view illustrating an example of a second arrangement pattern of second conductive contact pins disposed on a second substrate;

FIG. 5 is an expanded view of a cross-section of the main part of a first embodiment of the pin holder illustrated in FIG. 2;

FIG. 6 is a plan view for explaining the construction of signal transmission conduction paths provided in a third substrate;

FIG. 7 is a diagram for explaining the area of the strip line;

FIG. 8 is a diagram for explaining the area of the microstrip line;

FIG. 9 is a diagram for explaining an example of the 3-dimensional construction of a signal transmission conduction path provided in the third substrate;

FIG. 10 is a cross-sectional view illustrating an example of conductive contact pin that can be applied to each of the embodiments of the present invention;

FIG. 11 is a cross-sectional view illustrating another example of conductive contact pin that can be applied to each of the embodiments of the present invention;

FIG. 12 is a plan view illustrating another example of the first arrangement pattern of first conductive contact pins disposed on the first substrate;

FIG. 13 is a plan view illustrating another example of the second arrangement pattern of second conductive contact pins disposed on the second substrate;

FIG. 14 is an expanded view of a cross-section of the main part of a second embodiment of the pin holder illustrated in FIG. 2;

FIG. 15 is an expanded view of a cross-section of the main part of a third embodiment of the pin holder illustrated in FIG. 2;

Detailed Description

The following is a detailed explanation of each embodiment of the IC device socket according to the present invention, using FIGS. 1 through 15. In the explanations of the drawings, duplicate explanations of the same element with the same reference numeral are omitted.

The IC device socket according to the present embodiment includes a first substrate located on the side on which the IC device is installed and has a plurality of first conductive contact pins disposed on

the surface in opposition to the IC device; a second substrate located on the side of the circuit board that operates the IC device and that has a plurality of second contact pins disposed on the surface in opposition to the circuit board; and a third substrate disposed between the first and second substrates, having a plurality of conduction paths that electrically connect pins of the plurality of first conductive contact pins and the plurality of second conductive contact pins that have the same function. The third substrate is separated from at least one of first and second substrates. Also, the arrangement of the first conductive contact pins disposed on the IC device side surface of the first substrate and the arrangement pattern of the second conductive contact pins disposed on the circuit board side surface of the second substrate are different, in order to electrically connect each of the terminals of the IC device to the corresponding terminals of the circuit board.

On the other hand, in recent years, with the higher processing speeds of IC devices, the signals handled by the IC devices are becoming higher in frequency. Depending on the IC device, the signal may have a frequency of several hundred MHz, or even higher than 1GHz. Therefore there is also a demand for IC device sockets that can transmit high frequency signals, corresponding to these high signal frequencies. Therefore in the present embodiment, the impedance may be adjusted by adopting a coaxial construction for the conductive contact pin retention construction that constitutes a part of the signal path in the first and second substrates, and by having for example a strip line construction or microstrip line construction in the third substrate, which is disposed between the first and second substrates. In this way, the IC device socket according to the present embodiment reduces high frequency signal transmission loss between the IC device installed on the IC device socket and the circuit board.

FIG. 1 is a perspective view illustrating the construction of an embodiment of an IC device socket according to the present invention. FIG. 2 illustrates the cross-sectional construction along the line I-I in the IC device socket 100 illustrated in FIG. 1. The IC device socket 100 according to the present embodiment includes a pin holder 1, and a body 8 that supports the pin holder 1 provided on the outer periphery of the pin holder 1. The pin holder 1 includes a first substrate 210 having first conductive contact pins 4, a second substrate 220 having second conductive contact pins 6, and a third substrate 230 disposed between the first and second substrates 210, 220. A plurality of holes is provided on the top surface 210a (surface on the IC device side) of the first substrate 210 to form a first arrangement pattern, and by inserting the plurality of first conductive contact pins 4 into their corresponding holes, the first conductive contact pins 4 form the first arrangement pattern. Also, a plurality of holes is provided on the bottom surface 220b (surface on the side of the circuit board such as inspection device or the like) of the second substrate 220 to form a second arrangement pattern that is different from the first arrangement pattern, and by inserting the plurality of second conductive contact pins 6 into their corresponding holes, the second conductive contact pins 6 form the second arrangement pattern. The third substrate 230 includes a plurality of conduction paths, and each conduction path electrically connects pins of the plurality of first conductive contact pins and the plurality of second conductive contact pins that have the

same function. In other words, of the plurality of first conductive contact pins 4 and the plurality of second conductive contact pins 6, conductive contact pins that function as power supply pins, conductive contact pins that function as ground pins, and conductive contact pins that function as signal transmission pins are electrically connected by their respective conduction path. The first through third substrates 210 to 230 are integrally fixed to the body 8 using fixing fittings 83, and relative movement of the first through third substrates 210 to 230 with respect to the body 8 is prevented by the fixing fittings 83.

The body 8 has a guide part or guide wall 81 for arranging an IC device (not shown on the drawings) on a specific position on the top surface 210a of the first substrate 210, and also has a positioning part (in this embodiment, positioning pins 82 illustrated in FIG. 2) for positioning the pin holder 1 on a specific position on a device for operating the IC device, for example an inspection device (not shown on the drawings) for inspecting the IC device. When necessary, the body 8 is mounted on the pin holder 1. Also, the first through third boards 210 to 230 may have a hole or notch for positioning in cooperation with positioning means.

Also, in order to accurately position the IC device with respect to the pin holder 1, a positioning device may be used separate from the pin holder 1. In this case the body 8 may be omitted.

FIG. 3 is a plan view illustrating an example of first arrangement pattern of the first conductive contact pins 4 disposed on the top surface 210a of the first substrate 210. Also, FIG. 4 is a plan view illustrating an example of second arrangement pattern of the second conductive contact pins 6 disposed on the bottom surface 220b of the second substrate 220.

As illustrated in FIG. 3, a plurality of holes is provided in the top surface 210a of the first substrate 210 so as to electrically connect the plurality of first conductive contact pins 4 and the terminals of the IC device installed on the pin holder 1. Each of the plurality of first conductive contact pins 4 is inserted into their corresponding holes, so that the plurality of first conductive contact pins 4 form the first arrangement pattern PA1a. In FIG. 3, an example wherein the first arrangement pattern PA1a of the first conductive contact pins 4 is a 6x6 rectangular array pattern is illustrated. Also, 821a through 821d illustrated in FIG. 3 are through holes through which the fixing fittings 83 pass.

On the other hand, as illustrated in FIG. 4, a plurality of holes is provided in the bottom surface 220b of the second substrate 220 so as to electrically connect the plurality of second conductive contact pins 6 and the terminals of the circuit board on which the pin holder 1 is installed. Each of the plurality of second conductive contact pins 6 is inserted into their corresponding holes, so that the plurality of second conductive contact pins 6 form the second arrangement pattern PA1b which is different from the first arrangement pattern PA1a. In FIG. 4, an example wherein the second arrangement pattern PA1b of the second conductive contact pins 6 is a double 6x3 rectangular array pattern is illustrated. Also, 822a through 822d illustrated in FIG. 4 are through holes through which the fixing fittings 83 pass.

In the examples illustrated in FIG. 3 and FIG. 4, the pitch between the pins in the longitudinal and lateral directions of the first and second arrangement patterns PA1a, PA1b are the same, but the pin

arrangements are different. The pitch between pins in the longitudinal and lateral directions may also be different. Also, the first and second arrangement patterns may be geometrically similar but with a different pitch between pins (FIG. 8 and FIG. 9 as described later). In addition, the number of pins constituting the pattern may be different between the first and second arrangement pattern.

5 In this way, in the pin holder 1 according to the present embodiment, the first arrangement pattern PA1a of the first conductive contact pins 4 and the second arrangement pattern PA1b of the second conductive contact pins 6 are different. Also, as illustrated in FIG. 5, each of the first conductive contact pins 4 is electrically connected with a corresponding second conductive contact pin of the second conductive contact pins 6 via the plurality of conduction paths provided in the third substrate 230.

10 Therefore, the pin holder 1 is capable of electrically connecting each of the terminals of the of the circuit board with the corresponding terminals IC device, whose pitch between terminals, arrangement, and number are different from the pitch between terminals, arrangement, and number of the terminals of the circuit board.

FIG. 5 is an expanded view of a cross-section of the main part of the first embodiment of the pin holder illustrated in FIG. 2. In the embodiment illustrated in FIG. 5, the third substrate 230 has a separate construction from that of the first substrate 210 and the second substrate 220.

In FIG. 5, first the first substrate 210 is formed from a base member 2110 made from a dielectric such as glass epoxy resin or the like, having at least one dielectric layer 2111 embedded in the base member 2110 (or a separate dielectric layer may be provided), with conductor layers 2112, 2113 such as copper or the like formed on the top surface and the bottom surface of the dielectric layer 2111. Therefore the dielectric layer 2111 the conductor layers 2112, 2113 formed on both sides thereof work together to constitute a condenser. In other words, the first substrate 210 is made by stacking the materials (part of the base member) that constitute the base member 2110, the conductor layers 2112, 2113, and the dielectric layer 2111. Also, to increase the capacitance of the condenser, preferably the dielectric constant of the dielectric layer 2111 is high, for example, preferably the dielectric layer 2111 is made from a high dielectric material having a dielectric constant greater than the dielectric constant of the base member 2110. For example, Embedded Capacitor Material (ECM) manufactured by 3M may be used as the high dielectric material. ECM is high dielectric material formed in flexible sheet form. This type of board can be manufactured by the methods of manufacturing printed circuit boards. The condenser realized by ECM or the like does not affect the high frequency properties, so it does not have to be provided within the substrate in particular, but this is an effective construction for power supply stability. The material that constitutes the first substrate 210, in other words, the material of the base member 2110 may include paper instead of glass fiber, and may include phenol resin or polyamide resin instead of epoxy resin. Also silver or gold may be used instead of copper as the material of the conductor layers 2112, 2113. The dielectric layers 2111 may include polymer. Preferably the dielectric layer 2111 includes polymer and a plurality of particles, specifically it is manufactured by mixing resin and particles. Preferred resins include

epoxy resin, polyimide resin, poly(vinylidene fluoride) resin, cyanoethyl pullulan resin, benzocyclobutene resin, polynorbornene resin, polytetrafluoroethylene resin, acrylate resin, mixtures thereof. The particles include dielectric (or insulating) particles having a dielectric constant higher than the dielectric constant of the polymer, typical examples of which include barium titanate, barium strontium titanate, titanium oxide, lead zirconium titanate, and mixtures thereof.

The thickness of the dielectric layer 2111 may be, for example, greater than or equal to 0.5 micrometers or less than or equal to 100 micrometers. The thinner the thickness the higher the capacitance of the capacitor, so this is preferable, for example the thickness may be less than or equal to 15 micrometers, or less than or equal to 10 micrometers. However, a greater thickness preferable from the point of view of adhesion strength, for example the thickness may be greater than or equal to one micrometer

Also, the higher the relative permittivity of the dielectric layers the better, for example the relative permittivity may be greater than or equal to 10, or greater than or equal to 12. There is no particular upper limit on the relative permittivity, but the relative permittivity may be, for example, less than or equal to 30, or less than or equal to 20, or less than or equal to 16.

Of the conductor layers formed on both sides of the dielectric layer 2111, one conductor layer 2112 is electrically connected to a power supply pin of the IC device socket 100 to constitute a power supply layer, and the other conductor layer 2113 is electrically connected to a ground pin of the IC device socket 100 to constitute a ground (GND) layer. The top surface 210a of the first substrate 210 illustrated in FIG. 5 coincides with the top surface of the base member 2110, and the bottom surface 210b of the first substrate 210 coincides with the bottom surface of the base member 2110. Also, each dielectric layer and the conductor layers formed on both sides thereof are disposed over the whole of the first substrate 210. Therefore, a condenser with an area that is approximately the same as the area of the first substrate 210 can be formed.

The first substrate 210 further includes a plurality of through holes that connect the top surface 210a and the bottom surface 210b, and conductive members 2151 to 2156 are formed on the inside surfaces of the through holes by plating with a metal such as copper, gold, silver, or the like. At least a part of each of the first conductive contact pins 2141 to 2146 are inserted into their corresponding through hole. In the embodiment illustrated in FIG. 5, the first conductive contact pins 2142, 2143, 2145 are ground pins, the first conductive contact pins 2141, 2146 are signal transmission pins, and the first conductive contact pin 2144 is a power supply pin.

Each of the conductive contact pins 2141 to 2146 pass through the first substrate 210 from the top surface 210a towards the bottom surface 210b. In detail, the first conductive contact pins 2142, 2143, 2145 which are ground pins are press fit into their corresponding through holes while contacting the conductive members 2152, 2153, 2155, and in this way each ground pin is supported by the first substrate 210. Also, the conductive members 2152, 2153, 2155 electrically contact the conductive layer 2113,

which is the ground layer. The first conductive contact pin 2144 which is the power supply pin is press fit into the corresponding through hole while contacting the conductive members 2154, and in this way the power supply pin is supported by the first substrate 210. The conductive member 2154 electrically contacts the conductive layer 2112, which is the power supply layer.

5 On the other hand, the first conductive contact pins 2141, 2146, which are signal transmission pins, are inserted into their corresponding through holes without contacting the conductive members 2151, 2156. In other words, the aperture diameter of the through holes corresponding to the pin body diameter d of the first conductive contact pins 2141, 2146 is set to D ($D > d$), to constitute a coaxial wiring path within the first substrate 210. The conductive members 2151, 2156 that are a constant distance from
10 the first conductive contact pins 2141, 2146 are electrically connected to the conductive layer 2113, which is the ground layer. Also, in this patent specification, "coaxial wiring path" means the state in which the first conductive contact pins 2141, 2146 and the conductive members 2151, 2156 do not contact and are mutually insulated from each other, and the pin bodies are covered with an electrically conductive material (electromagnetically shielded), and does not only mean the case where the conductive
15 contact pin and the conductive members are cylindrical and coaxial. Therefore, the outer surface of the conductive contact pin and the inner surface of the conductive member may be cylindrical surfaces that are eccentric to each other.

Plate shaped protective members 2121, 2122 are provided on or above the top surface 210a and the bottom surface 210b of the first substrate 210. The plate shaped protective members 2121, 2122 each
20 have through holes provided corresponding to the first conductive contact pins 2141 through 2146, and the diameter of each of these through holes is smaller than the diameter d of the pin bodies. The first conductive contact pins 2141 through 2146 are securely retained in the first substrate 210 by inserting plunger tips into the corresponding through holes of the plate shaped protective members. The plate shaped protective members 2121, 2122 have the function of preventing the first conductive contact pins
25 2141 through 2146 from falling out, as well as controlling the amount of displacement (oscillation) of the plunger tips of the first conductive contact pins 2141 through 2146 in directions approximately normal to the axial direction of the first conductive contact pins 2141 through 2146.

In addition, the first base member 2110 has layer shaped grounded conductors 2131, 2132 for grounding on or above the surfaces thereof (the surfaces corresponding to the top surface 210a and
30 bottom surface 210b of the first substrate 210) near the plungers of the first conductive contact pins 2141, 2146, which are signal pins. Each ground conductor layer is electrically connected to the conduction members 2152, 2153, 2155 (plating layer provided on the inside surface of the through holes into which the ground pins are inserted) which are connected to the first conductive contact pins 2142, 2143, 2145 which are the ground pins, and are not electrically connected to the first conductive contact pins 2141,
35 2146 which are signal transmission pins. In this way, a conductor layer at the same voltage as the ground layer is disposed near the plunger, which has a diameter smaller than that of the pin body, so it is possible

to compensate for the inductance component of the tip of the plunger, and reduce insertion losses and near end crosstalk of the signal pins. Also, providing a ground conductor layer on the surface layer of the base member 2110 can be achieved by a normal multi-layer substrate manufacturing process, and a larger capacitance component can be obtained than providing the ground conductor layer as an internal layer of the base member 2110. In FIG. 5, for clarity the conductor layers 2131, 2132 for grounding and the plate shaped protective members 2121, 2122 are illustrated as separated, but the two may contact.

Next, the construction of the signal transmission pins (first conductive contact pins 2141, 2122) that constitute the coaxial wiring path in the first substrate 210 is explained in detail. In other words, in the first substrate 210 as illustrated in FIG. 5, the first conductive contact pins 2142, 2143, 2145 are ground pins, the first conductive contact pins 2141, 2146 are signal transmission pins, and the first conductive contact pin 2144 is the power supply pin.

Each of the first conductive contact pins extend approximately vertically from the top surface 210a to the bottom surface 210b of the first surface 210 penetrating the first substrate 210. In particular, the first conductive contact pins 2141, 2146, which are signal transmission pins, do not contact the corresponding conductive members 2151, 2156 when inserted into the corresponding through holes, but are isolated. As a result of this construction, the first conductive contact pins 2141, 2146 and their corresponding conductive members 2151, 2156 co-operate to constitute coaxial conduction paths. A dielectric material such as resin or ceramic or the like may be disposed or filled between the signal transmission pins and their corresponding conductive members. Alternatively, instead of filling the space between the outer surface of the pin bodies and the inner surfaces of the conductive members with dielectric or the like, a gaseous phase such as air, nitrogen, oxygen, or the like may be used, or a vacuum may be used.

The coaxial wiring paths are constituted to have a predetermined characteristic impedance. For example, when the pin bodies of the first conductive contact pins 2141, 2146 are cylinders of diameter d , the corresponding conductive members 2151, 2156 are hollow cylinders with internal diameter D , and the two cylinders are coaxial, the characteristic impedance Z_0 of the coaxial wiring path is given by the following equation. Where ϵ is the dielectric constant of the dielectric material (in the present embodiment, dielectric material or air) between the conductive contact pin and the conductive member. By selecting D , d , and ϵ as appropriate, it is possible to obtain the required characteristic impedance for each signal transmission pin.

$$Z_0 = 60/\epsilon^{1/2} \cdot \ln(D/d)$$

As illustrated in FIG. 5, in the first substrate 210, the conductive members 2151, 2156 are electrically connected to the conductor layer 2113, which is the ground layer, disposed within the base member 2110. In the example in FIG. 5, the conductor layer 2113 is a conductor in layer form disposed within the base member 2110, and each of the conductive members, except the conductive member 2154 that is in contact with the first conductive pin 2144 which is the power supply pin, are electrically

connected together via the conductor layer 2113. However, the construction of the connection portion for grounding the conductive members 2151, 2156 is not limited to the example in FIG. 5, but, for example, a wiring construction may also be used.

The first substrate 210 may be formed as substantially integral, but it may be manufactured by assembling several members, taking into consideration the ease of assembly of the first conductive contact pins and arrangement of the ground layer (or wiring), and so on. For example, to dispose the ground layer (conductor layer 2113) in layer form within the substrate 210, the base member 2110 in plate form may be formed from a plurality of layers stacked in the thickness direction, with the conductor layer sandwiched between layers. In addition, taking into consideration the formation of conductive members (for example coating) on the inner surfaces of the through holes into which the first conductive contact pins are inserted, the thickness of the base member 2110 can be made approximately equal to the length of the pin bodies of each of the first conductive contact pins 4, and after forming the conductive members on the inner surfaces of the through holes, the plate shaped protective members 2121, 2122 can be bonded to the base member 2110.

As in the embodiment illustrated in FIG. 5, in the case of a substrate with the pin bodies of the signal transmission pins in a coaxial construction, the characteristic impedance Z_0 of the pin bodies can be defined by the above equation, but conventionally the plunger was not surrounded by the ground conductor, so it behaved as an inductance. Therefore, by disposing the ground conductor layer near the plunger, as in the embodiment in FIG. 5, and adding a capacitance component to the ground, the plunger inductance component is compensated for, and the properties are improved. In more detail, if the plunger inductance value is L_0 , if there is a capacitance component between the plunger and the ground that satisfies $Z_0 = (L_0/C_0)^{1/2}$, where C_0 is the capacitance component, the difference between the plunger characteristic inductance and the pin body characteristic inductance is within a predetermined error, and it is possible to compensate for the degradation in the high frequency properties. At the same time, it is possible to reduce crosstalk between adjacent signal transmission pins as a result of the existence of the electrical connection between the signal transmission pins and the ground pins.

In other words, the second substrate 220 is formed from a base member 2210 having a top surface 220a in opposition to the bottom surface 210b, and a bottom surface 220b in opposition to the top surface 220a, made from a dielectric such as glass epoxy resin or the like, having at least one dielectric layer 2211 embedded in the base member 2210 (or a separate dielectric layer may be provided), with conductor layers 2212, 2213 such as copper or the like formed on the top surface and the bottom surface of the dielectric layer 2211. One conductor layer 2212 is electrically connected to a power supply pin of the IC device socket 100 to constitute a power supply layer, and the other conductor layer 2213 is electrically connected to a ground pin of the IC device socket 100 to constitute a ground (GND) layer. Also, a plurality of holes is formed in the base member 2210, so that the second conductive contact pins 6 form

the second arrangement pattern PA1b when inserted, and conductive members 2251 to 2256 made from copper, gold, silver, or the like, are provided on the inside surface of the through holes.

In the second substrate 220, of the second conductive contact pins 6 inserted into their corresponding through holes, the second conductive contact pins 2242, 2243, 2245 are ground pins, the second conductive contact pins 2241, 2244 are signal transmission pins having the coaxial construction as described above, and the second conductive contact pin 2246 is the power supply pin.

Plate shaped protective members 2221, 2222 are provided on or above the top surface 220a and the bottom surface 220b of the second substrate 220. In addition, the base member 2210 has layer shaped grounded conductors (ground conductor layers) 2231, 2232 for grounding on or above the surfaces thereof (the surfaces corresponding to the top surface 220a and bottom surface 220b of the second substrate 220) near the plungers of the second conductive contact pins 2241, 2244 which are signal pins. In FIG. 5, for clarity the conductor layers 2231, 2232 for grounding and the plate shaped protective members 2221, 2222 are illustrated as separated, but the two may contact.

Next, the third substrate 230 as illustrated in FIG. 5 is disposed between the first substrate 210 and the second substrate 220. In other words, the third substrate 230 has a top surface 230a in opposition to the bottom surface 210b of the first surface 210, and a bottom surface 230b in opposition to the top surface 220a of the second substrate 220. In addition, the third substrate 230 is formed from a base member 2310 made from a dielectric such as glass epoxy resin or the like, having two dielectric layers 2311, 2314 embedded in the base member 2310, with conductor layers 2312, 2313 such as copper or the like formed on the top surface and the bottom surface of the dielectric layer 2311. Also, conductor layers 2315, 2316 such as copper or the like are formed on the top surface and the bottom surface of the dielectric layer 2314.

Of the conductor layers formed on both sides of the dielectric layer 2311, one conductor layer 2312 is electrically connected to a power supply pin of the IC device socket 100 to constitute a power supply layer, and the other conductor layer 2313 is electrically connected to a ground pin of the IC device socket 100 to constitute a ground (GND) layer. Also, of the conductor layers formed on both sides of the dielectric layer 2314, one conductor layer 2315 is electrically connected to a power supply pin of the IC device socket 100 to constitute a power supply layer, and the other conductor layer 2316 is electrically connected to a ground pin of the IC device socket 100 to constitute a ground (GND) layer. Also, the top surface 230a of the third substrate 230 illustrated in FIG. 5 coincides with the top surface of the base member 2310, and the bottom surface 230b of the third substrate 230 coincides with the bottom surface of the base member 2310. Each dielectric layer and the conductor layers formed on both sides thereof are disposed over the whole surface of the third substrate 230. Therefore, condensers with an area that is approximately the same as the area of the third substrate 230 can be formed. The materials used in the construction of the third substrate 230 are the same as those for the first and second substrates 210, 220 as described above.

The third substrate 230 also has a plurality of conduction paths that electrically connect pins of the first conductive contact pins 4 and the second conductive contact pins 6 that have the same function. These conduction paths include at least a group arranged to coincide with the first arrangement pattern PA1a (FIG. 3) and a group arranged to coincide with the second arrangement pattern PA1b (FIG. 4).

Specifically the conduction paths formed in the third substrate 230 include conduction paths for electrically connecting ground pins, a conduction path for electrically connecting power supply pins, and conduction paths for electrically connecting signal transmission pins.

In more detail, the conduction paths formed in the third substrate 230 include vertical connective elements that connect the top surface 230a and the bottom surface 230b, and horizontal connective elements that connect between vertical connective elements along directions normal to the direction from the top surface 230a to the bottom surface 230b. Of the connective elements, the vertical connective elements 2361 to 2366 are connective elements for electrically connecting ground pins, that electrically connect the conductor layers 2313, 2316 (horizontal connective elements for grounding) which are ground layers. The vertical connective elements 2371 to 2372 are connective elements for electrically connecting power supply pins, that electrically connect the conductor layers 2312, 2315 (horizontal connective elements for power supply) which are power supply layers. The vertical connective elements 2381 to 2384 are connective elements for electrically connecting signal transmission pins, that are insulated from and do not contact any of the ground layers 2312, 2316 and the power supply layers 2312, 2315.

In the example of FIG. 5, the vertical connective element 2361 has a contact pad 2361a on the top surface 230a and a contact pad 2361b on the bottom surface 230b, and is electrically connected to the second conductive contact pin 2242, which is a ground pin, via the contact pad 2361b. The vertical connective element 2362 has a contact pad 2362a on the top surface 230a and a contact pad 2362b on the bottom surface 230b, and is electrically connected to the second conductive contact pin 2243, which is a ground pin, via the contact pad 2362b. The vertical connective element 2363 has a contact pad 2363a on the top surface 230a and a contact pad 2363b on the bottom surface 230b, and is electrically connected to the first conductive contact pin 2142, which is a ground pin, via the contact pad 2363a. The vertical connective element 2364 has a contact pad 2364a on the top surface 230a and a contact pad 2364b on the bottom surface 230b, and is electrically connected to the first conductive contact pin 2143, which is a ground pin, via the contact pad 2364a. The vertical connective element 2365 has a contact pad 2365a on the top surface 230a and a contact pad 2365b on the bottom surface 230b, and is electrically connected to the first conductive contact pin 2145, which is a ground pin, via the contact pad 2365a. The vertical connective element 2366 has a contact pad 2366a on the top surface 230a and a contact pad 2366b on the bottom surface 230b, and is electrically connected to the second conductive contact pin 2245, which is a ground pin, via the contact pad 2366b. Each of the vertical connective element 2361 to 2366 are electrically connected via the ground layers 2313, 2316, which are horizontal connective elements, and as

a result, the first conductive contact pins 2142, 2143, 2145 and the second conductive contact pins 2242, 2243, 2245, which are ground pins, are electrically connected.

The vertical connective element 2371 has a contact pad 2371a on the top surface 230a and a contact pad 2371b on the bottom surface 230b, and is electrically connected to the first conductive contact pin 2144, which is a power supply pin, via the contact pad 2371a. The vertical connective element 2372 has a contact pad 2372a on the top surface 230a and a contact pad 2372b on the bottom surface 230b, and is electrically connected to the second conductive contact pin 2246, which is a power supply pin, via the contact pad 2372a. The vertical connective elements 2371, 2372 are electrically connected to the ground layers 2312, 2315, which are horizontal connective elements, so the first conductive contact pin 2144 and the second conductive contact pin 2246, which are power supply pins, are electrically connected.

In addition, the vertical connective element 2381 is a conductive member that connects the top surface 230a and the bottom surface 230b and is provided on the inside surface of a through hole, and on the top surface 230a side, a drilled hole 2381a is formed by removing a part of the conductive member with a drill. Also, the vertical connective element 2381 has a contact pad 2381b on the bottom surface 230b, and is electrically connected to the second conductive contact pin 2241, which is a signal transmission pin, via the contact pad 2381b. The vertical connective element 2382 is a conductive member that connects the top surface 230a and the bottom surface 230b and is provided on the inside surface of a through hole, and on the bottom surface 230b side, a drilled hole 2382b is formed by removing a part of the conductive member with a drill. Also, the vertical connective element 2382 has a contact pad 2382a on the top surface 230a and is electrically connected to the first conductive contact pin 2141, which is a signal transmission pin, via the contact pad 2382a. The vertical connective element 2383 is a conductive member that connects the top surface 230a and the bottom surface 230b and is provided on the inside surface of a through hole, and on the bottom surface 230b side, a drilled hole 2383b is formed by removing a part of the conductive member with a drill. Also, the vertical connective element 2383 has a contact pad 2383a on the top surface 230a and is electrically connected to the first conductive contact pin 2146, which is a signal transmission pin, via the contact pad 2383a. The vertical connective element 2384 is a conductive member that connects the top surface 230a and the bottom surface 230b and is provided on the inside surface of a through hole, and on the top surface 230a side, a drilled hole 2384a is formed by removing a part of the conductive member with a drill. Also, the vertical connective element 2384 has a contact pad 2384b on the bottom surface 230b, and is electrically connected to the second conductive contact pin 2244, which is a signal transmission pin, via the contact pad 2384b. The vertical connective element 2381 and the vertical connective element 2382 are electrically connected by the horizontal connective element 2391. Also, the vertical connective element 2383 and the vertical connective element 2384 are electrically connected by the horizontal connective element 2392. FIG. 6 explains the horizontal construction of the horizontal connective elements 2391, 2392, the line L in FIG. 6 coincides with the cross-section illustrated in FIG. 5.

In particular, the horizontal connective elements 2391, 2392 are disposed in spaces that are sandwiched between the ground layers 2313, 2316 with insulating material (a part of the base member 2310) therebetween, and a strip line construction is realized by this construction. One of the dielectric layers provided in the third substrate 230 and the conductor layers formed on both sides thereof may be omitted. In this case, a microstrip line construction is realized by the horizontal connective elements 2391, 2392 and one of the ground layers (2313 or 2316).

The conductor layers 2313, 2316, which are ground layers, are electrically connected to the first conductive contact pins 2142, 2143, 2145, which are the ground pins of the first conductive contact pins 4, and the second conductive contact pins 2242, 2243, which are the ground pins of the second conductive contact pins 6. Preferably each of the conductor layers 2313, 2316 have sufficient area to sandwich the horizontal connective elements 2391, 2392, which constitute conduction paths for electrically connecting signal transmission pins. In the present embodiment, the conductor layers 2313, 2316 are disposed covering the whole horizontal surface of the third substrate 230. However, the conductor layers 2313, 2316 are arranged insulated from the conductive contact pins apart from the ground pins.

In this way, the third substrate 230 includes a part of the conduction path that transmits signals (horizontal connective elements 2391, 2392) and the grounded conductor layers 2313, 2316 located on both sides thereof, so these horizontal connective elements 2391, 2392 function as a strip line. Also, by setting the wire width of the horizontal connective elements 2391, 2392 and the distance between adjacent conductor layers as appropriate in accordance with the conductivity of the conductor wiring and the specific permittivity of the substrate 2, signal reflections between each signal transmission pin and conduction paths within the third substrate 230 that are electrically connected to each signal transmission pin are suppressed to a minimum in respect of the frequencies in the signals supplied to the IC device. In this way, in the third substrate 230, it is possible to minimize transmission losses of high frequency signals due to transmission between signal transmission pins via the signal transmission conduction paths 2381, 2391, 2382 or other signal transmission conduction paths 2383, 2392, 2384.

FIG. 7 explains strip lines, and as illustrated in FIG. 7, and if the width of a conduction path S1 is W, the thickness of the conduction path S1 is t, the distance between conduction layers G1, G2 adjacent to the conduction path S1 with the base member (insulating material) I1 therebetween is h, and the dielectric constant of the base member is ϵ_r , the characteristic impedance Z_0 of the strip line is given by the following Equation (1). Therefore, by adjusting the value of each of the parameters in Equation (1), impedance matching can be carried out in the third substrate 230, and impedance matching between the circuit board and the pin holder 1 may be carried out.

[Equation 1]

In addition, microstrip lines with controlled characteristic impedance may be provided in the third substrate 230 by disposing conduction paths on the surface layers of the third substrate 230. FIG. 8 explains microstrip lines, and as illustrated in FIG. 8, if the width of a conduction path S2 is W, the

thickness of the conduction path S2 is t , the thickness of the base member (insulating material) I2 provided between the conduction path S2 and conductor layer G3 is h , and the dielectric constant of the base member I2 is ϵ_r , the characteristic impedance Z_0 of the microstrip line is given by the following Equation (2). Therefore, by adjusting the value of each of the parameters in Equation (2), impedance matching can be carried out in the third substrate 230, and impedance matching between the circuit board and the pin holder 1 may be carried out.

[Equation 2]

In the pin holder 1, in the first and second substrates 210, 220, the signal transmission pins 2141, 2146, 2241, 2244 have the coaxial construction described above, and in the third substrate 230 the signal impedance is controlled by the strip lines (or microstrip lines) 2391, 2392 as signal transmission conduction paths, so it is possible to match the output impedance of the IC device, such as an LSI or the like, and the characteristic impedance of the circuit board using the pin holder 1. The impedance of the third substrate 230 may be matched with the impedance of one of the IC device and the circuit board to the extent that it is possible to receive a high frequency signal transmitted from one to the other, and the impedance of the third substrate 230 of the pin holder 1, in particular the impedance of the conduction paths, is not limited to complete matching with the impedance of the IC device and the circuit board.

Also, the signal transmission conduction paths formed in the third substrate 230 (in the example in FIG. 5, the signal path constituted by the connective elements 2381, 2391, 2382, and the signal path constituted by the connective elements 2382, 2392, 2384) are constructed as illustrated in FIG. 9. FIG. 9 illustrates an example of the three-dimensional construction of the conduction path within the third substrate 230 that electrically connects the signal transmission pin 2141 of the first conductive contact pins 4 and the signal transmission pin 2241 of the second conductive contact pins 6. As illustrated in FIG. 9, the vertical connective elements 2381, 2382 are conductive members provided on the inside surface of through holes connecting the top surface 230a and the bottom surface 230b of the third substrate 230, so normally a part of the top side of the vertical connective element 2381 and a part of the bottom side of the vertical connective element 2382 are unnecessary conduction paths for the horizontal connective element (strip line 2391), and they function as stubs. Therefore, in the example in FIG. 5, these unnecessary portions are removed by drilling, and the drilled holes 2381a, 2382b are formed.

As explained above, the IC device socket 100 according to the present embodiment can electrically connect each terminal of the circuit board and the corresponding terminals of the IC device, which has a pitch and arrangement of terminals that is different from the pitch and arrangement of terminals of the circuit board. Also, in the IC device socket 100, the signal transmission pins are electrically connected via the conduction paths that are constituted to match the impedance of the conductive contact pins (signal transmission pins) connected to the signal terminals of the IC device and the impedance of the conductive contact pins (signal transmission pins) that are connected to the signal terminals of the circuit board, with respect to the frequencies of the signals supplied to the IC device.

Therefore the IC device socket 100 can reduce the transmission losses of the signals transmitted between the IC device and the circuit board.

(Construction of the Conductive Contact Pins)

In the embodiment as described above, the conductive contact pins that are used may have a so-called spring probe construction. For example, FIG. 10 is a cross-sectional view illustrating an example of conductive contact pin 4, 6 that can be applied to each embodiment of the present invention, and a side cross-sectional view of a conductive contact pin 400 is illustrated as an example that corresponds to the conductive contact pins 4, 6.

The conductive contact pin 400 includes an approximately cylindrical shaped pin body 401 that is inserted into the substrate, a first contact part 402 that projects from one end (the bottom end in the example illustrated in the drawing) of the pin body 401 and that can contact a bottom surface of a hole formed in a substrate or a terminal of another substrate of a circuit board or the like via the through hole formed in the substrate, and a second contact part 403 that projects from the other end (the top end in the example illustrated in the drawing) of the pin body 401 and that can contact a top surface of a hole formed in a substrate or a terminal of an IC device or the like via the through hole formed in the substrate. The pin body 401 and each of the contact parts 402, 403 are made from an electrically conductive material. The internal diameter of the top end and bottom end of the pin body 401 is narrower than the internal diameter of the center part of the pin body 401. Also, a flange is formed in the side surface of each contact part 402, 403 that contacts the bottom end or top end of the pin body 401 from the inside and that prevents each contact part 402, 403 from falling out from the pin body 401.

An elastic member having electrical conductivity such as a metal spring 404 is provided within the pin body 401. The spring 404 impels the two contact parts 402, 403 towards the bottom end or the top end of the pin body 401 so that each contact part 402, 403 can move in the axial direction of the pin body 401. Therefore, when one end of the contact pin 400 presses against a terminal of an IC device or the like along the axial direction, a force acts on the contact parts 402, 403 in the opposite direction to the direction of pressing, so there is sound contact between the contact parts 402, 403 and the terminal. Therefore the conductive contact pin 400 is soundly connected electrically to the terminal or the like that is contacted by the contact part 402 or 403.

Also, FIG. 11 is a cross-sectional view illustrating another example of conductive contact pin 4, 6 that can be applied to each embodiment of the present invention, and a side cross-sectional view of a conductive contact pin 410 is illustrated as an example that corresponds to the conductive contact pins 4, 6.

The conductive contact pin 410 includes an approximately cylindrically shaped pin body 411 formed from an electrically conductive metal, that is inserted into a hole or through hole formed in the substrate, a long and narrow pin shaped plunger 412, and a coil shaped spring 413. Both the plunger 412

and the coil shaped spring 413 are made from an electrically conducting metal, and are housed within the pin body 411.

The pin body 411 includes a first portion 411a that is open on the bottom side, a second portion 411c that is collinear with the first portion, and a tapering portion 411b that connects the first portion 411a and the second portion 411c and whose internal diameter varies progressively in the direction of extension of the pin body 411. The internal diameter of the first portion 411a near the bottom opening (for example, the bottom surface of a hole or the opening of a through hole that is in opposition to a circuit board) of the pin body 411 is smaller than the internal diameter of the second portion 411c that is the center portion of the pin body 411. The pin body 411 has a third portion 411d above the second portion 411c, that is connected to the second portion 411c and has an internal diameter that is narrower than that of the second portion 411c, and an opening is formed on the top surface of the third portion 411d.

The coil shaped spring 413 housed within the pin body 411 includes an upper portion 413a that is housed in the second portion 411c of the pin body 411, and a lower portion 413b that is connected to the upper portion 413a. The upper portion 413a has elasticity and can be compressed in the axial direction of the upper portion 413a, in other words, in the direction of extension of the pin body 411. Also, the external diameter of the upper portion 413a is approximately the same as or smaller than the internal diameter of the second portion 411c of the pin body 411. The lower portion 413b is formed continuous with the upper portion 413a, and in the lower portion 413b the spring is wound more densely than in the upper portion 413a. Also, the external diameter of the lower portion 413b is smaller than that of the upper portion 413a, and is approximately the same as or smaller than the internal diameter of the first portion 411a of the pin body 411. Therefore, the diameter of the upper portion of the coil shaped spring 413 (in other words, the portion located within the second portion 411c of the pin body 411) is larger than the internal diameter of the first portion 411a of the pin body 411. As a result, the pin body 411 can prevent the coil shaped spring 413 from falling out of the pin body 411. In addition, the upper portion 413a of the coil shaped spring 413 has a length that is approximately the same as the length of the second portion 411c of the pin body 411. On the other hand, the length of the lower portion 413b of the coil shaped spring 413 is longer than the length of the first portion 411a of the pin body 411. Therefore, the lower portion 413b of the coil shaped spring 413 that is inserted into the pin body 411 projects from the bottom opening of the pin body 411, and the bottom end of the coil shaped spring 413 contacts a terminal or the bottom of a hole of a substrate, so that they are electrically connected. Also, the plunger 412, which is described later, is constantly impelled upwards by the coil shaped spring 413.

The lower portion 413b of the coil shaped spring 413 is constructed so that in the free state of the coil shaped spring 413 (the state when it is not compressed), adjacent turns of the spring contact each other. Therefore, at the lower portion 413b of the coil shaped spring 413, the cross-sectional area of the conduction path formed by the coil shaped spring 413 and the pin body 411 is increased, so it is possible

to reduce the resistance to conduction of the conduction path. Also, the conduction path is not coil shaped, but can be formed as linear shaped approximately parallel to the direction of extension of the coil shaped spring 413. Therefore, even when a high frequency signal is applied to the contact pin, it is possible to reduce the inductance generated at this portion. In the present embodiment, the upper portion 413a and the lower portion 413b are constituted by varying the external diameter and the winding pitch of a single spring. Therefore it is possible to reduce the number of components and manufacture the elastic member at low cost.

Also, the conductive contact pin 410 may be constructed so that in the free state of the coil shaped spring the adjacent windings of the spring do not contact each other, and when the IC device or circuit board compress the coil shaped spring installed in the pin holder, the adjacent windings of the lower portion of the spring do contact. In the case where the lower portion of the coil shaped spring is constructed so that the adjacent windings of the spring contact in advance, a conduction path approximately parallel to the direction of extension of the coil shaped spring is formed regardless of the amount of compression of the coil shaped spring, so it is possible to more reliably reduce the conduction path.

On the other hand, in the second portion 411c of the pin body 411, the coil shaped spring 413 is not densely wound, so the coil shaped spring 413 has elasticity along the longitudinal direction of the pin body 411.

In the present embodiment, the elastic member is constituted from a single coil shaped spring, but the elastic member may be constituted in another form. For example, two coil shaped springs with different external diameters or spring constants may be inserted in series into the pin body 411. Also, these coil shaped springs may be integrated.

Alternatively, the lower portion of the coil shaped spring may be constructed from a metal sleeve or metal rod. The metal sleeve or metal rod may be joined to the upper portion of the coil shaped spring near the top end of the metal sleeve or metal rod using a commonly known method. For example, a method of mechanically engaging the two or a method of bonding with an electrically conductive adhesive may be adopted as the joining method. In addition, the upper portion of the coil shaped spring may be an electrically conductive elastic member, and the upper portion may be constituted from, for example, an electrically conductive elastomer, an air spring made from an electrically conductive material, or a leaf spring that can compress in the direction of extension of the pin body 411, and so on.

The plunger 412 housed in the pin body 411 is a conductor that is electrically connected to a terminal of the IC device or the top surface of a hole formed in the substrate, and the coil shaped spring 413 and the pin body 411.

The top end of the plunger 412 projects from the opening in the top of the pin body 411 so as to securely contact a terminal of the IC device or a conductor provided in the top surface of a hole formed in

the substrate. On the other hand, the bottom end of the plunger 412 is inserted into the interior of the coil shaped spring 413. A flange 412a is formed in approximately the center in the longitudinal direction of the plunger 412 having a diameter that is larger than that of the other portions of the plunger 412. The bottom end of the flange 412a butts against the top end of the coil shaped spring 413. Therefore, when the plunger 412 is pressed by a terminal of the IC device or the like, the plunger 412 moves downward, and the plunger 412 compresses the coil shaped spring 413 along the longitudinal direction of the pin body 411. In this way, the plunger 412 and the coil shaped spring contact soundly, and it is possible to prevent poor contact between the plunger 412 and the coil shaped spring 413. Also, the contact area between the plunger 412 and coil shaped spring 413 and pin body 411 increases, so it is possible to reduce the resistance of the conduction path from the plunger 412 and coil shaped spring 413 via the pin body 411.

Preferably the length of the plunger 412 is designed so that even when the plunger 412 is moved to the bottom end of its range of motion, the bottom end of the plunger 412 is contained within the large internal diameter portion (in other words, the second portion 411c) of the pin body 411. By setting the length of the plunger 412 in this way, when the IC device or circuit board is removed from the pin holder, it is possible to prevent the bottom end of the plunger 412 from becoming sandwiched in the narrow diameter portion of the coil shaped spring 413 and not being able to withdraw.

Also, when the coil shaped spring 413 is in the compressed state, preferably the bottom end portion of the plunger 412 contacts the sparsely wound portion of the coil shaped spring 413. When the plunger 412 contacts the inner peripheral surface of the coil shaped spring 413 and the coil shaped spring 413 bends, the plunger 412 is pressed back by the elastic reaction force. When this elastic reaction force is large, the friction between the coil shaped spring 413 and the plunger 412 becomes large, and there is a danger that the movement of the plunger 412 in the vertical direction could be hindered. The stiffness of the sparsely wound portion of the coil shaped spring 413 is lower than the stiffness of the densely wound portion. Therefore, when the bottom end portion of the plunger 412 contacts the coil shaped spring, the contacted portion of the coil spring is sparsely wound, so the elastic reaction force acting on the plunger 412 is small, and as a result the plunger 412 can smoothly move in the vertical direction.

In addition, preferably the densely wound portion of the coil spring 413 is short, so that the upper portion 413a of the coil spring 413 is substantially constituted from the sparsely wound portion only.

The shorter the densely wound portion of the coil spring 413, the longer the dimension of the sparsely wound portion of the coil spring 413, or the portion that can exhibit elasticity in the longitudinal direction, can be. Therefore, the shorter the densely wound portion of the coil spring 413, the longer the amount of movement of the plunger 412 can be made. In addition, when the amount of movement of the plunger 412 is increased, it is possible to reduce the spring constant of the sparsely wound portion. Therefore, even when the positions of the terminals of the IC device that contact the plurality of conductive contact pins 410 retained in the pin holder differ in the height direction (the axial direction of

the conductive contact pins 410), the variation of the contact pressure between the plunger 412 and IC device terminal is small between each conductive contact pin, so a stable contact state can be obtained.

The internal diameter of the pin body 411 is narrow near the top opening. This narrow portion engages with the top end of the flange 412a of the plunger 412, and determines the top end of the range of movement of the plunger 412.

According to another embodiment, the inside shape of each hole formed in the substrate of the pin holder may be formed to the same shape as the inside shape of the pin body 411 of the conductive contact pin 410 illustrated in FIG. 11. Then a conductor is formed inside each hole, and the plunger 412 and coil spring 413 of the conductive contact pin 410 illustrated in FIG. 11 may be disposed as illustrated in FIG. 11. In this case, the plunger 412 and the coil spring 413 constitute the conductive contact pin.

As described above, a person skilled in the art to which the present invention pertains can make various modifications within the scope of the present invention in accordance with the form of implementation.

(Modified Example of Arrangement Pattern)

FIG. 12 is a plan view illustrating another example of first arrangement pattern of the first conductive contact pins 4. Also, FIG. 13 is a plan view illustrating another example of second arrangement pattern of the second conductive contact pins 6.

As illustrated in FIG. 12, a plurality of holes is provided in the top surface 310a of a first substrate 310 to electrically connect the plurality of first conductive contact pins 4 and the terminals of the IC device installed on the pin holder. Each of the plurality of first conductive contact pins 4 is inserted into their corresponding holes, so that the plurality of first conductive contact pins 4 form a first arrangement pattern PA2a. In FIG. 12, an example wherein the first arrangement pattern PA2a of the first conductive contact pins 4 is a 6x6 rectangular array pattern with pitch P1 is illustrated. Also, 823a through 823d illustrated in FIG. 12 are through holes through which the fixing fittings 83 (FIG. 2) pass.

On the other hand, as illustrated in FIG. 13, a plurality of holes is provided in the bottom surface 320b of the second substrate 230 to electrically connect the plurality of second conductive contact pins 6 and the terminals of the circuit board installed on the pin holder. Each of the plurality of second conductive contact pins 6 is inserted into their corresponding holes, so that the plurality of second conductive contact pins 6 form the second arrangement pattern PA2b which is different from the first arrangement pattern PA2a. In FIG. 13, an example wherein the second arrangement pattern PA2b of the second conductive contact pins 6 is also a 6x6 rectangular array pattern is illustrated, but the pitch between conductive contact pins P2 (>P1) is different from that of the first arrangement pattern PA2a.. Also, 824a through 824d illustrated in FIG. 13 are through holes through which the fixing fittings 83 (FIG. 2) pass.

In the examples illustrated in FIG. 12 and FIG. 13, the first and second arrangement patterns PA2a, PA2b are geometrically similar with different pitch in the longitudinal and lateral directions. The

first and second arrangement patterns may differ not only in pitch and arrangement, but also in numbers of pins.

(Second Embodiment)

FIG. 14 is an enlarged cross-sectional view of the main part of a pin holder 1A according to the second embodiment of the IC device socket 100 according to the present invention. The pin holder 1A according to the embodiment illustrated in FIG. 14 also constitutes a part of the IC device socket 100 as illustrated in FIG. 1 and FIG. 2, the same as for the embodiment in FIG. 5. However, the pin holder 1A according to the present embodiment includes a first substrate 410, a second substrate 420, and a third substrate 430, but differs from the embodiment of FIG. 5 in that the first substrate 410 and the third substrate 430 are integral, and the second substrate 420 and third substrate 430 are constituted separately. Apart from these points of difference, the construction and materials of each of the substrates 410 to 430 are the same as the embodiment of FIG. 5.

First, the construction of the first substrate 410 as illustrated in FIG. 14 is described in detail. The first substrate 410 has a construction that is integral with that of the third substrate 430 by stacking or bonding onto the third substrate 430, but the first substrate 410 is substantially the same as the first substrate 210 in the embodiment in FIG. 5 in construction and constituent materials.

In other words, the first substrate 410 is formed from a base member 4110 having a top surface 410a in opposition to the IC device (not shown), and a bottom surface 410b in opposition to the top surface 420a, made from a dielectric such as glass epoxy resin or the like, having at least one dielectric layer 4111 embedded in the base member 4110 (or a separate dielectric layer may be provided), with conductor layers 4112, 4113 such as copper or the like formed on the top surface and the bottom surface of the dielectric layer 4111. Also, a plurality of through holes is formed in the base member 4110, so that the first conductive contact pins 4 form the first arrangement pattern PA1b (the pattern PA2a in FIG. 12 may also be used) when inserted, and conductive members 4151 to 4156 made from copper, gold, silver, or the like, are provided on the inside surface of these through holes.

Of the conductor layers formed on both sides of the dielectric layer 4111, one conductor layer 4112 is electrically connected to a power supply pin of the IC device socket 100 to constitute a power supply layer, and the other conductor layer 4113 is electrically connected to a ground pin of the IC device socket 100 to constitute a ground (GND) layer. The top surface 410a of the first substrate 410 illustrated in FIG. 14 coincides with the top surface of the base member 4110, and the bottom surface 410b of the first substrate 410 coincides with the bottom surface of the base member 4110. Additionally, the bottom surface 410b is directly connected to the top surface 430a of the third substrate 430. Each dielectric layer and the conductor layers formed on both sides thereof are disposed over the whole surface of the first substrate 410. Therefore, a condenser with an area that is approximately the same as the area of the first substrate 410 can be formed.

In the first substrate 410, of the first conductive contact pins 4 inserted into their corresponding through holes, the first conductive contact pins 4142, 4143, 4145 are ground pins, the first conductive contact pins 4141, 4146 are signal transmission pins having the coaxial construction as described above, and the first conductive contact pin 4144 is the power supply pin.

5 Each of the conductive contact pins 4141 to 4146 pass through the first substrate 410 from the top surface 410a towards the bottom surface 410b. In detail, the first conductive contact pins 4142, 4143, 4145 which are ground pins are press fit into their corresponding through holes while contacting the conductive members 4152, 4153, 4155, and in this way each ground pin is supported by the first substrate 410. Also, the conductive members 4152, 4153, 4155 electrically contact the conductive layer 4113, 10 which is the ground layer. The first conductive contact pin 4144 which is the power supply pin is press fit into the corresponding through hole while contacting the conductive members 4154, and in this way the power supply pin is supported by the first substrate 410. The conductive member 4154 electrically contacts the conductive layer 4112, which is the power supply layer.

On the other hand, the first conductive contact pins 4141, 4146, which are signal transmission 15 pins, are inserted into their corresponding through holes without contacting the conductive members 4151, 4156. In other words, the aperture diameter of the through holes corresponding to the pin body diameter d of the first conductive contact pins 4141, 4146 is set to D ($D > d$), to constitute a coaxial wiring path within the first substrate 410. The conductive members 4151, 4156 that are a constant distance from the first conductive contact pins 4141, 4146 are electrically connected to the conductive layer 4113, 20 which is the ground layer.

A plate shaped protective member 4121 is provided on or above the top surface 410a of the first substrate 410. The plate shaped protective member 4121 has through holes provided corresponding to the first conductive contact pins 4141 through 4146, and the diameter of each of these through holes is smaller than the diameter d of the pin bodies. The first conductive contact pins 4141 through 4146 are 25 securely retained in the first substrate 410 by inserting plunger tips into the corresponding through holes of the plate shaped protective member 4121.

In addition, the base member 4110 has a layer shaped grounded conductor (ground conductor layer) 4131 for grounding on or above the surface thereof (the surface corresponding to the top surface 410a of the first substrate 410) near the plungers of the first conductive contact pins 4141, 4146, which 30 are signal transmission pins. The ground conductor layer 4131 is electrically connected to the conduction members 4152, 4153, 4155 (plating layer provided on the inside surface of the through holes into which the ground pins are inserted) which are connected to the first conductive contact pins 4142, 4143, 4145 which are the ground pins, and are not electrically connected to the first conductive contact pins 4141, 4146 which are signal transmission pins. In this way, a conductor layer at the same voltage as the ground 35 layer is disposed near the plunger, which has a diameter smaller than that of the pin body, so it is possible to compensate for the inductance component of the tip of the plunger, and reduce insertion losses and

near end crosstalk of the signal pins. Also, providing a ground conductor layer on the surface layer of the base member 4110 can be achieved by a normal multi-layer substrate manufacturing process, and a larger capacitance component can be obtained than providing the ground conductor layer as an internal layer of the base member 4110. In FIG. 14, for clarity the ground conductor layer 4131 and the plate shaped protective member 4121 are illustrated as separated, but the two may contact.

Next, the construction of the second substrate 420 illustrated in FIG. 14 is explained. The construction and materials of the second substrate 420 are substantially the same as those of the second substrate 220, so duplicated explanations are omitted.

In other words, the second substrate 420 is formed from a base member 4210 having a top surface 420a in opposition to the bottom surface 430b of the third substrate 430 that is integrated with the first substrate 410, and a bottom surface 420b in opposition to the top surface 420a, made from a dielectric such as glass epoxy resin or the like, having at least one dielectric layer 4211 embedded in the base member 4210 (or a separate dielectric layer may be provided), with conductor layers 4212, 4213 such as copper or the like formed on the top surface and the bottom surface of the dielectric layer 4211. One conductor layer 4212 is electrically connected to a power supply pin of the IC device socket 100 to constitute a power supply layer, and the other conductor layer 4213 is electrically connected to a ground pin of the IC device socket 100 to constitute a ground (GND) layer. Also, a plurality of through holes is formed in the base member 4210, so that the second conductive contact pins 6 form the second arrangement pattern (the pattern in FIG. 4 or FIG. 13) when inserted, and conductive members 4251 to 4256 made from copper, gold, silver, or the like, are provided on the inside surface of these through holes.

In the second substrate 420, of the second conductive contact pins 6 inserted into their corresponding through holes, the second conductive contact pins 4242, 4243, 4245 are ground pins, the second conductive contact pins 4241, 4244 are signal transmission pins having the coaxial construction as described above, and the second conductive contact pin 4246 is the power supply pin.

Plate shaped protective members 4221, 4222 are provided on or above the top surface 420a and the bottom surface 420b of the second substrate 420. In addition, the second base member 420 has layer shaped ground conductors 4231, 4232 for grounding on or above the surfaces thereof (the surfaces corresponding to the top surface 420a and bottom surface 420b of the second substrate 420) near the plungers of the second conductive contact pins 4241, 4244, which are signal pins. In FIG. 14, for clarity the conductor layers 4231, 4232 for grounding and the plate shaped protective members 4211, 4222 are illustrated as separated, but the two may contact.

Next, the third substrate 430 as illustrated in FIG. 14 is substantially the same as the third substrate 230 of the embodiment of FIG. 5 in construction and constituent materials, apart from the bottom surface 410b of the first substrate 410 as described above being in direct contact with the top surface 430a of the third substrate 430, so duplication of explanations is omitted.

In other words, the third substrate 430 has a top surface 430a in opposition to the bottom surface 410b of the first substrate 410, and a bottom surface 430b in opposition to the top surface 420a of the second substrate 420. In addition, the third substrate 430 is formed from a base member 4310 made from a dielectric such as glass epoxy resin or the like, having two dielectric layers 4311, 4314 embedded in the base member 4310, with conductor layers 4312, 4313 such as copper or the like formed on the top surface and the bottom surface of the dielectric layer 4311. Also, conductor layers 4315, 4316 such as copper or the like are formed on the top surface and the bottom surface of the dielectric layer 4314. Also, each of the conductor layers 4312, 4315 is electrically connected to a power supply pin of the IC device socket 100 to constitute a power supply layer, and each of the conductor layers 4313, 4316 are electrically connected to a ground pin of the IC device socket 100 to constitute a ground (GND) layer.

Vertical connective elements 4381 to 4384 that constitute a part of the signal transmission conduction paths, vertical connective elements 4361 to 4366 that constitute a part of the ground conduction paths, and vertical connective elements 4371 and 4372 that constitute a part of the power supply conduction paths are provided in the third substrate 430. Also, the vertical connective elements 4381, 4382 are electrically connected by a horizontal connective element 4391, and the horizontal connective element 4391 functions as a strip line sandwiched by the conductor layers 4313, 4316 that each constitute ground layers, with the base member 4310 disposed therebetween. Likewise, the vertical connective elements 4383, 4384 are electrically connected by a horizontal connective element 4392, and the horizontal connective element 4392 functions as a strip line sandwiched by the conductor layers 4313, 4316 that each constitute ground layers, with the base member 4310 disposed therebetween.

In the third substrate 430, the vertical connective elements 4381, 4384 have contact pads 4381b, 4384b on the bottom surface 430b that are electrically connected to the conductive contact pins 4241, 4244, which are signal transmission pins. Also, drilled holes 4381a, 4384a are provided on the top surface side of the vertical connective elements 4381, 4384 to avoid stubs in the signal transmission paths by removing a part of the vertical connective elements 4381, 4384. On the other hand, the vertical connective elements 4382, 4383 have contact pads 4382a, 4383a on the top surface 430a that are electrically connected to the conductive contact pins 4141, 4146, which are signal transmission pins. Also, drilled holes 4382b, 4383b are provided on the bottom surface side of the vertical connective elements 4382, 4383 to avoid stubs in the signal transmission paths by removing a part of the vertical connective elements 4382, 4383. The vertical connective elements 4361 to 4366 for grounding have contact pads 4361a to 4366a respectively located on the top surface 430, and contact pads 4361b to 4366b located on the bottom surface 430b. In addition, the vertical connective elements 4371, 4372 for power supply have contact pads 4371a, 4372a respectively located on the top surface 430, and contact pads 4371b to 4372b located on the bottom surface 430b.

In the embodiment as illustrated in FIG. 14 as described above, the third substrate is integrated with the first substrate and constituted separate from the second substrate, but the third substrate may be integrated with the second substrate and constituted separate from the first substrate.

(Third Embodiment)

FIG. 15 is an enlarged cross-sectional view of the main part of a pin holder 1B according to the third embodiment of the IC device socket 100 according to the present invention. The pin holder 1B according to the embodiment illustrated in FIG. 15 also constitutes a part of the IC device socket 100 as illustrated in FIG. 2, the same as for the embodiments in FIG. 5 and FIG. 14. However, the pin holder 1B according to the present embodiment includes a composite substrate 510 that integrates the constructions of the first substrate 210, 410 and the third substrate 230, 430 in each of the embodiments described above, and a second substrate 520. In other words, in FIG. 15, the top half of the composite substrate 510 is the first substrate portion corresponding to the first substrate 210, 410 in the first and second embodiments, and the bottom half of the composite substrate 510 is the third substrate portion corresponding to the third substrate 230, 430 in the first and second embodiments. Therefore, in this patent specification, when referring to the composite substrate 510 of the third embodiment, the first substrate indicates the top half of the composite substrate 510. Also, in this patent specification, when referring to the composite substrate 510 of the third embodiment, the third substrate indicates the bottom half of the composite substrate 510.

First, the composite substrate 510 includes a base member 5110 having a top surface 510a in opposition to an IC device (not shown on the drawings), and a bottom surface 510b in opposition to the second substrate 520, made from a dielectric such as glass epoxy resin or the like, and dielectric layers 5111, 5114 embedded in the base member 5110. Conductor layers 5112, 5113 such as copper or the like are formed on the top surface and the bottom surface of the dielectric layer 5111, and conductor layers 5115, 5116 such as copper or the like are formed on the top surface and the bottom surface of the dielectric layer 5114. Also, a plurality of through holes or holes whose bottom surface is covered in electrically conductive material is formed in the base member 5110, so that the first conductive contact pins 4 form the first arrangement pattern PA1b (the pattern PA2a in FIG. 12 may also be used) when inserted, and conductive members 5151 to 5156 made from copper, gold, silver, or the like, are provided on the inside surface of these holes. In addition, through holes or holes are provided in the base member 5110 so as to form the arrangement pattern of the second conductive contact pins 6 inserted into the second substrate 520, and vertical connective elements 5381, 5361, 5362, 5384, 5363, 5371 are provided on the inside surface of these holes, as conduction paths that electrically connect pins of the first conductive contact pins 4 and the second conductive contact pins 6 that have the same function.

Of the conductor layers formed on both sides of the dielectric layer 5111, one conductor layer 5112 is electrically connected to a power supply pin of the IC device socket 100 to constitute a power supply layer, and the other conductor layer 5113 is electrically connected to a ground pin of the IC device

socket 100 to constitute a ground (GND) layer. Also, of the conductor layers formed on both sides of the dielectric layer 5114, one conductor layer 5115 is electrically connected to a power supply pin of the IC device socket 100 to constitute a power supply layer, and the other conductor layer 5116 is electrically connected to a ground pin of the IC device socket 100 to constitute a ground (GND) layer. The top surface 510a of the composite substrate 510 illustrated in FIG. 15 coincides with the top surface of the base member 5110, and the bottom surface 510b of the composite substrate 510 coincides with the bottom surface of the base member 5110. Also, each dielectric layer and the conductor layers formed on both sides thereof are disposed over the whole of the composite substrate 510. Therefore, condensers with an area that is approximately the same as the area of the composite substrate 510 can be formed.

In the composite substrate 510, of the first conductive contact pins 4 inserted into their corresponding through holes, the first conductive contact pins 5142, 5143, 5145 are ground pins, the first conductive contact pins 5141, 5146 are signal transmission pins, and the first conductive contact pin 5144 is the power supply pin.

The first conductive contact pins 5142, 5143, 5145 which are ground pins are press fit into their corresponding through holes while contacting the conductive members 5152, 5153, 5155, and in this way each ground pin is supported by the composite substrate 510. Also, the conductive members 5152, 5153, 5155 electrically contact both the conductive layers 5113, 5116, which are ground layers. The first conductive contact pin 5144 which is the power supply pin is press fit into the corresponding through hole while contacting the conductive members 5154, and in this way the power supply pin is supported by the composite substrate 510. The conductive member 5154 is electrically connected to the conductive layers 5112, 5115, which are power supply layers.

On the other hand, the first conductive contact pins 5141, 5146, which are signal transmission pins, are inserted into their corresponding holes without contacting the conductive members 5151, 5156. The bottoms of these holes are provided with contact pads 5382, 5383 which constitute a portion of the signal path in a state electrically insulated from the conductive members 5151, 5156. In other words, the aperture diameter of the through holes corresponding to the pin body diameter d of the first conductive contact pins 5141, 5146 is set to D ($D > d$), to constitute a coaxial wiring path within the composite substrate 510. The conductive members 5151, 5156 that are a constant distance from the first conductive contact pins 5141, 5146 are electrically connected to both the conductive layers 5113, 5116 which are ground layers.

Here, the contact pad 5382 provided in the bottom of the hole onto which the first conductive contact pin 5141 is inserted is electrically connected to the vertical connective element 5381 via the horizontal connective element 5391. The horizontal connective element 5391 is located between the ground layers 5411, 5412 provided within the base member 5110 of the composite substrate 510, and as a result of this construction, the horizontal connective element 5391 functions as a strip line. On the other hand, the contact pad 5383 provided in the bottom of the hole onto which the first conductive contact pin

5146 is inserted is electrically connected to the vertical connective element 5384 via the horizontal connective element 5392. The horizontal connective element 5392 is located between the ground layers 5411, 5412 provided within the base member 5110 of the composite substrate 510, similar to the horizontal connective element 5391, and as a result of this construction, the horizontal connective element 5392 functions as a strip line. Each of the ground layers 5411, 5412 that sandwich the horizontal connective elements 5391, 5392 are electrically connected to the conductive members 5152, 5153, 5155 that contact the conductive contact pins 5142, 5143, 5145, which are ground pins. Also, drilled holes 5381a, 5384a are provided in the top of the vertical connective element 5181 (on the top surface side of the composite substrate 510) and the top of the vertical connective element 5184 (on the top surface side of the composite substrate 510), respectively, that constitute a part of the signal transmission conduction paths. These drilled holes 5381a, 5384a are holes formed by removing a part of the vertical connective element 5381 and the vertical connective element 5382 with a drill, in order to prevent stubs.

A plate shaped protective member 5121 is provided on or above the top surface 510a of the composite substrate 510. The plate shaped protective member 5121 has through holes provided corresponding to the first conductive contact pins 5141 to 5146, and the diameter of each of these through holes is smaller than the diameter d of the pin bodies. The first conductive contact pins 5141 through 5146 are securely retained in the composite substrate 510 by inserting plunger tips into the corresponding through holes of the plate shaped protective member 5121.

In addition, the base member 5110 has layer shaped grounded conductors (ground conductor layers) 5131, 5132 for grounding on or above the surfaces thereof (the surfaces corresponding to the top surface 510a and bottom surface 510b of the composite substrate 510) near the plungers of the second conductive contact pins 5141, 5146 which are signal pins. The ground conductor layers 5131, 5132 are electrically connected to the conduction members 5152, 5153, 5155 (plating layer provided on the inside surface of the through holes into which the ground pins are inserted) which are connected to the first conductive contact pins 5142, 5143, 5145, which are the ground pins, and are not electrically connected to the first conductive contact pins 5141, 5146, which are signal transmission pins. In this way, a conductor layer at the same voltage as the ground layer is disposed near the plunger, which has a diameter smaller than that of the pin body, so it is possible to compensate for the inductance component of the tip of the plunger, and reduce insertion losses and near end crosstalk of the signal pins. Also, providing a ground conductor layer on the surface layer of the base member 5110 can be achieved by a normal multi-layer substrate manufacturing process, and a larger capacitance component can be obtained than providing the ground conductor layer as an internal layer of the base member 5110.

In FIG. 15, for clarity the conductor layer 5131 for grounding and the plate shaped protective member 5121 are illustrated as separated, but the two may contact. Also, in the example illustrated in FIG. 15, the ground conductor layer 5132 provided on the bottom surface (the surface corresponding to the bottom surface 510b of the composite substrate 510) of the base member 5110 also functions as a pad

that directly contacts the conductive contact pins 5242, 5243, 5245 that function as ground pins among the second conductive contact pins 6 retained by the second substrate 520. On the other hand, the vertical connective elements 5381, 5384, which function as a part of the conduction paths of the signal transmission pins, have on the bottom surface of the base member 5110 contact pads 5381b, 5384b respectively, which are electrically connected to the conductive contact pins 5241, 5244, which are signal transmission pins from among the conductive contact pins 6 retained by the second substrate 520.

Next, the construction of the second substrate 520 as illustrated in FIG.15 explained, but the second substrate 520 is substantially the same as the second substrate 220, 420 of the first and second embodiments as described above in construction and constituent materials, so duplication of explanations is omitted.

In other words, the second substrate 520 is formed from a base member 5210 having a top surface 520a in opposition to the bottom surface 510b of the composite substrate 510, and a bottom surface 520b in opposition to the top surface 520a, made from a dielectric such as glass epoxy resin or the like, having at least one dielectric layer 5211 embedded in the base member 5210 (or a separate dielectric layer may be provided), with conductor layers 5212, 5213 such as copper or the like formed on the top surface and the bottom surface of the dielectric layer 5211. One conductor layer 5212 is electrically connected to a power supply pin of the IC device socket 100 to constitute a power supply layer, and the other conductor layer 5213 is electrically connected to a ground pin of the IC device socket 100 to constitute a ground (GND) layer. Also, a plurality of holes is formed in the base member 5210, so that the second conductive contact pins 6 form the second arrangement pattern PA1b when inserted, and conductive members 5251 to 5256 made from copper, gold, silver, or the like, are provided on the inside surface of the through holes.

In the second substrate 520, of the second conductive contact pins 6 inserted into their corresponding through holes, the second conductive contact pins 5242, 5243, 5245 are ground pins, the second conductive contact pins 5241, 5244 are signal transmission pins having the coaxial construction as described above, and the second conductive contact pin 5246 is the power supply pin.

Plate shaped protective members 5221, 5222 are provided on or above the top surface 520a and the bottom surface 520b of the second substrate 520. In addition, the base member 5210 has layer shaped grounded conductors (ground conductor layers) 5231, 5232 for grounding on or above the surfaces thereof (the surfaces corresponding to the top surface 520a and bottom surface 520b of the second substrate 520) near the plungers of the second conductive contact pins 5241, 5244 which are signal pins. In FIG. 15, for clarity the conductor layers 5231, 5232 for grounding and the plate shaped protective members 5221, 5222 are illustrated as separated, but the two may contact.

List of reference numbers:

1, 1A, 1B ... Pin holder,
 100 ... IC device socket,
 210, 410 ... First substrate,
 220, 420, 520 ... Second substrate,
 230, 430 ... Third substrate,
 510 ... Composite substrate (first substrate + third substrate),
 4, 2141 to 2146, 4141 to 4146, 5141 to 5146 ... First conductive contact pin,
 6, 2241 to 2246, 4241 to 4246, 5241 to 5246 ... Second conductive contact pin,
 2361 to 2366, 2371 to 2372, 2381 to 2384, 2391 to 2392, 4361 to 4366, 4371 to 4372,
 4381 to 4384, 4391 to 4392, 5381 to 5384, 5391 to 5392 ... Conduction path,
 2121, 2122, 2221, 2222, 4121, 4122, 4221, 4222, 5121, 5221, 5222 ... Protective member.

Following are exemplary embodiments of an IC device socket according to aspects of the present invention.

Embodiment 1 is an IC device socket, comprising: a first substrate having a plurality of first conductive contact pins that extend through the interior thereof and that form a first arrangement pattern; a second substrate having a plurality of second conductive contact pins that extend through the interior thereof and that form a second arrangement pattern that is different from the first arrangement pattern, and each of the second conductive contact pins correspond to one of the first conductive contact pins; and a third substrate disposed between the first and second substrates, and having a plurality of conduction paths in the interior thereof, and each conduction path electrically connects one of the first conductive contact pins with the corresponding second conductive contact pin, wherein, the third substrate is separated from at least one of the first and second substrates.

Embodiment 2 is the IC device socket according to embodiment 1, wherein the third substrate is separated from the first and second substrates.

Embodiment 3 is the IC device socket according to embodiment 1, further comprising a body that supports the first through third substrates, that includes a guide portion for positioning an IC device that is to be inspected on a specific position on the surface of the first substrate, and a construction that minimizes variations in the relative positions of the first through third substrates.

Embodiment 4 is the IC device socket according to embodiment 1, wherein the first substrate includes a bottom surface in opposition to the second substrate, a top surface in opposition to the bottom

surface, and a plurality of holes that extend from the top surface to the bottom surface, and at least a part of one first conductive contact pin is inserted into the corresponding hole, and a protective member is provided on or above at least one of the top surface and the bottom surface, the protective member has a plurality of through holes and at least a part of one first conductive contact pin is inserted into the corresponding through hole, so that the axes in the longitudinal direction of each of the plurality of first conductive contact pins approximately coincide with the center line axis of the corresponding hole of the first substrate, conductive members are provided on the inside surface of each hole of the first substrate, and at least one of the plurality of first conductive contact pins is inserted into the corresponding hole so that it is electrically insulated from the conductive member provided on the inside surface of the corresponding hole in the first substrate.

Embodiment 5 is the IC device socket according to embodiment 4, wherein dielectric material is disposed in a gap between the conductive member provided on the inside surface of the corresponding hole and the first conductive contact pin inserted in the corresponding hole.

Embodiment 6 is the IC device socket according to embodiment 1, wherein the second substrate includes a top surface in opposition to the first substrate, a bottom surface in opposition to the top surface, and a plurality of holes that extend from the top surface to the bottom surface, and at least a part of one second conductive contact pin is inserted into the corresponding hole, and a protective member is provided on or above at least one of the top surface and the bottom surface, the protective member has a plurality of through holes and at least a part of one second conductive contact pin is inserted into the corresponding through hole, so that the axes in the longitudinal direction of each of the plurality of second conductive contact pins approximately coincide with the center line axis of the corresponding hole of the second substrate, conductive members are provided on the inside surface of each hole of the second substrate, and at least one of the plurality of second conductive contact pins is inserted into the corresponding hole so that it is electrically insulated from the conductive member provided on the inside surface of the corresponding hole in the second substrate.

Embodiment 7 is the IC device socket according to embodiment 1, wherein the third substrate has a construction in which a dielectric layer and a pair of conductor layers that sandwich the dielectric layer from both the first substrate side and the second substrate side thereof is embedded within the third substrate.

Embodiment 8 is the IC device socket according to embodiment 1, wherein the third substrate has a construction in which at least one of a strip line and a microstrip line is embedded within the third substrate.

Although specific embodiments have been illustrated and described herein for purposes of description of the preferred embodiment, it will be appreciated by those of ordinary skill in the art that a wide variety of alternate and/or equivalent implementations calculated to achieve the same purposes may be substituted for the specific embodiments shown and described without departing from the scope of the present invention. Those with skill in the mechanical, electro-mechanical, and electrical arts will readily appreciate that the present invention may be implemented in a very wide variety of embodiments. This application is intended to cover any adoptions or variations of the preferred embodiments discussed herein. Therefore, it is manifestly intended that this invention be limited only by the claims and the equivalents thereof.

What is claimed is:

1. An IC device socket, comprising: a first substrate having a plurality of first conductive contact pins that extend through the interior thereof and that form a first arrangement pattern;

5 a second substrate having a plurality of second conductive contact pins that extend through the interior thereof and that form a second arrangement pattern that is different from the first arrangement pattern, and each of the second conductive contact pins correspond to one of the first conductive contact pins; and

10 a third substrate disposed between the first and second substrates, and having a plurality of conduction paths in the interior thereof, and each conduction path electrically connects one of the first conductive contact pins with the corresponding second conductive contact pin,

wherein,

the third substrate is separated from at least one of the first and second substrates.

15 2. The IC device socket according to claim 1, wherein the third substrate is separated from the first and second substrates.

20 3. The IC device socket according to claim 1, further comprising a body that supports the first through third substrates, that includes a guide portion for positioning an IC device that is to be inspected on a specific position on the surface of the first substrate, and a construction that minimizes variations in the relative positions of the first through third substrates.

25 4. The IC device socket according to claim 1, wherein the first substrate includes a bottom surface in opposition to the second substrate, a top surface in opposition to the bottom surface, and a plurality of holes that extend from the top surface to the bottom surface, and at least a part of one first conductive contact pin is inserted into the corresponding hole, and a protective member is provided on or above at least one of the top surface and the bottom surface,

30 the protective member has a plurality of through holes and at least a part of one first conductive contact pin is inserted into the corresponding through hole, so that the axes in the longitudinal direction of each of the plurality of first conductive contact pins approximately coincide with the center line axis of the corresponding hole of the first substrate,

conductive members are provided on the inside surface of each hole of the first substrate, and

at least one of the plurality of first conductive contact pins is inserted into the corresponding hole so that it is electrically insulated from the conductive member provided on the inside surface of the corresponding hole in the first substrate.

5. The IC device socket according to claim 4, wherein dielectric material is disposed in a gap between the conductive member provided on the inside surface of the corresponding hole and the first conductive contact pin inserted in the corresponding hole.

6. The IC device socket according to claim 1, wherein the second substrate includes a top surface in opposition to the first substrate, a bottom surface in opposition to the top surface, and a plurality of holes that extend from the top surface to the bottom surface, and at least a part of one second conductive contact pin is inserted into the corresponding hole, and a protective member is provided on or above at least one of the top surface and the bottom surface,

the protective member has a plurality of through holes and at least a part of one second conductive contact pin is inserted into the corresponding through hole, so that the axes in the longitudinal direction of each of the plurality of second conductive contact pins approximately coincide with the center line axis of the corresponding hole of the second substrate,

conductive members are provided on the inside surface of each hole of the second substrate, and at least one of the plurality of second conductive contact pins is inserted into the corresponding hole so that it is electrically insulated from the conductive member provided on the inside surface of the corresponding hole in the second substrate.

7. The IC device socket according to claim 1, wherein the third substrate has a construction in which a dielectric layer and a pair of conductor layers that sandwich the dielectric layer from both the first substrate side and the second substrate side thereof is embedded within the third substrate.

8. The IC device socket according to claim 1, wherein the third substrate has a construction in which at least one of a strip line and a microstrip line is embedded within the third substrate.

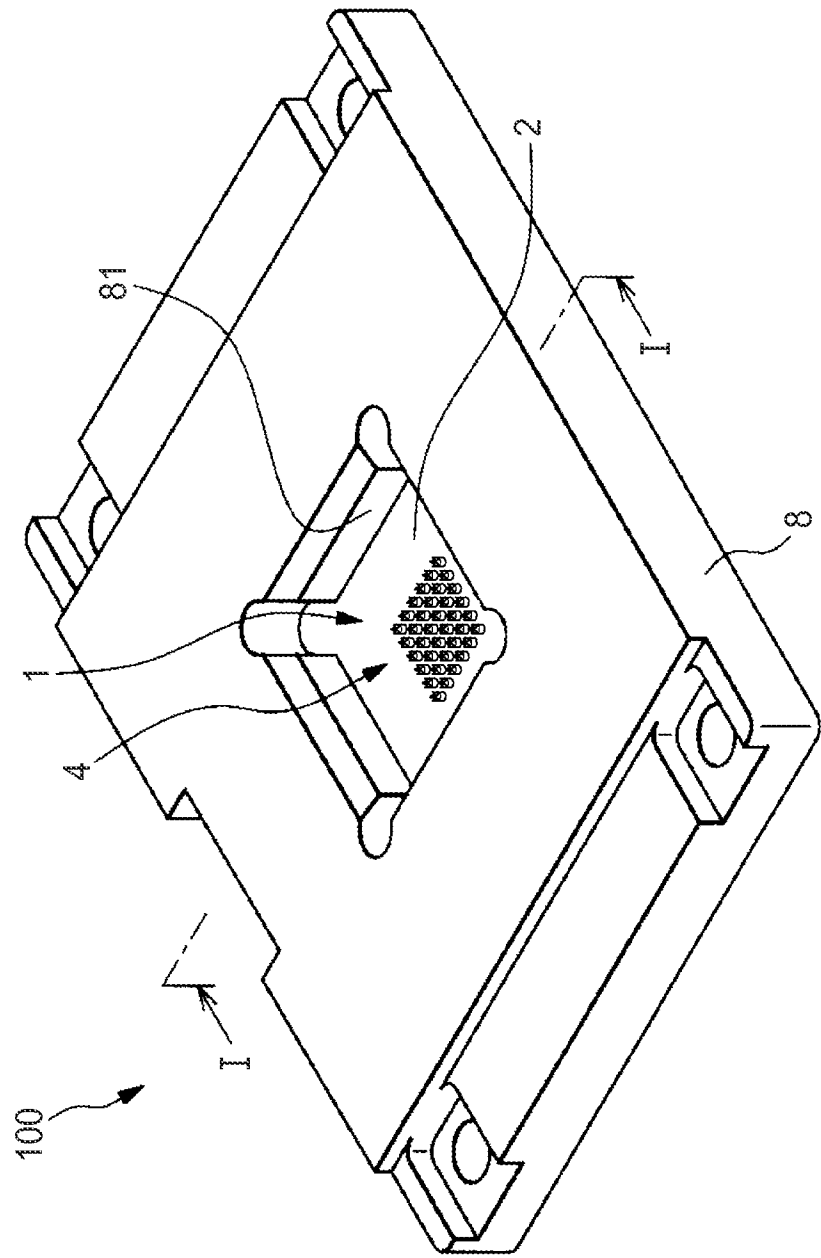


FIG. 1

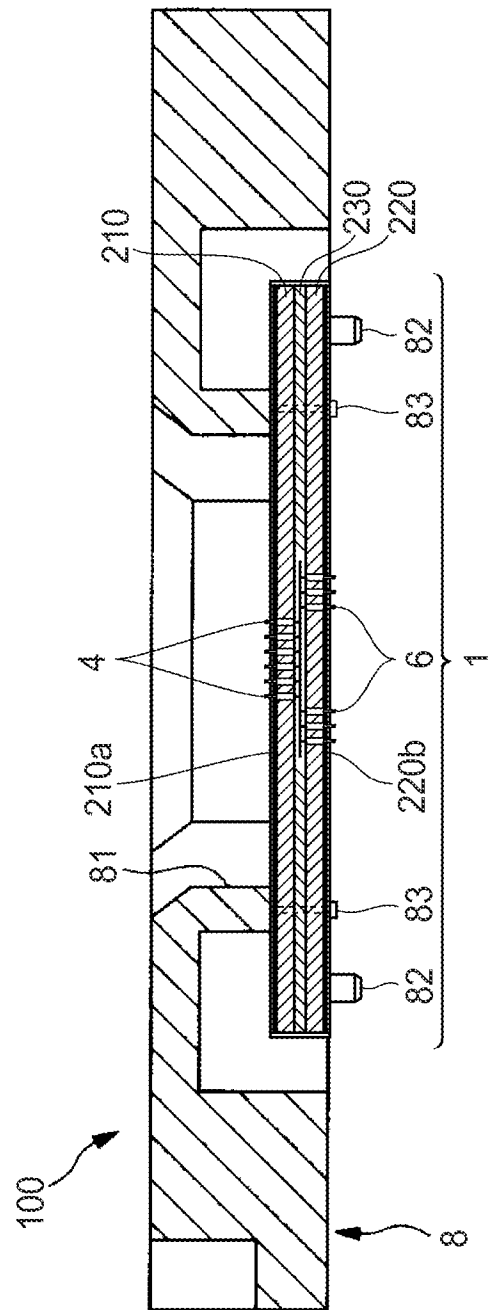


FIG. 2

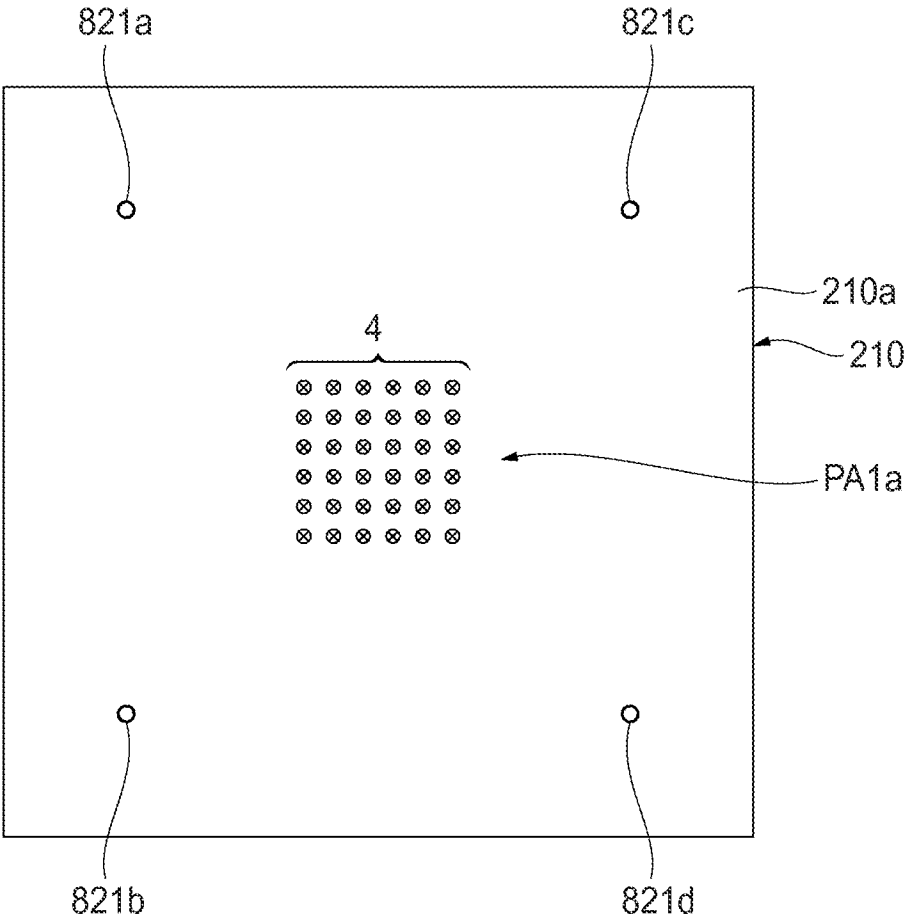
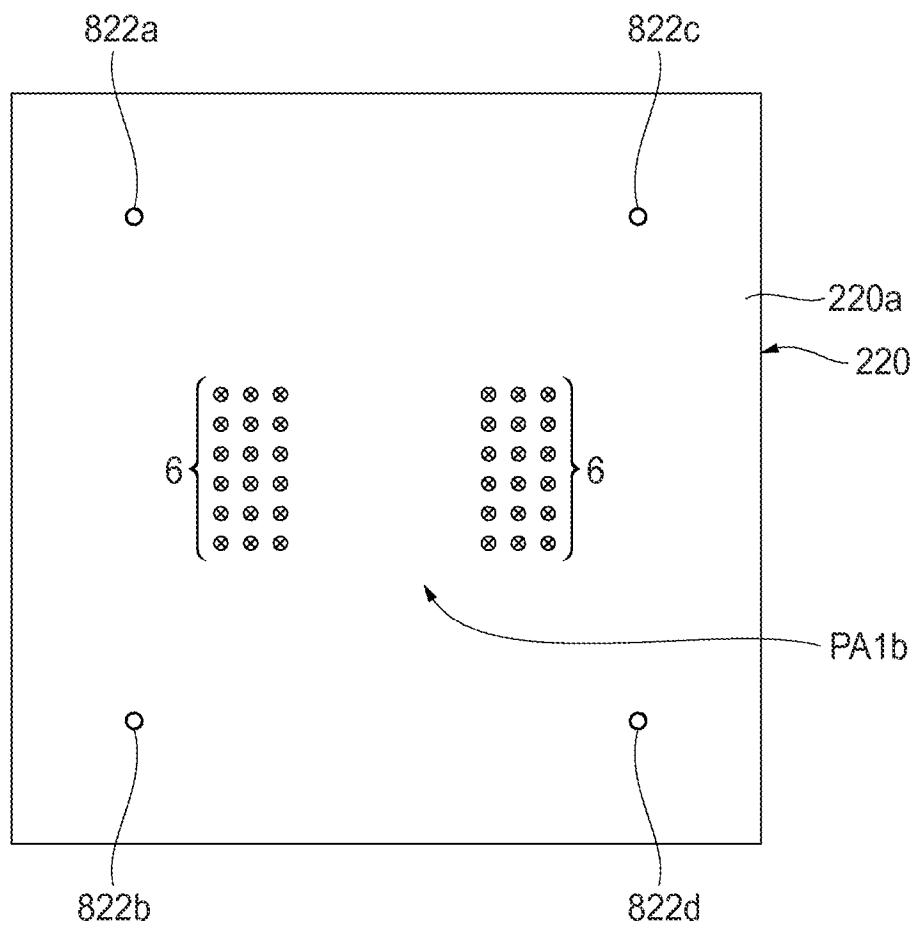
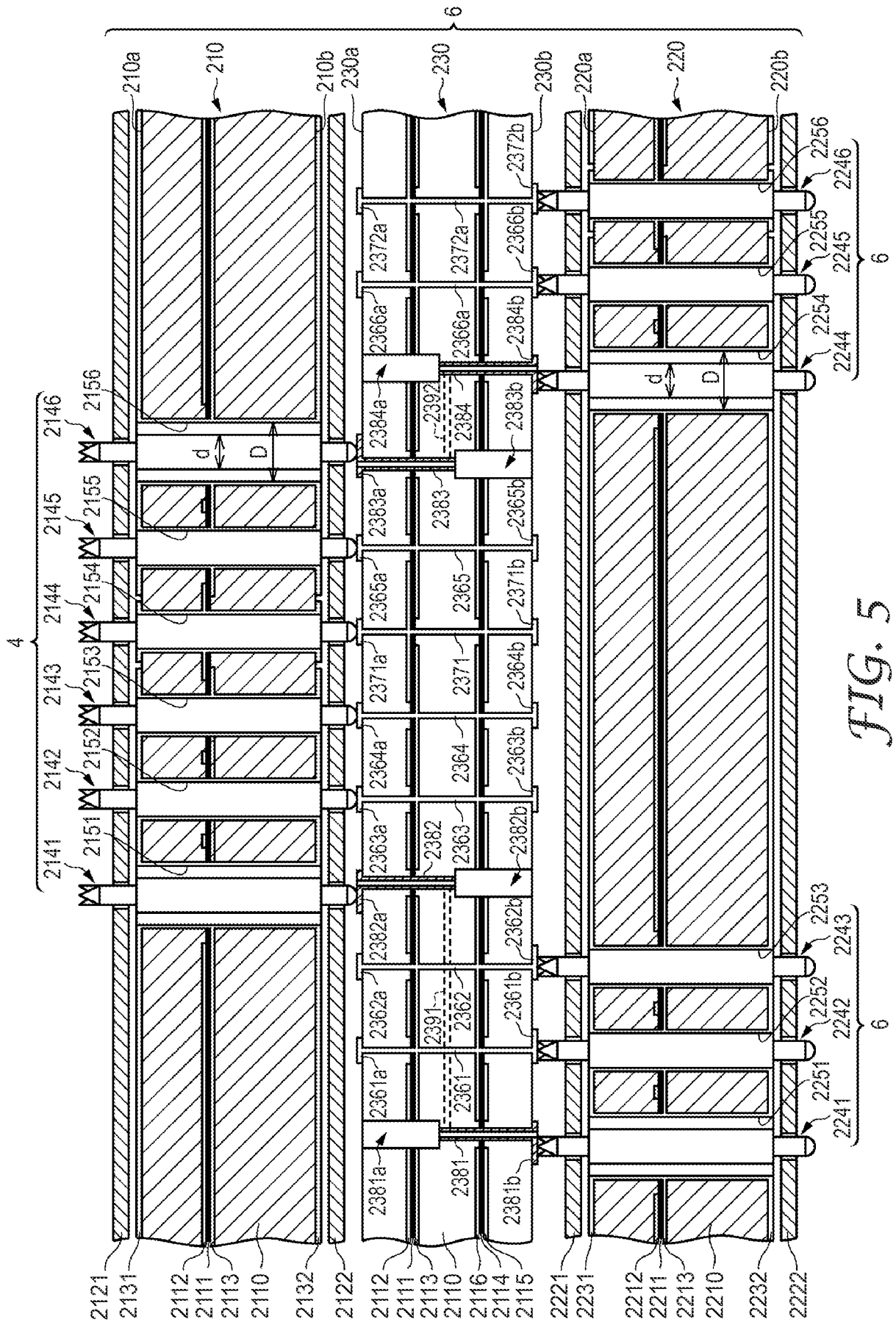


FIG. 3

4/13

*FIG. 4*



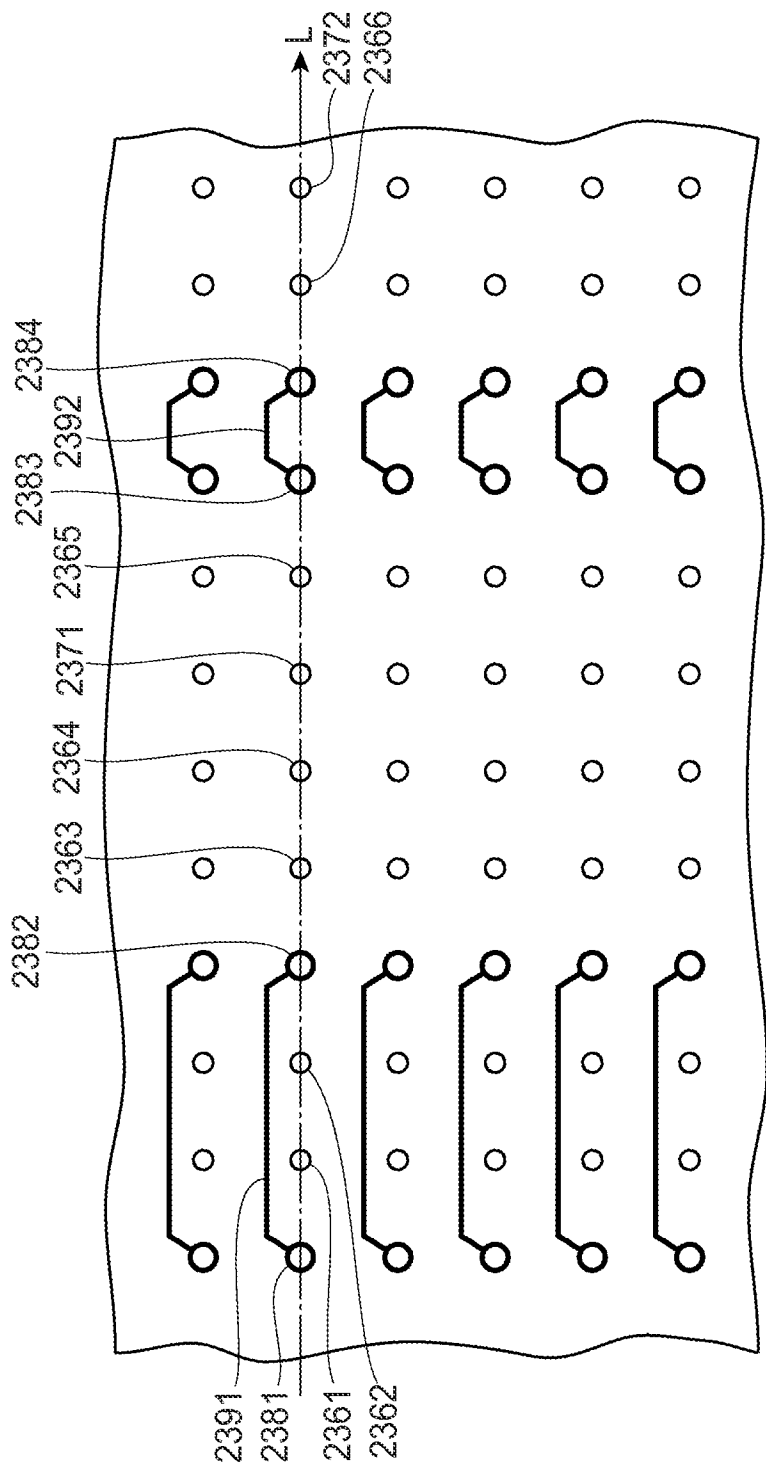


FIG. 6

7/13

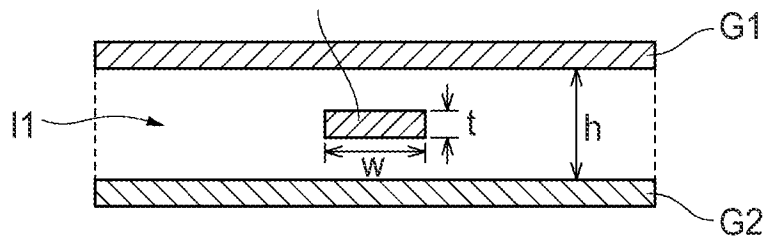


FIG. 7

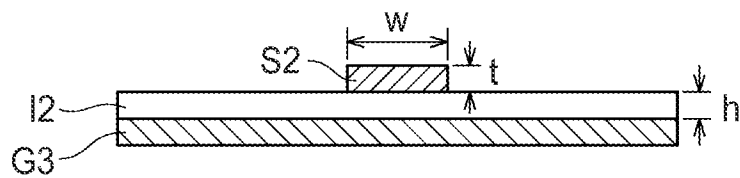


FIG. 8

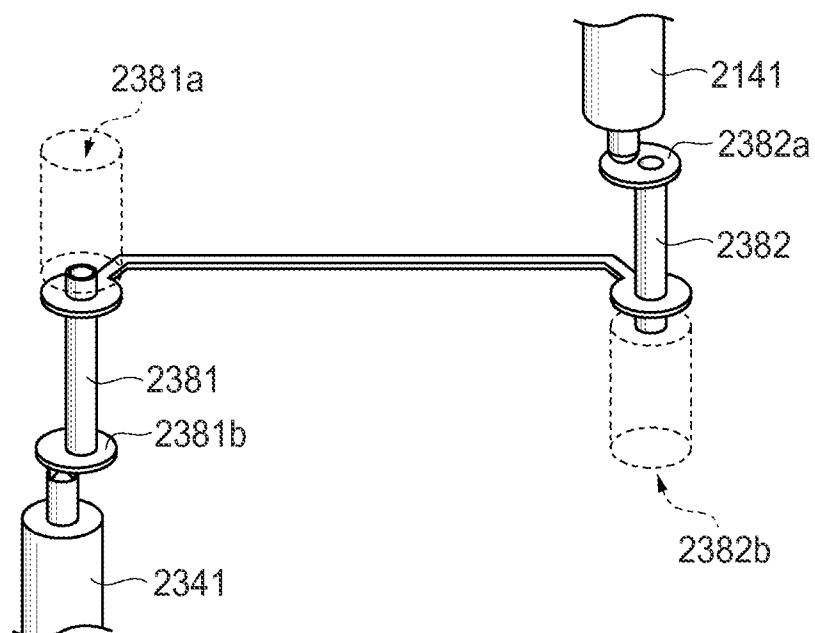
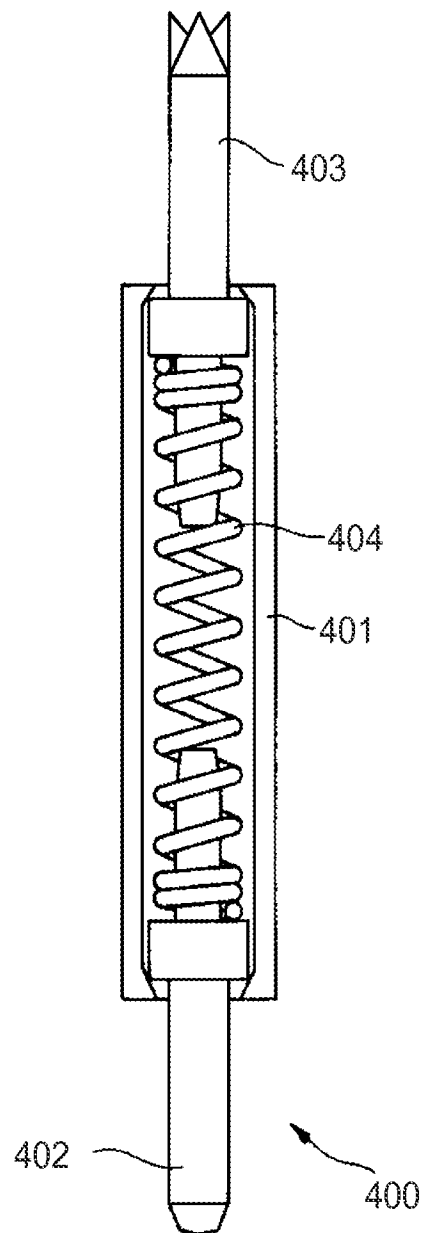
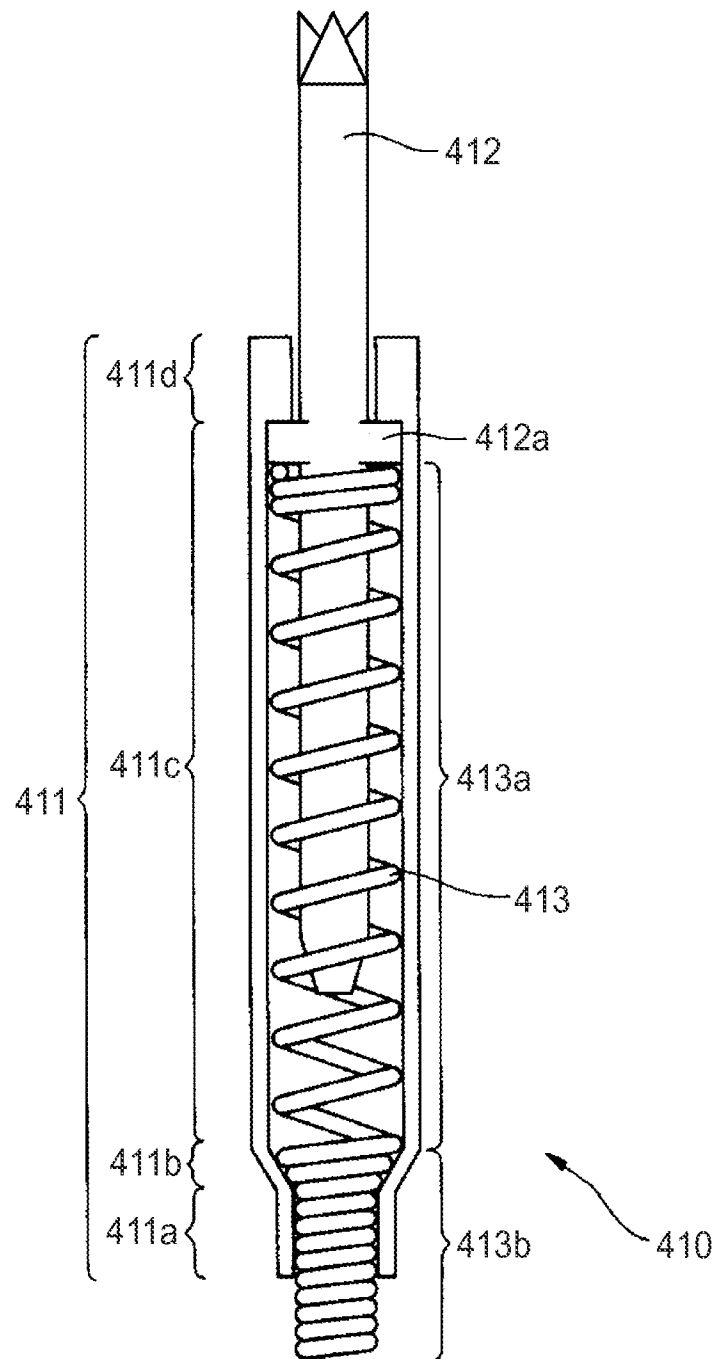


FIG. 9

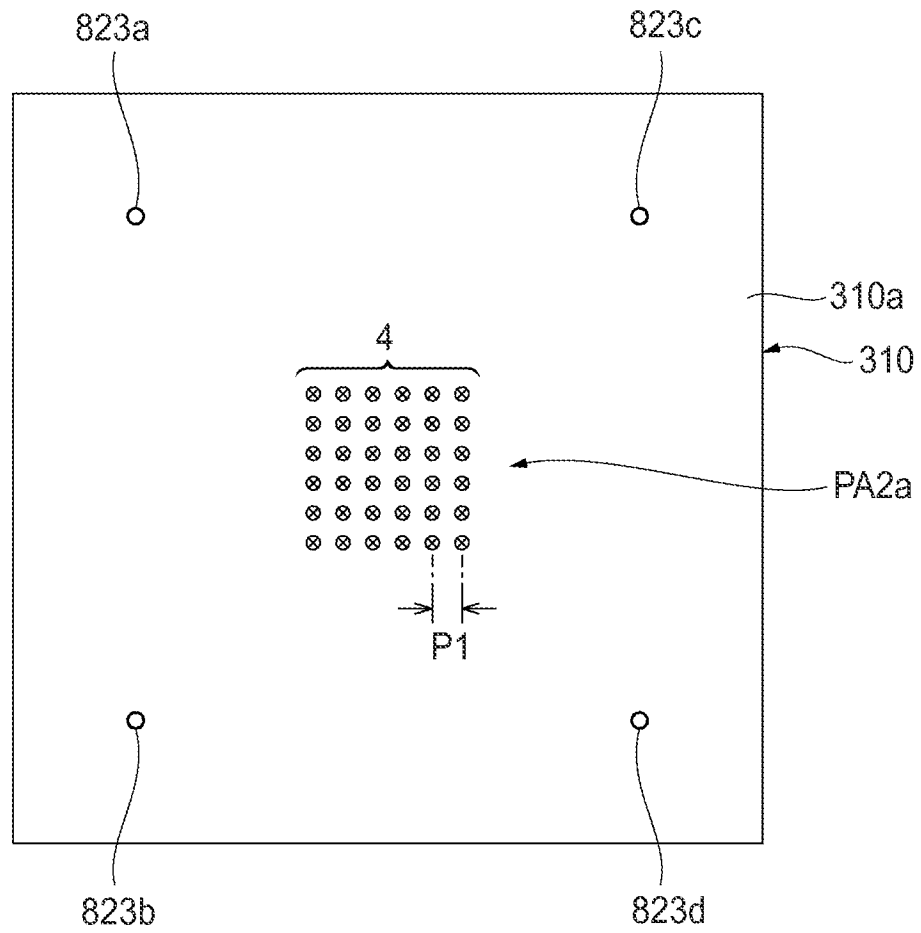
8/13

*FIG. 10*

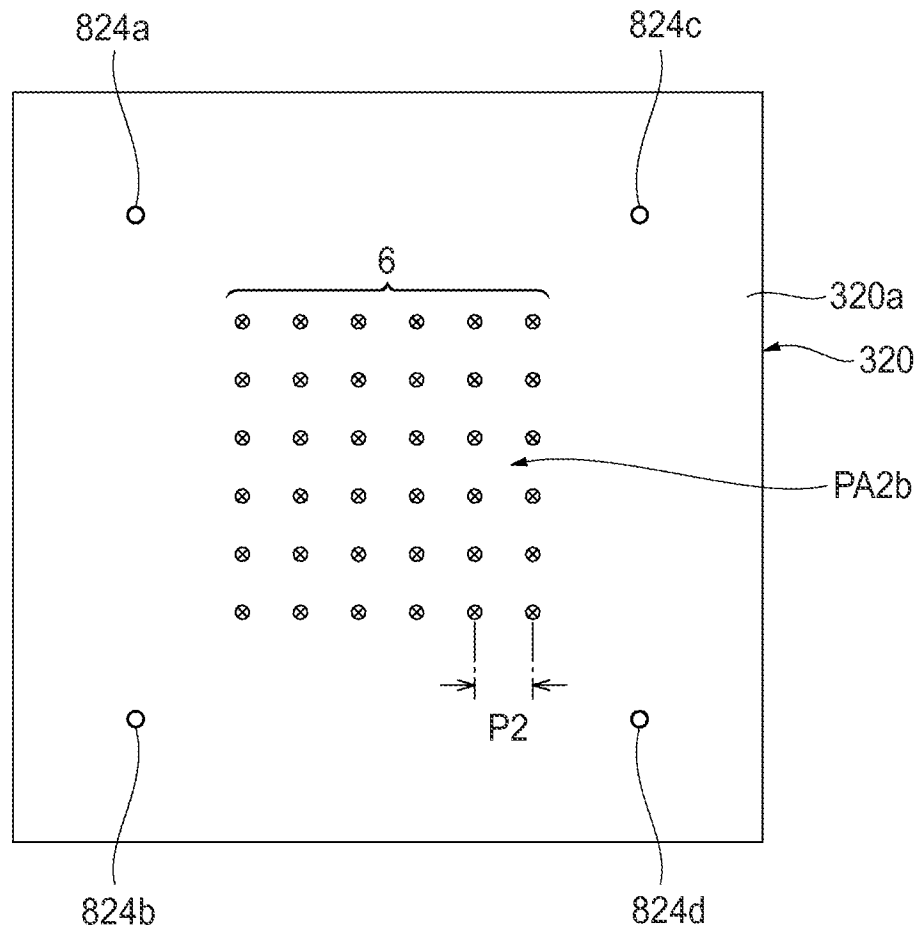
9/13

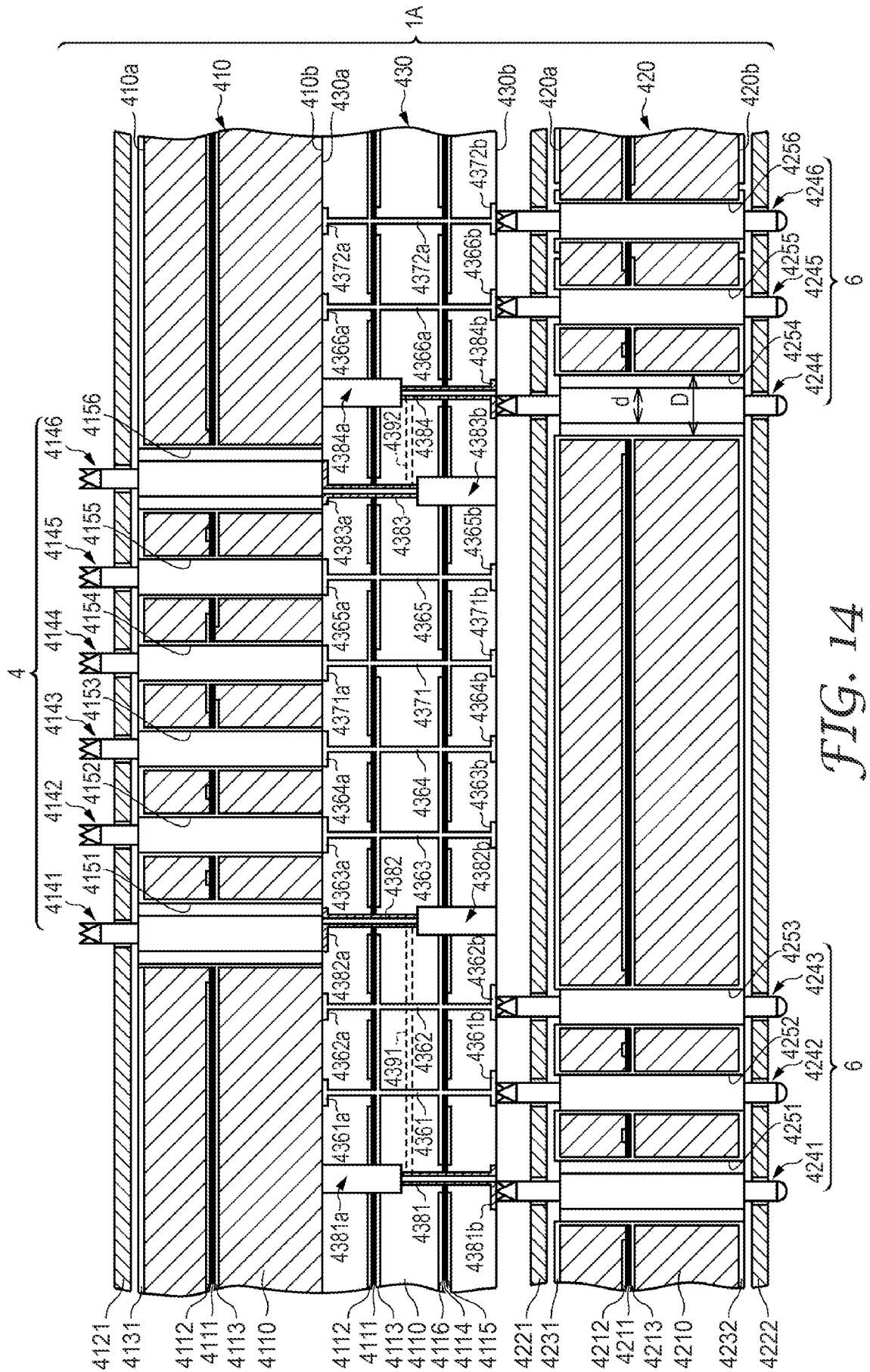
*FIG. 11*

10/13

*FIG. 12*

11/13

*FIG. 13*



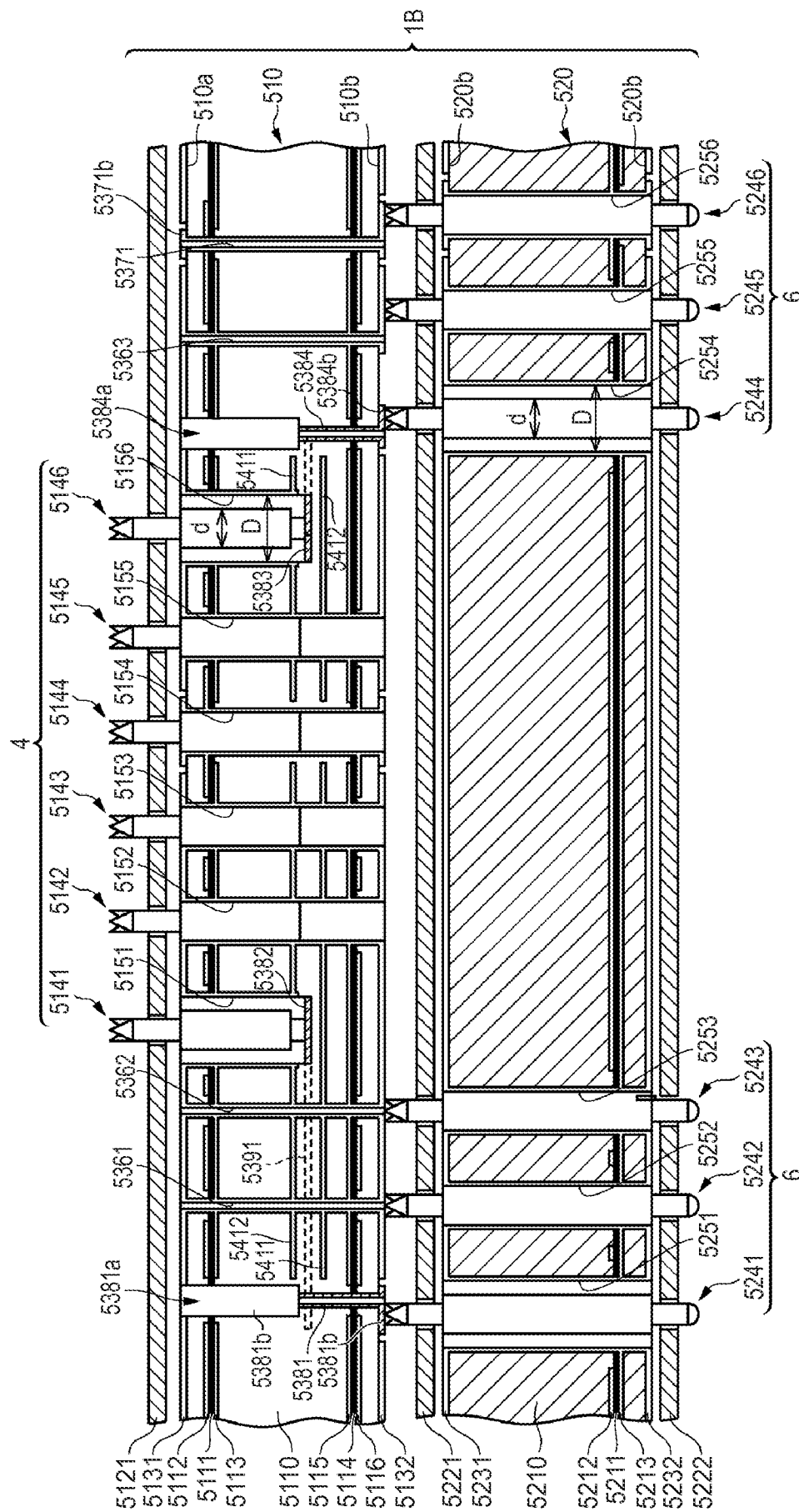


FIG. 15

INTERNATIONAL SEARCH REPORT

International application No
PCT/US2012/023066

A. CLASSIFICATION OF SUBJECT MATTER
INV. G01R1/04
ADD.

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
G01R H05K H01R

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

EPO-Internal, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2003/134526 A1 (CHENG WEI-JEN [TW] ET AL) 17 July 2003 (2003-07-17) paragraphs [0034], [0043]	1-8
A	US 2004/179339 A1 (MAYER DAVID [US]) 16 September 2004 (2004-09-16) abstract figure 2	1-8



Further documents are listed in the continuation of Box C.



See patent family annex.

* Special categories of cited documents :

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Date of the actual completion of the international search

25 June 2012

Date of mailing of the international search report

04/07/2012

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Authorized officer

Bernardini, Andrea

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No

PCT/US2012/023066

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 2003134526 A1	17-07-2003	TW 555993 B US 2003134526 A1	01-10-2003 17-07-2003
US 2004179339 A1	16-09-2004	US 2004179339 A1 US 2006028801 A1	16-09-2004 09-02-2006