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(71) Applicant: BOARD OF TRUSTEES OF MICHIGAN
STATE UNIVERSITY [US/US]; 246 Administration
Building, East Lansing, Michigan 48824 (US).(72) Inventor: CHAKRABARTTY, Shantanu; 65 Agateway,
Williamston, Michigan 48895 (US).(74) Agents: FALCOFF, Monte L. et al.; Harness, Dickey &
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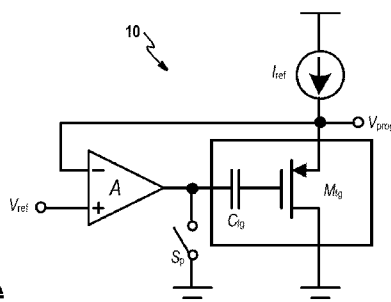
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USING THE SAME

FIG. 2A



(57) Abstract: A linear hot-electron injection technique is provided for a non-volatile memory arrangement. The non-volatile memory is comprised of: a floating gate transistor; a capacitor with a first terminal electrically coupled to the gate node of the floating gate transistor; a current reference circuit electrically coupled to the source node of the floating gate transistor; and a feedback circuit electrically coupled between the source node of the floating gate transistor and a second terminal of the capacitor. The feedback circuit operates to adjust a voltage at the gate node of the floating gate transistor in accordance with a source-to-drain voltage across the floating gate transistor.

NON-VOLATILE MEMORY WITH LINEAR HOT-ELECTRON INJECTION TECHNIQUE AND STRAIN GAUGE USING THE SAME

GOVERNMENT RIGHTS

[0001] This invention was made with Government support under
5 Contract No. 0954752 and Contract No. 1127606 awarded by the National
Science Foundation. The U. S. Government has certain rights in this invention.

CROSS-REFERENCE TO RELATED APPLICATIONS

[0002] This application claims the benefit of U.S. Provisional
10 Application No. 61/602,247, filed on February 23, 2012. The entire disclosure of
the above application is incorporated herein by reference.

FIELD

[0003] The present disclosure relates to a linear hot-electron injection
15 technique which simplifies the programming procedure for a non-volatile memory
as well as a self-powered strain gauge enabled by this technique.

BACKGROUND

[0004] As non-volatile programmable circuit elements, floating-gate
20 (FG) transistors have been extensively used for designing EEPROMs and flash
memories, for designing analog signal processors, and for designing energy
scavenging sensors. In particular, when a large number of on-chip voltage and
current biases are required, as is the case for analog neural-network ICs and
field-programmable analog arrays (FPAAS), floating-gates provide an ultra-
25 compact approach for implementing field-programmable biases. Also, due to the
non-volatile nature of the FG transistors, the bias values are retained across
brown-outs and power-outages, making the technology also attractive for energy
scavenging sensors.

[0005] The common method for programming FG transistors is by
30 using Fowler-Nordheim (FN) tunneling or by using hot-electron injection. The
procedure is illustrated in Figures 1A and 1B which shows the cross-sectional
area of an FG p-channel MOS (pMOS) transistor and its layout. The polysilicon

gate of the pMOS transistor is electrically insulated by silicon-dioxide (hence the name "floating-gate"), and any electron injected onto the gate is retained for a long period of time (8 bits precision for 8 years). FN tunneling removes the electrons from FG node by applying a high-voltage V_{tun} ($> 15\text{V}$ in $0.5\mu\text{m}$ CMOS process) across a parasitic nMOS capacitor C_{tun} . However, the use of high-voltage also restricts the usage of FN tunneling for selective programming and therefore it is only employed to globally remove the electrons from all on-chip floating-gates.

[0006] Hot-electron injection, however, requires lower voltage ($\approx 4.2\text{V}$ in $0.5\mu\text{m}$ CMOS process) than tunneling and hence is the primary mechanism for selective programming of floating-gates. The hot-electron programming procedure, as shown in Figure 1A, involves selection of the FG transistor (using switches) followed by applying $V_{\text{sd}} > 4.2\text{V}$ across the source and the drain terminals. The large electric field near the drain of the pMOS transistor creates impact-ionized hot-electrons whose energy when exceeds the gate-oxide potential barrier ($\approx 3.2\text{eV}$) can get injected onto the floating-gate. Because the hot-electron injection in a pMOS transistor is a positive feedback process and can only be used to add electrons to the floating-gate, the process needs to be carefully controlled and periodically monitored to ensure the floating-gate voltage is programmed to a desired precision. The methods proposed in literature achieve the desired precision either by adjusting the duration for which the FG transistor is injected or by adjusting the magnitude of the injection pulses.

[0007] In this disclosure, a linear hot-electron injection technique is set forth which simplifies the programming procedure and can achieve a linear programming range as large as 4V . The procedure employs an active feedback mechanism to ensure that all the non-linear factors affecting the hot-electron injection are held constant, thus achieving a linear, stable and controllable injection rate. This is unlike the feedback methods that have been previously used for programming FG memories, where an off-chip amplifier circuit is used for indirect programming. The proposed linear injection technique results in a much simpler and more predictable programming procedure.

[0008] Additionally, the proposed linear injection technique is then used to develop a self-powered static-strain sensor.

[0009] This section provides background information related to the present disclosure which is not necessarily prior art.

5

SUMMARY

[0010] A linear hot-electron injection technique is provided for a non-volatile memory arrangement. The non-volatile memory is comprised of: a floating gate transistor; a capacitor with a first terminal electrically coupled to the gate node of the floating gate transistor; a current reference circuit electrically coupled to the source node of the floating gate transistor; and a feedback circuit electrically coupled between the source node of the floating gate transistor and a second terminal of the capacitor. The feedback circuit operates to adjust a voltage at the gate node of the floating gate transistor in accordance with a source-to-drain voltage across the floating gate transistor, thereby achieving a linear injection technique. The non-volatile memory further includes a switch electrically coupled between the second terminal of the capacitor and ground, such that the switch is opened to inject current into the floating gate transistor and is closed to remove electrons from the floating gate transistor.

[0011] In one aspect of the disclosure, the feedback circuit is further defined as an operational amplifier having an inverting terminal electrically coupled to the source node of the floating gate transistor, a non-inverting terminal electrically coupled to a reference voltage and an output electrically coupled to the second terminal of the capacitor.

[0012] In another aspect of the disclosure, a self-powered static-strain sensor is implemented using the linear hot-electron injection technique. The sensor is self-powered by piezoelectric transducers which convert mechanical energy due to strain-variations into electrical energy. A differential injector topology is used to measure static-strain by integrating the difference between the signal energy generated during positive and negative strain-cycles. Each differential integrator is implemented using the non-volatile memory arrangement noted above.

[0013] This section provides a general summary of the disclosure, and is not a comprehensive disclosure of its full scope or all of its features. Further areas of applicability will become apparent from the description provided herein. The description and specific examples in this summary are intended for purposes of illustration only and are not intended to limit the scope of the present disclosure.

DRAWINGS

[0014] Figure 1A is a cross-sectional view of a pMOS FG transistor along with the circuits used for conventional hot-electron programming;

[0015] Figure 1B is a diagram depicting an exemplary layout of the pMOS FG transistor;

[0016] Figure 2A is a schematic of an exemplary circuit arrangement for a non-volatile memory that employs a linear hot-electron injection technique;

[0017] Figures 2B and 2C are schematics illustrating the non-volatile memory during programming mode and biasing mode, respectively;

[0018] Figure 3 is a graph showing the measured injection current into the memory circuit when the source voltage is varied;

[0019] Figure 4 is a schematic of an alternative circuit arrangement for the non-volatile memory using a single-stage, single-ended amplifier;

[0020] Figure 5 is a schematic showing an array of memory circuit that employ a linear hot-electron injection technique;

[0021] Figures 6A and 6B are graphs showing the measured linear injection response when I_{ref} and V_{ref} , respectively, is varied;

[0022] Figure 7 is a diagram illustrating the principle underlying a self-powered static-strain sensor;

[0023] Figure 8 is a schematic of an exemplary architecture for a self-powered static-strain sensor;

[0024] Figure 9 is a diagram of an experimental test setup for the self-powered static-strain sensor;

[0025] Figure 10 is a graph illustrating sensor output with symmetrical positive and negative cycles;

[0026] Figure 11 is a graph illustrating sensor output with different positive and negative cycles;

[0027] Figure 12 is a schematic of an experimental setup of a strain-gauge attached to a plexi-glass beam;

5 [0028] Figures 13A-13C are graphs illustrating time-varying strain measurements when the plexi-glass beam is periodically deformed at select maximum strain values;

[0029] Figure 14 is a graph illustrating measured voltage change at the output of the positive-cycle injector;

10 [0030] Figure 15 is a graph illustrating output voltages of the piezoelectric transducer for a nominal strain-cycle;

[0031] Figure 16 is a graph illustrating measured voltage change at the output of the negative-cycle injector; and

15 [0032] Figures 17A and 17B are graphs illustrating difference in measure voltage change between positive-cycle and negative-cycle injectors under different conditions.

[0033] The drawings described herein are for illustrative purposes only of selected embodiments and not all possible implementations, and are not intended to limit the scope of the present disclosure. Corresponding reference
20 numerals indicate corresponding parts throughout the several views of the drawings.

DETAILED DESCRIPTION

[0034] Figure 2A depicts an exemplary circuit arrangement 10 for a
25 non-volatile memory that employs a linear hot-electron injection technique. The circuit arrangement 10 is comprised of a floating gate transistor M_{fg} , a capacitor C_{fg} , a current reference source I_{ref} and a feedback circuit. The feedback circuit is electrically coupled between a source node of the floating gate transistor M_{fg} and a terminal of the capacitor C_{fg} while the other terminal of the capacitor
30 C_{fg} is electrically coupled to a gate node of the floating gate transistor M_{fg} . More specifically, the feedback circuit may be implemented by an operational amplifier A having an inverting terminal electrical coupled to the source node of the

floating gate transistor M_{fg} , a non-inverting terminal electrically coupled to a reference voltage and an output electrically coupled to the second terminal of the capacitor. The circuit arrangement further includes a switch S_p electrically coupled between the second terminal of the capacitor and ground and a controller (not shown) interfaced with the switch S_p to control operation thereof. Other arrangements for the circuit are also contemplated by this disclosure.

[0035] Operating principle for the linear hot-electron injection technique is set forth in detail below. Impact-ionized hot-electron injection (IHEI) current, I_{inj} , in a pMOS transistor has been shown to be dependent on the transistor source current I_s , the source-to-drain voltage V_{sd} and the gate-to-drain voltage V_{gd} across the transistor. This dependence can be expressed in functional form as

$$I_{inj} = f(I_s, V_{sd}, V_{gd}), \quad (1)$$

where $f(\cdot)$ is an arbitrary function. To our knowledge, the exact form of the mathematical function $f(\cdot)$ is not known and in literature many empirical models have been proposed to approximate $f(\cdot)$. For example, the following IHEI model has been shown to be valid for all operating regions of the transistor (weak, moderate and strong inversion):

$$I_{inj} = \alpha I_s \exp\left(\frac{\lambda V_{sd}}{V_{inj}}\right) \exp\left[-\frac{\beta}{(V_{gd} + \delta)^2}\right], \quad (2)$$

where $\alpha, \lambda, \beta, \delta$ and V_{inj} are the parameters of the model which are estimated from measured data. For the proposed linear injection technique, all the factors which affect the injection current such as I_s, V_{sd} and V_{gd} are held constant so that the injection current I_{inj} according to equation (1) is constant. Continuing with circuit arrangement 10, its operational principle is explained with reference to Figures 2B and 2C.

[0036] During the programming or injection mode of circuit in Figure 2B, the switch S_p is open which activates the negative feedback loop formed by the opamp A and the floating-gate transistor M_{fg} . The source current is held constant at I_{ref} which ensures that the source-to-gate voltage V_{sg} is held constant by appropriately adjusting the control-gate voltage V_{cg} . Thus, according

to equation (1) the injection current will remain constant. The programming is enabled for a fixed duration t_p which ensures that a fixed amount of charge is injected onto the floating-gate. During the read-out mode as shown in Fig. 2C, the switch S_p is closed which connects the control-gate to a reference potential (ground in this case). The floating-gate voltage V_{fg} of the pMOS transistor is determined by the charge injected during the programming phase and the capacitor C_{fg} . The formal analysis of the linear injector is now presented by taking into account the effect of the finite gain of the opamp and injection small signal parameters derived from the measurement results.

10 **[0037]** According to equation (1), the injection current I_{inj} in the circuit arrangement 10 of Fig. 2B (without considering the effect of thermal-noise) is given by

$$I_{inj} = f(I_{ref}, V_s, V_{fg}), \quad (3)$$

which can be linearized about the injection current I_{inj}^0 for incremental source voltage ΔV_{fg} as

$$I_{inj} = I_{inj}^0 + G_s \Delta V_s + G_{fg} \Delta V_{fg}, \quad (4)$$

where $G_s = \partial I_{inj} / \partial V_s$ denotes the injection transconductance parameter with respect to the source terminal and $G_{fg} = \partial I_{inj} / \partial V_{fg}$ denotes the injection transconductance parameter with respect to the floating-gate terminal.

20 Assuming the reference current is constant, the small-signal analysis of the pMOS current leads to

$$\Delta I_{ref} = (g_m + g_d) \Delta V_s - g_m \Delta V_{fg} = 0, \quad (5)$$

where $g_m = \partial I_{ref} / \partial V_g$ and $g_d = \partial I_{ref} / \partial V_d$ are the transconductance small-signal parameters with respect to the gate and drain terminals. Then $\Delta V_s \approx \Delta V_{fg}$ when $g_m \gg g_d$ for the pMOS transistor in saturation region. If V_{tun}, V_s, V_d and V_b denote the tunneling voltage, source voltage, drain voltage and bulk voltage of the floating-gate transistor, and $C_{fg}, C_{tun}, C_s, C_d, C_b$ denote the capacitances (parasitic and non-parasitic) which couple these nodes with the floating-gate, then the charge stored on the floating-gate can be expressed as

$$30 \quad Q = C_{fg}(V_{fg} - V_{cg}) + C_{tun}(V_{fg} - V_{tun}) + C_s(V_{fg} - V_s) + C_d(V_{fg} - V_d) + C_b(V_{fg} - V_b). \quad (6)$$

Since the feedback topology in the circuit of Fig. 2B maintains all the node voltages except V_{fg} at a constant potential, the charge variation ΔQ can be simplified as

$$\Delta Q = \Delta V_{fg} C_T \quad (7)$$

where $C_T = (C_{fg} + C_{tun} + C_s + C_d + C_b)$ is the total capacitance associated with the floating-gate. If the gain of the opamp is assumed to be A_v , then the feedback loop ensures

$$\Delta V_{cg} + \frac{\Delta Q}{C_T} = -A_v \Delta V_s + \frac{\Delta Q}{C_T} = \Delta V_{fg} \approx \Delta V_s, \quad (8)$$

Thus,

$$\Delta V_s = \frac{\Delta Q}{C_T(1+A_v)}, \quad (9)$$

where, V_s remains constant for infinite A_v . The charge variation ΔQ in (9) can be expressed with the injection current as

$$\Delta Q = -I_{inj} \Delta t. \quad (10)$$

[0038] Applying equations (8)-(10) into (4) and letting $\Delta t \rightarrow 0$, the following first-order differential equation is obtained:

$$\frac{dI_{inj}}{dt} + \frac{G_s + G_{fg}}{C_T(1+A_v)} I_{inj} = 0, \quad (11)$$

which leads to

$$I_{inj} = I_{inj}^0 \exp \left[-\frac{(G_s + G_{fg})t}{C_T(1+A_v)} \right]. \quad (12)$$

Equation (12) shows that the finite gain of the opamp will introduce temporal dependency in the injection current which will introduce an error in programming of the floating-gate voltage. Given the duration of the injection pulse to be t_p , the programming error can be computed as

$$\frac{\Delta V_{fg}}{V_{fg}} = \frac{\Delta I_{inj}}{I_{inj}} = \exp \left[-\frac{(G_s + G_{fg})t_p}{C_T(1+A_v)} \right]. \quad (13)$$

[0039] Figure 3 shows the measured injection current when the source voltage is varied and all the other parameters are held constant. Based on the measured data, the small signal parameter G_s, G_{fg} can be estimated to range from 0.149fS to 2.316fS when the reference current is changed between 45nA and 90nA. Hence, based on equation (13), an amplifier with a small-signal

gain of 40dB should be enough to achieve a linear injection resolution greater than 16-bit. However, the programming accuracy will also be affected by the thermal noise while injection electrons onto the floating-gate capacitor. This error is approximately given by $V_n \approx \sqrt{KT/C_T}$, where C_T is the total capacitance (including parasitics) at the floating-gate. For our implementation $C_T \approx 100fF$ which leads to $V_n \approx 200\mu V$. Measurements that show that thermal noise is indeed the limiting factor determining the accuracy of the proposed linear programming technique.

[0040] Figure 4 depicts an alternative embodiment of a non-volatile memory 40 that employs a linear hot-electron injection technique. In this arrangement, the feedback circuit is implemented using a single stage, single-ended amplifier 41 (in place of the differential amplifier shown in Figure 1). The gate of the feedback pMOS transistor 41 is connected to the source of the floating-gate transistor M_{fg} and forms a common-source amplifier biased using the current sink I_0 ; otherwise, the memory circuit operates in the manner described above. This configuration also ensures that the source, gate and drain terminals of M_{fg} are held at a constant potential during hot-electron injection. Other implementations for the feedback circuit are also contemplated by this disclosure.

[0041] Figure 5 depicts another non-volatile memory arrangement 50 having an array of memory circuits. Each memory circuit 52 is comprised of a floating gate transistor, a current reference source, a gate capacitor, a tunneling capacitor, a switch and a feedback circuit arranged in the manner described above. Each memory circuit 52 may use an operational amplifier to implement the feedback circuit. Alternatively, a single operational amplifier may be shared amongst the memory circuits 52. A controller 53 is interfaced with the switch in each of the memory circuits for controlling state thereof. In an exemplary embodiment, the controller may be implemented as a field programmable gate array (FPGA).

[0042] The circuit shown in Figure 5 has been prototyped in a 0.5- μm standard CMOS process. For this process the typical gate-oxide thickness is approximately 14 nm and the minimum drain-to-source voltage required to

trigger hot-electron injection is 4.2V. For each cell, the constant current reference is implemented using two cascaded pMOS transistors M_1 and M_2 . The source voltage V_s of the floating-gate transistor M_{fg} is given by

$$V_s = V_{dd} - nV_{bl} + n\frac{\Delta Q}{C_T}, \quad (14)$$

- 5 where n is the sub-threshold slope factor, V_{dd} and V_{bl} is the supply and biasing voltages, ΔQ is the programmed charge and C_T is total capacitance on floating-gate node. The gain requirements on the feedback amplifier is less than 40dB, which can be achieved using a single stage differential amplifier as shown in Figure 5. The programmable voltage ΔV in Figure 2B is measured using a buffer
- 10 at V_s . The digital pulses controlling the switch S_p are generated using an FPGA where during each programming cycle, S_p is disabled for 50MS and is enabled during the measurement cycle. In Figure 5, C_{tun} is a tunneling capacitor which is used for removing electrons from the floating-gate by FN tunneling. A tunable current reference has been used for generating I_{ref} on-chip which reduces the
- 15 effect of external noise on the measured results. The magnitude of I_{ref} can be varied by tuning the magnitude of an external resistor. The current reference also provides the biasing voltage for the amplifiers A (OP) and the buffer. The FG cell itself with opamp occupies only $60\mu\text{m} \times 60\mu\text{m}$ area. Table I below summarizes the specification of the fabricated programmable voltage bias
- 20 generator which has been validated using experiments described in the following sections.

TABLE I

Specifications of the Linear Injection Circuit

5

Process	0.5- μ m standard CMOS
Floating-gate capacitance	100fF
Programming range	0.1-4.1 V
Pulse-width	50ms
Maximum accuracy	13.4-bit
Minimum injection rate	6.9 μ V/cycle
Power dissipation (Programming mode)	500nW
Power dissipation (Biasing mode)	250nW

[0043] The first set of experiments was designed to measure the linear programming range for the proposed voltage bias generator. Before the injection pulses are applied for programming, the supply voltage was ramped up to 6.5V, S_p was enabled and V_s was set to a voltage greater than 4.3V using FN tunneling. The rate of injection was controlled digitally by S_p and by using different combinations of V_{ref} and I_{ref} . After each programming cycle, V_s was measured using an off-chip analog-to-digital converter. Since the least significant bit (LSB) voltage for differential non-linearity (DNL) is less than 0.4mV, the equivalent resolution is above 13.4-bit. The response verifies the hypothesis set forth above that constant injection rate can be obtained by regulating the non-linear parameters of the pMOS transistor. The deviation from the linear injection model occurs at the end points of the operating voltage is due to the finite operating range of the amplifier A. Thus, the proposed approach can achieve a rail-to-rail linear programming range which is an order of magnitude larger than any previous reported results, as shown in the comparison Table II below.

TABLE II

Performance Comparison

5

Reference	Range	Accuracy	Integration level	Array programming
This work	4V	13.4-bit	Fully on-chip	Enabled
[10]	0.13V (10-640pA)	< 8-bit	Off-chip	Enabled
[11]	0.3V (500p-1 μ A)	9-bit	Only I-V on-chip	Enabled
[12]	0.63V (6p-20 μ A)	9.5-bit	Fully on-chip	Enabled
[15]	1V	6.5-bit	Fully on-chip	No
[16]	2V	10-bit	Off-chip	No

[0044] Based on the injection model expressed by equation (2), the injection current, also known as the injection rate for the linear case, is determined by either V_{ref} or I_{ref} . The next set of experiments investigated the effect of changing V_{ref} and I_{ref} on the linear injection rate. For the first experiment, V_{ref} was held constant and different I_{ref} were used. Figure 6A shows the measured result when $V_{ref}=4.9V$ and I_{ref} was varied from 100nA to 30nA in steps of 10nA. For each biasing current, 1,000 programming cycles were applied to the FG element and the voltage reduction after each cycle was recorded. As shown in Figure 6A, all the programming response are linear and the injection rate decreases monotonically with the reduction in I_{ref} , which conforms to the previously reported results for IHEI observed in pMOS transistors.

[0045] For the next experiment, I_{ref} was held constant and different V_{ref} were used during the injection process. Figure 6B shows the measured results for the case when $I_{ref}=50nA$ and V_{ref} was varied from 5V to 4.65V in the step of 50mV. Again, the programming response is linear and the injection rate decreases monotonically with the reduction in V_{ref} .

[0046] For both the experiments, the average injection rate can be calculated using linear regression over the measured data. It can be readily shown that a slower injection rate, or a finer resolution, can be achieved with smaller V_{ref} or I_{ref} , however, at the cost of longer programming time. From the experiments, the smallest injection rate was found to be $6.9\mu\text{V}/\text{cycle}$ when $V_{ref}=4.6\text{V}$ and $I_{ref}=30\text{nA}$. The largest linear injection rate than can be achieved using the circuit in Fig. 4 is $250\mu\text{V}/\text{cycle}$ when $V_{ref}=5\text{V}$ and $I_{ref}=100\text{nA}$. Also note that increasing capacitor C_{fg} in Fig. 4 should increase the programming accuracy, but at the expense of reduced programming speed.

[0047] Measuring static-strain using a piezoelectric transducer poses a challenge since the device only responds to dynamic variations in strain. In another aspect of this disclosure, a self-powered static-strain sensor is presented to meet this challenge. The sensor uses a differential configuration to measure the cumulative energy during each strain-cycle. The principle is illustrated in Figure 7 which shows the electrical signal generated by a piezoelectric cantilever beam. The positive and negative cycles of the electrical signal correspond to the deformation of the cantilever in each direction about the natural-axis or the resting state. If the cantilever returns back to its resting state (no stored potential energy), the energy transduced during the positive strain-cycle should be equal to the energy transduced during negative strain-cycle. However, if the transducer is subjected to deformation (or subjected to static-strain), there will be a difference between the positive and negative signal cycles which if integrated and measured will signify the magnitude of static-strain.

[0048] Figure 8 depicts an exemplary architecture for the self-powered static-strain sensor 80. The sensor includes a piezoelectric transducer 82 coupled via rectifiers 83, 84 to a pair of non-volatile memory circuits 85, 86. A low-frequency model of a piezoelectric transducer is shown in Figure 8 which consists of a strain-dependent voltage source V and a decoupling capacitor. For a piezoelectric cantilever with dimensions $L \times b \times h$ and deformed according to the diagram shown in Fig. 7, the open-source voltage (V) generated across the transducer as a function of the applied mechanical force (F) is given by:

$$V = \frac{Fg_{31}}{b} = SY^E h_{g31} = \frac{SY^E d_{31}h}{\epsilon} \quad (15)$$

10 where g_{31} and d_{31} are piezoelectric constants, S is the applied mechanical strain, Y^E is the short circuit elastic modulus and ϵ is the electrical permittivity. The capacitance C is given by:

$$C = \frac{Lb\epsilon}{h} \quad (16)$$

During the positive and negative strain-cycles (see Fig. 1) the voltages generated are given by:

$$V^+(t) = \frac{S^+(t)Y^E d_{31}h}{\epsilon} \text{ and } V^-(t) = \frac{S^-(t)Y^E d_{31}h}{\epsilon} \quad (17)$$

where $S^+(t)$ and $S^-(t)$ are the time-dependent positive and negative strain variations. The static-strain (s_s) can therefore be computed according to:

$$\begin{aligned} S_s &= \frac{\int (S^+(t) - S^-(t)) dt}{\frac{\epsilon}{Y^E d_{31}h}} \\ &= \frac{\epsilon}{Y^E d_{31}h} [\int V^+(t) dt - \int V^-(t) dt] \end{aligned} \quad (18)$$

Thus, the static-strain can be computed by measuring the difference in electrical energy transduced in each of the strain-cycles.

[0049] The exemplary architecture for the self-powered static-strain sensor 80 is based on equation (18). The piezoelectric transducer 82 is configured to generate a voltage signal in response to a mechanical strain thereon. A first rectifier 83 is electrically coupled to one terminal of the piezoelectric transducer 82 and operable to extract a positive voltage V^+ from the voltage signal; whereas, a second rectifier 84 is electrically coupled to the other terminal of the piezoelectric transducer 82 and is operable to extract a negative

voltage V^- from the voltage signal. In the exemplary embodiment, the rectifiers 83, 84 are implemented by diodes although other implementations are contemplated by this disclosure. Rectified voltages are in turn used to power the pair of non-volatile memory circuits 85, 86.

5 **[0050]** In the exemplary embodiment, the non-volatile memory circuits 85, 86 are implemented using the linear hot-electron injection technique as set forth in detail above and, in particular, the memory circuit depicted in Figure 2A. During the integration mode, the switch S is open which activates the negative feedback loop formed by the opamp A and the floating-gate transistor
10 M_{fg} . The source current is held constant at I_{ref} which ensures that the source-to-gate voltage V_{sg} remains constant during injection. The opamp A ensures that the source-to-drain voltage V_{sd} is held constant. V_{cg} will linearly increase to maintain V_{fg} constant. Thus, V_{gd} is also held constant. So, according to equation (1) the injection current will remain constant. The programming is
15 enabled for a fixed duration t_2 which ensures that a fixed amount of charge is injected onto the floating-gate. During the read-out mode, the switch S_2 is closed which makes $V_{cg} = 0$. The floating-gate voltage V_{fg} of the pMOS transistor is determined by the charge injected during the integration phase and the total capacitor C_T at the floating-gate node. The change in floating gate voltage ΔV_{fg}
20 can be calculated with the following equations:

$$\Delta V_{fg} = \frac{1}{C_T} \int I_{inj} dt = \frac{I_{inj}}{C_T} \Delta t \quad (19)$$

where Δt is the duration of injection. As I_{ref} is constant $\Delta V_{fg} = \Delta V_s$ which is read through a unity-gain buffer as shown in Figure 3. The ratio I_{inj}/C_T is the slope of the integrator which will be constant making the response linear.

25 **[0051]** The integration range of the linear p-IHEI circuit was measured experimentally. The supply voltage V_{dd} was set to 6.5V, S_2 was enabled and V_s was initialized to 4.1V (using FN-tunneling). After each integration cycle, V_s was measured using an off-chip analog-to-digital converter.

Since the least significant bit (LSB) voltage for differential non-linearity (DNL) is less than 0.4mV, the equivalent resolution is above 13.4-bit.

[0052] The self-powered strain-sensor has been prototyped in a 0.5- μm standard CMOS process. A complete sensor node occupies an area of 1400 μm x 1800 μm . Seven p-IHEI injectors integrated on the chip along with voltage references, read-out circuitry, two charge pumps to generate the high voltage needed for tunneling and injection, a ring oscillator and digital control circuitry.

[0053] The low-frequency model (see Fig. 8) of the piezoelectric transducer was emulated using two discrete COTS amplifiers shown in Figure 9. The voltage levels and the magnitude of the decoupling capacitor was chosen according to equations (16). The output of the emulated piezo-transducer was connected to the memory circuits through the diode bridge as shown in Fig. 8.

[0054] In the first experiment, a signal with symmetrical positive and negative cycles was applied. Note that a minimum voltage level is required for the memory circuits to start integrating (injecting). However, this voltage level is 4.2V (for a 0.5- μm CMOS process) which can be easily generated by a piezoelectric transducer under open-load conditions. The frequency of the signal was set to 140Hz and S_2 was enabled for 5 seconds, 50 times respectively for both the memory circuit. This amounted to approximately $140 \times 5 \times 50 = 3500$ cycles of integration. The single ended output from each of the memory circuits is shown in Fig. 10. Note that the output voltage (proportional to the static-strain) is the difference between the two single-ended output. Even though the energy in the positive and negative cycles are equal, the differential output ΔV_s is not exactly zero, as shown in Fig. 10. This can be attributed to different injection rates due to mismatch in the opamp offset voltage in the memory circuits.

[0055] In the next experiment the energy of the positive cycle was increased compared to the negative cycle as shown in Fig. 11 (insert). This time, one of the memory circuit integrates at a faster rate than the other, resulting in the increase in magnitude of the differential output voltage as shown

in Fig. 11. This result validates the proof-of-concept operation of the self-powered strain-sensor.

[0056] In-vivo monitoring of mechanical strain is important in the study of osteoporosis or muscular dystrophy where the objective is to understand the progressive failure and degradation mechanisms of biomechanical structures like bones, muscles or ligaments. For example, repetitive strains greater than approximately $1500\mu\epsilon$ can lead to fatigue damage and possible stress-fractures in bone. Conversely, strain-levels lower than $500\mu\epsilon$ are thought to increase the risk of bone absorption and osteoporosis.

10 The conventional and most popular method of measuring strain in-vivo is to use a passive strain-gauge (metallic or silicon-based) where the change in the electrical resistance is modulated by the change in the electrical resistance is modulated by the change in mechanical strain. Another emerging method for in-vivo strain measurement is using fiber Bragg grating (FBG) sensors which

15 measures spectroscopic changes due to mechanical displacement of an implanted optical fiber. Even though both these techniques can precisely measure instantaneous strain-levels down to a few $\mu\epsilon$, they are passive in nature and do not provide any historical information about the strain signal which could be used for understanding progression of mechanical degradation. An example

20 of the historical information could be some measure of the strain-energy dissipated through the biomechanical structure or could be the running average of the strain signal during the entire observation period. Without historical information, the strain-measurement could be prone to ageing artifacts of the gauge and could also be prone to the degradation in the adhesion between the gauge and the biomechanical structure being monitored. In principle, passive

25 strain-gauges could be complemented with additional circuitry that continuously read, process and store the desired information. Continuous operation of the add-on circuitry could be achieved through powering using implanted energy storage devices (batteries or super-capacitors) that are periodically recharged

30 either remotely or by using scavenging energy in-vivo. However, small volume requirements of the strain-gauge sensor severely limits the capacity of energy storage and in-vivo energy harvesting devices.

[0057] In the last set of experiments, the static-strain sensor 80 was interfaced with a piezoelectric transducer and was attached to a mechanical phantom that was designed to act as a biomechanical structure. The piezoelectric transducer chosen for this experiment was a commercial PZT ceramic (PZT-5H) available from Piezo Systems Inc. Note that due to lead (Pb) content, PZT transducers are generally considered bioincompatible. However, the transducer is used in this work to demonstrate the proposed proof-of-concept, even though the design could be easily translated to a polymer based piezoelectric transducer. Also, appropriate packaging and shielding ensures that PCT transducers can be used in biomechanical studies as has been reported before. Table III summarizes the mechanical and electrical specification of the PZT transducer.

TABLE III

15 Material Specifications of the PZT-5H Transducer

Length(l)	2.5 inch
Width (w)	1.25 inch
Thickness (h)	.02 inch
Material	Lead Zirconate Titanate (PZT)
Electrodes	Nickel
Capacitance	73nF
Strain/Field(d_{31})	$-190 \times 10^{-12} \text{ m/V}$
Field /Stress(g_{31})	$-11.6 \times 10^{-3} \text{ V-m/N}$
coupling(k_{31})	0.35
Elastic Modulus (Y^E)	$5.2 \times 10^{10} \text{ N/m}^2$

[0058] As a biomechanical phantom, a plexi-glass beam to which the PZT transducer was attached is used as shown in Fig. 12. A programmable servo-motor was used to apply stress on the beam and the induced strain was measured/calibrated using a metallic strain-gauge as shown in the figure. The dynamics of the servo-motor was controlled using a PWM (Pulse Width

Modulated) signal generated by a field-programmable gate array (FPGA). By adjusting the number of PWM cycles, the forward and backward movement of the motor shaft can be accurately controlled. The output of the PZT transducer is directly connected to the sensor IC with no additional power-sources.

5 **[0059]** The mechanical calibration of the set up was performed using a 350 Ohm(R) general purpose resistance strain-gauge. The strain-gauge was connected to a Wheatstone bridge as shown in Fig. 12 and the circuit component values are shown in Table IV. Fig. 12 also shows a calibration strain-gauge used in the Wheatstone bridge, which was used to compensate for temperature variations in strain measurements. A commercial, fully differential instrumentation amplifier was used to amplify the difference in voltages across the Wheatstone bridge.

TABLE IV

15 Strain-Gauge Specifications

R	350 Ω
R ₁	1k Ω
Gauge Factor (GF)	2.11
V_{ref}	5V

[0060] Fig. 13 shows the plots of time-varying strain (of different amplitudes) that is induced in the plexi-glass beam and Fig. 15 shows the output across the PZT transducer for one specific case. It can be clearly seen in Fig. 15 that the output voltage of the transducer shows positive and negative voltage cycles that correspond to the direction of the deformation of the beam. For all the experiments, the nominal strain-levels were chosen to be consistent with the levels experienced in biomechanical structures. The output of the sensor was measured after every 10 loading cycles and measured results are shown in Fig. 14 and Fig. 16 corresponding to both the injectors. The result shows that the response of both the injectors are similar, indicating that the energy in the positive and negative strain cycles are similar. This is expected since the plexi-

glass beam is allowed to return to its resting state (zero static strain state). However, unlike conventional strain-gauges, the self-powered gauge provides a historical indicator of the L_1 norm that is proportional to the energy dissipated through the PZT and hence the plexi-glass beam. The energy is proportional to the average of the output generated by both the injectors. This historical information could be more useful for determining progression of damage in a structure than just a passive static-strain measurement.

[0061] To demonstrate that the proposed sensor IC can indeed measure quasi-static strain using a real piezoelectric transducer, the following experiment was designed. The servo-motor was programmed to generate strain-levels according to the waveform. The waveform shows that the plexi-glass beam is not allowed to return to its resting-state, implying that the measured strain at the start of the experimental run is not equal to the measured strain at the end of the experimental run. After each run, the output of the injectors are measured before the beam is subjected to a similar strain-cycle. Fig. 17A shows difference between the output of the injectors decreases with each run, which is proportional to the level of the quasi-static strain. Also the first injector measures a larger decrease in the output voltage as compared to the second injector. When the same experiment is repeated however, after swapping the input terminals of the sensor, the second injector measures a larger decrease in the output voltage (after calibrating for mismatch effects) as shown in Fig. 17B, which is consistent with the expected results.

[0062] In this disclosure, a self-powered static-strain sensor is provided using a differential configuration of a linear p-IHEI (piezo-IHEI) circuit. The sensor is powered directly from ambient strain-variations and therefore does not require any batteries. For this reason, the proposed sensor could be miniaturized and used in in-vivo and embedded monitoring application. However, the sensor requires a minimum voltage-level (or strain-level) for operation which introduces dead-zones in its response which is unlike traditional strain-gauges that can be used to measure ultra-low levels of strain. Also, the current version of the self-powered sensor suffers from mismatch due to its

analog components (rectifiers, references and floating-gate injectors) and is sensitive to temperature variations. Compensation of mismatch therefore requires post-measurement calibration. The mismatch (in injection rates) between the injectors is first estimated (using controlled mechanical excitation) and is then used for calibration.

[0063] Another important aspect is the scalability of the concept and design to deep-sub-micron and nanoscale (CMOS) processes. In this regard, note that hot-electrons require a minimum of 3.2eV to surmount the silicone-di-oxide barrier (difference in conduction band levels) and unfortunately this value does not scale with technology. For this reason, high-voltage charge-pumps would still be required at least for interrogation and programming. However, in sub-100 nm processes quantum mechanical tunneling through gate-oxide could be used instead of the hot-electron injection process. But it remains to be verified how the physics of tunneling could be exploited to obtain the functionality of the strain-gauge. Also, gate-leakage could also pose a significant data retention problem for the processes with smaller feature size.

[0064] Another important consideration is the long-term reliability of the self-powered strain-gauge. Most high-voltage failure mechanisms in a CMOS process are attributed to: (a) avalanche breakdown and (b) oxide breakdown. In avalanche breakdown, the impact ionization leads to a positive feedback process that culminates with the failure of the transistor. In this work, the avalanche process is carefully controlled by starving the source current of the transistor. As a result, the injector is a negative feedback circuit where the number of electrons injected into the oxide is significantly limited. In fact the injector has operated continuously for days without observing any failure. The second failure mechanism is due to the oxide breakdown where repeated application of high electric field creates traps finally lead to its breakdown. For the $0.5 - \mu m$ CMOS process voltages greater than 15 V are required for quantum mechanical tunneling and for creating stress related artifacts. As described earlier FN-tunneling is only used for initialization and reprogramming of the sensor which is performed very infrequently.

[0065] The foregoing description of the embodiments has been provided for purposes of illustration and description. It is not intended to be exhaustive or to limit the disclosure. Individual elements or features of a particular embodiment are generally not limited to that particular embodiment, but, where applicable, are interchangeable and can be used in a selected embodiment, even if not specifically shown or described. The same may also be varied in many ways. Such variations are not to be regarded as a departure from the disclosure, and all such modifications are intended to be included within the scope of the disclosure.

10

CLAIMS

What is claimed is:

1. A non-volatile memory arrangement, comprising:
 - 5 a floating gate transistor having a gate node and a source node;
 - a capacitor having a first terminal and a second terminal, the first terminal electrically coupled to the gate node of the floating gate transistor;
 - a current reference circuit electrically coupled to the source node of the floating gate transistor and operable to source a current therein; and
 - 10 a feedback circuit electrically coupled between the source node of the floating gate transistor and the second terminal of the capacitor, and operable to adjust a voltage at the gate node of the floating gate transistor in accordance with a source-to-drain voltage across the floating gate transistor.
- 15 2. The non-volatile memory arrangement of claim 1 wherein the current reference circuit operates to hold the source current constant, thereby ensuring that the source-to-gate voltage of the floating gate transistor remains constant.
- 20 3. The non-volatile memory arrangement of claim 1 wherein the current reference circuit is implemented by two transistors in a cascading arrangement.
- 25 4. The non-volatile memory arrangement of claim 1 wherein the feedback circuit is further defined as an operational amplifier having an inverting terminal electrically coupled to the source node of the floating gate transistor, a non-inverting terminal electrically coupled to a reference voltage and an output electrically coupled to the second terminal of the capacitor.
- 30 5. The non-volatile memory arrangement of claim 1 wherein the feedback circuit is further defined as a single-stage, single ended amplifier.

6. The non-volatile memory arrangement of claim 1 further comprises a tunnel capacitor electrically coupled to the gate node of the floating gate transistor for removing electrons from the floating gate transistor.

5 7. The non-volatile memory arrangement of claim 1 further comprises a switch electrically coupled between the second terminal of the capacitor and ground; and
a controller interfaced with the switch to control operation thereof, such that the switch is opened to inject current into the floating gate transistor and is
10 closed to remove electrons from the floating gate transistor.

8. A method for programming a non-volatile memory circuit having a floating gate transistor, comprising:
providing a feedback circuit between a source node of the floating gate
15 transistor and a first terminal of a capacitor, the second terminal of the capacitor electrically coupled to a gate node of the floating gate transistor;
injecting a current into the source node of the floating gate transistor;
adjusting dynamically, by the feedback circuit, a voltage at the gate node
of the floating gate transistor in accordance with source-to-drain voltage across
20 the floating gate transistor.

9. The method of claim 8 further comprises opening a switch to inject current into the floating gate transistor, the switch electrically coupled between the first terminal of the capacitor and ground; and closing the switch to remove
25 electrons from the floating gate transistor.

10. The method of claim 9 further comprises removing electrons from the floating gate transistor via a tunnel capacitor electrically coupled to the gate node of the floating gate transistor.

30

11. The method of claim 8 further comprises operating the floating gate transistor in weak-inversion mode when current is injected therein.

12. The method of claim 8 further comprises implementing the feedback circuit as an operational amplifier having an inverting terminal electrically coupled to the source node of the floating gate transistor, a non-inverting terminal electrically coupled to a reference voltage and an output electrically coupled to the second terminal of the capacitor.

13. A non-volatile memory arrangement comprising:
an array of memory circuits, each memory circuit includes
10 a floating gate transistor having a gate node and a source node;
a capacitor having a first terminal and a second terminal, the first terminal electrically coupled to the gate node of the floating gate transistor;
a current reference circuit electrically coupled to the source node of
15 the floating gate transistor and operable to source a current therein;
a feedback circuit electrically coupled between the source node of the floating gate transistor and the second terminal of the capacitor, and operable to adjust a voltage at the gate node of the floating gate transistor in accordance with a source-to-drain voltage across the floating gate transistor; and
20 a switch electrically coupled between the second terminal of the capacitor and ground; and
a controller interfaced with each of the switches in the array of memory circuits to control operation thereof.

14. The non-volatile memory arrangement of claim 13 wherein the current reference circuit in each memory circuit operates to hold the source current constant, thereby ensuring that source-to-gate voltage of the corresponding floating gate transistor remains constant.

15. The non-volatile memory arrangement of claim 13 wherein the current reference circuit is implemented by two transistors in a cascading arrangement.

5 16. The non-volatile memory arrangement of claim 13 wherein the feedback circuit is further defined as an operational amplifier having an inverting terminal electrically coupled to the source node of the floating gate transistor, a non-inverting terminal electrically coupled to a reference voltage and an output electrically coupled to the second terminal of the capacitor.

10

17. The non-volatile memory arrangement of claim 13 further comprises a tunnel capacitor electrically coupled to the gate node of the floating gate transistor for removing electrons from the floating gate transistor.

15 18. A self-powered static-strain sensor, comprising:
a piezoelectric member having a first and second terminal and operable to generate a voltage signal in response to a mechanical strain;

a first rectifier electrically coupled to the first terminal of the piezoelectric member and operable to extract a positive voltage from the voltage signal;

20 a first non-volatile memory circuit powered by the positive voltage received from the first rectifier, the first non-volatile memory includes

a first floating gate transistor having a gate node and a source node;

25 a first capacitor having a first terminal and a second terminal, the first terminal electrically coupled to the gate node of the first floating gate transistor;

a first current source electrically coupled to the source node of the first floating gate transistor and operable to source an injection current into the first floating gate transistor; and

30 a first feedback circuit electrically coupled between the source node of the first floating gate transistor and the second terminal of the first capacitor, and operable to adjust a voltage at the gate node of the floating

gate transistor in accordance with a source-to-drain voltage across the first floating gate transistor;

a second rectifier electrically coupled to the second terminal of the piezoelectric member and operable to extract a negative voltage from the voltage signal;

a second non-volatile memory circuit powered by the negative voltage received from the second rectifier, the second non-volatile memory includes

a second floating gate transistor having a gate node and a source node;

a second capacitor having a first terminal and a second terminal, the first terminal electrically coupled to the gate node of the second floating gate transistor;

a second current source electrically coupled to the source node of the second floating gate transistor and operable to source an injection current into the second floating gate transistor; and

a second feedback circuit electrically coupled between the source node of the second floating gate transistor and the second terminal of the first capacitor, and operable to adjust a voltage at the gate node of the second floating gate transistor in accordance with a source-to-drain voltage across the second floating gate transistor.

19. The self-powered static-strain sensor of claim 18 wherein the first current source is configured to receive the positive voltage and generate the injection current for the first floating gate transistor, and the second current source is configured to receive the negative voltage and generate the injection current for the second floating gate transistor.

20. The self-powered static-strain sensor of claim 18 wherein the first and second feedback circuits are further defined as an operational amplifier having an inverting terminal electrically coupled to the source node of the respective floating gate transistor, a non-inverting terminal electrically coupled to

a reference voltage and an output electrically coupled to the second terminal of the capacitor.

21. The self-powered static-strain sensor of claim 18 wherein the first
5 and second non-volatile memory circuits further include a tunnel capacitor electrically coupled to the gate node of the respective floating gate transistor for removing electrons from the floating gate transistor.

22. The self-powered static-strain sensor of claim 21 wherein the first
10 and second non-volatile memory circuits further include a switch electrically coupled between the second terminal of the capacitor and ground, such that the switch is closed to remove electrons from the respective floating gate transistor.

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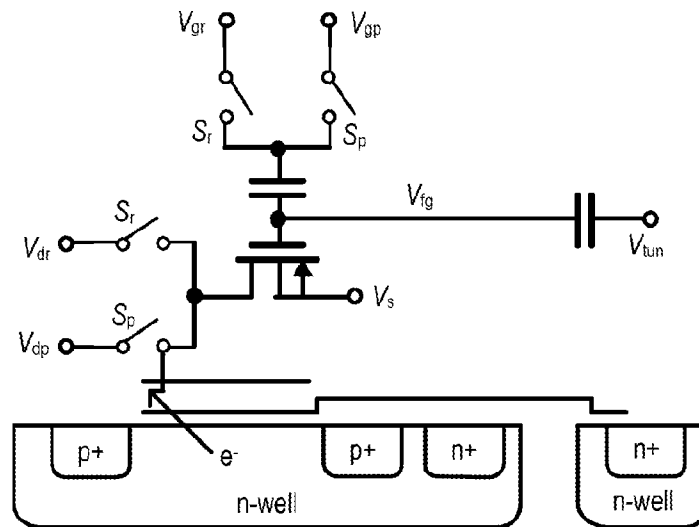


FIG. 1A

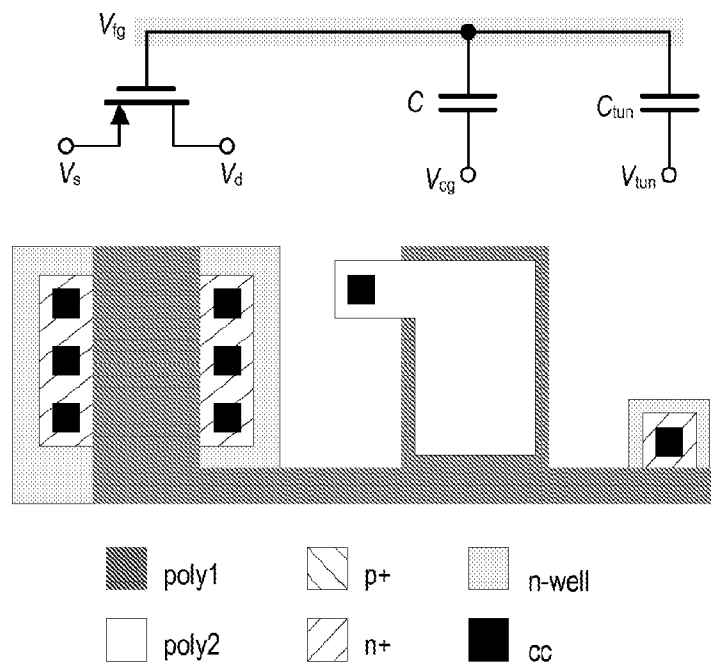
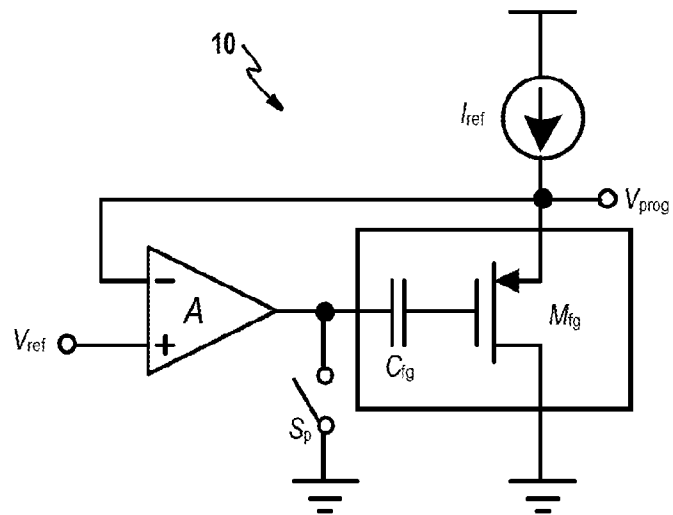
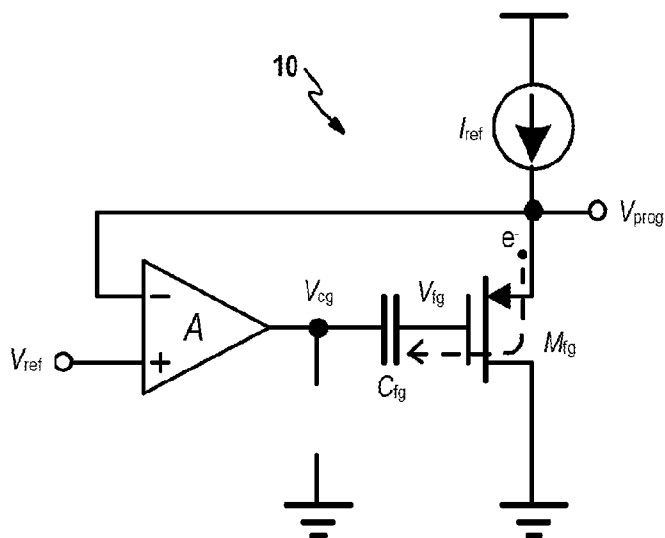
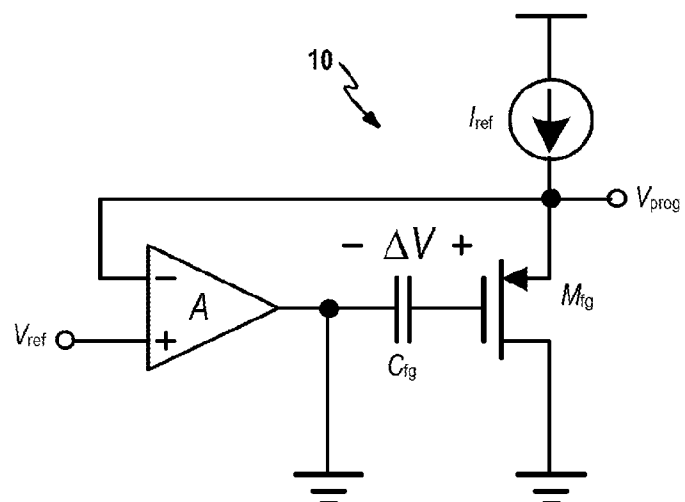
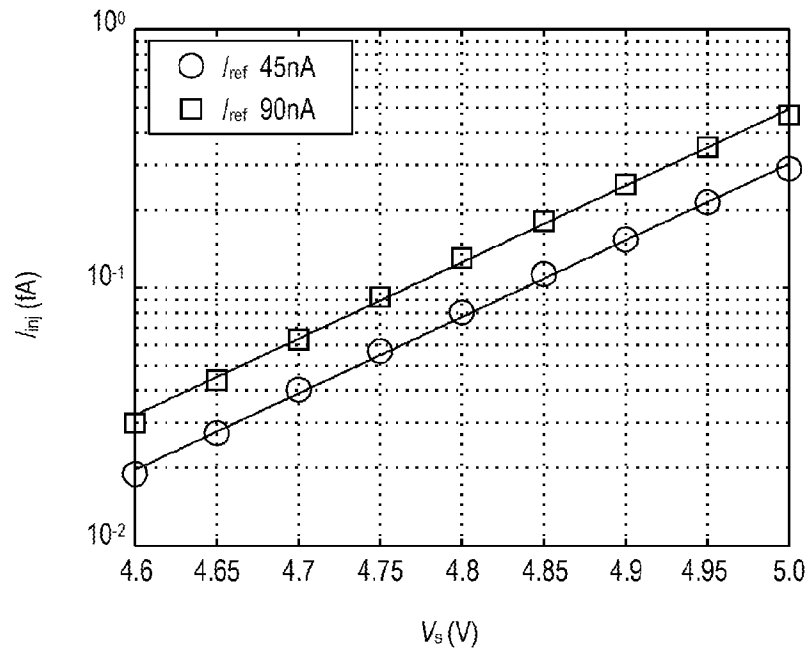
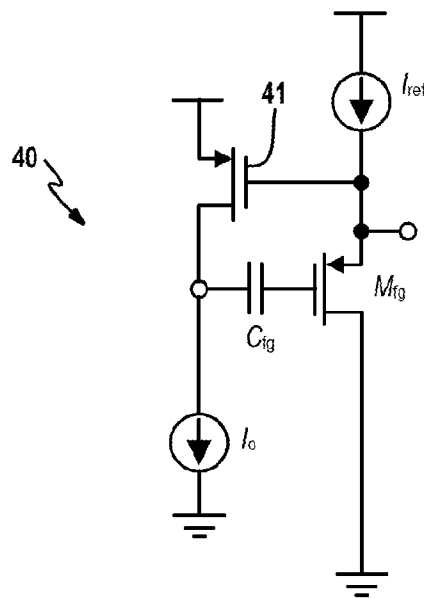


FIG. 1B

FIG. 2A**FIG. 2B****FIG. 2C**

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**FIG. 3****FIG. 4**

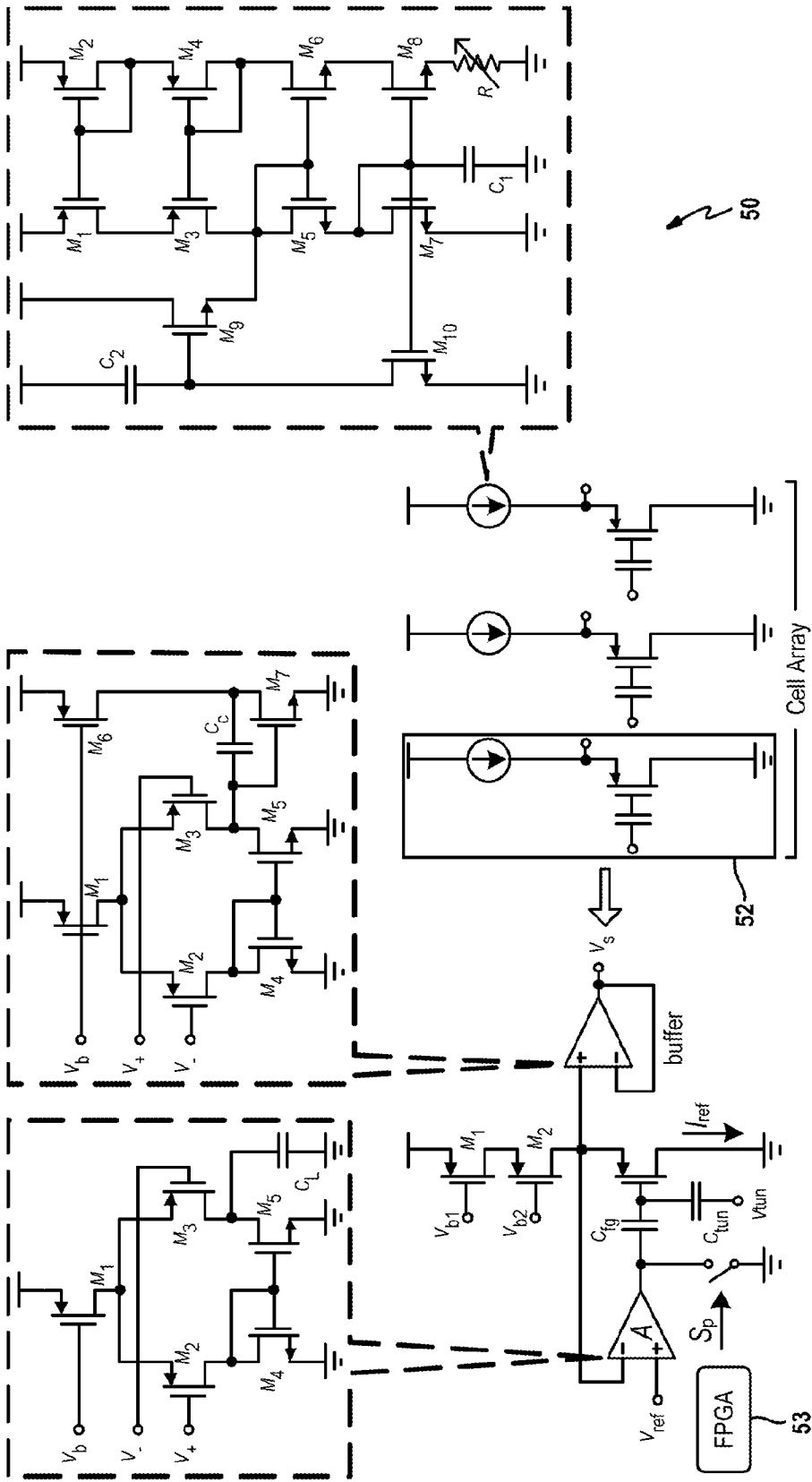
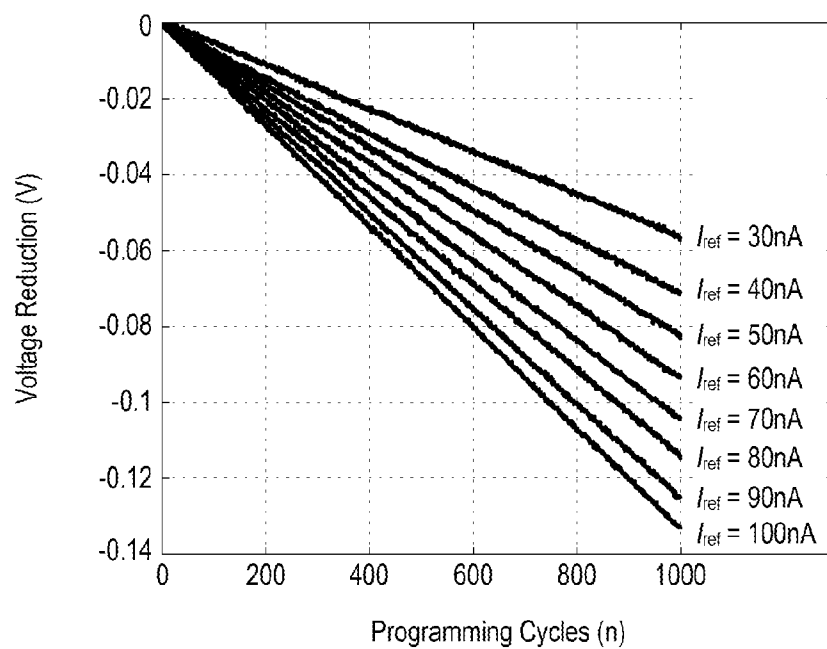
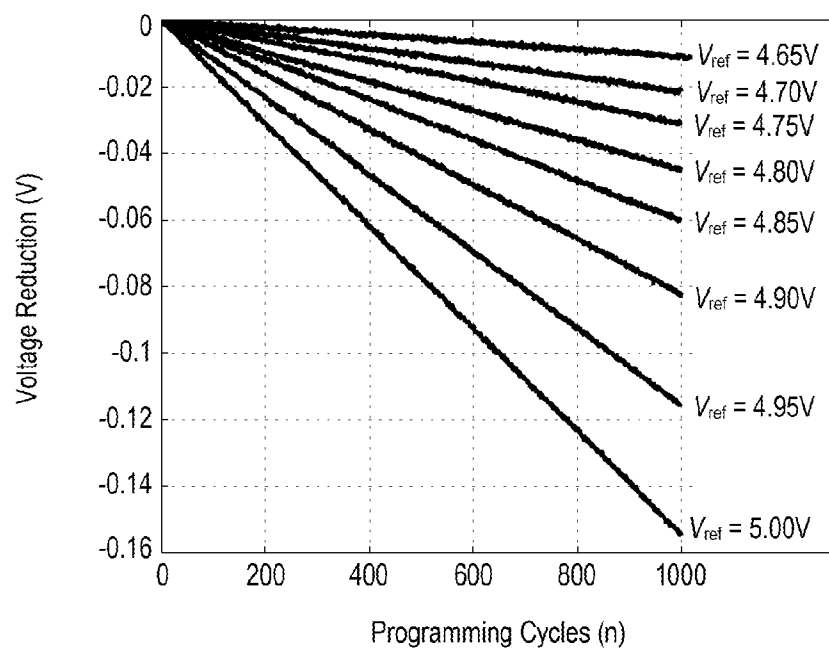
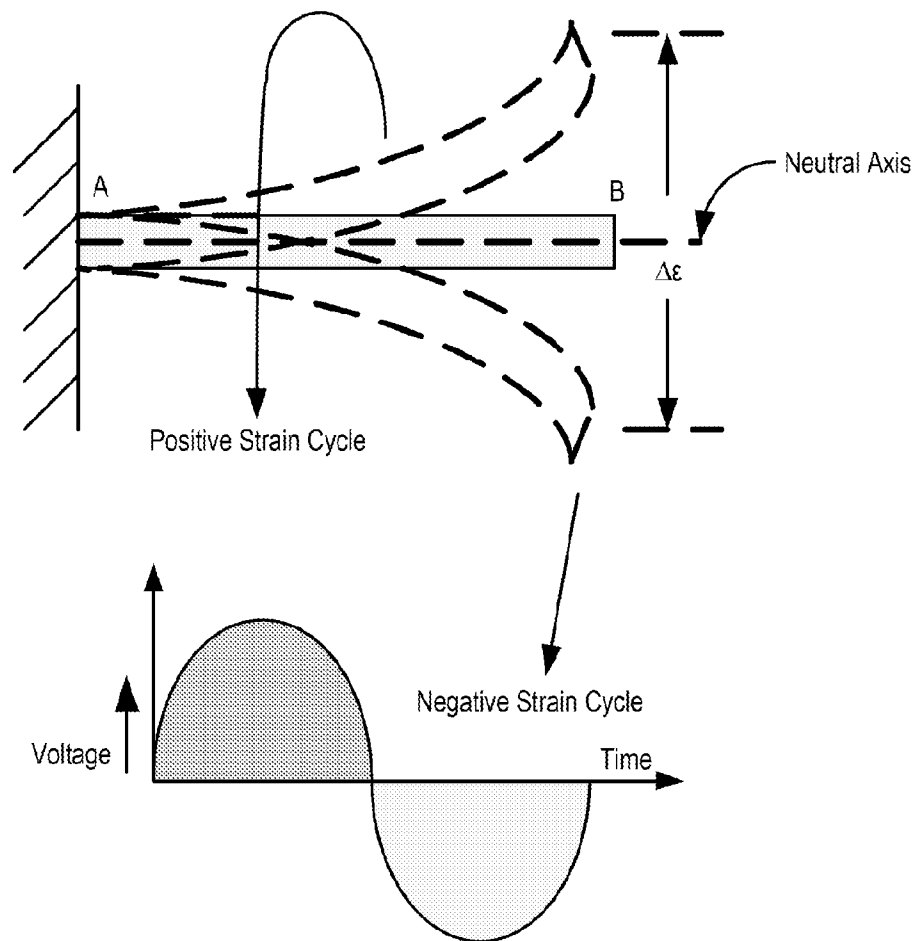


FIG. 5

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**FIG. 6A****FIG. 6B**

**FIG. 7**

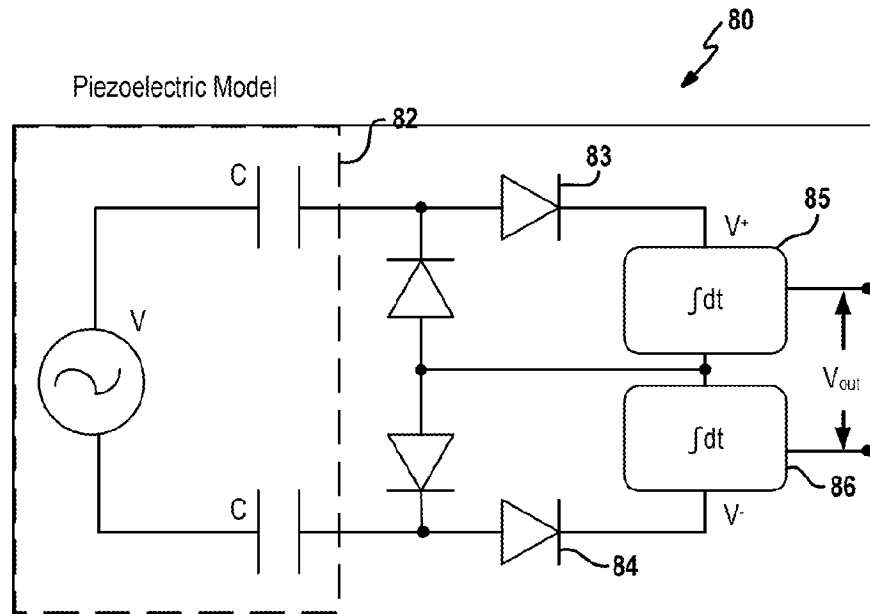


FIG. 8

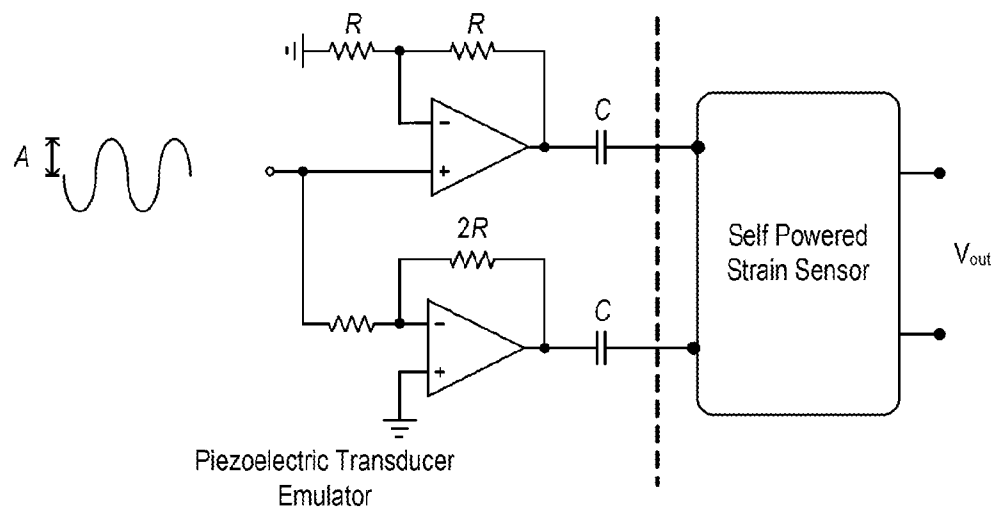
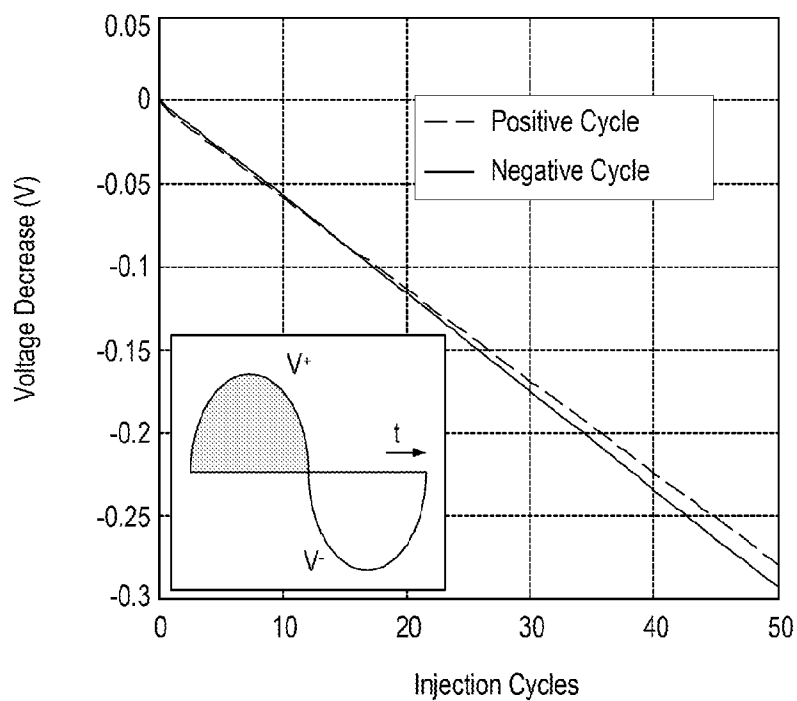
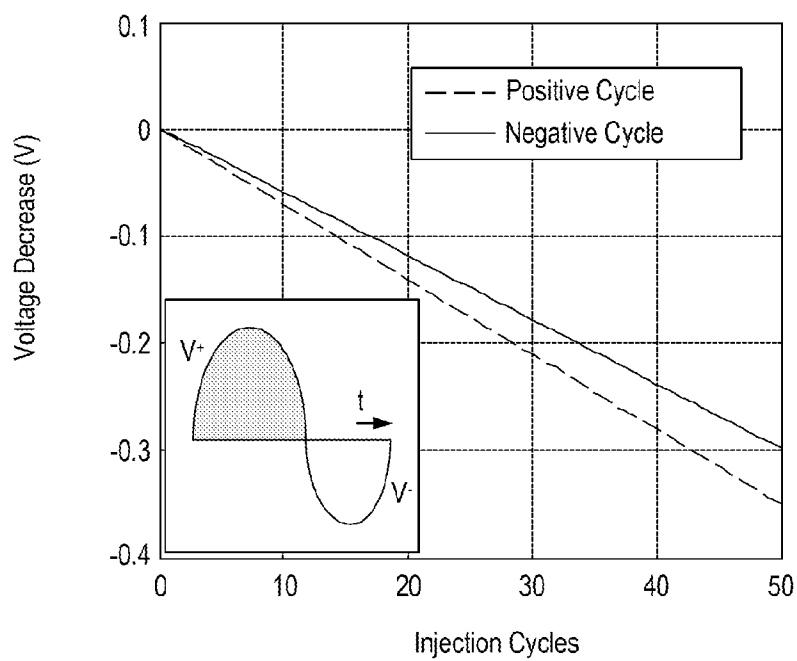


FIG. 9

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**FIG. 10****FIG. 11**

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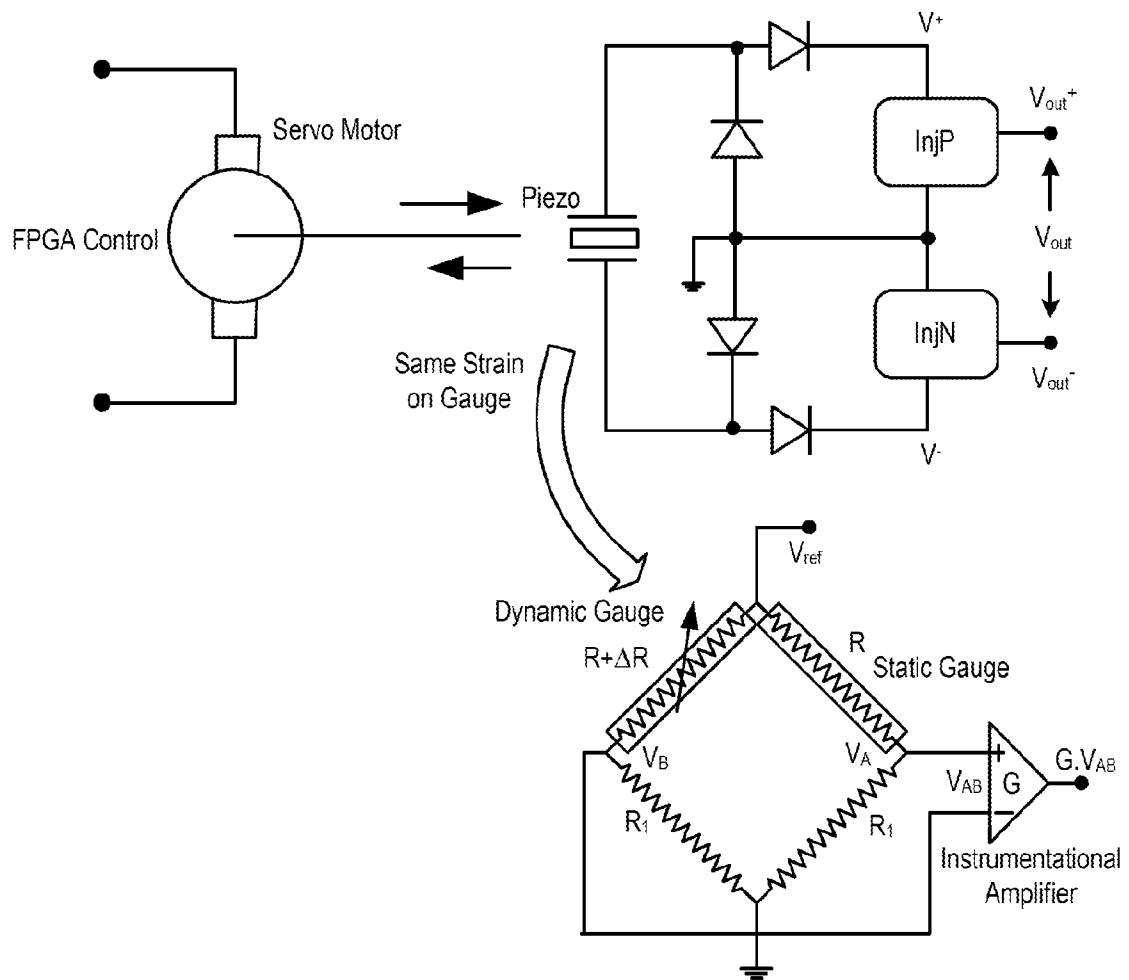
**FIG. 12**

FIG. 13A

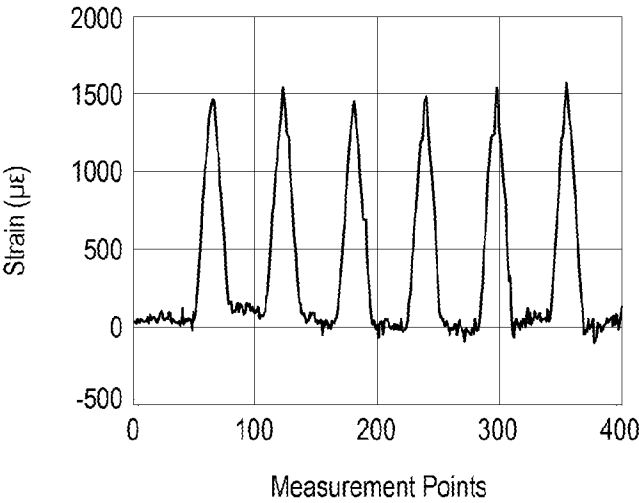
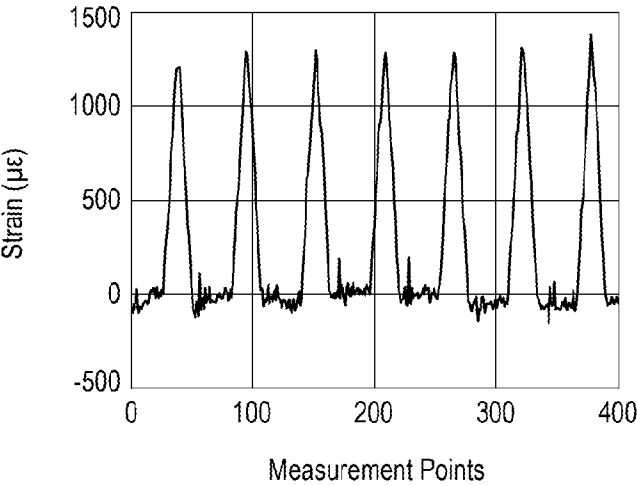
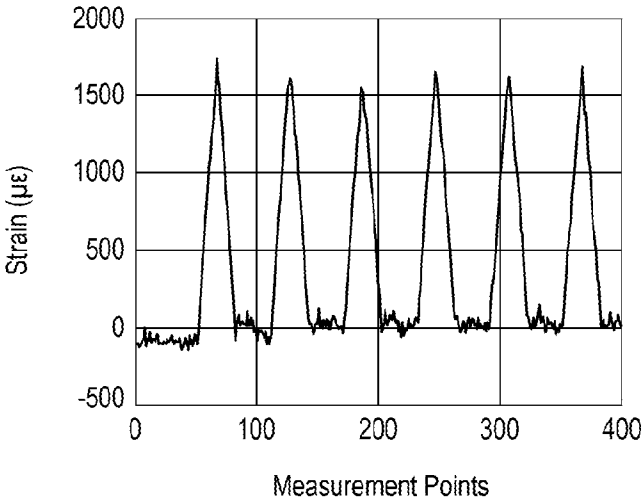


FIG. 13B

FIG. 13C



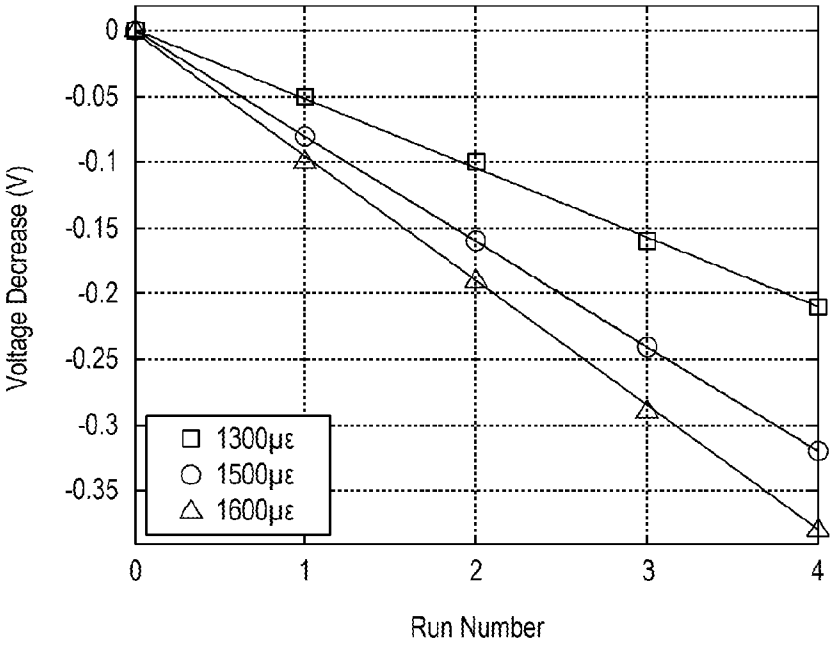


FIG. 14

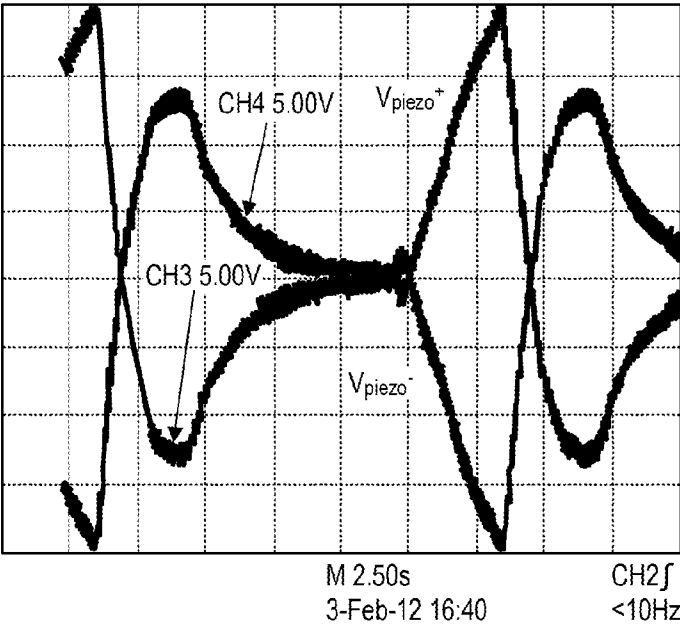
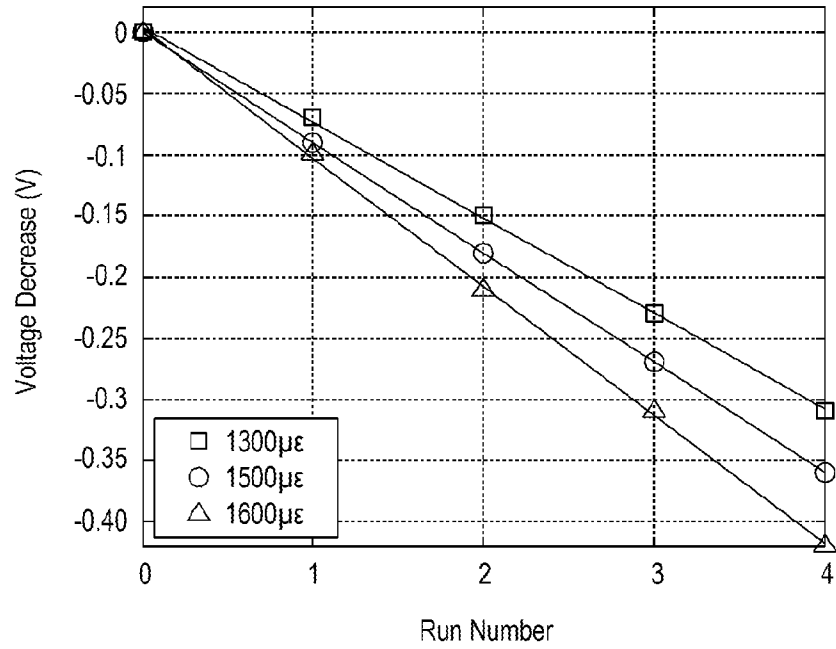
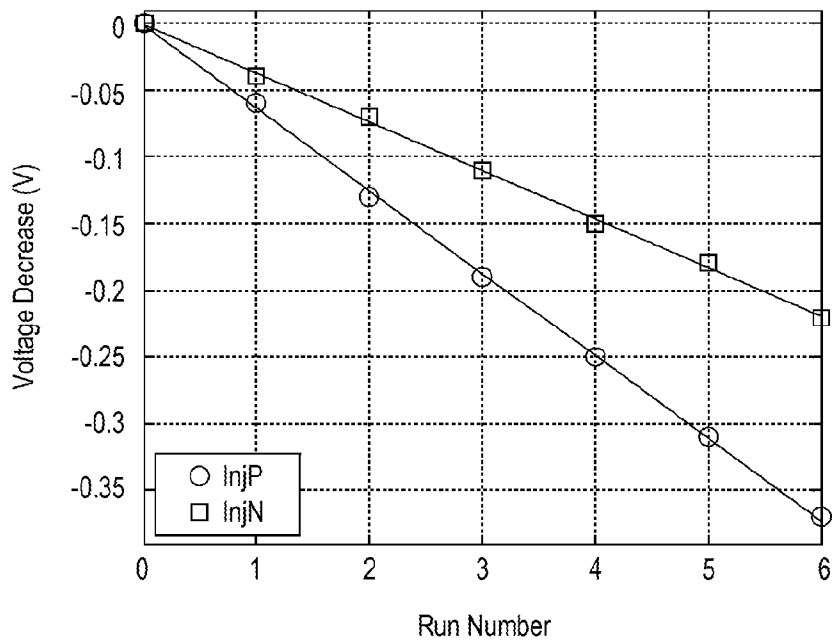
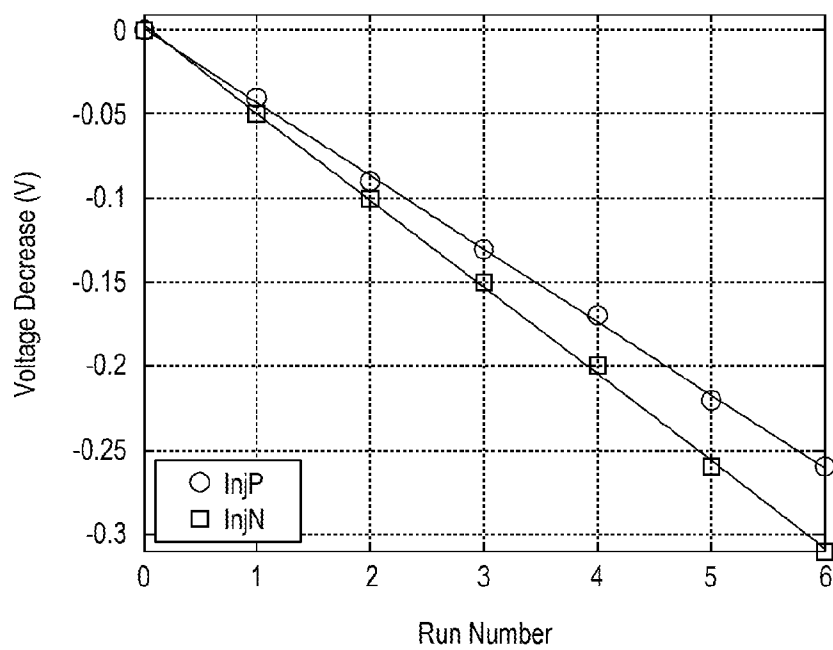


FIG. 15

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**FIG. 16****FIG. 17A**

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**FIG. 17B**

INTERNATIONAL SEARCH REPORT

International application No

PCT/US2013/023407

A. CLASSIFICATION OF SUBJECT MATTER

INV. G11C16/34 G01B7/16 G11C27/00
ADD.

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

G11C G01B

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

EPO-Internal, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 5 880 993 A (KRAMER ALAN [US] ET AL) 9 March 1999 (1999-03-09)	1,2,4, 7-9, 12-14,16
Y	column 3, line 60 - column 6, line 43;	6,10,17
A	figures 2-5	3,5,11, 15
X	----- US 6 040 996 A (KONG SIK ON [SG]) 21 March 2000 (2000-03-21) column 10, line 38 - column 13, line 45; figures 11a-13	1,8,13
Y	----- US 5 386 132 A (WONG CHUN C D [US]) 31 January 1995 (1995-01-31) column 14, line 33 - column 19, line 62; figures 16-21	6,10,17
A	column 22, line 30 - column 23, line 25; figures 25a,b	1,8,13
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Further documents are listed in the continuation of Box C.



See patent family annex.

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Date of the actual completion of the international search

21 May 2013

Date of mailing of the international search report

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Name and mailing address of the ISA/

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Fax: (+31-70) 340-3016

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INTERNATIONAL SEARCH REPORT

International application No
PCT/US2013/023407

C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT		
Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 5 200 919 A (KAYA CETIN [US]) 6 April 1993 (1993-04-06) column 3, line 45 - column 9, line 14; figures -----	1,6,8, 10,13,17
A	US 4 797 856 A (LEE WINSTON K M [US] ET AL) 10 January 1989 (1989-01-10) column 4, line 16 - column 6, line 33; figures 2-4 -----	1,8,13

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2013/023407

Box No. II Observations where certain claims were found unsearchable (Continuation of item 2 of first sheet)

This international search report has not been established in respect of certain claims under Article 17(2)(a) for the following reasons:

1. ☐ Claims Nos.:
because they relate to subject matter not required to be searched by this Authority, namely:
2. ☐ Claims Nos.:
because they relate to parts of the international application that do not comply with the prescribed requirements to such an extent that no meaningful international search can be carried out, specifically:
3. ☐ Claims Nos.:
because they are dependent claims and are not drafted in accordance with the second and third sentences of Rule 6.4(a).

Box No. III Observations where unity of invention is lacking (Continuation of item 3 of first sheet)

This International Searching Authority found multiple inventions in this international application, as follows:

see additional sheet

1. ☐ As all required additional search fees were timely paid by the applicant, this international search report covers all searchable claims.
2. ☐ As all searchable claims could be searched without effort justifying an additional fees, this Authority did not invite payment of additional fees.
3. ☐ As only some of the required additional search fees were timely paid by the applicant, this international search report covers only those claims for which fees were paid, specifically claims Nos.:
4. ☒ No required additional search fees were timely paid by the applicant. Consequently, this international search report is restricted to the invention first mentioned in the claims; it is covered by claims Nos.:

1-17

Remark on Protest

- ☐ The additional search fees were accompanied by the applicant's protest and, where applicable, the payment of a protest fee.
- ☐ The additional search fees were accompanied by the applicant's protest but the applicable protest fee was not paid within the time limit specified in the invitation.
- ☐ No protest accompanied the payment of additional search fees.

INTERNATIONAL SEARCH REPORT

International Application No. PCT/US2013/023407

FURTHER INFORMATION CONTINUED FROM PCT/SA/ 210

This International Searching Authority found multiple (groups of) inventions in this international application, as follows:

1. claims: 1-17

Floating gate memory cell with feedback loop from drain(source) terminal to control gate to effect a linear programming rate, programming method for this circuit and corresponding array of such circuits.

2. claims: 18-22

A piezoelectric strain gauge incorporating two floating gate memory cells as integrators; the difference between the stored values is proportional to the static strain of the measured object. The cells are powered by the piezo-generated electric energy.

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No

PCT/US2013/023407

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
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US 6040996 A	21-03-2000	SG 123527 A1 US 6040996 A	26-07-2006 21-03-2000
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