United States Patent [19]

Iwade

[11] **3,910,030**

[45] **Oct. 7, 1975**

[54] **DIGITAL CLOCKS**

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[52] **U.S. Cl.**..... **58/50 R;** 58/34; 58/85.5

[51] **Int. Cl.**[2].. **G04B 19/30;** G04C 9/00; G04B 9/00

[58] **Field of Search**..... 58/50 R, 34, 85.5; 340/336

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Primary Examiner—Edith Simmons Jackmon

Attorney, Agent, or Firm—Roland Plottel, Esq.

[57] **ABSTRACT**

A digital clock comprises a plurality of luminous digit display tubes which are arranged to display times, a source of clock pulse of a predetermined frequency, and electronic counter means responsive to the clock pulse for operating the digit display tubes in a predetermined sequence.

7 Claims, 20 Drawing Figures

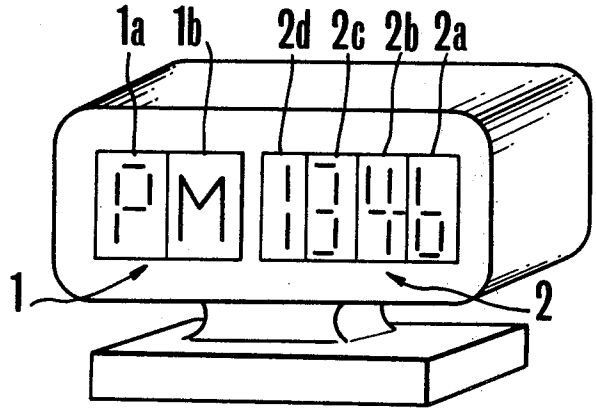


FIG. 1

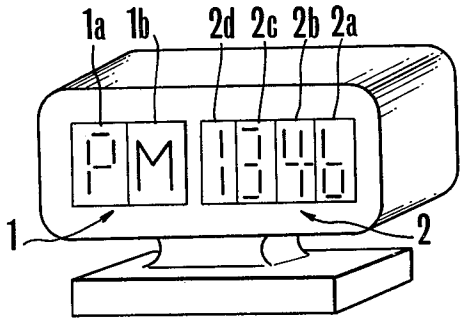


FIG. 2

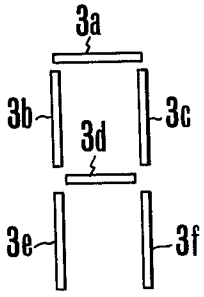


FIG. 3A



FIG. 3B

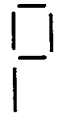


FIG. 4

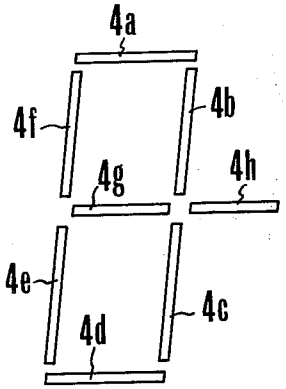
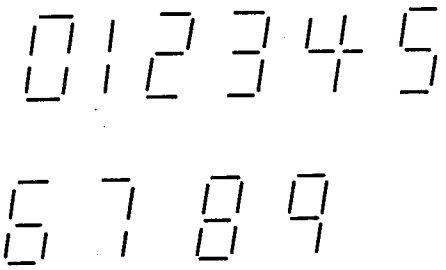


FIG. 5



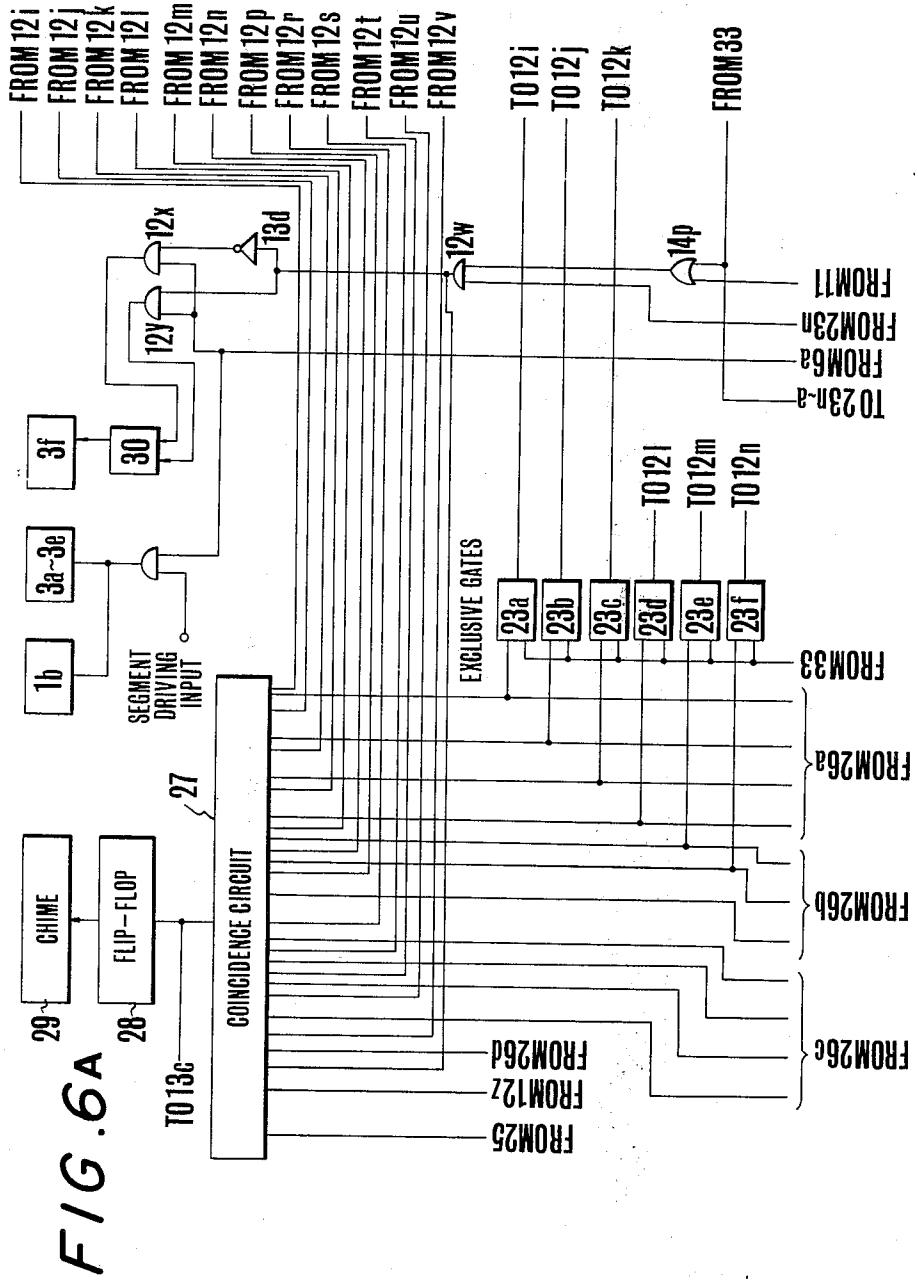

FROM 12i
FROM 12j
FROM 12k
FROM 12l
FROM 12m
FROM 12n
FROM 12p
FROM 12r
FROM 12s
FROM 12t
FROM 12u
FROM 12v
TO 12i
TO 12j
TO 12k
FROM 33
12x
13d
12w
14p
12y
FROM 11
FROM 23n
FROM 6a
TO 23n-a
3f
30
TO 12l
TO 12m
TO 12n
3a-3e
EXCLUSIVE GATES
23a
23b
23c
23d
23e
23f
1b
SEGMENT DRIVING INPUT
FROM 33
FROM 26a
27
FROM 26b
CHIME
FLIP-FLOP
COINCIDENCE CIRCUIT
FROM 26c
29
28
TO 13c
FROM 26d
FROM 12z
FROM 25

FIG. 6A

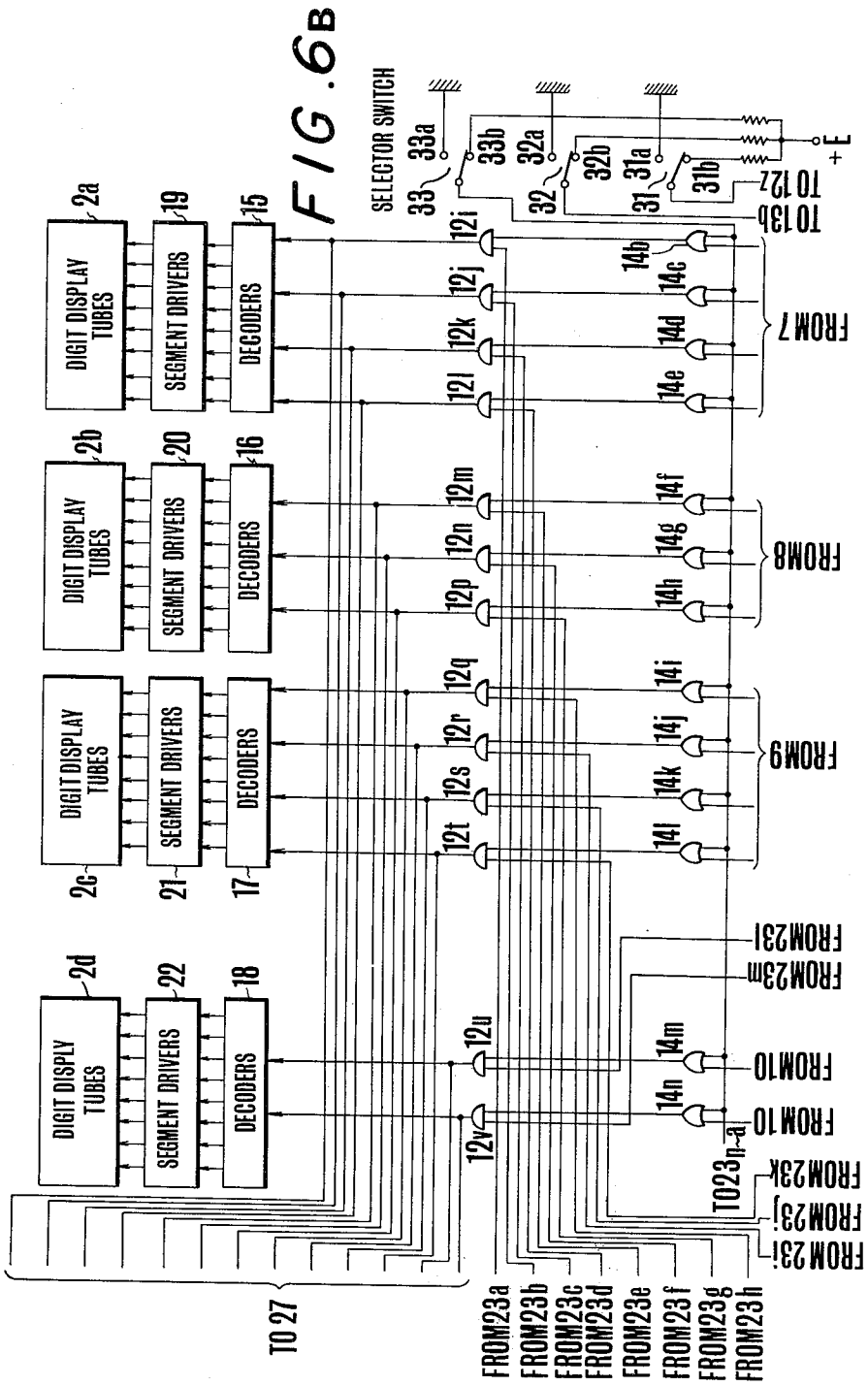

DIGIT DISPLAY TUBES
SEGMENT DRIVERS
DECODERS
SELECTOR SWITCH
TO 27
FROM23a
FROM23b
FROM23c
FROM23d
FROM23e
FROM23f
FROM23g
FROM23h
FROM23i
FROM23j
FROM23k
FROM23l
FROM23m
FROM7
FROM8
FROM9
FROM10
TO 12z
TO 13b
TO 23n-a
+E

FIG. 6B

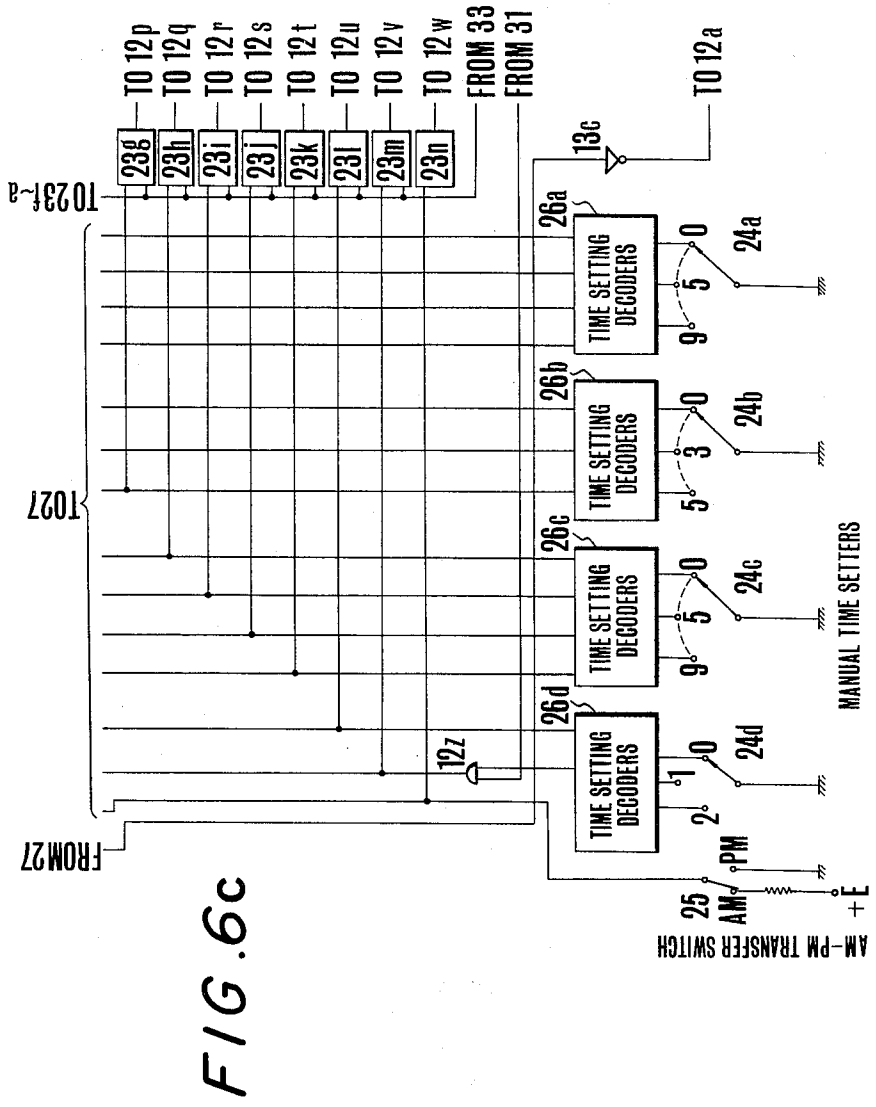

TO 12p
TO 12q
TO 12r
TO 12s
TO 12t
TO 12u
TO 12v
TO 12w
FROM 33
FROM 31
TO 12a
23g
23h
23i
23j
23k
23l
23m
23n
1023f~a
1027
FROM 27
13c
12z
26a
26b
26c
26d
TIME SETTING DECODERS
24a
24b
24c
24d
MANUAL TIME SETTERS
25
AM
PM
+E
AM-PM TRANSFER SWITCH

FIG. 6c

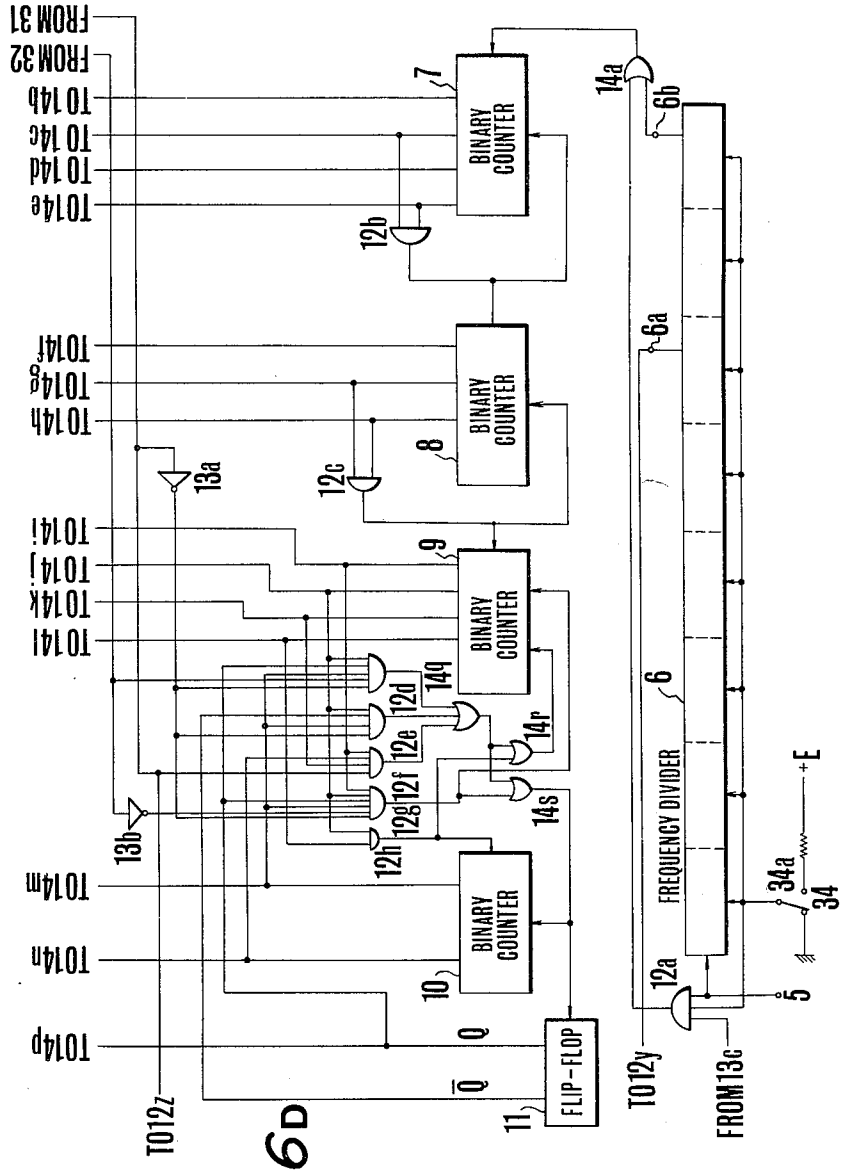

FROM 31
FROM 32
TO 14b
TO 14c
TO 14d
TO 14e
TO 14f
TO 14g
TO 14h
TO 14i
TO 14j
TO 14k
TO 14l
TO 14m
TO 14n
TO 14p
TO 12z
13a
13b
BINARY COUNTER
7
8
9
10
12b
12c
12d
12e
12f
12g
12h
14q
14r
14s
FLIP-FLOP
11
Q
$\bar{Q}$
14a
6b
6a
6
FREQUENCY DIVIDER
12a
5
34a
34
+E
TO 12y
FROM 13c

FIG. 6D

FIG.7 FIG.8 FIG.9 FIG.10 FIG.11

MINUTES	TENS	MINUTES
0 LLLL	0	LLL
1 HLLL	1	HLL
2 LHLL	2	LHL
3 HHLL	3	HHL
4 LLHL	4	LLH
5 HLHL	5	HLH
6 LHHL		
7 HHHL		
8 LLLH		
9 HLLH		

HOURS	TENS	HOURS
0 LLLL	0	LL
1 HLLL	1	HL
2 LHLL	2	LH
3 HHLL		
4 LLHL		
5 HLHL		
6 LHHL		
7 HHHL		
8 LLLH		
9 HLLH		

AM.PM	
AM	H
PM	L

FIG.12

0	LLLL
1	HLLL
2	LHLL
3	HHLL
4	LLHL
5	HLHL
6	LHHL
7	HHHL
8	LLLH
9	HLLH

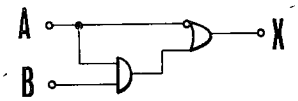
FIG. 6

Fig. 6 A	Fig. 6 B
Fig. 6 C	Fig. 6 D

FIG. 13

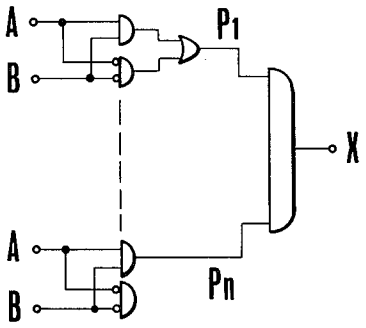
0	H	H	H	H	H	H	L	L
1	L	H	H	L	L	L	L	L
2	H	H	L	H	H	L	H	L
3	H	H	H	H	L	L	H	L
4	L	H	H	L	L	H	H	H
5	H	L	H	H	L	H	H	L
6	H	L	H	H	H	H	H	L
7	H	H	H	L	L	L	L	L
8	H	H	H	H	H	H	H	L
9	H	H	H	H	L	H	H	L

FIG. 14



$\bar{A} + A \cdot B = X$

FIG. 15



$Pn = A \cdot B + \bar{A} \cdot \bar{B}$

$X = P_1 \text{----} Pn$

DIGITAL CLOCKS

BACKGROUND OF THE INVENTION

This invention relates to a digital clock, more particularly a digital clock driven by an electronic driving circuit.

A digital clock of early stage comprises a plurality digit wheels which are arranged side by side so as to display the time, in terms of minutes, hours and or days and are driven by mechanical means such as an electric motor and gear trains. Accordingly, the adjustment of the displayed time can be accomplished relatively simply in a manner similar to ordinary clocks. However, modern digital clocks utilize luminescent display tubes, each having a plurality of luminous segments which are arranged in a predetermined pattern, for example a letter 8. A complicated electronic driving circuit is used to selectively energized the luminous segments so as to selectively display one of 10 digits 0 through 9. Accordingly, it is impossible to readily change the displayed digits as in the mechanical clocks.

SUMMARY OF THE INVENTION

Accordingly an object of this invention is to provide a novel electronic digital clock which has compact construction and is easy to operate.

It is an object of this invention to provide an improved electronic digital clock capable of adjusting at a high speed the displayed digits.

According to this invention there is provided a plurality of luminous digit display tubes which are arranged to display times, a source of clock pulse of a predetermined frequency, and electronic counter means responsie to said clock pulse for operating said digit display tubes in a predetermined sequence.

BRIEF DESCRIPTION OF THE DRAWINGS

In the accompanying drawings,

FIG. **1** shows a perspective view of a digital clock to which the invention can be applied;

FIG. **2** shows an arrangement of the luminous segments of a display tube for displaying letters A and P in the PM - AM display section;

FIGS. **3A** and **3B** show letters A and P, respectively, displayed by the display tube shown in FIG. **2**;

FIG. **4** shows an arrangement of the luminous segments of a digit display tube utilized in the time display section of the digital clock shown in FIG. **1**;

FIG. **5** shows digits **0** to **9** inclusive displayed by the digit display tube shown in FIG. **4**;

FIG. **6** shows connections between FIGS. **6A**, **6B**, **6C** and **6D** briefly explained hereunder;

FIGS. **6A**, **6B**, **6C** and **6D**, when combined in accordance with indications, show a block diagram of one embodiment of a digital clock embodying the invention;

FIGS. **7** to **11** show diagrams to explain the operations of the first to fourth binary counters and of the control flip-flop circuit shown in FIGS. **6C** and **6D**;

FIGS. **12** and **13** show the relationship between the input signals and the output signals of the decoding circuits **15** to **18** shown in FIG. **6B**;

FIG. **14** shows a connection diagram of the exclusive gate circuits utilized in FIGS. **6A** and **6C**;

FIG. **15** shows a connection diagram of the coincidence gate circuit utilized in FIG. **6A**.

DESCRIPTION OF THE PREFERRED EMBODIMENT

A digital clock shown in FIG. **1** comprises an AM - PM display section **1** including two display tubes **1a** and **1b** for displaying forenoon (AM) and afternoon (PM) and a time display section **2** including four digit display tubes **2***a*, **2***b*, **2***c* and **2***d* for displaying "minutes", "tens minutes" "hours" and "tens hours", respectively.

As shown in FIG. **2**, the display tube **1a** of the AM - PM display section **1** comprises **6** luminous segments **3***a* through **3***f*. When all of these segments are energized a letter A meaning AM is displayed as shown in FIG. **3A** whereas when segments **3***a* through **3***c* are energized a letter P meaning PM is displayed. In other words, letters A and P are selectively displayed dependent upon whether segment **3f** is energized or not.

Each of the digit display tubes **2***a* to **2***d* of the time display section **2** comprises **8** luminous segments **4***a* through **4***h* which are arranged as shown in FIG. **4** and by the selective energization of these luminous segments it is possible to display any one of digits **0** through **9** as shown in FIG. **5.**

As shown in FIGS. **6A**, **6B**, **6C** and **6D**, the digital clock of this invention comprises an input terminal **5** which is connected to receive a clock pulse of 1 MHz from a crystal oscillator, not shown, and a frequency divider **6** which is connected to receive the 1 MHz clock pulse for delivering a 1 Hz pulse to output terminal **6***a* and a 1/**60** Hz pulse to output terminal **6***b*. To display the time, there are provided a first 4 bit binary counter **7** which operates as shown in FIG. **7** for displaying "minutes," a second 3 bit binary counter **8** which operates as shown in FIG. **8** for displaying "tens minutes," a third 4 bit binary counter **9** which operates as shown in FIG. **9** for displaying "hours" a fourth 2 bit binary counter **10** which operates as shown in FIG. **10** for displaying "tens hours" and a control flip-flop circuit **11** which operates to control the luminous segment **3***f* of the display tube **1***a* of the AM - PM display section **1** in a manner shown in FIG. **11.** There are also provided AND gate circuits **12***a* through **12***z*, NOT gate circuits **13***a* through **13***d*, OR gate circuits **14***a* through **14***s*, first to fourth decoders **15** through **18** for "minutes," "tens minutes," "hours" and "tens hours" which are connected to first to fourth segment drivers **19** through **22** respectively for "minutes," "tens minutes," "hours" and "tens hours."

The outputs of segment drivers **19** through **22** are connected to respective luminous segments of digit display tubes **2***a* to **2***d* respectively. There are provided exclusive gate circuits **23***a* through **23***n*, each having a construction as shown in FIG. **14,** manual time selectors **24***a* through **24***d* for setting "minutes", "tens minutes", "hours" and "tens hours" respectively, a AM - PM transfer switch **25** for controlling the energization of the luminous segment **3f** of the diaplay tube **1***a*, time setting decoders **26***a* through **26***d* for "minutes", "tens minutes", "hours" and "tens hours," respectively, a coincidence gate circuit **27** having a construction as shwon in FIG. **15,** a flip-flop circuit **28,** - a chime **29,** and a flip-flop circuit **30** for controlling luminous segment **3***f* of the display tube **1***a* of the AM - PM display section **1.**

31 designates a first selector switch provided with a stationary contact **31***a* for use in clocks for displaying 12 o'clocks and a stationary contact **31***b* for use in

clocks for displaying 24 o'clocks, 32 designates a second selector switch provided with a stationary contact 32*a* for setting the noon at 12 o'clock, and a stationary contact for setting the noon at 0 o'clock, and 33 designates a display selector switch provided with a stationary contact 33*b* for displaying on the AM - PM display section 1 and the time display section 2 the time set by the manual time setters 24*a* through 24*d* for "minutes", "tens minutes," "hours" and "tens hours" respectively, and by the AM - PM transfer switch 35, and an idle stationary contact 33*a* which does not display any time. 34 designates a manual switch which is used to open AND gate circuit 12*a* for supplying the clock pulse directly to the first binary counter 7 when it is operated to manually set the time.

In operation, the 1 MHz clock pulse supplied to input terminal 5 enters into frequency divider 6 which supplies a pulse of 1/60 Hz to the first binary counter 7 via output terminal 6h and OR gate circuit 14*a*. In response to this pulse, the binary counter 7 operates in a manner as shown in FIG. 7 and when its content reaches LHLH, AND gate circuit 12*b* is opened to reset the first binary counter 7 and to supply the content of the first binary counter 7 to the second binary counter 8. The second binary counter 8 continues its operation until its content reaches LHH at which time AND gate circuit 12*c* is opened to reset the second binary counter 8 and to supply the content thereof to the third binary counter 9. Accordingly, the third binary counter 9 operates in a manner as shown in FIG. 9 and when its content reaches LHLH AND gate circuit 12*h* is opened to reset the third binary counter 9 and to supply the content thereof to the fourth binary counter 10.

A. 12 o' clock clock wherein the noon is displayed as 0 o'clock

The first selector switch 31 is thrown to the stationary contact 31*a* for establishing a L level and the second selector switch 32 is thrown to the stationary contact 32b for establishing a H level. After displaying the times AM1, AM2, AM3 . . . , the third binary counter 9 operates. AND gate circuit 12*d* is opened when the content of the third binary counter 9 reaches LHLL which shows 2, when the content of the fourth binary counter 10 reaches HL which shows 1 and when the control flip-flop circuit 11 assumes H level which shows AM, whereby the third binary counter 9 is reset via OR gate circuit 14*r*, the fourth binary counter 10 is reset through OR gate 14*s*, and the control flip-flop circuit 11 is set to the L level state which shows the PM. In this manner, after displaying the noon as PM"O" and thence the times PM1, PM2 . . . , when the control flip-flop circuit 11 is set to level L which shows PM, AND gate circuit 12*a* opens when the content of the third binary counter 9 reaches LHLL which shows 2 and when the content of the fourth binary counter 10 reaches HL which shows 1. Opening of the AND gate circuit 12c displays the times AM1, AM2 . . . in the same manner as above described. In this manner, the clock can operate as a 12 o'clock wherein the noon is displayed as 0 o'clock.

B. 24 o'clocks clock wherein the noon is displayed as 12 o'clocks

The first selector switch 31 is thrown to stationary contact 31*b* to establish H level and the second selector switch 32 is thrown to stationary contact 32*a* to establish L level. After displaying the times AM1, AM2 . . . the third binary counter 9 operates. When its content reaches HHLL which represents 3, AND gate circuit 12*g* is opened when the content of the fourth binary counter 10 reaches HL which represents 1. Consequently the third and fourth binary counters 9 and 10 continue to count without being reset and the control flip-flop circuit 11 is set to L level which represents PM. Consequently, the display in the AM - PM display section is changed from AM to PM so that thereafter times PM13, PM14 . . . are sequentially displayed.

Then when the third binary counter 9 operates to arrange its content to HLHL which represents 5, AND gate circuit 12*f* is opened when the content of the fourth counter 10 reaches LH which represents 2 whereby the third binary counter 9 is reset via OR gate circuits 14*q* and 14*r*, the fourth binary counter 10 is reset via OR gate circuit 14*s* and the control flip-flop circuit 11 is set to L level representing AM. Accordingly, the display in the AM - PM section is changed to AM, and thereafter times AM1, AM2 . . . are sequentially displayed. In this manner, the clock operates as 24 o'clocks clock wherein the noon is displayed as 12 o'clock.

C. 12 o'clocks clock wherein the noon is displayed as 12 o'clocks

The first selector switch 31 is thrown to stationary contact 31*a* for establishing L level. After displaying the times AM1, AM2 . . . the third binary counter 9 operates. When the content thereof reaches HHLL which represents 3, when the content of the fourth binary counter 10 reaches HL which represents 1 and when the control flip-flop circuit 11 assumes H level which represents AM, AND gate circuit 12*g* is opened whereby the fourth binary counter 10 is reset via OR gate circuit 14*s* and the control flip-flop circuit 11 is set to level L which represents PM. Consequently, the display in the AM - PM display section 1 is changed to PM displaying afternoon. Thereafter, times PM1, PM2 . . . are displayed sequentially. When the content of the third binary counter 9 reaches LHLL which represents 2 and when the content of the fourth binary counter 10 reaches HL which represents 1, AND gate circuit 12*c* is opened whereby the display in the AM - PM display section is changed to AM representing forenoon and thereafter times AM1, AM2 . . . are displayed sequentially. In this manner, the clock can operates as a 12 o'-clocks clock wherein the noon is displayed as 12 o'-clocks.

As above described first to fourth binary counters 7 through 10 and control flip-flop circuit 11 operate in a manner as shown in FIGS. 7 through 11, and the outputs of these circuit elements are applied to decoders 15 through 18 via OR gate circuits 14*b* through 14*p* and AND gate circuits 12*i* through 12*w*. The decoders 15 through 18 operate as shown in FIG. 13 so that their outputs luminesce respective luminous segments of digit display tubes 2*a* through 2*d* of the time display section 2 via segment drivers 19 through 22, respectively thereby selective by displaying the digits 0 to 9 shown in FIG. 5.

AND gate circuit 12*i* through 12*w* operates as follows. When the display selector switch 33 is thrown to stationary contact 33*a* to establish L level, the two inputs to each one of exclusive gate circuits 23*a* through 23*n* assume L level to provide an output of H level.

These H level outputs are supplied to one inputs of respective AND gate circuits **12***i* through **12***w* so that these AND gate circuits are opened by the pulses applied to the other inputs thereof.

When AM and PM are displayed for displaying forenoon and afternoon, as the display tubes **1***a* and **1***b* of the AM - PM section **1** are driven by a 1 Hz pulse having a period of one second which is supplied through output terminal **6***a* of the frequency divider **6** these display tubes are caused to flicker at a frequency of one per second.

The luminous segment **3***f* of the display tube **1***a* of the AM - PM section **1** is energized when the output terminal Q of the controlled flip-flop circuit **11** assumes H level, which is applied to luminous segment **1***b* via OR gate circuit **14***p*, AND gate circuits **12***w* and **12***y* and flip-flop circuit **30.**

When the output terminal Q of the control flip-flop circuit **11** assumes H level or when its output terminal Q assumes L level, OR gate circuit **14***p* and AND gate circuit **12***w* produce outputs of L level which are converted into a signal of H level by the operation of NOT gate circuit **13***d* to reset flip-flop circuit **30** via AND gate circuit **12***x* thus deenergizing the luminous segment **3***f*.

In this manner AM and PM respectively representing forenoon and afternoon are alternatively displayed and the displays AM and PM are caused to flicker once per second.

Time adjustments are performed in the following manner.

The AM - PM transfer switch **25** is operated to select forenoon AM or afternoon PM. Then, manual time selectors **24***a* through **24***d* are operated to set any desired time. The outputs of the manual time selectors **24***a* through **24***d* are decoded by the time setting decoders **26***a* through **26***d* as shown in FIGS. **7** through **10** and the outputs of these decoders are applied to exclusive gate circuits **23***a* through **23***n*.

When manual switch **34** is thrown to stationary contact **34***a*, the frequency divider **6** will be reset by the clock pulse and the clock pulse will be impressed upon first to fourth digital counters **7** through **10** via AND gate circuit **12***a* thereby operating these counters at a high speed.

On the other hand, when the display selector switch **33** is thrown to the stationary contact **33***b* to establish H level which is applied to one inputs of respective exclusive gate circuits **23***a* through **23***n*. Further, as the signal representing AM or PM selected by the AM - PM transfer switch **25** and the signals representing the times which have been set by the manual time setters **24***a* through **24***d* are applied to the other inputs of the exclusive gate circuits **23***a* through **23***n* they produce outputs of H level which are applied to one inputs of AND gate circuits **12***i* through **12***w*. Consequently, the outputs from the first to fourth binary counters **7** through **10** and from the control flip-flop circuit **11** are applied to the display tubes of the AM - PM display section **1** and the time display section **2** thereby displaying AM or PM together with time. The outputs from binary counters **7** through **10** and from the control flip-flop circuit are also applied to the coincidence circuit **27** whereby the coincidence of the outputs from the AM - PM transfer switch **25**, time setters **24***a* through **24***d*, control flip-flop circuit **11** and first to fourth binary counters **7** through **10** is determined. The coincidence output from the coincidence circuit **27** is sent to chime **29** via flip-flop circuit **28** thereby operating the chime. The coincidence output is also sent to AND gate circuit **12***a* via NOT gate circuit **13***c* thereby closing AND gate circuit **12***a*. Closure of the AND gate circuit **12***a* terminates the high speed time adjusting operation provided by the first to fourth binary counters **7** through **10** and the control flip-flop circuit **11.** Immediately thereafter, manual switch **34** is thrown to stationary contact **34***b* thereby restoring the normal operation of the frequency divider **6** to close AND gate circuit **12***a*. Thereafter, the normal time display operation is performed.

Although, in the foregoing description, first to fourth binary counters were assumed to have different number of bits it will be clear that they can have the same number of bits.

Furthermore, it will be clear that the AM - PM display section may be caused to flicker at any desired frequency other than once per second.

As above described, the invention provides a novel digital clock in which the time displayed by digit display means can be adjusted at a high speed.

Although the invention has been shown and described in terms of its preferred embodiment it will be clear that the invention is by no means limited thereto but many changes and modifications will be obvious to one skilled in the art without departing from the true spirit and scope of the invention.

What is claimed is:

1. A digital clock comprising

a plurality of digit display means arranged to display times,

a source of clock pulses,

first means responsive to said clock pulses for producing a first output to operate said digit display means in a predetermined sequence,

manual means including means for entering desired times to be displayed coupled to said first means to produce a second output from said first means to operate said first means in the same sequence but at a high speed for rapidly changing the time displayed by said digit display means, and

coincidence means for comparing said times displayed by said digit display means and said desired times in said means for entering and for discontinuing said second output from said first means on coincidence.

2. A digital clock comprising a plurality of digit display means arranged to display times, a source of clock pulse of a predetermined frequency, a frequency divider for converting said clock pulse into a pulse of lower frequency, binary counter means for counting said pulse of lower frequency for operating said digit display means in a predetermined sequence, manually operated time setting means, means controlled by said manually operated time setting means for causing said binary counter means to count said clock pulse, a coincidence circuit for detecting the coincidence between the desired times in said manually operated time setting means and the content of said counter means and for controlling said controlled means to stop said binary counter means from counting said clock pulse.

3. The digital clock according to claim **2** wherein means is provided including logic input and manual switch to cause said clock to operate either a 24 o'clocks clock or a 12 o'clocks clock.

4. The digital clock according to claim 2 which further comprises display tubes for selectively displaying AM and PM.

5. The digital clock according to claim 4 which further comprises means for flickering the display of said AM and PM at a predetermined frequency.

6. The digital clock according to claim 2 wherein said digital display means comprises four luminous display tubes for displaying minutes, tens minutes, hours and tens hours respectively, each of said luminous display tubes including a plurality of luminous segments which are selectively energized to display any one of ten digits 0 through 9, and wherein said binary counter means comprises four serially connected binary counters each for controlling each of said luminous display tubes.

7. A digital clock comprising a plurality of digit display means adapted to display a time, a source of clock pulse of a predetermined high frequency, means for generating low frequency pulses from said source, counter means responsive to said low frequency pulse for producing in predetermined sequence outputs which in turn operate said plurality of digital display means, a plurality of manually operated time setting means for setting a desired time, manually operated switch means for causing said counter means to operate at a high speed by said clock pulse, and a coincidence circuit for detecting the coincidence between the outputs of said manually operated time setting means and said counter means and for disabling said manually operated switch means by the output of said coincidence circuit, whereby the time to be displayed on said plurality of digit display means is rapidly adjusted.

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