(12) **United States Patent**
You et al.

(10) **Patent No.: US 9,553,098 B2**
(45) **Date of Patent: *Jan. 24, 2017**

(54) **SEMICONDUCTOR DEVICES INCLUDING SEPARATE LINE PATTERNS**

(71) Applicant: **Samsung Electronics Co., Ltd.**, Suwon-si, Gyeonggi-do (KR)

(72) Inventors: **Jang-Hyun You**, Seoul (KR); **Hyeong Park**, Hwaseong-si (KR); **Bongtae Park**, Seoul (KR); **Jeehoon Han**, Hwaseong-si (KR)

(73) Assignee: **Samsung Electronics Co., Ltd.** (KR)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

This patent is subject to a terminal disclaimer.

(21) Appl. No.: **14/858,756**

(22) Filed: **Sep. 18, 2015**

(65) **Prior Publication Data**

US 2016/0013196 A1 Jan. 14, 2016

Related U.S. Application Data

(63) Continuation of application No. 14/200,610, filed on Mar. 7, 2014, now Pat. No. 9,171,853.

(30) **Foreign Application Priority Data**

Mar. 7, 2013 (KR) 10-2013-0024622

(51) **Int. Cl.**

H01L 27/115	(2006.01)
H01L 23/528	(2006.01)
H01L 23/532	(2006.01)
H01L 29/423	(2006.01)
H01L 29/49	(2006.01)

(Continued)

(52) **U.S. Cl.**

CPC ***H01L 27/11521*** (2013.01); ***H01L 23/528*** (2013.01); ***H01L 23/53209*** (2013.01); ***H01L 27/11519*** (2013.01); ***H01L 27/11548*** (2013.01); ***H01L 29/42324*** (2013.01); ***H01L 29/4933*** (2013.01); ***H01L 29/513*** (2013.01); ***H01L 29/7883*** (2013.01); *H01L 27/11524* (2013.01); *H01L 2924/0002* (2013.01)

(58) **Field of Classification Search**

CPC H01L 27/11521; H01L 27/11519; H01L 27/11548

See application file for complete search history.

(56) **References Cited**

U.S. PATENT DOCUMENTS

4,004,159 A * 1/1977 Rai H01L 29/7886 257/316
7,151,040 B2 12/2006 Tran et al.
7,298,005 B2 11/2007 Yoshikawa

(Continued)

FOREIGN PATENT DOCUMENTS

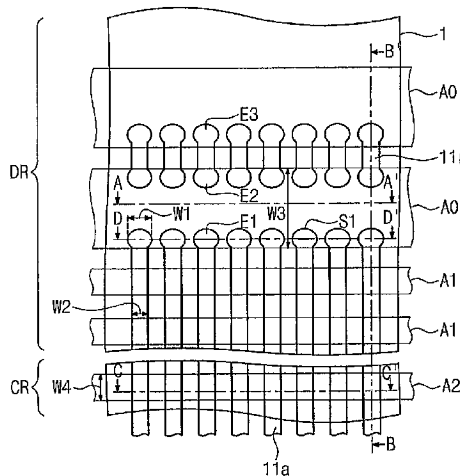
JP 2006-156657 6/2006
JP 2010-087263 4/2010

Primary Examiner — Mark Prenty
(74) *Attorney, Agent, or Firm* — Myers Bigel, P.A.

(57) **ABSTRACT**

A semiconductor device includes a plurality of lines disposed on a semiconductor substrate, and remaining line patterns disposed spaced apart from the lines on extensions from the lines. The lines include first end-portions adjacent to the remaining line patterns. The remaining line patterns include second end-portions adjacent to the lines. The first end-portions and second end-portions are formed to have mirror symmetry with respect to each other.

29 Claims, 26 Drawing Sheets



(51) **Int. Cl.**

H01L 29/51	(2006.01)
H01L 29/788	(2006.01)

(56) **References Cited**

U.S. PATENT DOCUMENTS

7,790,531	B2	9/2010	Tran	
8,076,205	B2	12/2011	Maekawa	
8,158,476	B2	4/2012	Tran et al.	
8,183,148	B2	5/2012	Aburada et al.	
8,216,938	B2	7/2012	Lee et al.	
8,368,182	B2	2/2013	Lee et al.	
8,461,053	B2	6/2013	Chen et al.	
9,171,853	B2 *	10/2015	You	H01L 27/11521
2009/0065956	A1	3/2009	Colburn et al.	
2011/0062595	A1	3/2011	Sim et al.	
2014/0252444	A1	9/2014	You et al.	

* cited by examiner

Fig. 1A

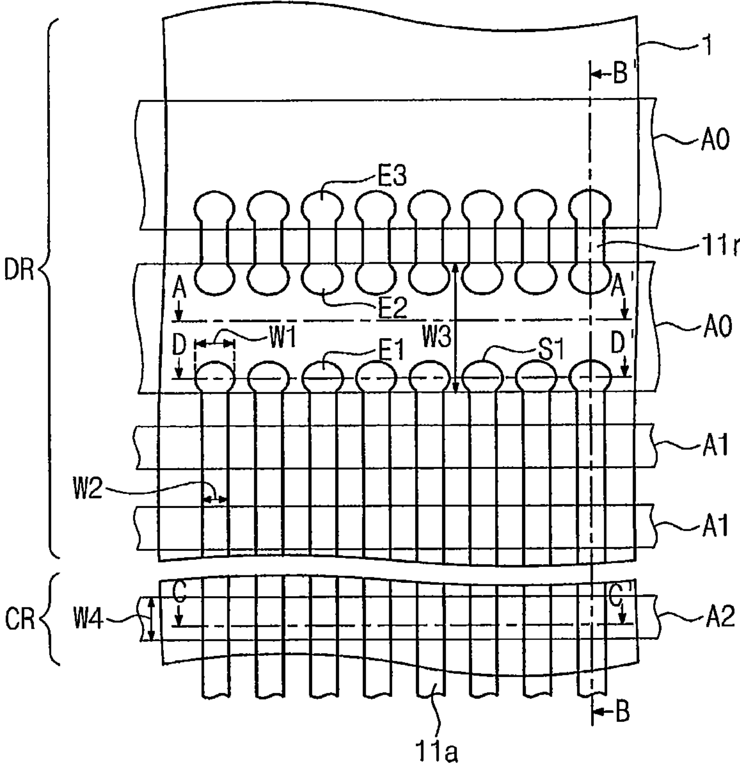


Fig. 1B

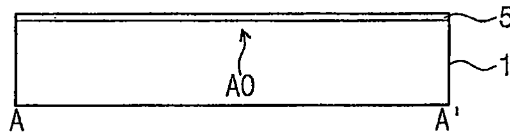


Fig. 1C

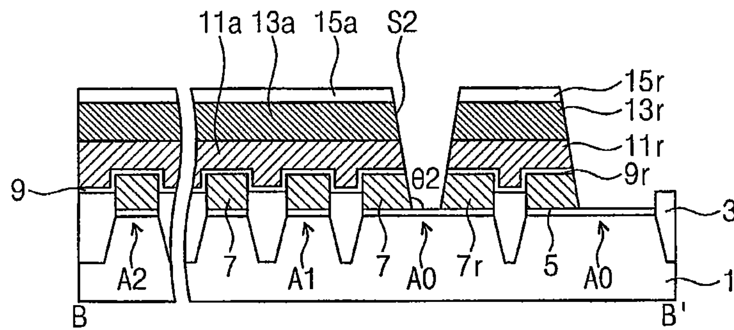


Fig. 1D

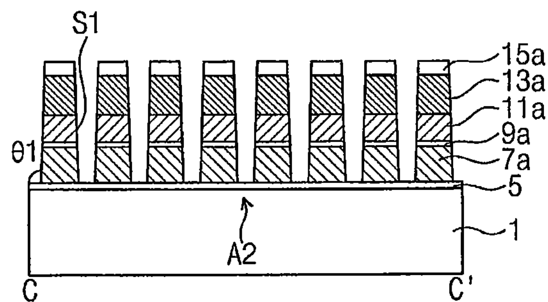


Fig. 1E

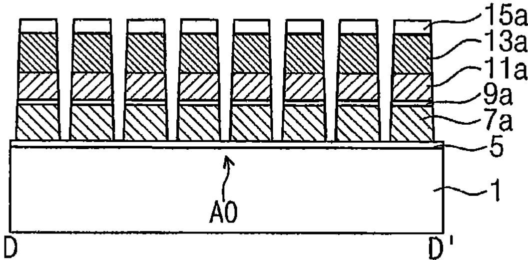


Fig. 1F

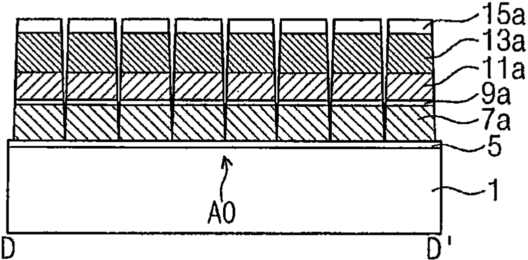


Fig. 2A

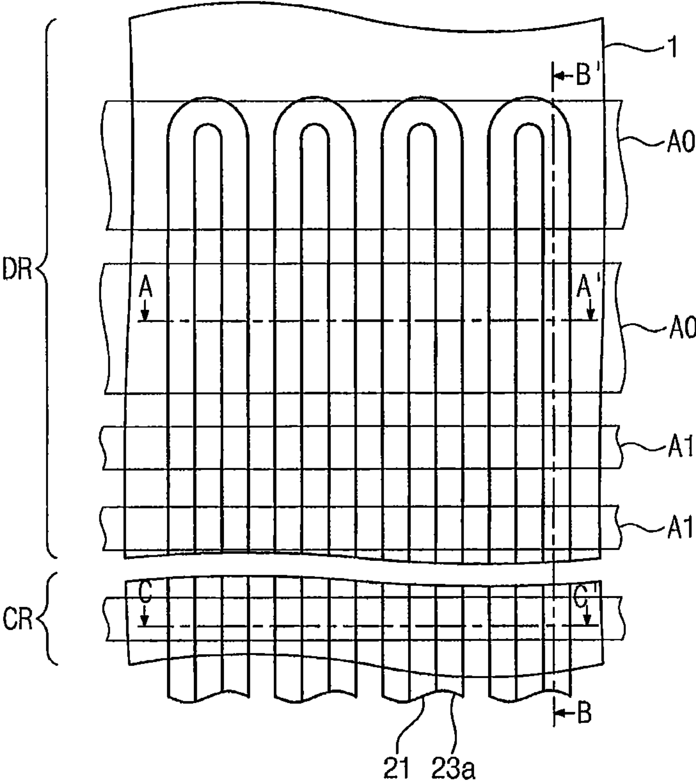


Fig. 2B

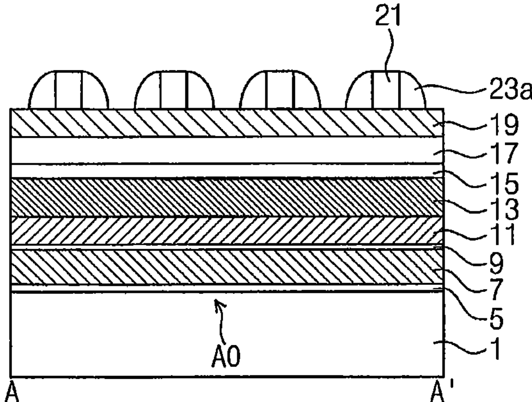


Fig. 2C

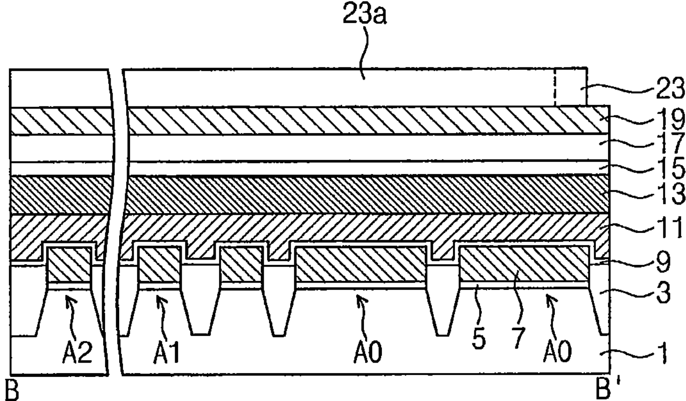


Fig. 2D

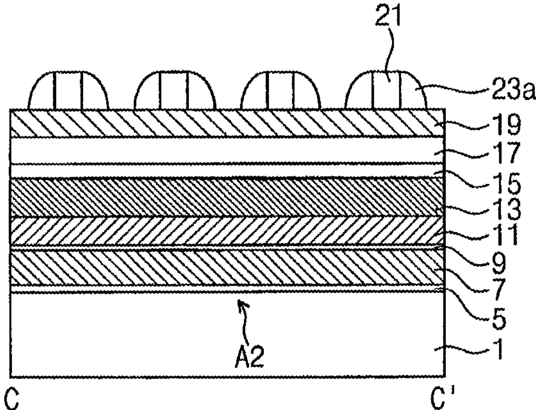


Fig. 3A

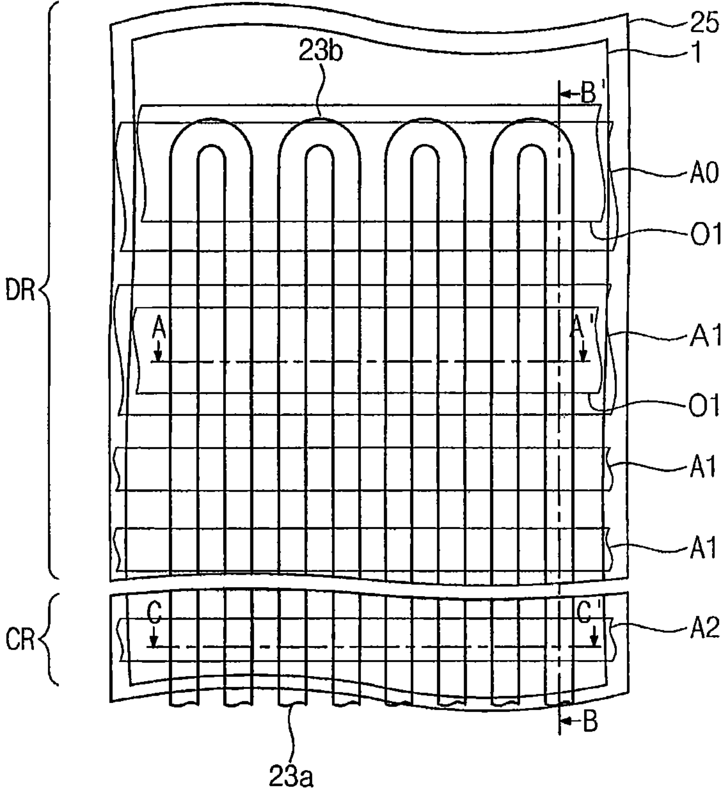


Fig. 3B

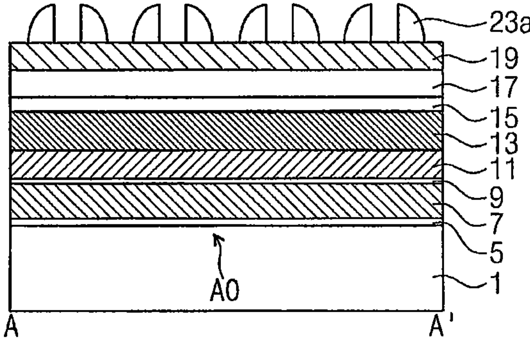


Fig. 3C

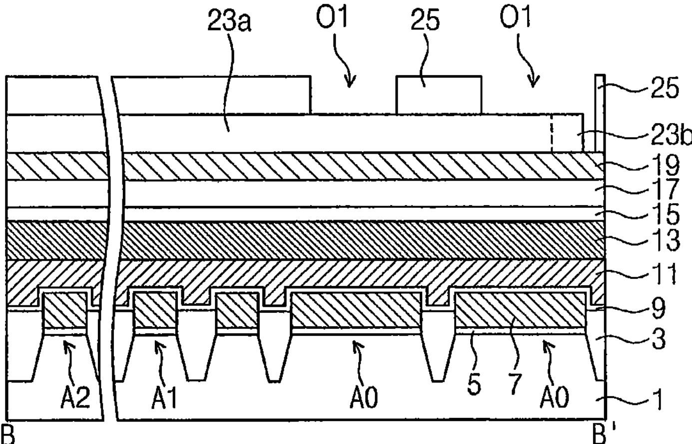


Fig. 3D

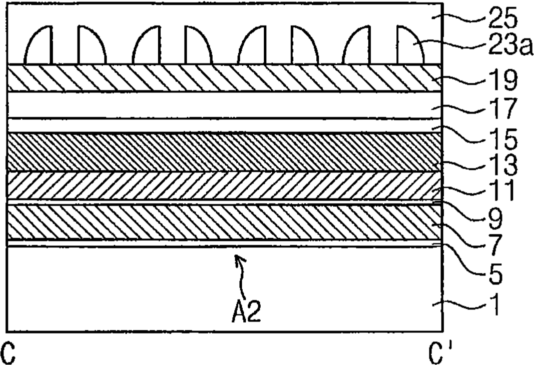


Fig. 4A

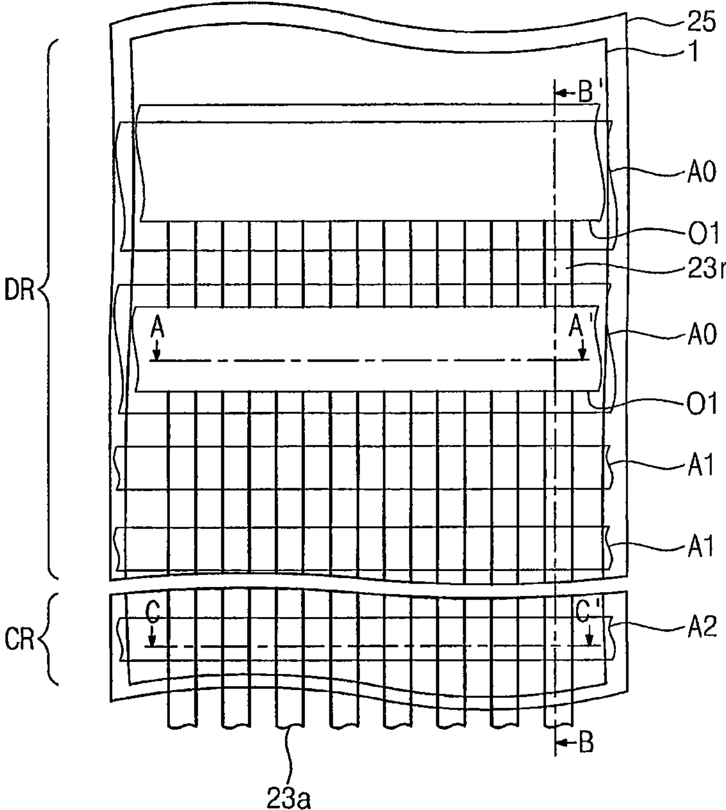


Fig. 4B

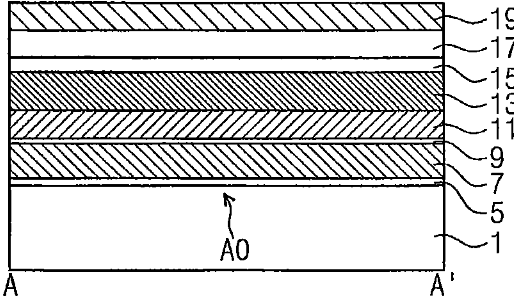


Fig. 4C

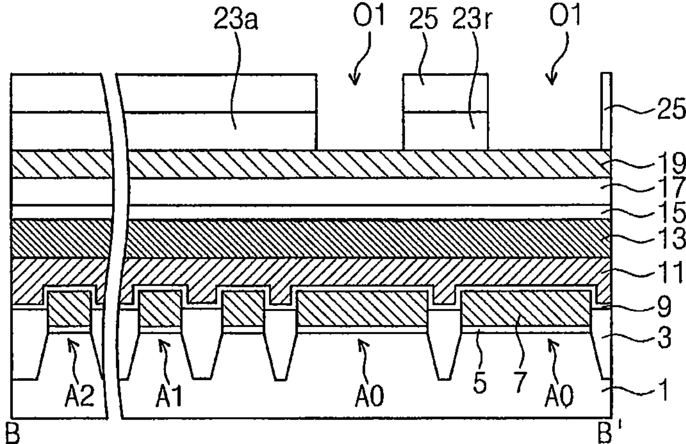


Fig. 4D

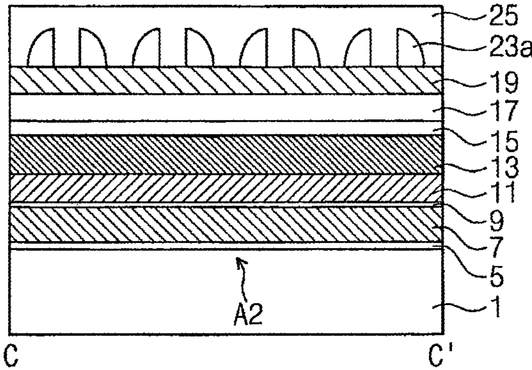


Fig. 5A

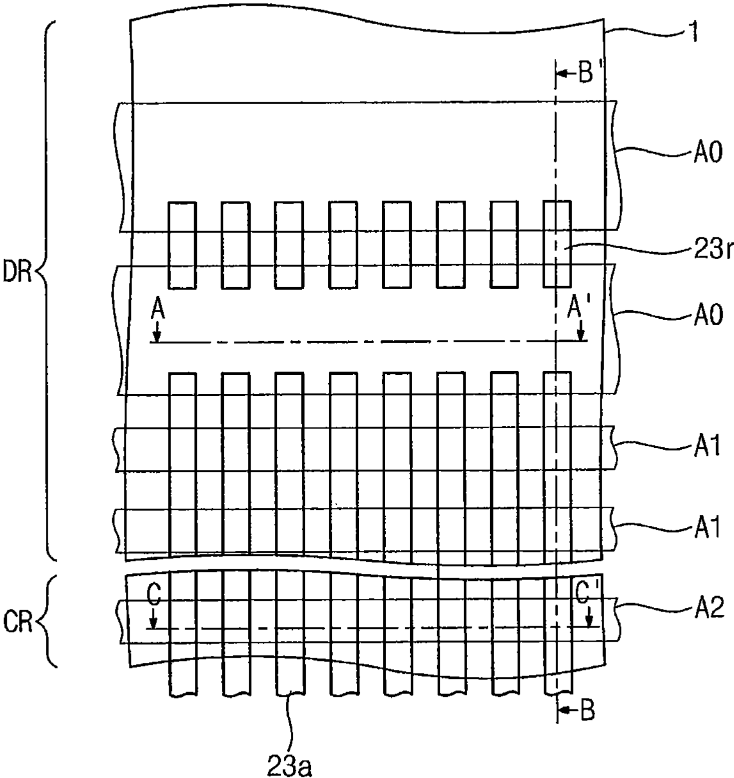


Fig. 5B

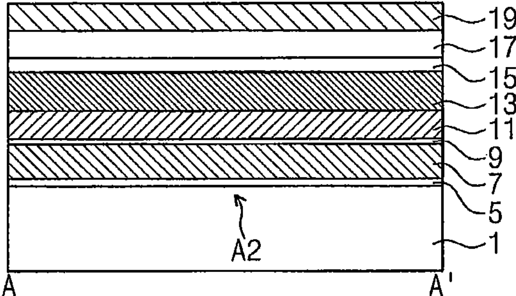


Fig. 5C

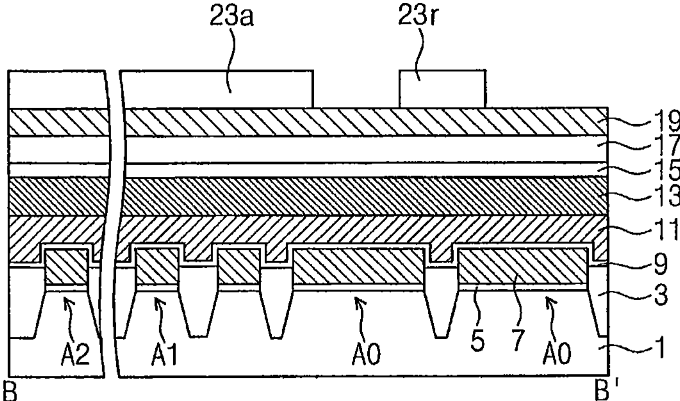


Fig. 5D

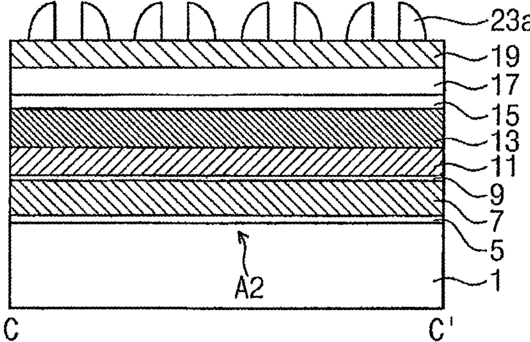


Fig. 6A

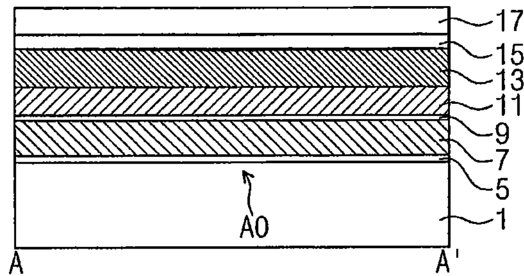


Fig. 6B

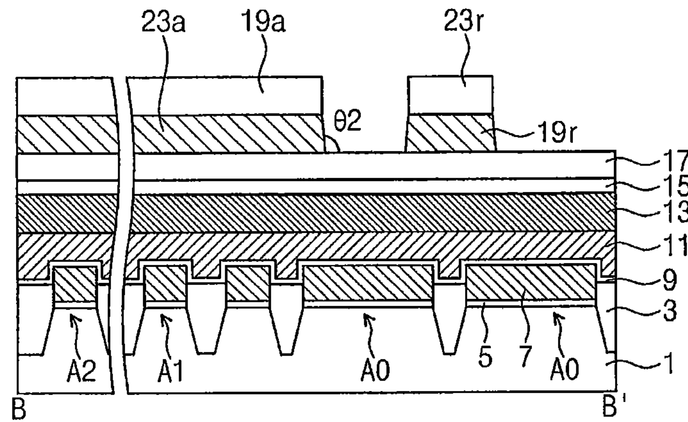


Fig. 6C

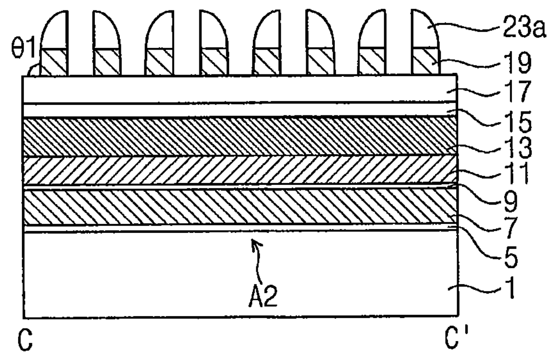


Fig. 7A

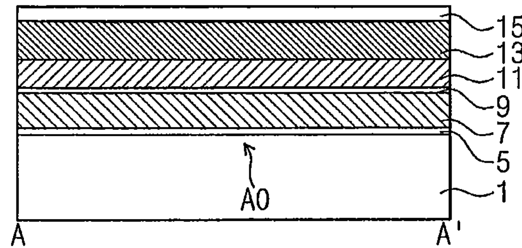


Fig. 7B

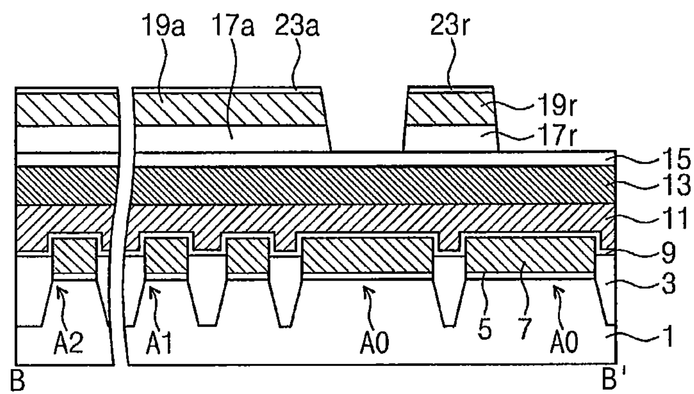


Fig. 7C

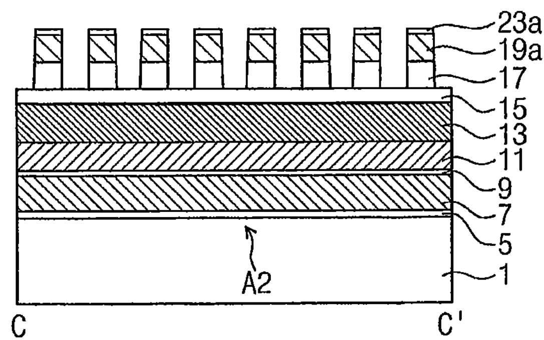


Fig. 8A

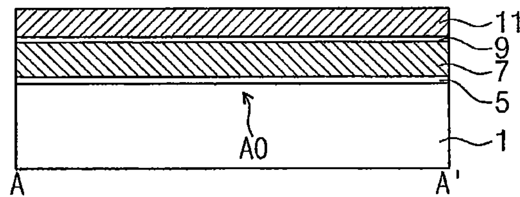


Fig. 8B

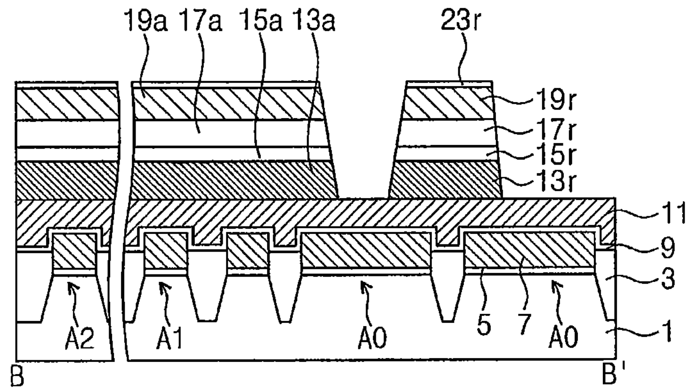


Fig. 8C

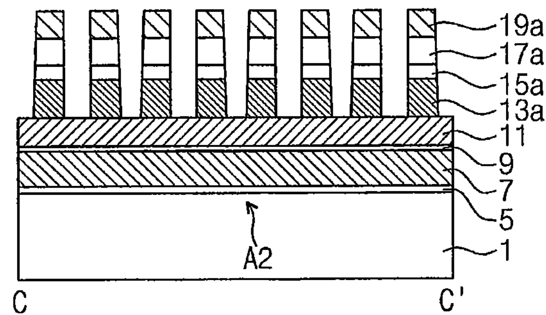


Fig. 9

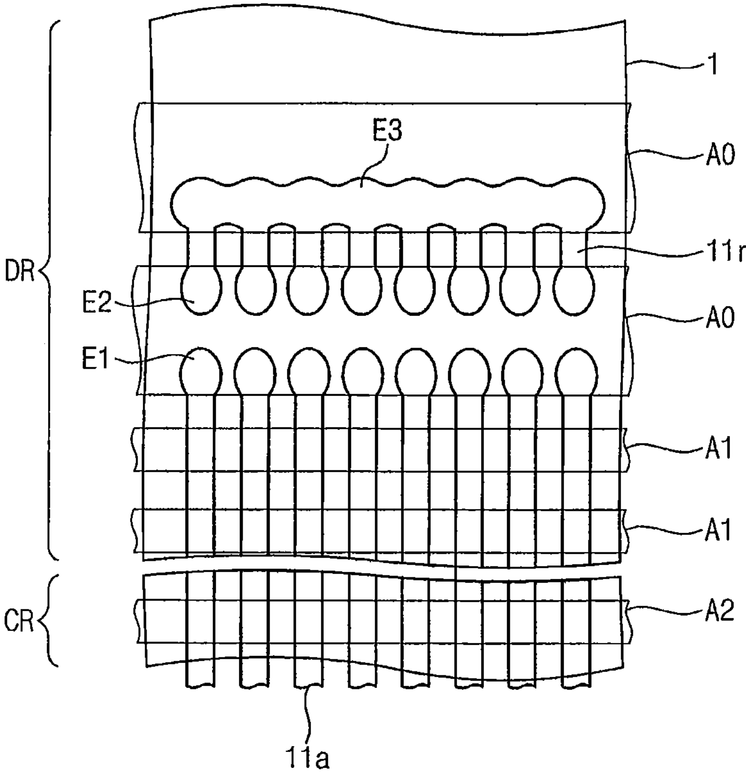


Fig. 10A

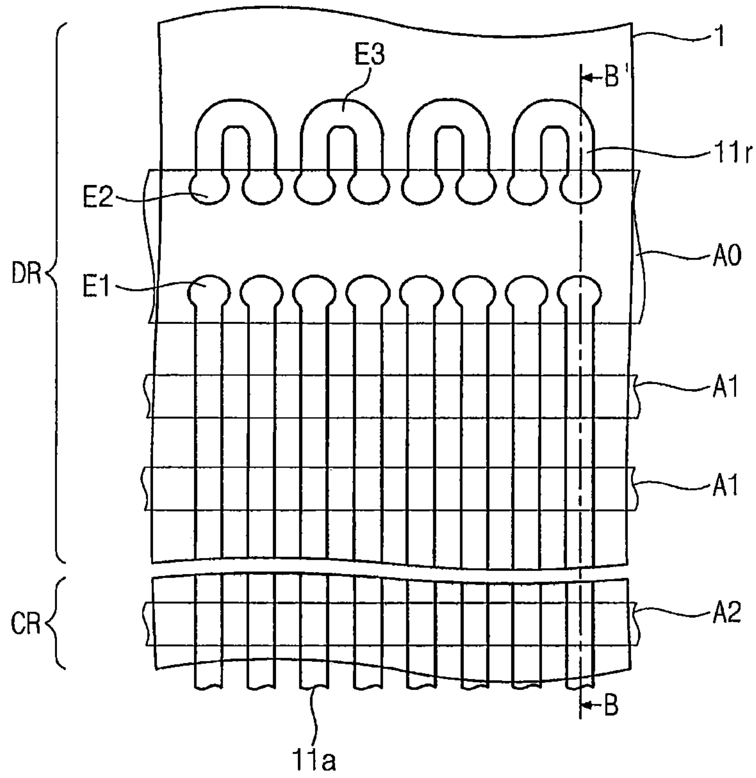


Fig. 10B

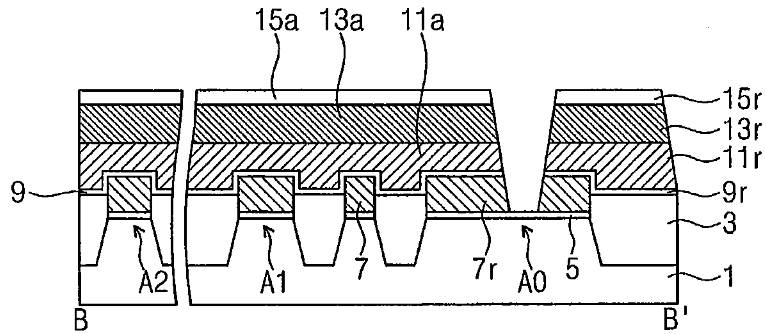


Fig. 11A

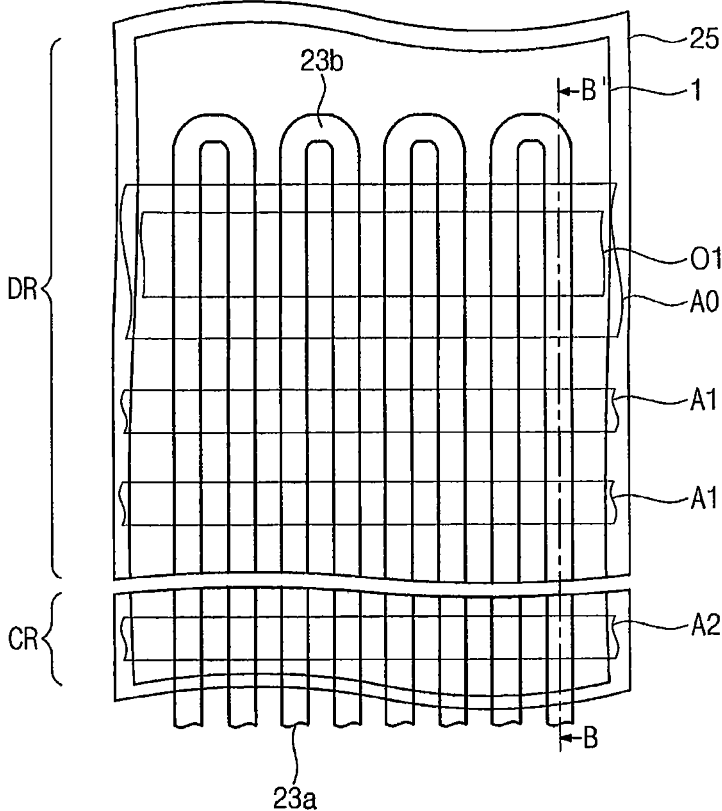


Fig. 11B

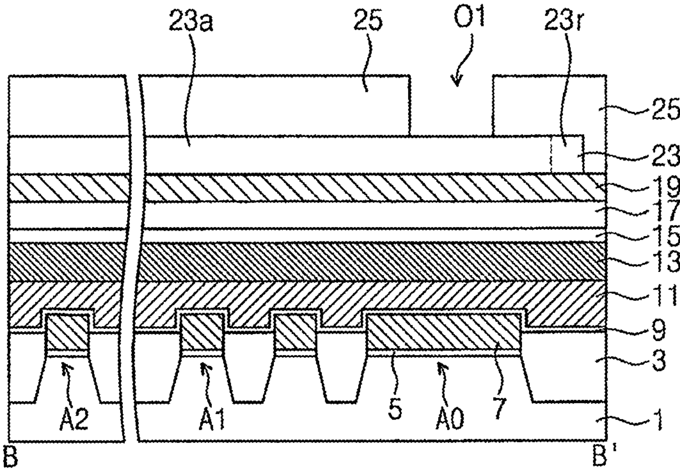


Fig. 12A

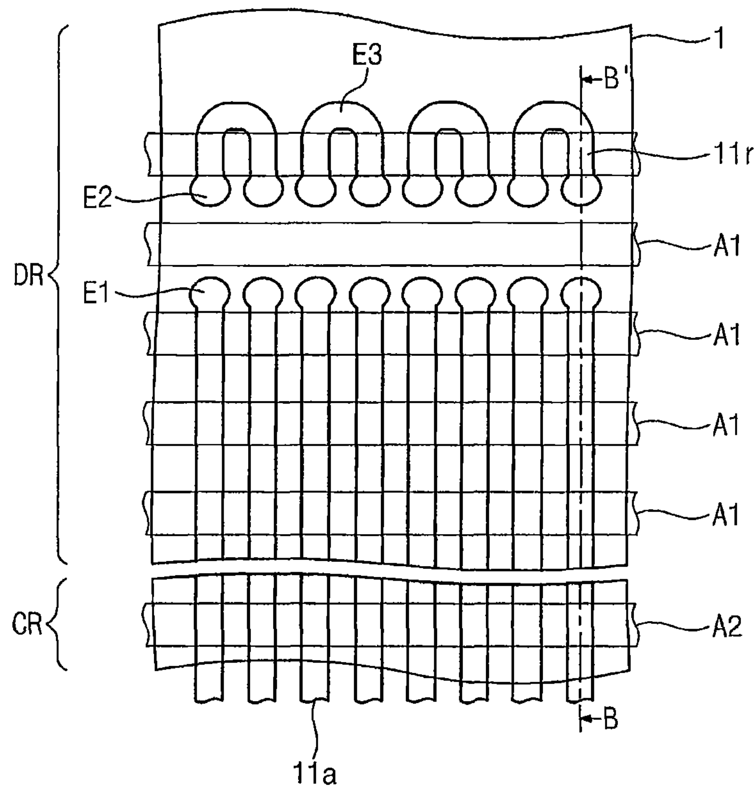


Fig. 12B

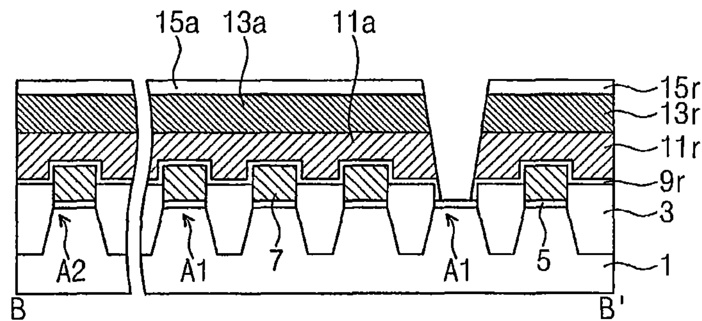


Fig. 13

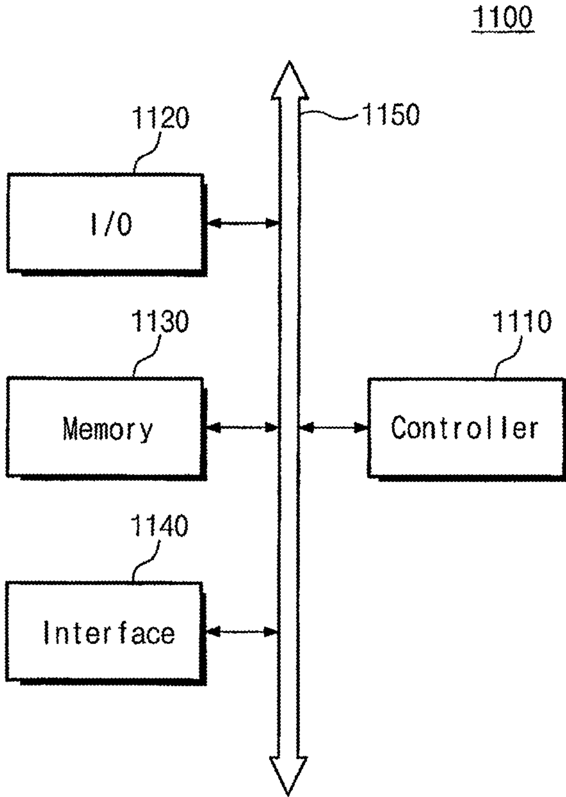


Fig. 14

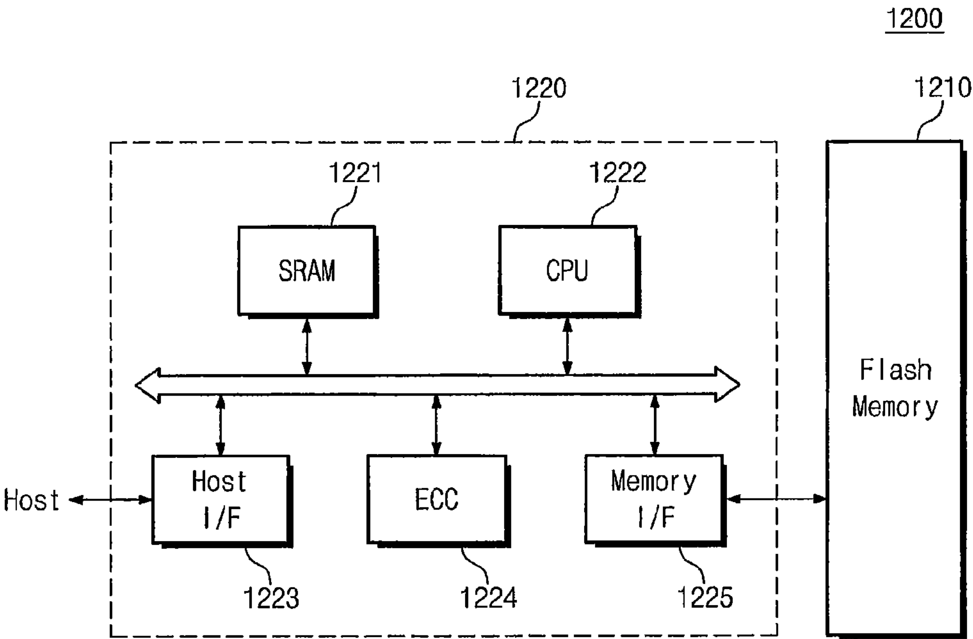
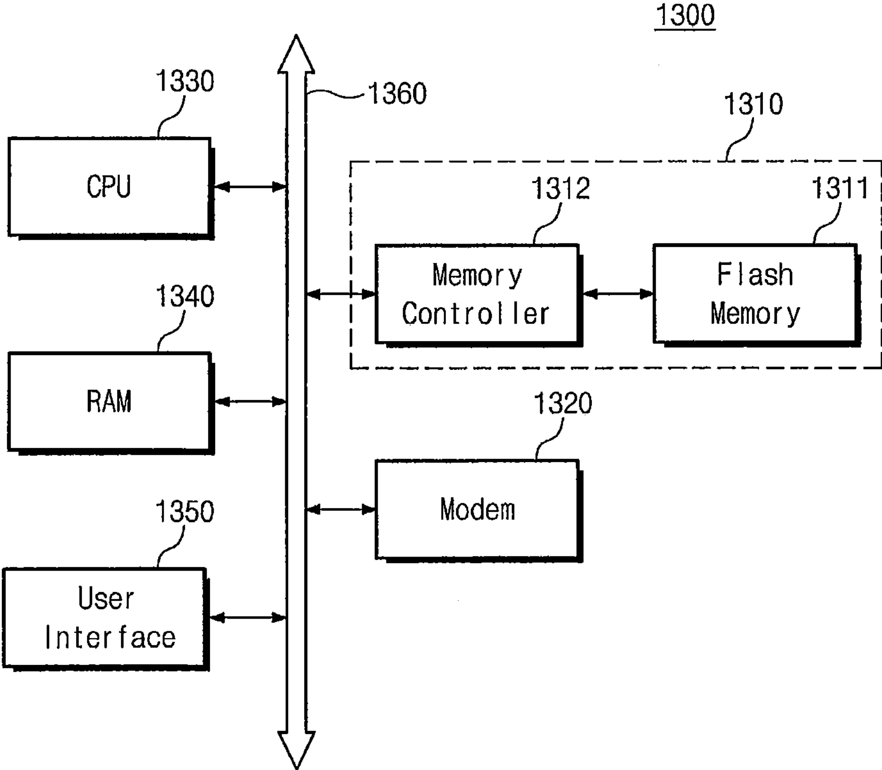


Fig. 15



SEMICONDUCTOR DEVICES INCLUDING SEPARATE LINE PATTERNS

CROSS-REFERENCE TO RELATED APPLICATION

This application claims the benefit of priority as a continuation of U.S. patent application Ser. No. 14/200,610, filed on Mar. 7, 2014, (now U.S. Pat. No. 9,171,853), which claims priority under 35 U.S.C. Section 119 to Korean Patent Application No. 10-2013-0024622, filed on Mar. 7, 2013, in the Korean Intellectual Property Office, and entitled: "Method of Fabricating Semiconductor Device and Device Fabricated Thereby." The disclosures of both of the above referenced applications are hereby incorporated herein in their entireties by reference.

BACKGROUND

1. Field

Example embodiments relate to a method of fabricating a semiconductor device and a semiconductor device fabricated thereby.

2. Description of the Related Art

Higher integration of semiconductor memory devices is desirable to satisfy consumer demands for superior performance and inexpensive prices.

SUMMARY

Embodiments are directed to a semiconductor device including a plurality of lines disposed on a semiconductor substrate, and remaining line patterns disposed spaced apart from the lines on extensions from the lines. The lines include first end-portions adjacent to the remaining line patterns. The remaining line patterns include second end-portions adjacent to the lines. The first end-portions and second end-portions are formed to have mirror symmetry with respect to each other.

Each of the first end-portions may have a width greater than the lines.

A sidewall slope of the first end-portions may be more gentle than a sidewall slope of the lines.

The semiconductor device may further include a device isolation layer disposed on the substrate to define a dummy active region and a cell active region. The dummy active region may be between the first end-portions and the second end-portions.

A width of the dummy active region may be greater than that of the cell active region.

The semiconductor device may further include dummy floating gates disposed between the lines and the dummy active region, and cell floating gates disposed between the lines and the cell active region.

At least some of adjacent ones of the dummy floating gates may be in contact with each other. All of the cell floating gates may be spaced apart from each other.

The remaining line patterns may be spaced apart from each other.

The remaining line patterns may further include third end-portions spaced apart from the second end-portions. Widths of the second and third end-portions may be greater than widths of the lines.

At least portions of the remaining line patterns may be connected to each other.

Embodiments are also directed to a method of fabricating a semiconductor device including forming a device isolation layer on a substrate to define a dummy active region and a cell active region, sequentially stacking an etch-target layer and a mask layer on the substrate, forming linear spacers and a spacer connecting portion, the linear spacers being spaced apart from each other on the mask layer and the spacer connecting portion connecting end-portions of the linear spacers, forming a mask pattern on the substrate to have a first opening partially exposing the linear spacers, the first opening being formed spaced apart from the spacer connecting portion, and removing portions of the linear spacers exposed by the first opening.

The first opening may overlap the dummy active region, in plan view.

The dummy active region may be formed to have a greater width than the cell active region.

The removing of the portions of the linear spacers exposed by the first opening may separate the linear spacers from the spacer connecting portion. The method may further include removing the mask pattern, and sequentially etching the mask layer and the etch-target layer using the linear spacers and the spacer connecting portion as an etch mask to form a line pattern and a connecting pattern overlapped by the linear spacers and the spacer connecting portion, respectively.

The mask pattern may include a second opening spaced apart from the first opening to expose the spacer connecting portion. The method may further include removing the portions of the linear spacers and the spacer connecting portion exposed by the first and second openings, respectively, to form a linear spacer portion and a remaining spacer line pattern spaced apart from each other, removing the mask pattern, and sequentially etching the mask layer and the etch-target layer using the linear spacer portion and the remaining spacer line pattern as an etch mask to form a line pattern and a remaining line pattern overlapped with the linear spacer portions and the remaining spacer line pattern.

Embodiments are also directed to a method of fabricating a semiconductor device, including forming a device isolation layer on a substrate to define dummy active regions and a cell active region, sequentially stacking an etch-target layer and a mask layer on the substrate, forming linear spacers and a spacer connecting portion, the linear spacers being spaced apart from each other on the mask layer and extending in first direction crossing the dummy active regions, the cell active region and the device isolation layer, and the spacer connecting portion connecting end-portions of the linear spacers in a first dummy active region of the dummy active regions, forming a mask pattern on the substrate, the mask pattern having a first opening extending in a second direction crossing the linear spacers, the first opening being spaced apart from the spacer connecting portion and exposing a section of the linear spacers, separating the linear spacers from the spacer connecting portion by removing the section of the linear spacers exposed by the first opening, removing the mask pattern, and sequentially etching the mask layer and the etch-target layer using the linear spacers as a mask to form a line pattern overlapped by the linear spacers.

The first opening may overlap a second dummy active region of the dummy active regions.

Sequentially etching the mask layer and the etch-target layer may further include etching using the spacer connecting portion as an etch mask to form a connecting pattern.

Forming the mask pattern may further include forming a second opening spaced apart from the first opening, the second opening extending in the second direction crossing the spacer connecting portion and exposing a section of the

spacer connecting portion. The method may further include forming a residual spacer line portion by removing the section of the spacer connecting portion exposed by the second opening, and sequentially etching the mask layer and the etch-target layer further includes etching using the residual spacer line portion as an etch mask to form a connecting pattern.

The second opening may overlap the first dummy active region.

BRIEF DESCRIPTION OF THE DRAWINGS

Features will become apparent to those of skill in the art by describing in detail exemplary embodiments with reference to the attached drawings in which:

FIG. **1**A illustrates a plan view of a semiconductor device according to example embodiments.

FIGS. **1**B through **1**E illustrate sectional views taken along lines A-A', B-B', C-C', and D-D', respectively, of FIG. **1**A.

FIG. **1**F illustrates a sectional view taken along line D-D' of FIG. **1**A to illustrate a semiconductor device according to a modification of example embodiments.

FIGS. **2**A, **3**A, **4**A, and **5**A illustrate plan views depicting stages of a method of fabricating a semiconductor device illustrated in FIG. **1**A.

FIGS. **2**B, **3**B, **4**B, **5**B, **6**A, **7**A, and **8**A illustrate sectional views depicting stages of a method of fabricating a semiconductor device having the section illustrated in FIG. **1**B.

FIGS. **2**C, **3**C, **4**C, **5**C, **6**B, **7**B, and **8**B illustrate sectional views depicting stages of a method of fabricating a semiconductor device having the section illustrated in FIG. **1**C.

FIGS. **2**D, **3**D, **4**D, **5**D, **6**C, **7**C, and **8**C illustrate sectional views depicting stages of a method of fabricating a semiconductor device having the section illustrated in FIG. **1**D.

FIG. **9** illustrates a plan view of a semiconductor device according to other example embodiments.

FIG. **10**A illustrates a plan view of a semiconductor device according to other example embodiments.

FIG. **10**B illustrates a sectional view taken along line B-B' of FIG. **10**A.

FIG. **11**A illustrates a plan view illustrating a method of fabricating a semiconductor device illustrated in FIG. **10**A.

FIG. **11**B illustrates a sectional view illustrating a method of fabricating a semiconductor device illustrated in FIG. **10**B.

FIG. **12**A illustrates a plan view of a semiconductor device according to other example embodiments.

FIG. **12**B illustrates a sectional view taken along line B-B' of FIG. **12**A.

FIG. **13** illustrates a schematic block diagram illustrating an example of memory systems including semiconductor devices according to example embodiments.

FIG. **14** illustrates a schematic block diagram illustrating an example of memory cards including semiconductor devices according to example embodiments.

FIG. **15** illustrates a schematic block diagram illustrating an example of information processing systems including semiconductor devices according to example embodiments.

DETAILED DESCRIPTION

Example embodiments will now be described more fully hereinafter with reference to the accompanying drawings; however, they may be embodied in different forms and should not be construed as limited to the embodiments set forth herein. Rather, these embodiments are provided so that this disclosure will be thorough and complete, and will fully convey exemplary implementations to those skilled in the art.

In the drawing figures, the dimensions of layers and regions may be exaggerated for clarity of illustration. It will also be understood that when a layer or element is referred to as being "on" another layer or substrate, it can be directly on the other layer or substrate, or intervening layers may also be present. Further, it will be understood that when a layer is referred to as being "under" another layer, it can be directly under, and one or more intervening layers may also be present. In addition, it will also be understood that when a layer is referred to as being "between" two layers, it can be the only layer between the two layers, or one or more intervening layers may also be present. Like reference numerals refer to like elements throughout.

Example embodiments are described herein with reference to cross-sectional illustrations that are schematic illustrations of idealized embodiments (and intermediate structures) of example embodiments. As such, variations from the shapes of the illustrations as a result, for example, of manufacturing techniques and/or tolerances, are to be expected. Thus, example embodiments should not be construed as limited to the particular shapes of regions illustrated herein but are to include deviations in shapes that result, for example, from manufacturing. For example, an implanted region illustrated as a rectangle may have rounded or curved features and/or a gradient of implant concentration at its edges rather than a binary change from implanted to non-implanted region. Likewise, a buried region formed by implantation may result in some implantation in the region between the buried region and the surface through which the implantation takes place. Thus, the regions illustrated in the figures are schematic in nature and their shapes are not intended to illustrate the actual shape of a region of a device and are not intended to limit the scope of example embodiments.

Unless otherwise defined, all terms (including technical and scientific terms) used herein have the same meaning as commonly understood by one of ordinary skill in the art to which example embodiments belong. It will be further understood that terms, such as those defined in commonly-used dictionaries, should be interpreted as having a meaning that is consistent with their meaning in the context of the relevant art and will not be interpreted in an idealized or overly formal sense unless expressly so defined herein.

FIG. **1**A illustrates a plan view of a semiconductor device according to example embodiments. FIGS. **1**B through **1**E illustrate sectional views taken along lines A-A', B-B', C-C', and D-D', respectively, of FIG. **1**A. FIG. **1**F illustrates a sectional view taken along line D-D' of FIG. **1**A to depict a semiconductor device according to a modification of example embodiments.

Referring to FIGS. **1**A through **1**E, a device isolation layer **3** may be provided on a substrate **1** to define dummy active regions A**0** and A**1** and cell active regions A**2**. The substrate **1** may include a dummy region DR and a cell region CR. The dummy active regions A**0** and A**1** may be provided on the dummy region DR, and the cell active regions A**2** may be provided on the cell region CR. The dummy active regions A**0** and A**1** may include first dummy active regions A**0** and second dummy active regions A**1**. Memory cells to be provided on the dummy active regions A**0** and A**1** may not be used to store data (or serve as dummy cells). Memory cells to be provided on the cell active regions A**2** may be used to store data. In example embodiments, the second dummy active regions A**1** may be formed to have substan-

tially the same width as a width W4 of the cell active region A2. A width W3 of the first dummy active region A0 may be greater than the width W4 of the cell active regions A2. In the present embodiment, the number of the first dummy active regions A0 may be two or more. The first dummy active regions A0 may be disposed at the outermost region of the cell region CR or spaced apart from the cell active regions A2 by the second dummy active regions A1 interposed therebetween.

The device isolation layer **3** may have a top surface that is higher than a top surface of the substrate **1**. A plurality of word lines **11***a* may be formed on the substrate **1** to cross the active regions A0, A1, and A2. Remaining word line patterns **11***r* may be provided spaced apart from and extending in a same direction as the word lines **11***a*. The remaining word line patterns **11***r* may be formed to cross over the first dummy active regions A0. A floating gate pattern **7** may be disposed between the word lines **11***a* and the active regions A1 and between the word lines **11***a* and the active regions A2. The floating gate pattern **7** may have a top surface that is higher than the top surface of the device isolation layer **3**. The word line **11***a* may be formed to face the top surface as well as side surfaces of the floating gate pattern **7**. Accordingly, it may be possible to increase a capacitance between the word line **11***a* and the floating gate pattern **7** and thereby improve operation characteristics of the device. In example embodiments, a tunnel insulating layer **5** may be interposed between the floating gate pattern **7** and the substrate **1**. A blocking insulating layer **9** may be interposed between the floating gate pattern **7** and the word line **11***a*. A remaining floating gate pattern **7***r* may be interposed between the remaining word line pattern **11***r* and the first dummy active region A0. A remaining blocking layer **9***r* may be interposed between the remaining floating gate pattern **7***r* and the remaining word line pattern **11***r*.

The word line **11***a* may include a first end-portion E1 adjacent to the remaining word line pattern **11***r*. The remaining word line pattern **11***r* may include a second end-portion E2 adjacent to the first end-portion E1 and a third end-portion E3 spaced apart from the second end-portion E2. The first end-portion E1 and the second end-portion E2 may be formed to have mirror symmetry with respect to a line interposed therebetween. The first end-portion E1 may have a width W1 that is greater than a width W2 of the word line **11***a*. A first angle θ1 between a sidewall S1 of the word line **11***a* that is positioned between the word lines **11***a*, and a top surface of the substrate **1** may be smaller than a second angle θ2 between a sidewall S2 of the first end-portion E1 and the top surface of the substrate **1**. The second angle is much bigger than 90° and the first angle is close to about 90°. For example, the sidewall slope of the sidewall of the first end-portion E1 may be more gentle (less steep) than the sidewall slope of the lines **11***a*. The second end-portions E2 may be spaced apart from each other, and the third end-portions E3 may be spaced apart from each other. The remaining word line patterns **11***r* may be spaced apart from each other. Accordingly, during a subsequent cleaning process, a cleaning solution for removing an impurity or by-product can be supplied without interruption. As a result, it may be possible to realize a highly-reliable semiconductor device.

Below the first end-portions E1, the floating gate patterns **7** may be spaced apart from each other, as shown in FIG. **1**E, or may be in contact with each other, as shown in FIG. **1**F. Although the floating gate patterns **7** below the first end-portions E1 may be connected to each other as shown in FIG. **1**F, such connections of the floating gate patterns **7** may not result in a malfunction of the device, because the first end-portions E1 are positioned on the dummy region DR. In addition, as shown in FIG. **1**D, the floating gate patterns **7** adjacent to the cell region CR may be spaced apart from each other.

In example embodiments, all of the floating gate patterns **7**, the remaining floating gate pattern **7***r*, the word line **11***a*, and the remaining word line pattern **11***r* may be formed of the same material, for example, a doped or undoped polysilicon layer. The tunnel insulating layer **5** may be formed of a silicon oxide layer. The blocking insulating layer **9** and the remaining blocking insulating layer **9***r* may be formed as a triple-layer including a silicon oxide layer, a silicon nitride layer, and a silicon oxide layer or a high-k dielectric layer.

Metal-containing layers **13***a* and **13***r* may be provided on the word line **11***a* and the remaining word line pattern **11***r*, respectively. In example embodiments, the metal-containing layer **13***a* and **13***r* may include a tungsten layer and/or a tungsten silicide layer. Capping patterns **15***a* and **15***r* may be provided on the metal-containing layers **13***a* and **13***r*, respectively.

Source/drain regions may be provided in portions of the substrate **1** located between the word lines **11***a*. The plurality of word lines **11***a* may each constitute a unit cell string, and at least one string selection line and at least one ground selection line may be provided at end portions, respectively, of the cell string.

According to the present embodiment, the semiconductor device may be configured to prevent bridging from occurring between the word lines **11***a*. Accordingly, it may be possible to prevent the device from malfunctioning.

FIGS. **2**A, **3**A, **4**A, and **5**A illustrate plan views depicting stages of a method of fabricating the semiconductor device illustrated in FIG. **1**A. FIGS. **2**B, **3**B, **4**B, **5**B, **6**A, **7**A, and **8**A illustrate sectional views depicting stages of a method of fabricating a semiconductor device having the section illustrated in FIG. **1**B. FIGS. **2**C, **3**C, **4**C, **5**C, **6**B, **7**B, and **8**B illustrate sectional views depicting stages of a method of fabricating a semiconductor device having the section illustrated in FIG. **1**C. FIGS. **2**D, **3**D, **4**D, **5**D, **6**C, **7**C, and **8**C illustrate sectional views depicting stages of a method of fabricating a semiconductor device having the section illustrated in FIG. **1**D.

Referring to FIGS. **2**A through **2**D, the tunnel insulating layer **5**, and the floating gate layer **7** may be sequentially stacked on the substrate **1** including the dummy region DR and the cell region CR. The floating gate layer **7**, the tunnel insulating layer **5**, and the substrate **1** may be partially etched to form trenches. An insulating layer may be formed to fill the trenches, and then the insulating layer may be recessed to form the device isolation layers **3**. The floating gate layer **7** may be formed of a doped or undoped polysilicon. As the result of the formation of the device isolation layers **3**, the first and second dummy active regions A0 and A1 and the cell active regions A2 may be delimited. In example embodiments, the first dummy active regions A0 may be formed to be wider than the cell active regions A2 and the second dummy active regions A1.

Next, a blocking insulating layer **9**, a word line layer **11**, a metal-containing layer **13**, a capping layer **15**, a first mask layer **17**, and a second mask layer **19** may be sequentially stacked on the substrate **1**. The word line layer **11** may be formed of a doped or undoped polysilicon. The metal-containing layer **13** may be formed of, for example, tungsten, and/or tungsten silicide. The capping layer **15** may be formed of, for example, a silicon nitride layer. The first mask

layer **17** may be formed of, for example, at least one oxide. The second mask layer **19** may be formed of, for example, polysilicon.

Next, a plurality of line-shaped first photoresist patterns **21** may be formed on the second mask layer **19**. Spacers **23***a* and **23***b* may be formed to cover sidewalls of the first photoresist patterns **21**. The spacers **23***a* and **23***b* may be formed of, for example, a silicon oxide. The spacers **23***a* and **23***b* may be formed to entirely cover the sidewalls of the first photoresist patterns. Accordingly, the spacers **23***a* and **23***b* may be formed to have a closed loop shape. The spacers **23***a* and **23***b* may include linear spacer portions **23***a* covering both sidewalls of the line-shaped first photoresist pattern **21** and a spacer connecting portion **23***b* covering an end-portion of the first photoresist pattern **21**. The spacer connecting portion **23***b* may be formed to connect the linear spacer portions **23***a* to each outer.

Referring to FIGS. **3**A through **3**D, the first photoresist pattern **21** may be removed by, for example, an ashing process. A second photoresist pattern **25** may be formed to have a plurality of openings O**1** that overlap with the first dummy active regions A**0**, respectively, and are spaced apart from each other. The openings O**1** may be formed to expose the spacer connecting portion **23***b* and a portion of the linear spacer portion **23***a* adjacent thereto. The remaining portion of the linear spacer portion **23***a* may be covered with the second photoresist pattern **25**.

Referring to FIGS. **4**A through **4**D, a trimming process may be performed to selectively remove the spacer connecting portion **23***b* and the portion of the linear spacer portion **23***a* adjacent thereto exposed by the openings O**1**. Accordingly, a remaining spacer pattern **23***r* may be formed between the openings O**1**.

Referring to FIGS. **5**A through **5**D, the second photoresist pattern **25** may be removed by an ashing process, and thus, top surfaces of the linear spacer portion **23***a*, the remaining spacer pattern **23***r*, the second mask layer **19** may be exposed.

Referring to FIGS. **1**A and **6**A through **6**C, the second mask layer **19** may be etched using the linear spacer portions **23***a* and the remaining spacer patterns **23***r* as an etch mask to form a second mask line pattern **19***a* and a remaining second mask pattern **19***r*. A space between the linear spacer portions **23***a* may be different from a space between the linear spacer portion **23***a* and the remaining spacer pattern **23***r* and pattern densities of the linear spacer portions **23***a* and the remaining spacer pattern **23***r* may be different from each other. Accordingly, there may be a spatial variation in the etching of the second mask layer **19**. For example, an etch-loading effect may occur at end-portions of the linear spacer portion **23***a* and the remaining spacer patterns **23***r*. For instance, a first angle θ**1** between a sidewall of the second mask line pattern **19***a* and the first mask layer **17** may be smaller than a second angle θ**2** between a sidewall of the end-portion of the remaining second mask pattern **19***r* and the first mask layer **17**. The second angle may be much bigger than 90° and the first angle may be almost close to about 90°. As the underlying layers **15**, **13**, **11**, **9**, and **7** are sequentially etched, the angles θ**1** and θ**2** may be transferred downward.

Referring to FIGS. **1**A, and **7**A through **7**C, the first mask **17** may be etched using the second mask patterns **19***a* and **19***r* as etch mask to form first mask patterns **17***a* and **17***r*. In the case where the linear spacer portion **23***a* and the remaining spacer patterns **23***r* are formed of the same material (e.g., oxide) as the first mask **17**, they may be removed or etched during the etching of the first mask **17**.

Referring to FIGS. **1**A, and **8**A through **8**C, the capping layer **15** and the metal-containing layer **13** may be sequentially etched using the second mask patterns **19***a* and **19***r* as an etch mask to form the capping patterns **15***a* and **15***r* and the metal-containing patterns **13***a* and **13***r*.

Thereafter, the word line layer **11**, the blocking insulating layer **9**, and the floating gate layer **7** may be sequentially patterned using the second and first mask patterns **19***a*, **19***r*, **17***a*, and **17***r* an etch mask, thereby forming the word line **11***a*, the remaining word line pattern **11***r*, and the floating gate patterns **7** and **7***r*, as shown in FIGS. **1**A through **1**E. In example embodiments, during the patterning process, the second and first mask patterns **19***a*, **19***r*, **17***a*, and **17***r* may be removed or etched to expose top surfaces of the capping patterns **15***a* and **15***r*.

If, in the trimming process, only the spacer connecting portion **23***b* is removed and the portion of the linear spacer portion **23***a* is not removed, the remaining spacer pattern **23***r* will not be formed. In this case, a variation in pattern density may be larger at the end-portion of the linear spacer portion **23***a* than between the linear spacer portions **23***a*, and thus, the angle θ**2** between the sidewall of the end-portion of the linear spacer portion **23***a* and the first mask layer **17** may become greater than the second angle θ**2** in the example embodiments. As the result of the downward transfer of the angles θ**1** and θ**2**, the lower the position of a pattern, the wider the pattern. By contrast, according to example embodiments, since the second angle θ**2** may be relatively small (approaching to about 90°), the downward enlargement in pattern width may be suppressed. Accordingly, it is possible to prevent a bridging between the patterns from occurring.

In addition, the end-portions E**1**-E**3** may be formed on the first dummy active region A**0** to have a relatively large width. Accordingly, it may be possible to prevent the occurrence of the bridge more effectively.

FIG. **9** illustrates a plan view of a semiconductor device according to other example embodiments.

Referring to FIG. **9**, the third end-portions E**3** of the remaining word line pattern **11***r* may be connected to each other. This may result from a low density of patterns in a region adjacent to the third end-portions E**3**. For example, the etch-loading effect may occur increasingly in the region adjacent to the third end-portions E**3**, and this may result in the connection between the remaining word line patterns **11***r*. Except for this difference, the semiconductor device according to the other example embodiments may be configured to have substantially the same or similar features as those of the previous embodiments.

FIG. **10**A illustrates a plan view of a semiconductor device according to other example embodiments. FIG. **10**B illustrates a sectional view taken along line B-B' of FIG. **10**A.

Referring to FIGS. **10**A and **10**B, according to other example embodiments, the semiconductor device may be configured in such a way that the number of the first dummy active regions A**0** is one. Further, the first dummy active region A**0** may be spaced apart from the third end-portion E3 of the remaining word line pattern **11***r*. An adjacent pair of the remaining word line patterns **11***r* may include the third end-portions E3 that are connected to each other to have a 'U'-shaped structure. Except for this difference, the semiconductor device according to other example embodiments may be configured to have substantially the same or similar features as those of the previous embodiments.

FIG. **11**A illustrates a plan view illustrating a method of fabricating a semiconductor device of FIG. **10**A. FIG. **11**B

illustrates a sectional view illustrating a method of fabricating a semiconductor device of FIG. **10**B.

Referring to FIGS. **11**A and **11**B, as previously described in the example embodiments, the blocking insulating layer **9**, the word line layer **11**, the metal-containing layer **13**, the capping layer **15**, the first mask layer **17**, the second mask layer **19**, the linear spacer portion **23***a*, and the spacer connecting portion **23***r* may be formed on the substrate **1** including the first dummy active region A**0**, the second dummy active regions A**1**, and the cell active regions A**2**. Here, the number of the first dummy active regions A**0** may be one. Next, the second photoresist pattern **25** may be formed to have an opening O**1**. In example embodiments, the opening O**1** may be formed to expose a portion of the linear spacer portion **23***a* spaced apart from the spacer connecting portion **23***r*.

Thereafter, as previously described in the example embodiments, the portion of the linear spacer portion **23***a* exposed by the opening O**1** may be removed. The second photoresist pattern **25** may be removed by an ashing process, and then, the underlying layers may be sequentially etched using the linear spacer portion **23***a* and the spacer connecting portion **23***b* spaced apart from each other as an etch mask. The etching process may be performed in the same or similar manner as that of the example embodiments.

FIG. **12**A illustrates a plan view of a semiconductor device according to other example embodiments. FIG. **12**B illustrates a sectional view taken along line B-B' of FIG. **12**A.

Referring to FIGS. **12**A and **12**B, in the semiconductor device according to other example embodiments, the width of, and the space between, the dummy active regions A**1** may be substantially equivalent to those of the cell active regions A**2**. All of the first end-portion E**1** of the word line **11***a* and the second end-portion and third end-portion E**2** and E**3** of the remaining word line patterns **11***r* may be provided on the device isolation layer **3**. Except for this difference, the semiconductor device according to other example embodiments may be configured to have substantially the same or similar features as those of the previous embodiments.

FIG. **13** illustrates a schematic block diagram depicting an example of a memory system including a semiconductor device according to example embodiments.

Referring to FIG. **13**, a memory system **1100** may be applied to a PDA (personal digital assistant), a portable computer, a web tablet, a wireless phone, a mobile phone, a digital music player, a memory card, and/or other devices that can transmit and/or receive data in a wireless communication environment.

The memory system **1100** may include a controller **1110**, an input/output device **1120** (e.g., a keypad and/or a display device), a memory **1130**, an interface **1140**, and a bus **1150**. The memory **1130** and the interface **1140** may communicate with each other through the bus **1150**.

The controller **1110** may include a microprocessor, a digital signal processor, a micro controller, and/or other process devices similar to a microprocessor, a digital signal processor, or a micro controller. The memory **1130** may be used to store an instruction executed by the controller **1110**. The input/output device **1120** may receive data and/or a signal from the outside of the system **1100** and/or transmit data and/or a signal to the outside of the system **1100**. For example, the input/output device **1120** may include a keyboard, a keypad, and/or a displayer.

The memory **1130** may include a nonvolatile memory device that may include the semiconductor device according to example embodiments. The memory **1130** may further include other kinds of memory, for example, a volatile memory device capable of random access or various other kinds of memories.

The interface **1140** may transmit data to a communication network and/or may receive data from a communication network.

FIG. **14** illustrates a schematic block diagram depicting an example of a memory card including a semiconductor device according to example embodiments.

Referring to FIG. **14**, a memory card **1200** for supporting a storage capability of a large capacity may be fitted with a semiconductor memory device **1210**, which may include a semiconductor device according to example embodiments. The memory card **1200** according to example embodiments may include a memory controller **1220** that may control data exchange between a host and the semiconductor memory device **1210**.

A static random access memory (SRAM) **1221** may be used as an operation memory of a processing unit **1222**. A host interface **1223** may include data exchange protocols of a host that may be connected to the memory card **1200**. An error correction block **1224** may detect and/or may correct errors that may be included in data readout from a multi bit semiconductor memory device **1210**. A memory interface **1225** may interface with the semiconductor memory device **1210** including a semiconductor device of at least some example embodiments. The processing unit **1222** may perform control operations for exchanging data of the memory controller **1220**. That the memory card **1200** including a semiconductor device according to example embodiments may include a ROM (not illustrated) storing code data for interfacing with the host.

FIG. **15** illustrates a schematic block diagram depicting an example of an information processing system including a semiconductor device according to example embodiments.

Referring to FIG. **15**, an information processing system **1300** may include a semiconductor memory system **1310** including a semiconductor memory device including a semiconductor device according to example embodiments. The semiconductor memory system **1310** may be mounted to an information processing system, for example, a mobile device and/or a desktop computer. The information processing system **1300** may also includes a modem **1320**, a central processing unit (CPU) **1330**, a RAM **1340**, and a user interface **1350**, which may be electrically connected to a system bus **1360**. The semiconductor memory system **1310** may include a semiconductor memory device **1311**, and a memory controller **1312**. A memory system **1310** may be a solid state drive SSD, and data that may be processed by the CPU **1330** and/or input from the outside may be stored in the SSD. The information processing system **1300** configured as described and including a semiconductor memory device may reliably store a large amount of data in the semiconductor memory system **1310**. The semiconductor memory system **1310** may conserve resources for error correction and a high speed data exchange function may be provided. The information processing system **1300** may also include an application chipset, a camera image processor (CIS) and/or an input/output device.

Furthermore, a semiconductor device and/or memory system that may include the same may be packaged in various kinds of ways. For instance, the semiconductor device and/or memory system may be employed in a Package on Package (PoP), Ball Grid Array (BGA), Chip Scale Package (CSP), Plastic Leaded Chip Carrier (PLCC), Plastic Dual In-line Package (PDIP), Die in Waffle Pack, Die in Wafer Form, Chip On Board (COB), Ceramic Dual In-line

Package (CERDIP), Plastic Metric Quad Flat Pack (MQFP), Thin Quad Flat Pack (TQFP), Small Outline Integrated Circuit (SOIC), Shrink Small Outline Package (SSOP), Thin Small Outline Package (TSOP), System In Package (SIP), Multi Chip Package (MCP), Wafer-level Fabricated Package (WFP), and/or Wafer-level Processed Stack Package (WSP) configuration.

By way of summation and review, higher integration of semiconductor memory devices is desirable to satisfy consumer demands for superior performance and inexpensive prices. However, the extremely expensive process equipment needed to increase pattern fineness sets a practical limitation on increasing integration for semiconductor memory devices. To overcome such a limitation, a double patterning technology is proposed.

The double patterning technology may allow for manufacturers to achieve a small feature size that is beyond a resolution limitation of an exposure system. For example, according to such double patterning technology, the formation of fine pitch patterns may include forming sacrificial patterns through a photolithography process, forming spacers on sidewalls of the sacrificial patterns, removing the sacrificial patterns, and etching an etch target layer using the spacers as an etch mask. However, as integration density of the semiconductor device increases, more advanced patterning methods are desirable.

In addition, when carrying out a wet etching process to form word line patterns having a high density adjacent to a DAM structure, there may be difficulty in providing the etching solution due to the presence of the DAM structure. Accordingly, a polymer to be etched may not be sufficiently removed, and a bridge may occur at end portions of the word lines. If dry etching is used, an etch loading effect may occur, which may be caused by a spatial difference in pattern density. Here, also, a bridge may occur at end portions of the word lines,

Embodiments provide a method in which a trim or cell node separation process is performed to a region provided in the same cell region and not to an end portion of the cell region. Accordingly, a trimmed structure may exist in the inner portion of the cell region, and a bridge may be prevented or avoided.

According to example embodiments, a semiconductor device may include lines and remaining line patterns, whose end-portions are provided to have symmetry with respect to each other. Accordingly, it may be possible to prevent a bridge from occurring between the lines.

According to example embodiments, a method of fabricating a semiconductor device may include a spacer trim process, in which a linear spacer spaced apart from a spacer connecting portion is partially removed. Accordingly, it may be possible to apply the same etching condition to both of the end-portion and the sidewall of the spacer and thereby to prevent a bridge from occurring between the lines. This method may also make it possible to prevent the bridge from occurring at end-portions of word lines of a NAND FLASH memory device. Further, even though the bridge occurs, it may be possible to confine a position of the bridge within a region between floating gates in a dummy active region, and thus, the memory device may be normally operated. As the result of the prevention of the bridge, it may be possible to increase a line width (or critical dimension) of the gate line and thereby to improve characteristics of memory cells.

Accordingly, embodiments provide a semiconductor device in which a bridge between conductive lines in prevented from occurring, and provide a method of fabricating a semiconductor device that prevents or avoids a bridge.

While example embodiments have been particularly shown and described, it will be understood by one of ordinary skill in the art that variations in form and detail may be made therein without departing from the spirit and scope of the attached claims.

Example embodiments have been disclosed herein, and although specific terms are employed, they are used and are to be interpreted in a generic and descriptive sense only and not for purpose of limitation. In some instances, as would be apparent to one of ordinary skill in the art as of the filing of the present application, features, characteristics, and/or elements described in connection with a particular embodiment may be used singly or in combination with features, characteristics, and/or elements described in connection with other embodiments unless otherwise specifically indicated. Accordingly, it will be understood by those of skill in the art that various changes in form and details may be made without departing from the spirit and scope of the present invention as set forth in the following claims.

What is claimed is:

1. A semiconductor device comprising:
- a semiconductor substrate including an active region;
- a plurality of conductive lines on the semiconductor substrate; and
- a plurality of conductive line patterns on the semiconductor substrate spaced apart from the plurality of conductive lines, wherein each of the plurality of conductive line patterns corresponds to a respective one of the conductive lines, wherein the plurality of conductive line patterns are arranged in pairs, wherein conductive line patterns of each pair are connected, and wherein conductive line patterns of different pairs are separate.

2. The semiconductor device of claim **1** wherein end portions of each of the plurality of conductive lines extend on the active region of the semiconductor substrate, and wherein end portions of each of the plurality of conductive line patterns extend on the active region of the emiconductor substrate.

3. The semiconductor device of claim **2** further comprising:
- a first plurality of floating gate patterns, wherein each of the first plurality of floating gate patterns is between a respective one of the end portions of the plurality of conductive lines and the active region; and
- a second plurality of floating gate patterns, wherein each of the second plurality of floating gate patterns is between a respective one of the end portions of the plurality of conductive line patterns and the active region, and wherein portions of the active region between the conductive lines and the conductive line patterns are free of the first and second pluralities of floating gate patterns.

4. The semiconductor device of claim **3** further comprising:
- a first plurality of blocking insulating layers, wherein each of the first plurality of blocking insulating layers is between a respective one of the plurality of conductive lines and a respective one of the first plurality of floating gate patterns; and
- a second plurality of blocking insulating layers, wherein each of the second plurality of blocking insulating layers is between a respective one of the plurality of conductive line patterns and a respective one of the second plurality of floating gate patterns.

5. The semiconductor device of claim 3 wherein the first plurality of floating gate patterns comprises a first plurality of polysilicon floating gate patterns, wherein the second plurality of floating gate patterns comprises a second plurality of polysilicon floating gate patterns, and wherein portions of the active region between the conductive lines and the conductive line patterns are free of polysilicon.

6. The semiconductor device of claim 1 wherein each of plurality of conductive lines comprises a layer of polysilicon, and wherein each of the plurality of conductive line patterns comprises a layer of polysilicon.

7. The semiconductor device of claim 6 wherein each of the plurality of conductive lines further comprises a layer of a metal and/or a metal silicide on the respective polysilicon layer, and wherein each of the plurality of conductive line patterns comprises a layer of a metal and/or a metal silicide on the respective polysilicon layer.

8. The semiconductor device of claim 1 wherein the plurality of conductive lines comprise a plurality of conductive word lines, and wherein the active region is a dummy active region, the semiconductor device further comprising:

a memory cell active region spaced apart from the dummy active region;

a plurality of floating gates on the memory cell active region, wherein each of the plurality of floating gates is between a respective one of the plurality of conductive word lines and the memory cell active region; and

a plurality of blocking insulating layers, wherein each of the plurality of blocking insulating layers is between a respective one of the plurality of conductive word lines and a respective one of the plurality of floating gates.

9. The semiconductor device of claim 8 further comprising:

a tunnel insulating layer between the plurality of floating gates and the memory cell active region.

10. The semiconductor device of claim 8 wherein a width of the dummy active region is greater than a width of the memory cell active region.

11. The semiconductor device of claim 2 widths of the end portions of each of the plurality of conductive lines is are greater than widths of portions of each of the plurality of conductive lines spaced apart from the active region.

12. A semiconductor device comprising:

a semiconductor substrate including an active region;

a plurality of conductive lines on the semiconductor substrate;

a first plurality of floating gate patterns, wherein each of the first plurality of floating gate patterns is between a respective one of the end portions of the plurality of conductive lines and the active region;

a plurality of conductive line patterns on the semiconductor substrate spaced apart from the plurality of conductive lines, wherein each of the plurality of conductive line patterns corresponds to a respective one of the conductive lines; and

a second plurality of floating gate patterns, wherein each of the second plurality of floating gate patterns is between a respective one of the end portions of the plurality of conductive line patterns and the active region, and wherein portions of the active region between the conductive lines and the conductive line patterns are free of the first and second pluralities of floating gate patterns.

13. The semiconductor device of claim 12 further comprising:

a first plurality of blocking insulating layers, wherein each of the first plurality of blocking insulating layers is between a respective one of the plurality of conductive fines and a respective one of the first plurality of floating gate patterns; and

a second plurality of blocking insulating layers, wherein each of the second plurality of blocking insulating layers is between a respective one of the plurality of conductive line patterns and a respective one of the second plurality of floating gate patterns.

14. The semiconductor device of claim 12 wherein the first plurality of floating gate patterns comprises a first plurality of polysilicon floating gate patterns, wherein the second plurality of floating gate patterns comprises a second plurality of polysilicon floating gate patterns, and wherein portions of the active region between the conductive lines and the conductive line patterns are free of polysilicon.

15. The semiconductor device of claim 12 wherein the end portions of the plurality of conductive lines on the active region have mirror symmetry with respect to the end portions of the plurality of conductive line patterns on the active region.

16. The semiconductor device of claim 15 wherein the plurality of conductive line patterns are arranged in pairs, wherein conductive line patterns of each pair are connected, and wherein conductive line patterns of different pairs are separate.

17. The semiconductor device of claim 12 wherein each of plurality of conductive lines comprises a layer of polysilicon, and wherein each of the plurality of conductive line patterns comprises a layer of polysilicon.

18. The semiconductor device of claim 17 wherein each of the plurality of conductive lines further comprises a layer of a metal and/or a metal silicide on the respective polysilicon layer, and wherein each of the plurality of conductive line patterns comprises a layer of a metal and/or a metal silicide on the respective polysilicon layer.

19. The semiconductor device of claim 12 wherein the plurality of conductive lines comprise a plurality of conductive word lines, and wherein the active region is a dummy active region, the semiconductor device further comprising:

a memory cell active region spaced apart from the dummy active region;

a plurality of floating gates on the memory cell active region, wherein each of the plurality of floating gates is between a respective one of the plurality of conductive word lines and the memory cell active region; and

a plurality of blocking insulating layers, wherein each of the plurality of blocking insulating layers is between a respective one of the plurality of conductive word lines and a respective one of the plurality of floating gates.

20. The semiconductor device of claim 19 further comprising:

a tunnel insulating layer between the plurality of floating gates and the memory cell active region.

21. The semiconductor device of claim 19 wherein a width of the dummy active region is greater than a width of the memory cell active region.

22. The semiconductor device of claim 12 widths of the end portions of each of the plurality of conductive lines is are greater than widths of portions of each of the plurality of conductive lines spaced apart from the active region.

23. A semiconductor device comprising:

a semiconductor substrate including an active region;

a plurality of conductive lines on the semiconductor substrate, wherein end portions of each of the plurality of conductive lines extend on the active region of the semiconductor substrate; and

a plurality of conductive line patterns on the semiconductor substrate spaced apart from the plurality of conductive lines, wherein end portions of each of the plurality of conductive line patterns extend on the active region of the semiconductor substrate, wherein each of the plurality of conductive line patterns corresponds to a respective one of the conductive lines, and wherein widths of the end portions of each of the plurality of conductive lines are greater than widths of portions of each of the plurality of conductive lines spaced apart from the active region.

24. The semiconductor device of claim **23** further comprising:

a first plurality of floating gate patterns, wherein each of the first plurality of floating gate patterns is between a respective one of the end portions of the plurality of conductive lines and the active region; and

a second plurality of floating gate patterns, wherein each of the second plurality of floating gate patterns is between a respective one of the end portions of the plurality of conductive line patterns and the active region, and wherein portions of the active region between the conductive lines and the conductive line patterns are free of the first and second pluralities of floating gate patterns.

25. The semiconductor device of claim **24** wherein the first plurality of floating gate patterns comprises a first plurality of polysilicon floating gate patterns, wherein the second plurality of floating gate patterns comprises a second plurality of polysilicon floating gate patterns, and wherein portions of the active region are free of polysilicon between the plurality of conductive lines and the plurality of conductive line patterns.

26. The semiconductor device of claim **25** further comprising:

a first plurality of blocking insulating layers, wherein each of the first plurality of blocking insulating layers is between a respective one of the plurality of conductive lines and a respective one of the first plurality of floating gate patterns; and

a second plurality of blocking insulating layers, wherein each of the second plurality of blocking insulating layers is between a respective one of the plurality of conductive line patterns and a respective one of the second plurality of floating gate patterns.

27. The semiconductor device of claim **23** wherein the plurality of conductive line patterns are arranged in pairs, wherein conductive line patterns of each pair are connected, and wherein conductive line patterns of different pairs are separate.

28. The semiconductor device of claim **23** wherein the plurality of conductive lines comprises a plurality of conductive word lines, and wherein the active region is a dummy active region, the semiconductor device further comprising:

a memory cell active region spaced apart from the dummy active region;

a plurality of floating gates on the memory cell active region, wherein each of the plurality of floating gates is between a respective one of the plurality of conductive word lines and the memory cell active region; and

a plurality of blocking insulating layers, wherein each of the plurality of blocking insulating layers is between a respective one of the plurality of conductive word lines and a respective one of the plurality of floating gates.

29. The semiconductor device of claim **23** wherein portions of the active region are free of polysilicon between the plurality of conductive lines and the plurality of conductive line patterns.

* * * * *