



(51) International Patent Classification:

H01L 29/78 (2006.01) *H01L 21/336* (2006.01)
H01L 29/16 (2006.01) *H01L 29/45* (2006.01)

(21) International Application Number:

PCT/US2014/012218

(22) International Filing Date:

20 January 2014 (20.01.2014)

(25) Filing Language:

English

(26) Publication Language:

English

(30) Priority Data:

61/767,922 22 February 2013 (22.02.2013) US
14/159,059 20 January 2014 (20.01.2014) US

(63) Related by continuation (CON) or continuation-in-part (CIP) to earlier application:

US 61/767,922 (CON)
Filed on 22 February 2013 (22.02.2013)

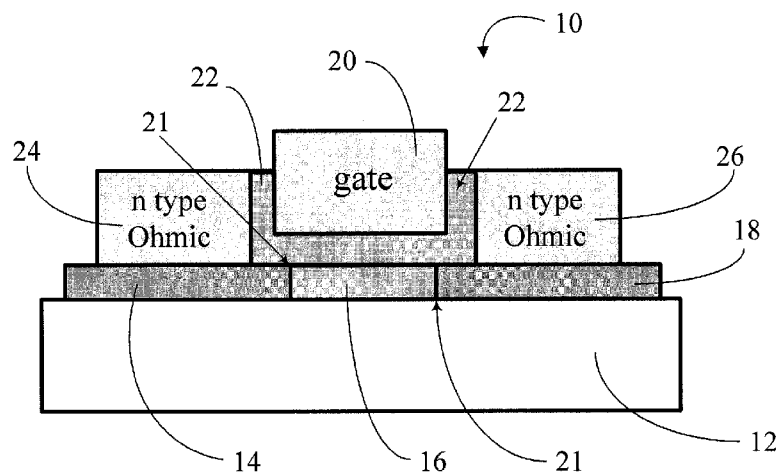
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(81) **Designated States** (unless otherwise indicated, for every kind of national protection available): AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BN, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IR, IS, JP, KE, KG, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LT, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PA, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SA, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(84) **Designated States** (unless otherwise indicated, for every kind of regional protection available): ARIPO (BW, GH, GM, KE, LR, LS, MW, MZ, NA, RW, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, KM, ML, MR, NE, SN, TD, TG).

[Continued on next page]

(54) Title: GRAPHENE HETEROSTRUCTURE FIELD EFFECT TRANSISTORS

**FIG. 1A**

(57) **Abstract:** A field effect transistor includes a substrate, a first graphene (Gr) layer on the substrate, a second graphene (Gr) layer on the substrate, a fluorographene (GrF) layer on the substrate and between the first and second graphene layers, a first ohmic contact on the first graphene layer, a second ohmic contact on the second graphene layer, a gate aligned over the fluorographene layer, and a gate dielectric between the gate and the fluorographene layer and between the gate and the first and second ohmic contacts.



Published:

— *with international search report (Art. 21(3))*

— *with amended claims (Art. 19(1))*

GRAPHENE HETEROSTRUCTURE FIELD EFFECT TRANSISTORS

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CROSS REFERENCE TO RELATED APPLICATIONS

[0001] This application is related to and claims priority
10 to U.S. Provisional Patent Application No. 61/767,922,
filed February 22, 2013, which is hereby incorporated by
reference in its entirety. This application is also
related to and claims priority to U.S. Non-Provisional
Patent Application No. 14/159,059, filed January 20, 2104,
15 which is hereby incorporated by reference in its entirety.

TECHNICAL FIELD

[0002] This disclosure relates to graphene transistors.

20

BACKGROUND

[0003] Several alternative forms of graphene transistors
have been described utilizing wideband gap materials.

[0004] L. Britnell et al., "Field-effect Tunneling
transistor based on vertical graphene heterostructures",
25 Science, vol. 335, p. 947, 2012 describe utilizing
hexagonal boron nitride (h-BN) or MoS₂ as a wideband gap
tunnel barrier for both vertical geometry field effect
transistors (FETs) and vertical graphene heterostructure
tunnel field effect transistors (FETs). The vertical
30 geometry field effect transistors (FETs) demonstrated an
on/off ratio of ~50 (h-BN). The vertical graphene
heterostructure tunnel field effect transistors (FETs)
demonstrated an on/off ratio of ~10⁴ (MoS₂).

[0005] H. Yang, J. Heo, S. Park, H. J. Song, D. H. Seo, K. E. Byun, P. Kim, I. Yoo, H. J. Chung, and K. Kim, "Graphene Barristor, a triode device with a gate-controlled Schottky barrier", Science, vol. 336, p. 6085, 2012 describe

5 graphene/Si vertical barristors with gate control of the graphene/Si Schottky barrier height.

[0006] W. Mehr, J. Dabrowski, J. C. Scheytt, G. Lippert, Y.-H. Xie, M. C. Lemme, M. Ostling, and G. Lupina, "Vertical Graphene Base Transistor", IEEE Electron Dev.

10 Lett., vol. 33, pp. 691, 2012 describe a vertical graphene base transistor.

[0007] What is needed are improved graphene transistors. The embodiments of the present disclosure are an attempt to answer these and other needs.

15

SUMMARY

[0008] In a first embodiment disclosed herein, a field effect transistor comprises a substrate, a first graphene (Gr) layer on the substrate, a second graphene (Gr) layer on the substrate, a fluorographene (GrF) layer on the substrate and between the first and second graphene layers, a first ohmic contact on the first graphene layer, a second ohmic contact on the second graphene layer, a gate aligned over the fluorographene layer, and a gate dielectric between the gate and the fluorographene layer and between the gate and the first and second ohmic contacts.

[0009] In another embodiment disclosed herein, an integrated circuit comprises a substrate, a first heterostructure field effect transistor comprising a first graphene (Gr) layer on the substrate, a second graphene (Gr) layer on the substrate, a first fluorographene (GrF)

layer on the substrate and between the first and second graphene layers, a first ohmic contact on the first graphene layer, a second ohmic contact on the second graphene layer, a first gate aligned over the first fluorographene layer, and a first gate dielectric between the first gate and the first fluorographene layer and between the first gate and the first and second ohmic contacts, wherein the first and second graphene (Gr) layers are n-type, and the first and second ohmic contacts are n-type, and a second heterostructure field effect transistor comprising a third graphene (Gr) layer on the substrate, a fourth graphene (Gr) layer on the substrate, a second fluorographene (GrF) layer on the substrate and between the third and fourth graphene layers, a third ohmic contact on the third graphene layer, a fourth ohmic contact on the fourth graphene layer, a second gate aligned over the second fluorographene layer, and a second gate dielectric between the second gate and the second fluorographene layer and between the second gate and the third and fourth ohmic contacts, wherein the first and second graphene (Gr) layers are n-type, and the first and second ohmic contacts are n-type.

[0010] In still another embodiment disclosed herein, a method of fabricating a heterostructure FET comprises forming graphene on a substrate, forming a graphene mesa by dry etching, forming a first ohmic contact for a source on one end of the graphene mesa, forming a second ohmic contact for a drain on an opposite end of the graphene mesa, forming an opening by masking and etching to expose a portion of the graphene between the first and second ohmic contacts, doping an exposed portion of the graphene with Fluorine, annealing to reduce defects, depositing a gate dielectric over the opening, and forming a gate over the gate dielectric.

[0011] These and other features and advantages will become further apparent from the detailed description and accompanying figures that follow. In the figures and description, numerals indicate the various features, like
5 numerals referring to like features throughout both the drawings and the description.

BRIEF DESCRIPTION OF THE DRAWINGS

10 [0012] FIG. 1A shows a diagram of an n-type graphene (Gr), fluorographene (GrF), and graphene (Gr) heterostructure FET (HFET) in accordance with the present disclosure;

[0013] FIG. 1B shows a band alignment diagram at zero source-drain bias for a Gr/GrF/Gr FET in accordance with
15 the present disclosure;

[0014] FIG. 1C shows a graph of a measured Gr/GrF/Gr diode current vs. diode voltage for two different devices with source-drain spacing of 150 nm and 250 nm, respectively, in accordance with the present disclosure;

20 [0015] FIG. 1D shows a graph of a measured graphene HFET channel resistance as a function of gate voltage in accordance with the present disclosure;

[0016] FIG. 2A shows a band alignment diagram at finite source-drain bias for a Gr/GrF/Gr FET in accordance with
25 the present disclosure;

[0017] FIG. 2B shows a measured direct current (DC) source-drain current-voltage characteristic graph in accordance with the present disclosure;

[0018] FIG. 2C shows a current transfer curve graph as a
30 function of gate voltage at room temperature in accordance with the present disclosure;

[0019] FIG. 3A shows an equivalent circuit for a graphene HFET as a series resistor network in accordance with the present disclosure;

5 [0020] FIG. 3B shows a channel current vs. V_{ds} graph at room temperature for $L_{ds} = 0.25\mu m$ and $L_{ds} = 0.5\mu m$, respectively, in accordance with the present disclosure;

[0021] FIG. 3C shows a graph of the calculated on-state current with respect to GrF barrier thickness in accordance with the present disclosure;

10 [0022] FIG. 4A shows a diagram of a p-type Gr/GrF/Gr HFET in accordance with the present disclosure;

[0023] FIG. 4B shows integration of n- and p-type graphene HFETs on a common substrate in accordance with the present disclosure; and

15 [0024] FIG. 5 shows a method of fabricating a lateral graphene heterostructure FET in accordance with the present disclosure.

20

DETAILED DESCRIPTION

[0025] In the following description, numerous specific details are set forth to clearly describe various specific embodiments disclosed herein. One skilled in the art, however, will understand that the presently claimed invention may be practiced without all of the specific details discussed below. In other instances, well known features have not been described so as not to obscure the invention.

30 [0026] Referring now to FIG. 1A a lateral graphene HFET 10 is shown that has a lateral graphene heterostructure

channel, which has a graphene (Gr) layer 14, a fluorographene (GrF) layer 16, and a graphene (Gr) layer 18 arranged laterally on a substrate 12, which may be Si, SiO₂, SiC, glass, or pyrex among other suitable substrate

5 materials. The fluorographene (GrF) layer 16 is between the graphene (Gr) layer 14 and the the graphene (Gr) layer 18. Ohmic contacts 24 and 26 are on the graphene (Gr) layer 14 and graphene (Gr) layer 18, respectively, for source and drain contacts. A gate 20, which may be any
10 metal, such as gold, is aligned with the fluorographene (GrF) layer 16 and insulated from the fluorographene (GrF) layer 16 by gate dielectric layer 22, which may be silicon nitride (SiN), silicon dioxide (SiO₂), Boron Nitride (BN), aluminum oxide (Al₂O₃), or hafnium oxide (HfO₂), among other
15 suitable insulators. As shown in FIG. 1A, the gate 20 is aligned with the fluorographene (GrF) layer 16 and the gate 20 has dimensions such that the gate 20 overlaps the fluorographene (GrF) layer 16 arranged laterally between the graphene (Gr) layer 14 and the graphene (Gr) layer 18.
20 The edges 21 on either side of the fluorographene (GrF) layer 16 are under and overlapped by gate 20. In order to overlap the fluorographene (GrF) layer 16, the gate 20 has a greater lateral dimension than the fluorographene (GrF) layer 16.

25 **[0027]** The GrF 16 is a wide bandgap material, providing a potential barrier to carrier transport between the graphene (Gr) layer 14 and the graphene (Gr) layer 18. The potential barrier of the GrF 16 is a function of the bias on gate 20. With no gate 20 bias, the graphene HFET 10 is
30 normally-off.

[0028] FIG. 1B shows a schematic sketch of the band alignment at zero source-drain bias for the graphene (Gr) 14, fluorographene (GrF) 16, and graphene (Gr) 18 HFET 10. The conduction and valence band offsets are defined by a

work function difference $\Delta\Phi = \Phi_{\text{Gr}} - \Phi_{\text{GrF}}$. FIG. 2A shows a simplified schematic sketch of the Gr/GrF/Gr band alignment at a finite source-drain bias.

[0029] The current vs. voltage characteristics were measured for lateral Gr/GrF/Gr diodes with lateral channel lengths (Lds) of 150 nm and 250 nm, as shown in FIG. 1C. The diodes showed highly nonlinear I-V curves with turn-on characteristics that indicate the formation of a potential barrier in the GrF layer 16 in the channel.

10 [0030] FIG. 1D shows a graph of measured graphene HFET channel resistance as a function of gate voltage V_{gs} , which shows the Gr 14/GrF 16/Gr 18 channel resistance varying from 3 G Ω to 30 k Ω , which is an on-off resistance ratio of 10^5 , at room temperature with a gate bias applied from 0 V to +5 V. By contrast, the on-off resistance ratio due to modulation of a graphene only channel is less than 10.

[0031] Lateral graphene HFETs according to the present disclosure have a stable operation up to 100 °C.

20 [0032] The heterostructure graphene HFET 10, as shown in FIG. 1A, is an n-type graphene HFET. In an n-type graphene HFET, the graphene (Gr) 14 and the graphene (Gr) 18 are n-type, and the ohmic contacts 24 and 26 are n type ohmic contacts, which may be titanium (Ti) based.

[0033] The heterostructure graphene HFETs were characterized at room temperature in terms of direct current (DC) source-drain current-voltage characteristics and transfer curves, as shown in FIGs. 2B and 2C. As shown in FIGs. 2B and 2C, current pinch-off is observed until the gate is biased to a sufficient positive voltage. The off-state current (I_{off}) was measured to be 0.7 $\mu\text{A}/\text{mm}$ at $V_{\text{ds}} = 1$ V and $V_{\text{gs}} = 0$ V, which shows that lateral graphene HFETs have a normally-off and enhancement-mode operation as a consequence of the GrF barrier 16 in the channel. For $V_{\text{gs}} >$

2 V, the graphene HFETs turned-on and a saturated on-state current (I_{on}) of 5.2 mA/mm for $V_{ds} = 1$ V was measured. The resulting I_{on}/I_{off} ratio at $V_{ds} = 1$ V was measured to be 7,000. The measured I-V curves, as shown in FIG. 2B, also show excellent saturation behavior of the source-drain current. FIG. 2B shows I-V curves for $V_{gs} = +4$ V, reference 30; $V_{gs} = +3.5$ V, reference 32; $V_{gs} = +3$ V, reference 34; $V_{gs} = +2.5$ V, reference 36; $V_{gs} = +2$ V, reference 38; and $V_{gs} = 0 - 2$ V, reference 40.

10 **[0034]** FIG. 3A shows an equivalent circuit for a graphene HFET as series resistor network, showing ohmic contact 24 resistance 50, graphene layer 14 resistance 52, GrF 16 resistance 54, graphene layer 18 resistance 56, and ohmic contact 26 resistance 58.

15 **[0035]** FIG. 3B shows a graph of the channel current versus V_{ds} at room temperature for channel length $L_{ds} = 0.25\mu\text{m}$ and $L_{ds} = 0.5\mu\text{m}$, respectively. The channel current density is 2.5 A/mm for $L_{ds} = 0.5\mu\text{m}$ and 3.1 A/mm for $L_{ds} = 0.25\mu\text{m}$ at $V_{ds} = 1$ V, as shown in FIG. 3B.

20 **[0036]** FIG. 3C is a graph of on-state current with respect to the GrF 16 barrier thickness. FIG. 3C shows a calculated on-state current density for Gr/GrF/Gr FETs with two different mean free paths of 8 nm and 50 nm, with the current density of 3.0 A/mm as $I_{ballistic}$. In the case of $\lambda =$
 25 50 nm, 1000 mA/mm of on-state current can be achieved with ~ 50 nm of GrF barrier thickness.

[0037] A heterostructure graphene HFET 60, as shown in FIG. 4A, may be a p-type graphene HFET. In a p-type graphene HFET 60, the lateral graphene heterostructure
 30 channel has a p-type graphene (Gr) layer 62, a fluorographene (GrF) layer 64, and a p-type graphene (Gr) layer 66 arranged laterally on a substrate 12. Ohmic contacts 68 and 69 are on the graphene (Gr) layer 62 and

graphene (Gr) layer 66, respectively, for source and drain contacts. The ohmic contacts 68 and 69 are p type ohmic contacts and may be palladium (Pd) based. A gate 70 is aligned with the fluorographene (GrF) layer 64 and

5 insulated from the fluorographene (GrF) layer 64 by gate dielectric layer 72. As shown in FIG. 4A, the gate 70 is aligned with the fluorographene (GrF) layer 64 and the gate 70 has dimensions such that the gate 70 overlaps the fluorographene (GrF) layer 64 arranged laterally between
10 the graphene (Gr) layer 62 and the graphene (Gr) layer 66. In order to overlap the fluorographene (GrF) layer 64, the gate 70 has a greater lateral dimension than the fluorographene (GrF) layer 64.

[0038] The n-type graphene HFET 10, shown in FIG. 1A, and
15 the p-type graphene HFET 60, shown in FIG. 4A, may be integrated on a common substrate 12, as shown in FIG. 4B.

[0039] As shown in the flow diagram of FIG. 5, a method of fabricating a lateral graphene heterostructure FET includes the following steps: in step 100 forming graphene on a
20 substrate by chemical vapor deposition (CVD) or epitaxial processes, in step 102 forming a graphene mesa by dry etching, in step 104 forming ohmic contacts on opposite ends of the graphene mesa for source and drain contact. The ohmic contacts may be either n-type or p-type, in step
25 106 forming an opening by masking and etching to expose a portion of the graphene between the source and drain, in step 108 doping the exposed portion of the graphene with Fluorine doping using either XeF₂ or other gas chemistry or gas plasma chemistry, in step 110 annealing to reduce
30 defects, in step 112 depositing a gate dielectric in the opening, and in step 114 forming a metal gate over the gate dielectric. This can be followed by a metal2 layer process to connect with other circuitry.

[0040] The step of forming graphene on a substrate or wafer may be use normal by epitaxial processes. Alternatively, the step of forming graphene on a substrate or wafer may be performed by using chemical vapor deposition (CVD) to deposit a graphene layer on a metal foil and then transferring the graphene layer to a substrate.

[0041] As discussed above, the substrate 12 may be Si, SiO₂, SiC, glass, or pyrex among other suitable substrate materials. The fluorographene (GrF) layer 16 formed between the graphene (Gr) layer 14 and the graphene (Gr) layer 18. The ohmic contacts 24 and 26 are formed on the graphene (Gr) layer 14 and graphene (Gr) layer 18, respectively, for source and drain contacts. The gate 20 is aligned with the fluorographene (GrF) layer 16 and insulated from the fluorographene (GrF) layer 16 by gate dielectric layer 22, which may be silicon nitride (SiN), silicon dioxide (SiO₂), Boron Nitride (BN), aluminum oxide (Al₂O₃), or hafnium oxide (HfO₂), among other suitable insulators.

[0042] In an n-type graphene HFET, the graphene (Gr) 14 and the graphene (Gr) 18 are n-type, and the ohmic contacts 24 and 26 are n type ohmic contacts, which may be titanium (Ti) based. In a p-type graphene HFET 60, the lateral graphene heterostructure channel has a p-type graphene (Gr) layer 62 and a p-type graphene (Gr) layer 66, and the ohmic contacts 68 and 69 are p type ohmic contacts and may be palladium (Pd) based.

[0043] All elements, parts and steps described herein are preferably included. It is to be understood that any of these elements, parts and steps may be replaced by other elements, parts and steps or deleted altogether as will be obvious to those skilled in the art.

CONCEPTS

At least the following concepts are included in the present disclosure.

5 Concept 1. A field effect transistor comprising:

a substrate;

a first graphene (Gr) layer on the substrate;

a second graphene (Gr) layer on the substrate;

a fluorographene (GrF) layer on the substrate and

10 between the first and second graphene layers;

a first ohmic contact on the first graphene layer;

a second ohmic contact on the second graphene layer;

a gate aligned over the fluorographene layer; and

a gate dielectric between the gate and the

15 fluorographene layer and between the gate and the first and second ohmic contacts.

Concept 2. The field effect transistor of Concept 1 wherein:

20 the first and second graphene (Gr) layers are n-type; and

the first and second ohmic contacts are n-type.

Concept 3. The field effect transistor of Concept 1

25 wherein:

the first and second graphene (Gr) layers are p-type;

and

the first and second ohmic contacts are p-type.

30 Concept 4. The field effect transistor of Concept 1

wherein the first graphene (Gr) layer, the fluorographene (GrF) layer, and the second graphene (Gr) layer are arranged laterally to one another on the substrate.

Concept 5. The field effect transistor of Concept 1 wherein the substrate comprises Si, SiO₂, SiC, glass, or pyrex.

Concept 6. The field effect transistor of Concept 1 wherein
5 the gate dielectric layer comprises silicon nitride (SiN), silicon dioxide (SiO₂), Boron Nitride (BN), aluminum oxide (Al₂O₃), or hafnium oxide (HfO₂).

Concept 7. The field effect transistor of Concept 1
10 wherein the first graphene (Gr) layer, the fluorographene (GrF) layer, and the second graphene (Gr) layer form a normally off channel.

Concept 8. The field effect transistor of Concept 1 wherein
15 an on-off resistance ratio is equal or greater than 10⁵.

Concept 9. The field effect transistor of Concept 1 wherein the gate overlaps the fluorographene (GrF) layer.

20 Concept 10. An integrated circuit comprising:

a substrate;

a first heterostructure field effect transistor
comprising:

a first graphene (Gr) layer on the substrate;

25 a second graphene (Gr) layer on the substrate;

a first fluorographene (GrF) layer on the
substrate and between the first and second graphene layers;

a first ohmic contact on the first graphene
layer;

30 a second ohmic contact on the second graphene
layer;

a first gate aligned over the first
fluorographene layer; and

a first gate dielectric between the first gate and the first fluorographene layer and between the first gate and the first and second ohmic contacts;

5 wherein the first and second graphene (Gr) layers are n-type, and the first and second ohmic contacts are n-type; and

a second heterostructure field effect transistor comprising:

10 a third graphene (Gr) layer on the substrate;
a fourth graphene (Gr) layer on the substrate;
a second fluorographene (GrF) layer on the substrate and between the third and fourth graphene layers;
a third ohmic contact on the third graphene layer;

15 a fourth ohmic contact on the fourth graphene layer;

a second gate aligned over the second fluorographene layer; and

20 a second gate dielectric between the second gate and the second fluorographene layer and between the second gate and the third and fourth ohmic contacts;

wherein the first and second graphene (Gr) layers are n-type, and the first and second ohmic contacts are n-type.

25

Concept 11. The integrated circuit of Concept 10 wherein the substrate comprises Si, SiO₂, SiC, glass, or pyrex.

30 Concept 12. The integrated circuit of Concept 10 wherein the first and second gate dielectric layers comprise silicon nitride (SiN), silicon dioxide (SiO₂), Boron Nitride (BN), aluminum oxide (Al₂O₃), or hafnium oxide (HfO₂).

Concept 13. The integrated circuit of Concept 10 wherein:

the first gate overlaps the first fluorographene (GrF) layer; and

the second gate overlaps the second fluorographene (GrF) layer.

5

Concept 14. A method of fabricating a heterostructure FET comprises:

forming graphene on a substrate;

forming a graphene mesa by dry etching;

10 forming a first ohmic contact for a source on one end of the graphene mesa;

forming a second ohmic contact for a drain on an opposite end of the graphene mesa;

15 forming an opening by masking and etching to expose a portion of the graphene between the first and second ohmic contacts;

doping an exposed portion of the graphene with Fluorine;

annealing to reduce defects;

20 depositing a gate dielectric over the opening; and forming a gate over the gate dielectric.

Concept 15. The method of Concept 14 wherein forming graphene on a substrate comprises epitaxial processes to
25 form graphene on the substrate, or using chemical vapor deposition (CVD) to deposit the graphene layer on a metal foil and then transferring the graphene layer to the substrate.

30 Concept 16. The method of Concept 14 wherein doping the exposed portion of the graphene with Fluorine doping comprises using XeF₂ or other gas chemistry or gas plasma chemistry.

35 Concept 17. The method of Concept 14 wherein:

the graphene is n-type; and
the first and second ohmic contacts are n-type.

Concept 18. The method of Concept 14 wherein:

5 the graphene is p-type; and
the first and second ohmic contacts are p-type.

Concept 19. The method of Concept 14 wherein the substrate
comprises Si, SiO₂, SiC, glass, or pyrex.

10

Concept 20. The method of Concept 14 wherein the gate
dielectric layer comprises silicon nitride (SiN), silicon
dioxide (SiO₂), Boron Nitride (BN), aluminum oxide (Al₂O₃),
or hafnium oxide (HfO₂).

15

Concept 21. The method of Concept 14 wherein the gate is
formed to overlap the portion of the graphene doped with
Fluorine.

20 **[0044]** Having now described the invention in accordance
with the requirements of the patent statutes, those skilled
in this art will understand how to make changes and
modifications to the present invention to meet their
specific requirements or conditions. Such changes and
25 modifications may be made without departing from the scope
and spirit of the invention as disclosed herein.

[0045] The foregoing Detailed Description of exemplary
and preferred embodiments is presented for purposes of
illustration and disclosure in accordance with the
30 requirements of the law. It is not intended to be
exhaustive nor to limit the invention to the precise
form(s) described, but only to enable others skilled in the
art to understand how the invention may be suited for a
particular use or implementation. The possibility of
35 modifications and variations will be apparent to

practitioners skilled in the art. No limitation is intended by the description of exemplary embodiments which may have included tolerances, feature dimensions, specific operating conditions, engineering specifications, or the like, and which may vary between implementations or with changes to the state of the art, and no limitation should be implied therefrom. Applicant has made this disclosure with respect to the current state of the art, but also contemplates advancements and that adaptations in the future may take into consideration of those advancements, namely in accordance with the then current state of the art. It is intended that the scope of the invention be defined by the Claims as written and equivalents as applicable. Reference to a claim element in the singular is not intended to mean "one and only one" unless explicitly so stated. Moreover, no element, component, nor method or process step in this disclosure is intended to be dedicated to the public regardless of whether the element, component, or step is explicitly recited in the Claims. No claim element herein is to be construed under the provisions of 35 U.S.C. Sec. 112, sixth paragraph, unless the element is expressly recited using the phrase "means for. . . ." and no method or process step herein is to be construed under those provisions unless the step, or steps, are expressly recited using the phrase "comprising the step(s) of. . . ."

WHAT IS CLAIMED IS:

1. A field effect transistor comprising:

a substrate;

5 a first graphene (Gr) layer on the substrate;

a second graphene (Gr) layer on the substrate;

a fluorographene (GrF) layer on the substrate and
between the first and second graphene layers;

a first ohmic contact on the first graphene layer;

10 a second ohmic contact on the second graphene layer;

a gate aligned over the fluorographene layer; and

a gate dielectric between the gate and the
fluorographene layer and between the gate and the first and
second ohmic contacts.

15

2. The field effect transistor of claim 1 wherein:

the first and second graphene (Gr) layers are n-type;
and

the first and second ohmic contacts are n-type.

20

3. The field effect transistor of claim 1 wherein:

the first and second graphene (Gr) layers are p-type;
and

the first and second ohmic contacts are p-type.

25

4. The field effect transistor of claim 1 wherein the
first graphene (Gr) layer, the fluorographene (GrF) layer,
and the second graphene (Gr) layer are arranged laterally
to one another on the substrate.

5. The field effect transistor of claim 1 wherein the substrate comprises Si, SiO₂, SiC, glass, or pyrex.

5 6. The field effect transistor of claim 1 wherein the gate dielectric layer comprises silicon nitride (SiN), silicon dioxide (SiO₂), Boron Nitride (BN), aluminum oxide (Al₂O₃), or hafnium oxide (HfO₂).

10 7. The field effect transistor of claim 1 wherein the first graphene (Gr) layer, the fluorographene (GrF) layer, and the second graphene (Gr) layer form a normally off channel.

15 8. The field effect transistor of claim 1 wherein an on-off resistance ratio is equal or greater than 10⁵.

9. The field effect transistor of claim 1 wherein the gate overlaps the fluorographene (GrF) layer.

20

10. An integrated circuit comprising:

a substrate;

a first heterostructure field effect transistor comprising:

25 a first graphene (Gr) layer on the substrate;
a second graphene (Gr) layer on the substrate;
a first fluorographene (GrF) layer on the substrate and between the first and second graphene layers;
a first ohmic contact on the first graphene
30 layer;

a second ohmic contact on the second graphene layer;

a first gate aligned over the first fluorographene layer; and

5 a first gate dielectric between the first gate and the first fluorographene layer and between the first gate and the first and second ohmic contacts;

wherein the first and second graphene (Gr) layers are n-type, and the first and second ohmic contacts are n-
10 type; and

a second heterostructure field effect transistor comprising:

a third graphene (Gr) layer on the substrate;

a fourth graphene (Gr) layer on the substrate;

15 a second fluorographene (GrF) layer on the substrate and between the third and fourth graphene layers;

a third ohmic contact on the third graphene layer;

a fourth ohmic contact on the fourth graphene
20 layer;

a second gate aligned over the second fluorographene layer; and

a second gate dielectric between the second gate and the second fluorographene layer and between the second
25 gate and the third and fourth ohmic contacts;

wherein the first and second graphene (Gr) layers are n-type, and the first and second ohmic contacts are n-type.

30 11. The integrated circuit of claim 10 wherein the substrate comprises Si, SiO₂, SiC, glass, or pyrex.

12. The integrated circuit of claim 10 wherein the first and second gate dielectric layers comprise silicon nitride (SiN), silicon dioxide (SiO₂), Boron Nitride (BN), aluminum
5 oxide (Al₂O₃), or hafnium oxide (HfO₂).

13. The integrated circuit of claim 10 wherein:

the first gate overlaps the first fluorographene (GrF) layer; and

10 the second gate overlaps the second fluorographene (GrF) layer.

14. A method of fabricating a heterostructure FET comprises:

15 forming graphene on a substrate;

forming a graphene mesa by dry etching;

forming a first ohmic contact for a source on one end of the graphene mesa;

20 forming a second ohmic contact for a drain on an opposite end of the graphene mesa;

forming an opening by masking and etching to expose a portion of the graphene between the first and second ohmic contacts;

25 doping an exposed portion of the graphene with Fluorine;

annealing to reduce defects;

depositing a gate dielectric over the opening; and

forming a gate over the gate dielectric.

15. The method of claim 14 wherein forming graphene on a substrate comprises epitaxial processes to form graphene on the substrate, or using chemical vapor deposition (CVD) to deposit the graphene layer on a metal foil and then
5 transferring the graphene layer to the substrate.

16. The method of claim 14 wherein doping the exposed portion of the graphene with Fluorine doping comprises using XeF₂ or other gas chemistry or gas plasma chemistry.
10

17. The method of claim 14 wherein:
the graphene is n-type; and
the first and second ohmic contacts are n-type.

15 18. The method of claim 14 wherein:
the graphene is p-type; and
the first and second ohmic contacts are p-type.

19. The method of claim 14 wherein the substrate comprises
20 Si, SiO₂, SiC, glass, or pyrex.

20. The method of claim 14 wherein the gate dielectric layer comprises silicon nitride (SiN), silicon dioxide (SiO₂), Boron Nitride (BN), aluminum oxide (Al₂O₃), or
25 hafnium oxide (HfO₂).

21. The method of claim 14 wherein the gate is formed to overlap the portion of the graphene doped with Fluorine.

AMENDED CLAIMS
received by the International Bureau on
01 JULY 2014
(01.07.2014)

WHAT IS CLAIMED IS:

1. A field effect transistor comprising:

- a substrate;
- a first graphene (Gr) layer on the substrate;
- a second graphene (Gr) layer on the substrate;
- a fluorographene (GrF) layer on the substrate and between the first and second graphene layers;
- a first ohmic contact on the first graphene layer;
- a second ohmic contact on the second graphene layer;
- a gate aligned over the fluorographene layer; and
- a gate dielectric between the gate and the fluorographene layer and between the gate and the first and second ohmic contacts;

wherein the first graphene (Gr) layer, the fluorographene (GrF) layer, and the second graphene (Gr) layer form a normally off channel.

2. The field effect transistor of claim 1 wherein:

- the first and second graphene (Gr) layers are n-type; and

- the first and second ohmic contacts are n-type.

3. The field effect transistor of claim 1 wherein:

- the first and second graphene (Gr) layers are p-type; and

- the first and second ohmic contacts are p-type.

4. The field effect transistor of claim 1 wherein the first graphene (Gr) layer, the fluorographene (GrF) layer, and the second graphene (Gr) layer are arranged laterally to one another on the substrate.
5. The field effect transistor of claim 1 wherein the substrate comprises Si, SiO₂, SiC, glass, or pyrex.
6. The field effect transistor of claim 1 wherein the gate dielectric layer comprises silicon nitride (SiN), silicon dioxide (SiO₂), Boron Nitride (BN), aluminum oxide (Al₂O₃), or hafnium oxide (HfO₂).
7. The field effect transistor of claim 1 wherein an on-off resistance ratio is equal or greater than 10⁵.
8. The field effect transistor of claim 1 wherein the gate overlaps the fluorographene (GrF) layer.
9. An integrated circuit comprising:
 - a substrate;
 - a first heterostructure field effect transistor comprising:
 - a first graphene (Gr) layer on the substrate;
 - a second graphene (Gr) layer on the substrate;
 - a first fluorographene (GrF) layer on the substrate and between the first and second graphene layers;

a first ohmic contact on the first graphene layer;

a second ohmic contact on the second graphene layer;

a first gate aligned over the first fluorographene layer; and

a first gate dielectric between the first gate and the first fluorographene layer and between the first gate and the first and second ohmic contacts;

wherein the first and second graphene (Gr) layers are n-type, and the first and second ohmic contacts are n-type; and

a second heterostructure field effect transistor comprising:

a third graphene (Gr) layer on the substrate;

a fourth graphene (Gr) layer on the substrate;

a second fluorographene (GrF) layer on the substrate and between the third and fourth graphene layers;

a third ohmic contact on the third graphene layer;

a fourth ohmic contact on the fourth graphene layer;

a second gate aligned over the second fluorographene layer; and

a second gate dielectric between the second gate and the second fluorographene layer and between the second gate and the third and fourth ohmic contacts;

wherein the third and fourth graphene (Gr) layers are p-type, and the third and fourth ohmic contacts are p-type.

10. The integrated circuit of claim 9 wherein the substrate comprises Si, SiO₂, SiC, glass, or pyrex.

11. The integrated circuit of claim 9 wherein the first and second gate dielectric layers comprise silicon nitride (SiN), silicon dioxide (SiO₂), Boron Nitride (BN), aluminum oxide (Al₂O₃), or hafnium oxide (HfO₂).

12. The integrated circuit of claim 9 wherein:

the first gate overlaps the first fluorographene (GrF) layer; and

the second gate overlaps the second fluorographene (GrF) layer.

13. A method of fabricating a heterostructure FET comprises:

forming graphene on a substrate;

forming a graphene mesa by dry etching;

forming a first ohmic contact for a source on one end of the graphene mesa;

forming a second ohmic contact for a drain on an opposite end of the graphene mesa;

forming an opening by masking and etching to expose a portion of the graphene between the first and second ohmic contacts;

doping an exposed portion of the graphene with Fluorine;

annealing to reduce defects;

depositing a gate dielectric over the opening; and

forming a gate over the gate dielectric.

14. The method of claim 13 wherein forming graphene on a substrate comprises epitaxial processes to form graphene on the substrate, or using chemical vapor deposition (CVD) to deposit the graphene layer on a metal foil and then transferring the graphene layer to the substrate.

15. The method of claim 13 wherein doping the exposed portion of the graphene with Fluorine doping comprises using XeF₂ or other gas chemistry or gas plasma chemistry.

16. The method of claim 13 wherein:

the graphene is n-type; and

the first and second ohmic contacts are n-type.

17. The method of claim 13 wherein:

the graphene is p-type; and

the first and second ohmic contacts are p-type.

18. The method of claim 13 wherein the substrate comprises Si, SiO₂, SiC, glass, or pyrex.

19. The method of claim 13 wherein the gate dielectric layer comprises silicon nitride (SiN), silicon dioxide (SiO₂), Boron Nitride (BN), aluminum oxide (Al₂O₃), or hafnium oxide (HfO₂).

20. The method of claim 13 wherein the gate is formed to overlap the portion of the graphene doped with Fluorine.

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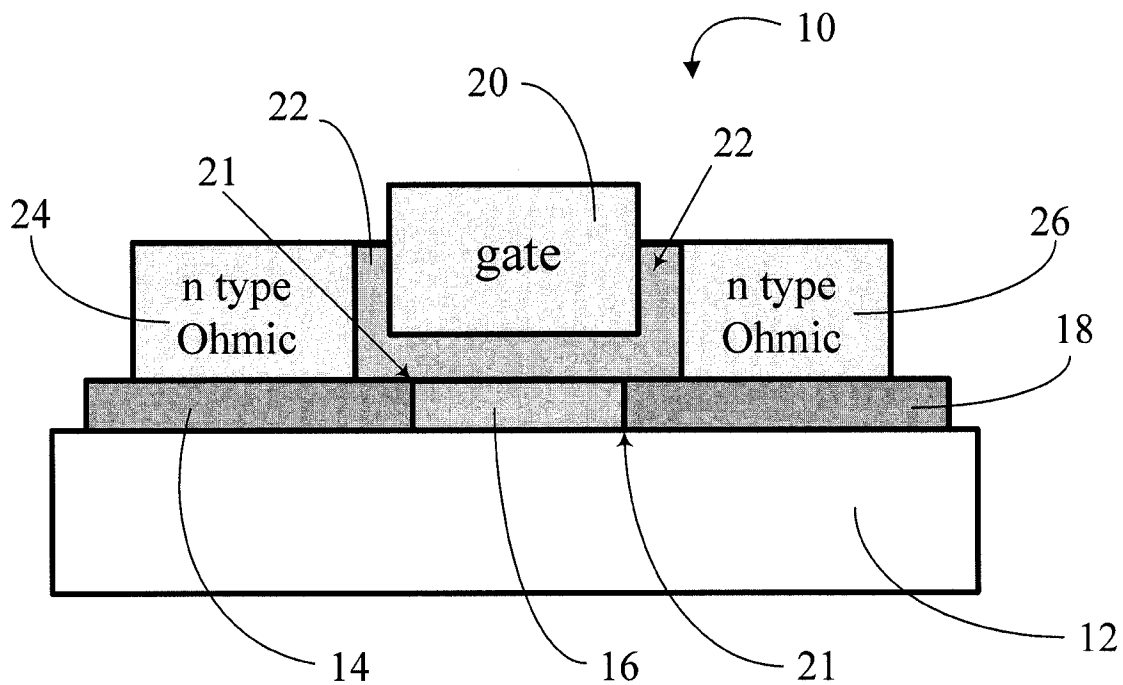


FIG. 1A

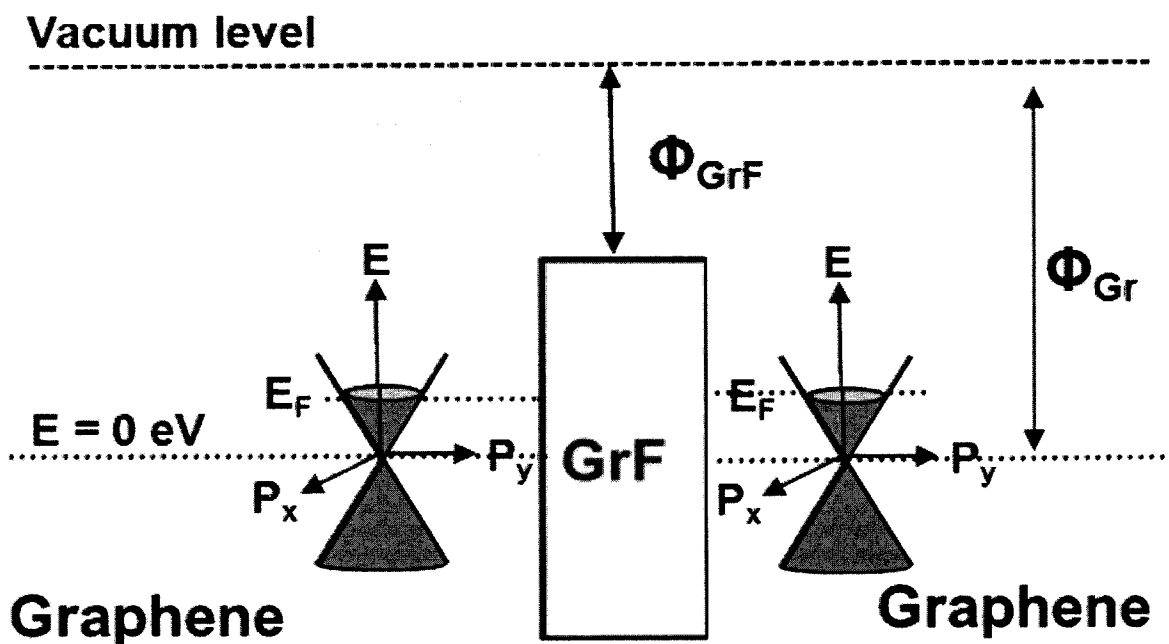
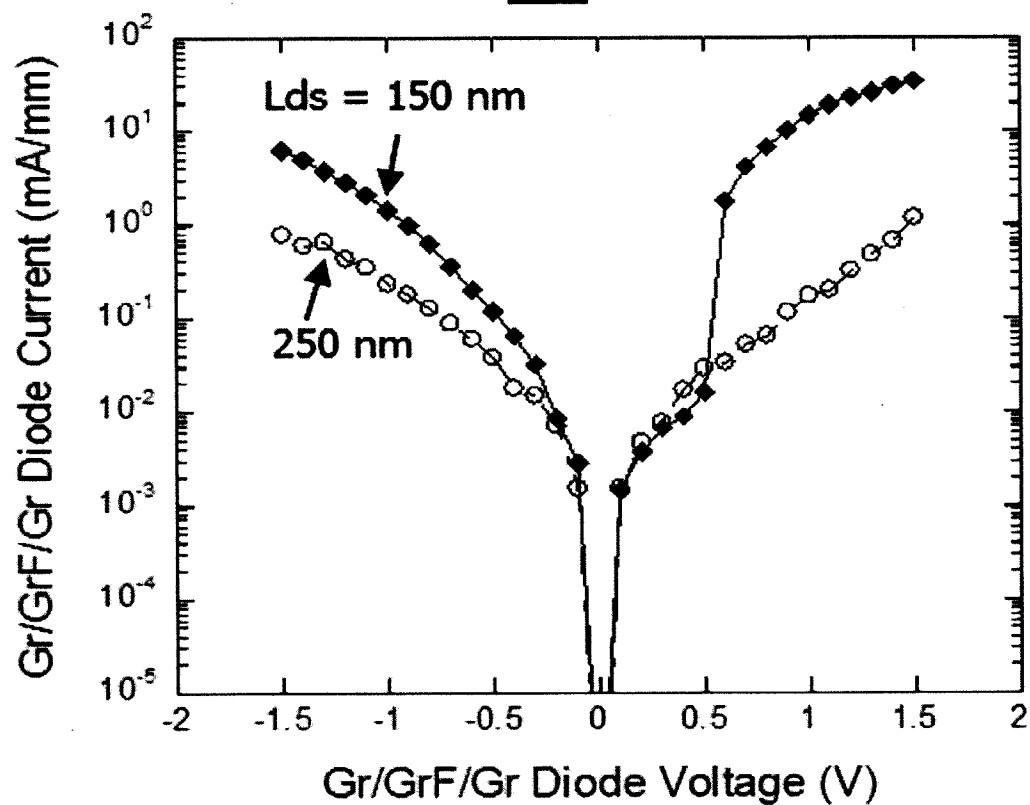
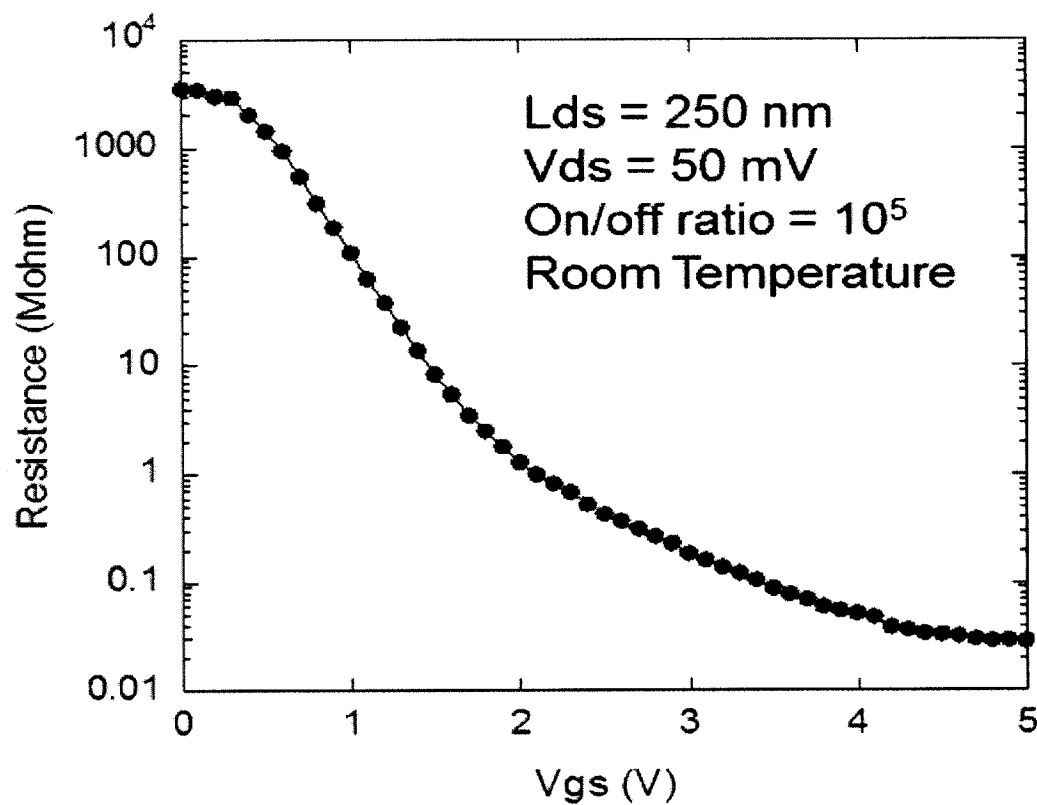


FIG. 1B

2/6**FIG. 1C****FIG. 1D**

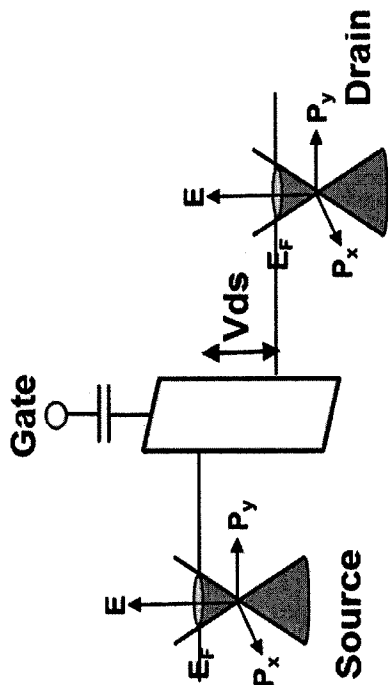


FIG. 2A

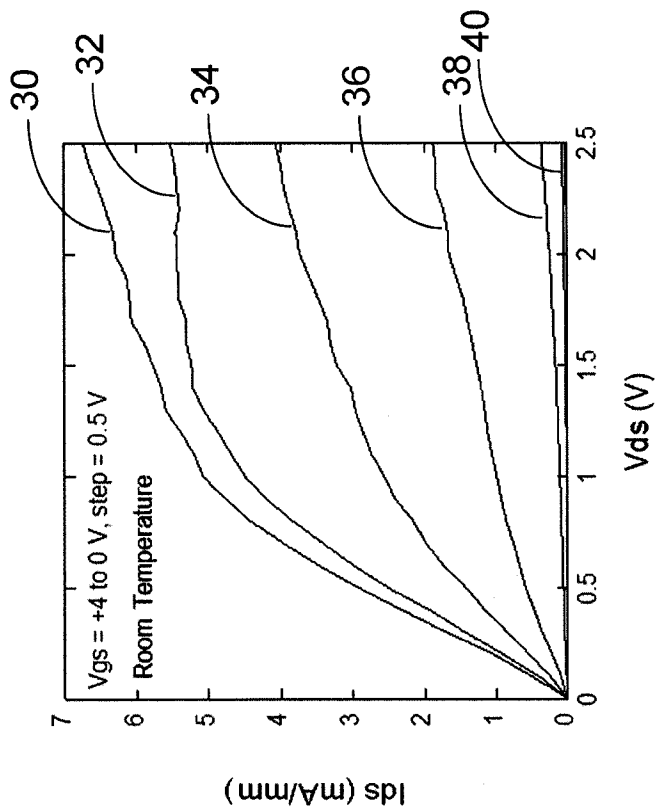


FIG. 2B

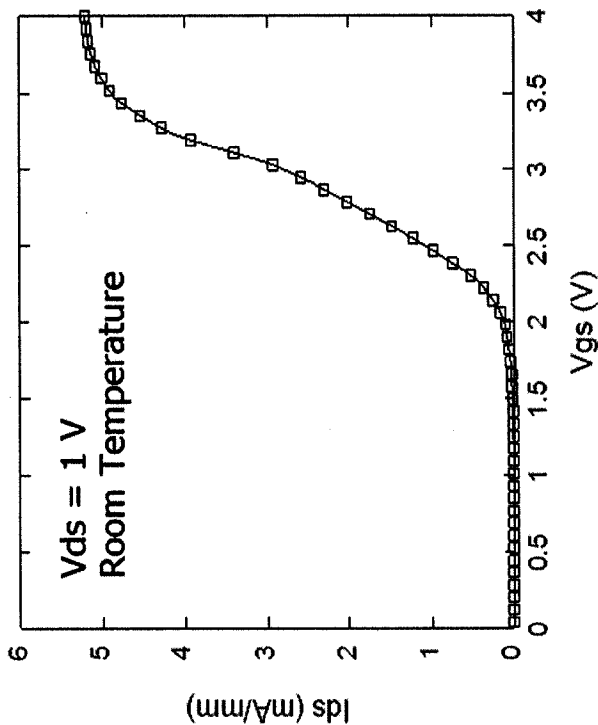
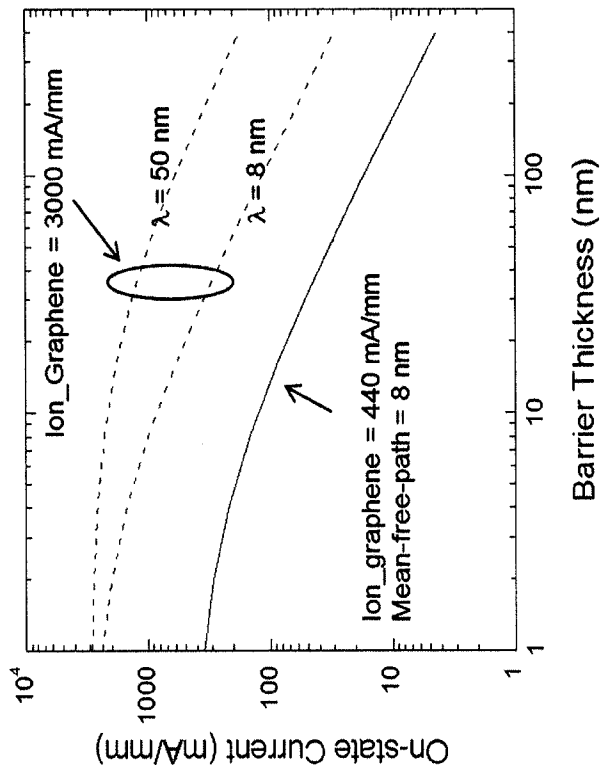
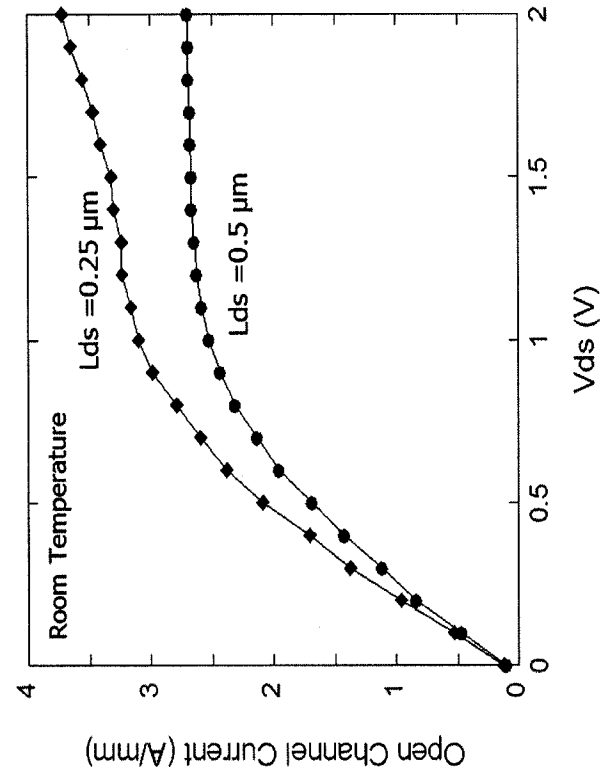
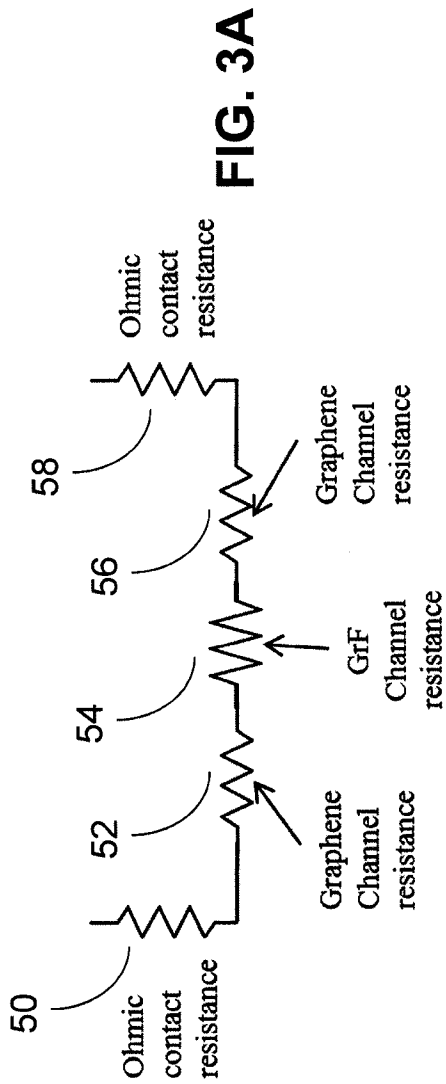


FIG. 2C



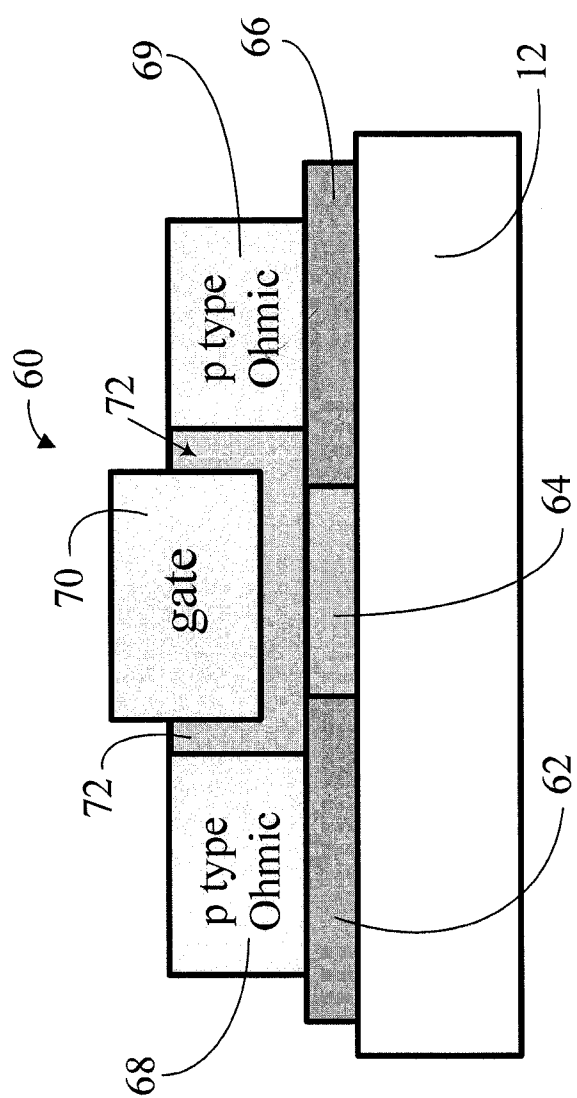


FIG. 4A

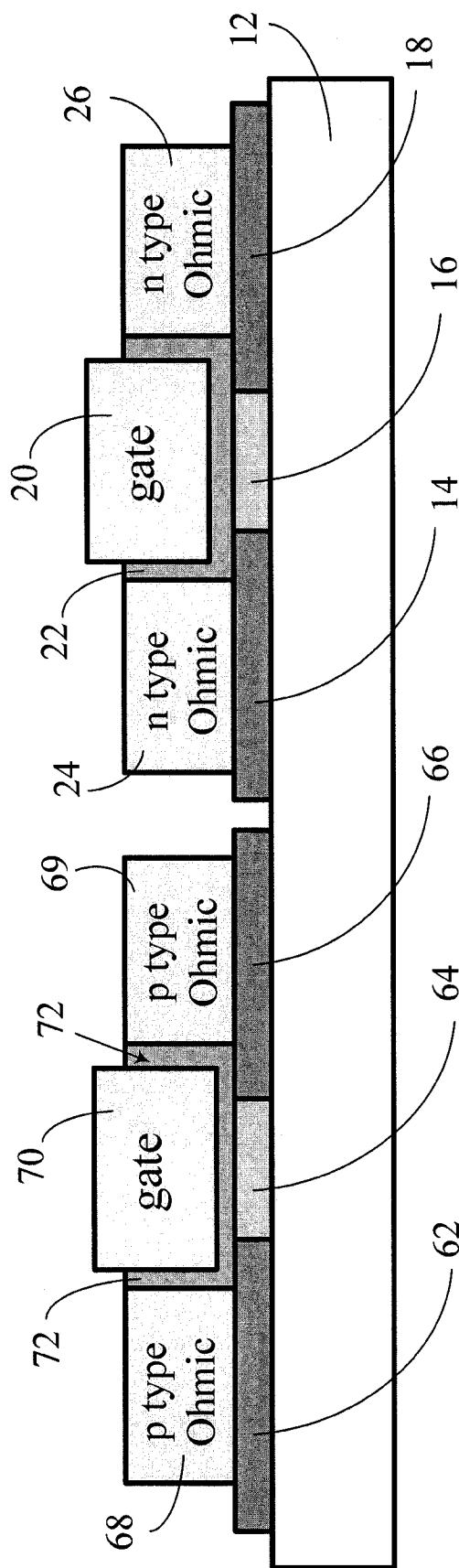


FIG. 4B

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FORMING GRAPHENE ON A SUBSTRATE	100
FORMING A GRAPHENE MESA BY DRY ETCHING	102
FORMING GRAPHENE OHMIC CONTACTS FOR A SOURCE AND A DRAIN	104
FORMING AN OPENING BY MASKING AND ETCHING TO EXPOSE A PORTION OF THE GRAPHENE BETWEEN THE SOURCE AND DRAIN	106
DOPING THE EXPOSED PORTION OF THE GRAPHENE WITH FLUORINE DOPING USING EITHER XEF ₂ OR OTHER GAS CHEMISTRY OR GAS PLASMA CHEMISTRY	108
ANNEALING TO REDUCE DEFECTS	110
DEPOSITING A GATE DIELECTRIC IN THE OPENING, AND	112
FORMING A GATE OVER THE GATE DIELECTRIC.	114

FIG. 5

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2014/012218**A. CLASSIFICATION OF SUBJECT MATTER****H01L 29/78(2006.01)i, H01L 29/16(2006.01)i, H01L 21/336(2006.01)i, H01L 29/45(2006.01)i**

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

H01L 29/78; C08K 5/03; H01L 21/336; H01L 21/04; C01B 31/02; H01L 29/66; C01B 31/04; C09D 201/04; H01L 29/16; H01L 29/45

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Korean utility models and applications for utility models

Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

eKOMPASS(KIPO internal) & Keywords: fluorographene, transistor, channel, gate, normally off

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2012-0085991 A1 (GUY COHEN et al.) 12 April 2012 See abstract, paragraphs [0031]-[0069] and figures 1-12B.	1,4-6,8,9
A		2,3,7,10-21
A	US 2011-0303121 A1 (ANDRE GEIM et al.) 15 December 2011 See abstract, paragraphs [0023]-[0038] and figures 1-5.	1-21
A	KR 10-2012-0136118 A (KUMOH NATIONAL INSTITUTE OF TECHNOLOGY INDUSTRY-ACADEMIC COOPERATION FOUNDATION) 18 December 2012 See abstract, paragraphs [0024]-[0050] and figures 1-12.	1-21
A	KR 10-2012-0068390 A (SAMSUNG ELECTRONICS CO., LTD.) 27 June 2012 See abstract, paragraphs [0043]-[0067] and figures 1-5e.	1-21
A	WO 2012-051597 A2 (THE REGENTS OF THE UNIVERSITY OF CALIFORNIA) 19 April 2012 See abstract and paragraphs [0004]-[0012].	1-21

☐ Further documents are listed in the continuation of Box C.☒ See patent family annex.

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"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search

12 May 2014 (12.05.2014)

Date of mailing of the international search report

12 May 2014 (12.05.2014)

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INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.

PCT/US2014/012218

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