

Oct. 3, 1967

L. A. CHAMBERLIN, JR

3,345,631

PHASED ARRAY RADAR ANTENNA SCAN CONTROL

Filed Sept. 18, 1964

5 Sheets-Sheet 1

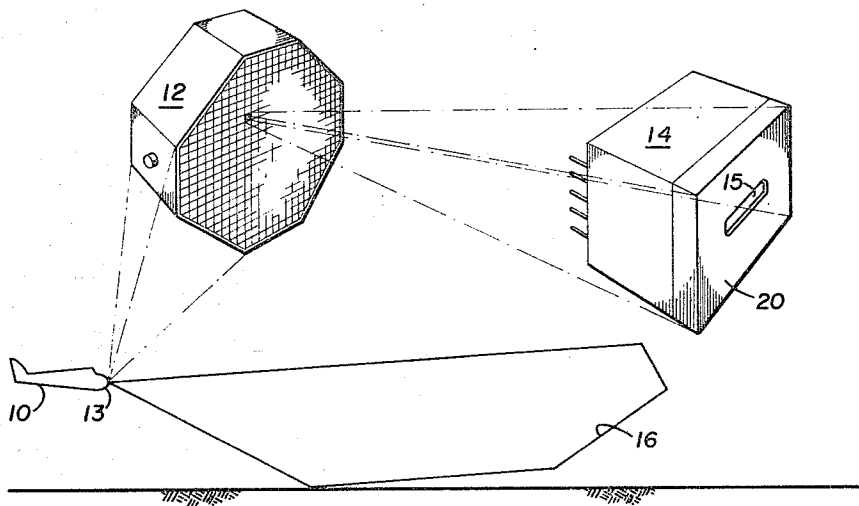


FIG. 1

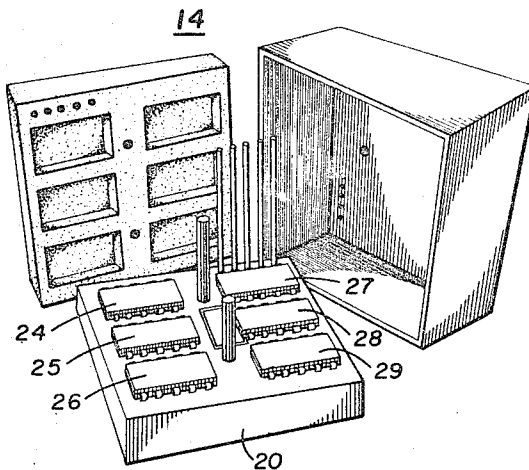


FIG. 2

INVENTOR

LEO A. CHAMBERLIN, JR.

BY *D. Kane*

ATTORNEY

Oct. 3, 1967

L. A. CHAMBERLIN, JR

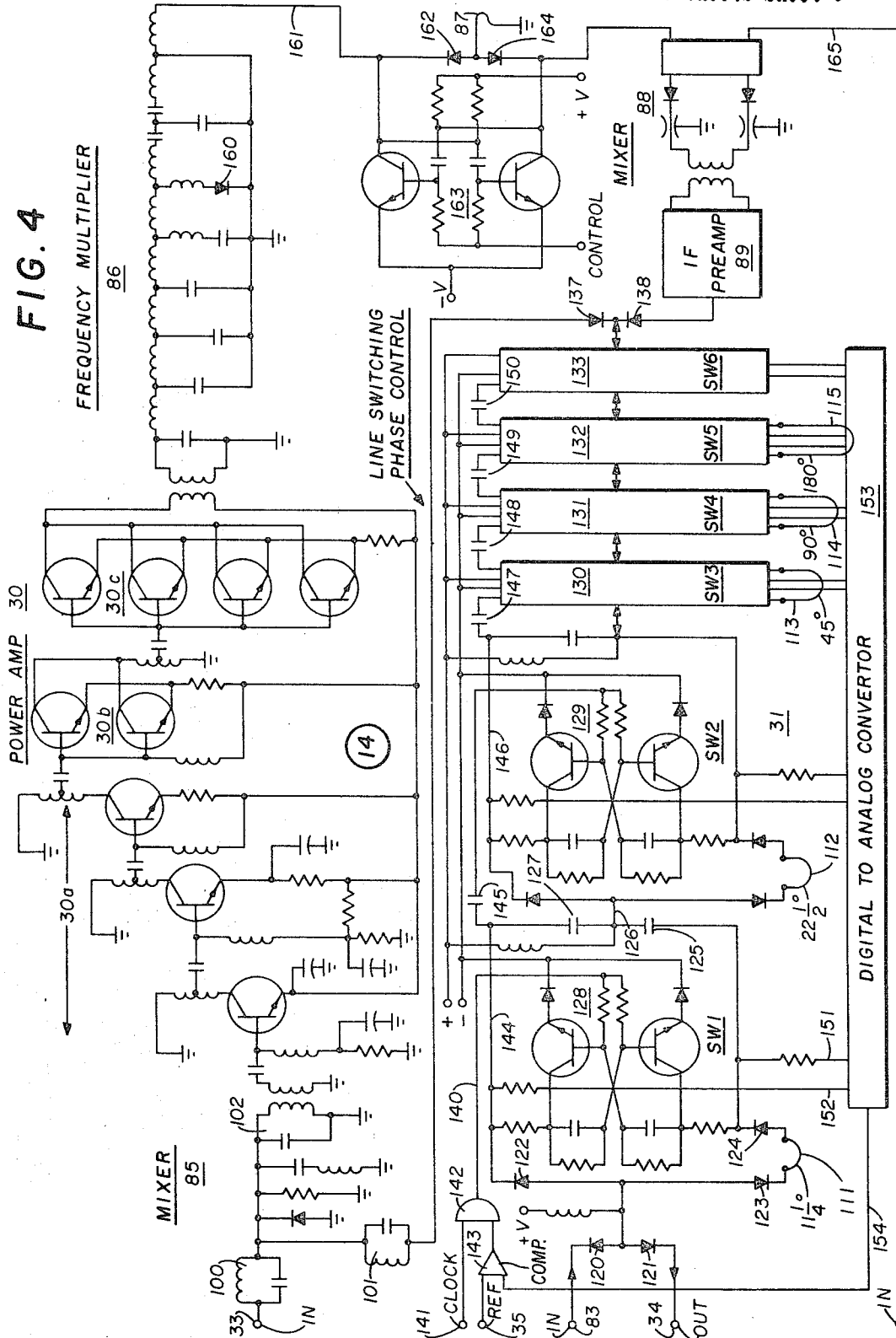
3,345,631

PHASED ARRAY RADAR ANTENNA SCAN CONTROL

Filed Sept. 18, 1964

5 Sheets-Sheet 3

FIG. 4



Oct. 3, 1967

L. A. CHAMBERLIN, JR

3,345,631

PHASED ARRAY RADAR ANTENNA SCAN CONTROL

Filed Sept. 18, 1964

5 Sheets-Sheet 4

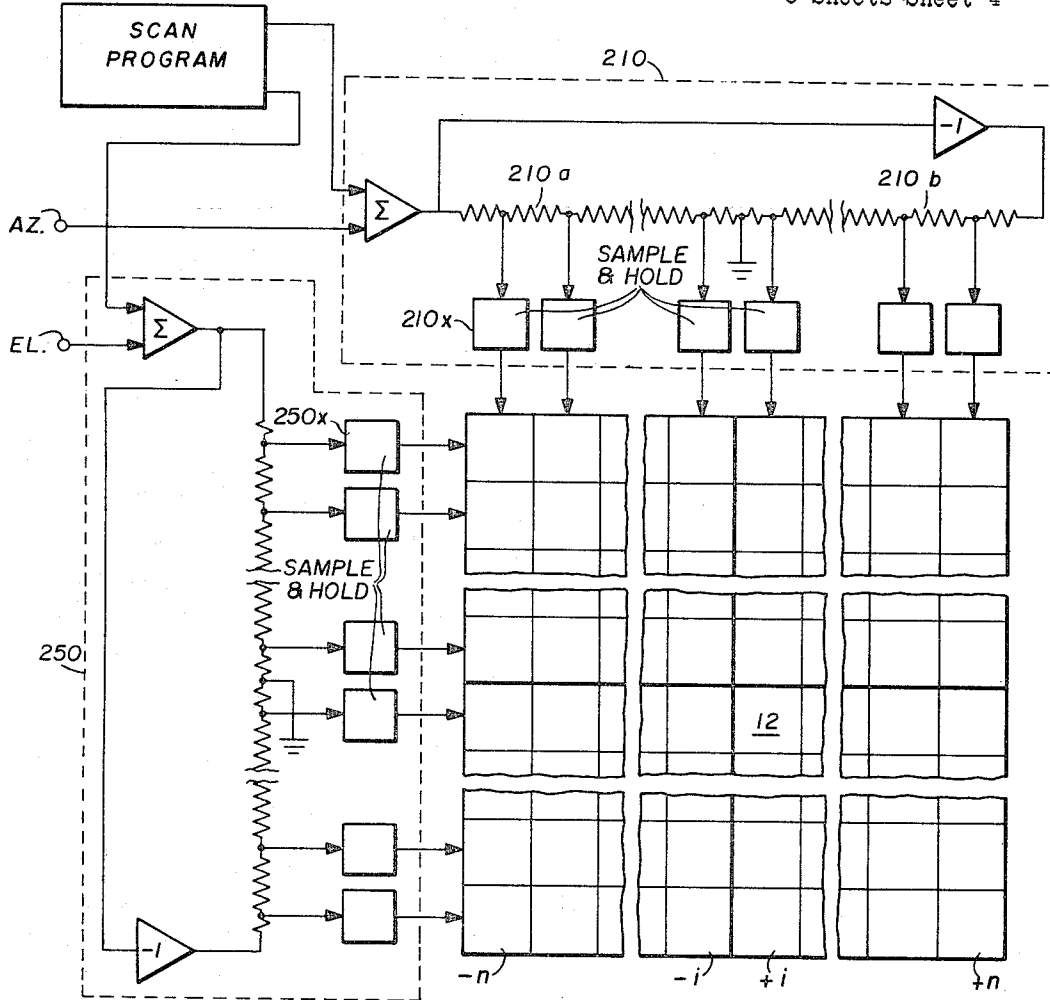


FIG. 6

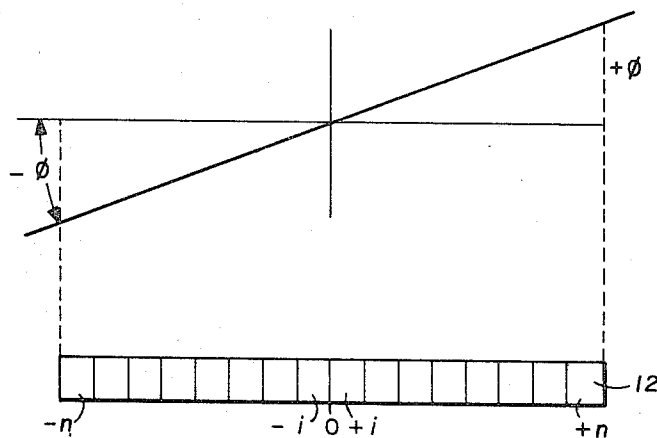


FIG. 5

Oct. 3, 1967

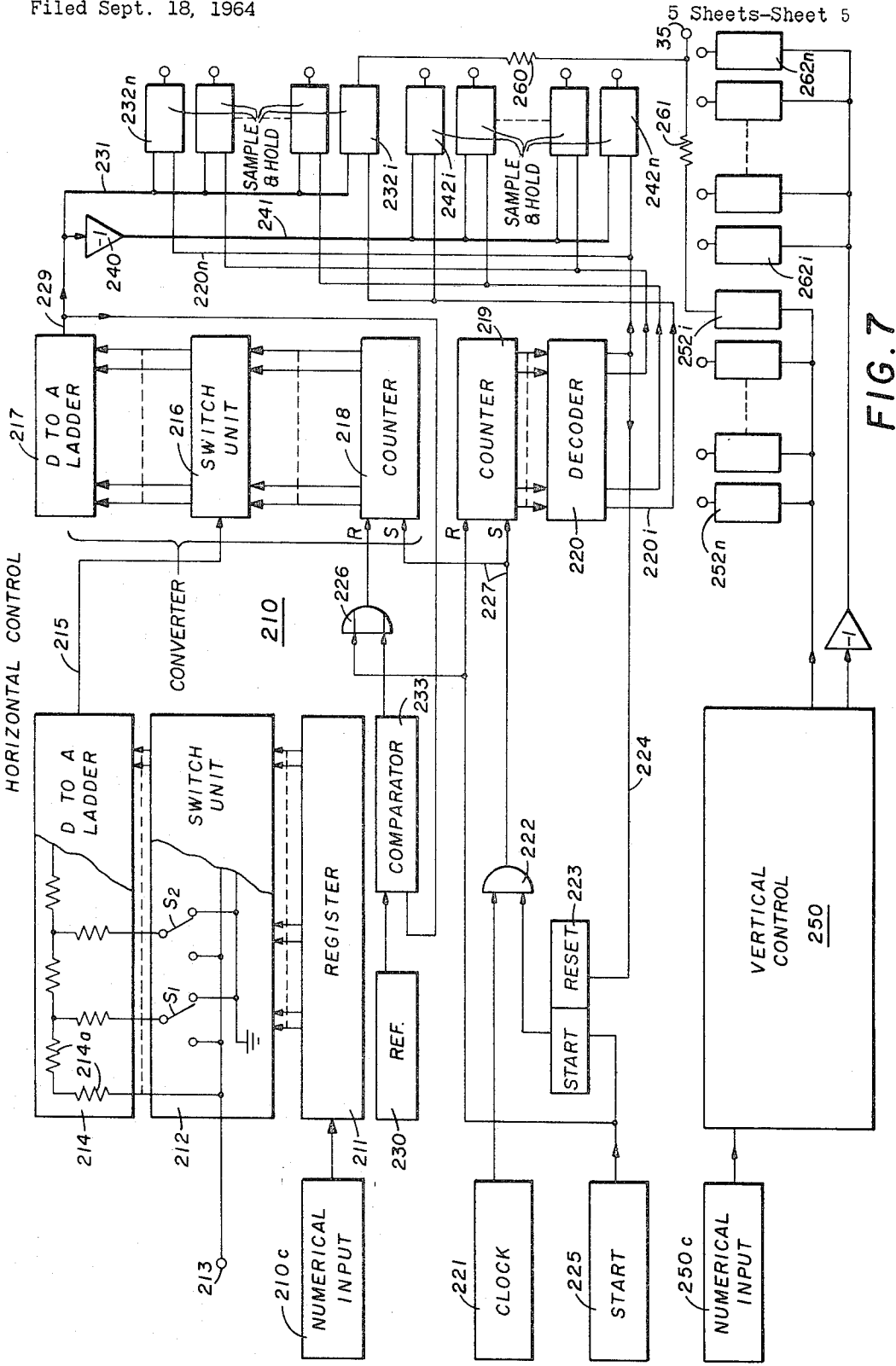
L. A. CHAMBERLIN, JR

3,345,631

PHASED ARRAY RADAR ANTENNA SCAN CONTROL

Filed Sept. 18, 1964

5 Sheets-Sheet 5



1

3,345,631

PHASED ARRAY RADAR ANTENNA SCAN CONTROL

Leo A. Chamberlin, Jr., Richardson, Tex., assignor to Texas Instruments Incorporated, Dallas Tex., a corporation of Delaware

Filed Sept. 18, 1964, Ser. No. 397,472

11 Claims. (Cl. 343-100)

This invention relates to radar antenna control and more particularly to a system for the control of phase shift components of a radar system for adjustment of the scan angle.

Phased array antennas are formed of radiating elements arranged in a planar array of rows and columns. In order to control the phase of the antenna excitation pulse, reference voltages are provided for each of the radiating elements in the antenna array. In operation, two sets of signal generators may be employed to generate rows and columns of voltages patterned to provide the desired phase shift across the antenna. A row voltage and column voltage for a given antenna element may be summed and applied as a reference voltage to a phase shifting device for a given antenna element to control the beam angle in two dimensions.

The present invention relates to a control system in which a reference voltage representative of a scan angle is treated for the production of a row or a column of reference voltages.

More particularly in accordance with the present invention, a plurality of sample-and-hold circuits sequentially store a stair-step voltage function produced under the control of a pair of synchronously driven counters, one of which counters is periodically reset. A decoder responsive to the second counter controls the sample-and-hold circuits. A reset circuit for the first counter is operative when the stair-step voltage reaches a level corresponding with an antenna reference voltage slightly less than that voltage which will produce a 360° phase shift.

In a more specific aspect, a generator is provided for generating a control voltage for a given row or column. A second generator produces stair-step voltage of maximum value proportional to the maximum phase shift for any antenna element. A digital-to-analog converter responsive to such voltage has a switching unit actuated by a first counter. A timing pulse train generator actuates the first counter and a second counter. A comparator connected to the reset terminal of the first counter has one input connection to the output of the converter and a second input connection to a reference voltage source to reset the first counter cyclically. A decoder is connected to the second counter for disabling both the counters. A sampling means responsive to the output of the converter and in response to the decoder acquires and holds a plurality of voltages of levels graded from maximum to minimum for application to antenna elements in a given row or column in the antenna.

For a more complete understanding of the present invention and for further objects and advantages thereof, reference may now be had to the following description taken in conjunction with the accompanying drawings in which:

FIGURE 1 diagrammatically illustrates the operation of an aircraft, its antenna array, and a functional electronic block employed to make up the array;

FIGURE 2 illustrates one form of a solid-state antenna module;

FIGURE 3 is a block diagram of the terrain-following radar of FIGURE 1;

FIGURE 4 is a block diagram of the electronics in each antenna module;

FIGURE 5 illustrates antenna beam steering;

2

FIGURE 6 is a diagram illustrating one mode of control of a phased array antenna; and

FIGURE 7 is a block diagram of the control network for beam steering.

The invention will be described as it is employed in a terrain-following radar. In this system, an aircraft 10 has an antenna unit 12 mounted in the nose 13. Antenna unit 12 is comprised of a multiplicity of functional electronic blocks, such as the block 14. In the example illustrated in FIGURE 1, 448 such blocks make up an antenna array of octagonal shape. The face of each block is of the order of one inch (1") square. Block 14 is adapted to be plugged into a suitable frame in the antenna unit 12 to transmit and receive electromagnetic energy by way of slot 15.

The video information made available by the radar is then processed to provide terrain-following capabilities. For example, in accordance with one mode of operation employed in a system known as the template system, a pre-master trigger is supplied to the template generator concurrently with each transmitted pulse from the antenna unit 12 to initiate a synthetic echo. This echo or template trigger occurs at a time range that is based upon the desired clearance altitude, the characteristics of the air frame, and the scan position. The range of the template trigger changes with the scan angle. The scan angle is varied by adjusting the relative phase relationships between the microwave energy applied to each of the modules in the antenna unit 12 during one vertical scan. The scan angle defines the template shape such as illustrate in FIGURE 1 by the outline 16. The video return or received signals are compared with the synthetic echos to obtain proportional command signals. The video return signal received before the synthetic echo signal is employed to generate climb commands. Similarly, the video return signal received after the synthetic echo generates dive commands.

Use of the present invention involves a multi-element, phased antenna array of solid-state construction capable of operation as above outlined as well as in other modes. A new and unique structural and functional relationship between integrated semiconductor circuits is employed for antenna excitation and for beam steering any of a plurality of modes.

The modules of antenna unit 12 are of identical construction and may be of the character illustrated in FIGURES 1 and 2, where a planar face member 20 is provided with a slot 15 leading to microwave circuits which are excited by pulses of an RF carrier of X-band frequency.

Antenna module 14 is unique in that it includes its own power generation circuit and receiver preamplifier circuit and in addition has its own phase shift circuit for beam steering. Included in the block 14 are a plurality of integrated circuits 24-29 which have the same gross appearance as units manufactured and sold by Texas Instruments Incorporated of Dallas, Tex., under the trademark "Solid Circuits."

The size of the module is determined or limited by the allowable spacing between radiating elements for avoidance of spurious grating lobes.

System block diagram

As shown in FIGURE 3, module 14 includes an RF unit 30, a phase shift unit 31, and a control network 32. The phase shift network receives low-power RF carrier pulses by way of a channel 33 and delivers output signals of IF frequency by way of channel 34. A beam steering or phase control voltage is applied to the control network 32 by way of channel 35. While only one module 14 has been shown in FIGURE 3, it is to be understood that

the 448 blocks illustrated in the antenna unit 12 of FIGURE 1 will similarly be excited and controlled from a manifold 40.

A source 41 supplies a pulsed RF carrier at 2.125 gc. to manifold 40 under the control of a pulse compression generator 44. An oscillator 42 supplies a pulsed phase control carrier at 125 mc. to the manifold 40. As will hereinafter be explained, the phase control carrier is employed for introducing a selected phase shift into the RF pulse from source 41. A local oscillator 43 applies a continuous low level voltage to manifold 40 at a frequency of 8.5 gc.

Output signals at an IF frequency appear on channel 34 and are applied from module 14 to manifold 40 for processing. As indicated, the IF signals from modules in the upper quarter of the antenna unit 12 are summed and appear on output channel 45. The sum of the IF output signals from the upper center quarter of the antenna unit 12 appears on channel 46. The sum of the IF output signals from the lower center quarter of the antenna unit 12 appears on channel 47, and corresponding signals from the lower quarter of antenna unit 12 appear on output channel 48.

Channels 45 and 47 are connected to the inputs of a 3 db hybrid coupler 50. The signals on channels 46 and 48 are applied to the inputs of a coupler 51. One output from coupler 50 is applied to a coupler 52 by way of a 45° phase delay unit 53. The second input to coupler 52 is supplied by one output of coupler 51. In a similar manner, a fourth coupler 54 is supplied by way of a phase delay unit 55 and by coupler 50. The output signals from couplers 52 and 54 are applied to IF amplifiers 56 and 57, respectively, which in turn feed pulse compression filters 58 and 59. Detectors 60 are driven by output signals from filters 58 and 59 and in turn drive a monopulse resolution improvement processor and video amplifier 61. A signal recognition circuit 62 excited by unit 61 drives a command computer 63, one output of which may be applied by way of a converter 64 to an autopilot 65.

An automatic gain control (AGC) 66 excited by the output of unit 61, controls IF amplifiers 56 and 57. A sensitivity time control (STC) unit 67 also feeds IF amplifiers 56 and 57 under the control of a timer synchronizer 68. Synchronizer 68 also feeds the command computer, as do command input function generators 69-73. Generator 69 is a scan computer indicating the direction of the antenna beam. If an objective is present, then the system generates a control signal for autopilot 65. Generator 70 provides a signal representative of velocity of the aircraft. Generator 71 generates a signal representative of the actual flight vector. Generator 72 is a ride control generator, and determines whether a rough or smooth course is followed, i.e., how abruptly the aircraft will change attitude when a target or obstacle is sensed. Generator 73 generates a signal representative of the aircraft pitch angle.

In the light of the foregoing description and with a knowledge of the various modes of operation of radar, it will be recognized that exacting requirements are placed upon the elements to be included in module 14. In order to provide antenna power at the level necessary, solid-state circuits are employed with circuit configurations such that the necessary power may be supplied to the antenna and the desired versatility and control thereof are available within the capabilities of solid-state semiconductor networks.

Antenna module circuit

FIGURE 4 is a lumped constant representation of integrated circuits for: (a) receiving compression-modulated RF carrier pulses at a relatively low-power level from channel 33; (b) receiving phase control carrier pulses on channel 83; (c) shifting the phase of the phase control carrier in the phase shift unit 31; (d) modulating the RF pulses with the phase shifted pulses in the mixer 85; (e) amplifying one of the modulation products in the

power amplifier 30; (f) stepping up the frequency of the high power signal in the frequency multiplier 86; (g) applying the final output pulses to an antenna 87; (h) detecting return signals to the antenna 87; (i) mixing the same in a mixer 88 at the input of a preamplifier 89; and (j) passing the detected signals from amplifier 89 through the phase shift unit 31 for delivery to an output channel 34.

For the purpose of the present example, the operation will be such that the RF pulses applied to channel 33 will be at a frequency of 2.125 gc., ± 0.625 mc., the swing of 1.25 mc. being from low frequency to high frequency by pulse compression generator control of the oscillator 41 as shown in FIGURE 3. The phase control carrier applied to terminal 83 will be at 125 mc. The signal applied to the antenna 87 will be 9 gc. and the output signal on channel 34 will be at 500 mc. The module delivers one watt peak power to the antenna 87 at 9 gc.

The compression-modulated RF carrier pulses applied to the channel 33 pass through a tuned filter 100 at the input of the mixer 85. A second tuned filter 101 is located in the output channel leading from the phase shift unit 31 and is tuned to 125 mc. for modulating the 2.125 gc. carrier pulse. The output circuit 102 is then tuned to the upper side band or 2.250 mc. for driving the power amplifier 30. The phase shifting unit 31 is employed to control the phase of the carrier at the output tuned circuit 102.

Phase shifting by line length switching

Beam scanning is provided for the antenna made up of a plurality of modules 14. As shown in FIGURE 4, beam scanning is produced by switching discrete lengths of transmission line into the antenna feed system and more particularly into the channel through which the 125 mc. phase control carrier is transmitted. This is a step-type phase shifter. The size of the smallest step is important in determining the complexity of the control circuit. In the unit 31, five transmission lines are employed and are of such length as to provide phase delay units 111-115 of $11\frac{1}{4}^\circ$, $22\frac{1}{2}^\circ$, 45° , 90° , and 180° delays, respectively, at a frequency of 500 mc. The 125 mc. signal applied to terminal 83 will undergo delays one-fourth of the amounts noted.

The phase shifter and switching unit 31 includes diodes 120 and 121 forming an input switch. The common juncture between diodes 120 and 121 is connected to diode switches 122 and 123. Delay line 111 is connected to diode 123 and thence, by way of diode 124 and condenser 125, to the input channel 126 leading to the second stage of the phase shifter 31. The diode 122 is connected by way of condenser 127 to channel 126. The switches 122, 123, and 124 are selectively biased under the control of a bistable multivibrator 128. A second multivibrator 129 controls transmission through, or the bypass channel for, the second delay line 112. Multivibrators 130, 131, and 132 similarly control inclusion or deletion of lines 113, 114, and 115, respectively, from the transmission channel for the 125 mc. phase control carrier. A sixth multivibrator 133 is connected to the output of multivibrator 132 and in turn feeds a TR switch comprised of diodes 137 and 138.

The switch control line 140 leading to the multivibrator is supplied from a clock input channel 141 at 1 mc. by way of an AND gate 142. The second terminal of the AND gate is fed by voltage comparator unit 143. The line 144 of multivibrator 128 is connected by way of condenser 145 to the input line 146 of multivibrator 129. Similarly, condensers 147-150 connect multivibrators 129-133 in a ripple-through configuration. From zero phase delay, the first clock pulse actuates multivibrator switch unit 128 to include line 111 in the 125 mc. circuit. The second clock pulse actuates units 128 and 129 to remove line 111 and to include line 112. The third pulse actuates unit 128 to include line 111

with line 112. The fourth pulse actuates units 128, 129, and 130 to remove lines 111 and 112 and to include line 113. Thus, a digital progression is employed in increasing the delay in the delay line unit.

The multivibrator 128 is coupled by way of lines 151 and 152 to a digital-to-analog converter 153. Similarly, all of the other multivibrators are coupled to the digital-to-analog converter so that the state of the switching networks is indicated by an analog signal on the output line 154. Switch unit 133, while introducing no delay, applies current to converter 153 proportional to 360° phase delay so that the line switching sequence may continue through two cycles or 720°. The output signal from converter 153 is applied to the second input of the voltage comparator 143.

In operation, a reference voltage representative of the desired phase delay for module 14 is applied to the input terminal 35. So long as the reference voltage exceeds the output from the converter 153, the output from the comparator 143 enables the AND gate 142. With the AND gate 142 conductive, the clock pulses from terminal 141 successively shift conduction between the various flip-flops. When the output of the converter 153 equals the reference voltage on channel 35, the AND gate 142 discontinues transmission of the clock pulses and the desired delay is then fixed in the phase shift unit 31. Thereafter, the simultaneous application of the compressed RF carrier pulse and the phase control carrier pulse to terminals 33 and 83, respectively, will produce a pulse of 2.25 gc. at the output of the tuned circuit 102 in the mixer 85. The phase of the 2.250 gc. signal at circuit 102 is equal to the phase delay in the unit 31.

The signal from mixer 85 is then applied to the power amplifier 30 for delivery of about two watts peak power at 2.25 gc. to the input of the frequency multiplier 86. The multiplier 86 consists of resonant circuits in which a diode 160 is the active element. The multiplier is a quadrupler for delivery to the output channel 161 of a pulse whose frequency is 9 gc. at a peak power level of about one watt. The latter pulse is applied by way of a TR switch diode 162 to the antenna 87 for radiation at the phase set by the phase delay unit 31.

Immediately after pulse transmission from the antenna, the control multivibrator 163 for the TR switch 162, 164 changes state so that return signals detected by the antenna 87 pass through TR switch diode 164 to the input to a mixer 88. The mixer 88 is supplied with an 8.5 gc. local oscillator signal on channel 165. The lower side band modulation product at 500 mc. is applied to the IF preamplifier 89. The latter signal then passes through the switch diode 138 and the phase shift unit 31 where the signal undergoes a delay of four times the delay of the phase control carrier. This is with the same delay unit setting as employed during the transmit operation. The delay IF signal then passes through the output switch diode 121 to the output channel 134 leading to the manifold. While not shown, control units for TR switch 120, 121 and TR switch 137, 138 will provide bias voltages therefor in the same manner as the bias is supplied TR switch 162, 164.

More particularly, it will be recalled that the phase control carrier applied to terminal 83 was at a frequency of 125 mc., and that it passed through the phase shift unit 31 to control the phase of the RF pulse applied to the antenna 87. Since the multiplier 86 quadruples the frequency, the phase shift introduced by the unit 31 is also quadrupled in the antenna drive signal as it appears on channel 161. Thus, with the output of the IF preamplifier 89 at 500 mc., the output signal on channel 34 will have exactly the same phase shift as introduced into the antenna drive pulse. Thus, the same phase shift unit is used for both the transmit and the receive cycle and the beam direction is the same for receiving as for transmitting.

With power amplifier 30 present, module 14 includes

its own power generation means and thus operates on low level signals from the manifold. The circuit 30 raises the power level by about 20 db in the preamplifier section 30a, about 6 db in the driver 30b, and about 4 db in the output section 30c. By way of example, the power applied to the input of the preamplifier would be about 2 milliwatts (mw.) peak or 0.2 mw. average power. The signal at the input to the driver 30b would be at about 200 mw. peak or 20 mw. average. The power applied to the output stage would be about 800 mw. peak or 80 mw. average. The power output from the output stage would be about 2 watts peak or 0.2 watt average power. The multiplier operates to increase the frequency from 2.25 gc. to 9 gc. with an insertion loss of 3 db to provide one watt peak power to the antenna 87. Thus, the power generation chain consists of 3 or 4 amplifier stages at 2.25 gc. followed by an X4 varactor multiplier with an output at 9 gc.

Beam steering reference voltage generation

The present invention is directed to a control system for generating families of reference voltages such as the voltage applied to terminal 35, FIGURE 4, in each module.

Where the antenna is made up of an array of elements arranged in rows and columns as shown in FIGURE 6, each of the rows and columns may be numbered for convenience according to their position in the array. To shift the beam of the antenna in a horizontal direction through an angle ϕ , FIGURE 5, the phase of the RF energy applied to the radiation structure in each module in each column must be shifted by an amount which is proportional to the angle ϕ , the angle that the beam is to be shifted from a line perpendicular from the face of the antenna. The phase shift for each module must also be dependent upon the location of the module in the array. FIGURE 5 shows a top view of the antenna unit 12 and a plot of the phase shift versus distance from the center of the antenna.

As shown in FIGURE 6, the control unit 210 generates a reference voltage which shifts the phase for the column $-n$ at the left edge of antenna 12 through the same phase angle. As represented by the tapped resistor 210a in unit 210, the voltages applied by way of sample and hold units 210x to the columns of the antenna. Sample and hold units 250x apply voltages to the rows of antenna modules. Voltages applied to the columns in the right antenna half are the same for each column but are graded from a maximum at the edge column to near zero at the center column. The left antenna half columns similarly are controlled by reference voltages such as might be derived from resistor 210b. The unit 250 similarly serves to control the vertical scan or beam position. To point the beam in a direction involving both the horizontal and vertical deflection, the reference voltage for a given antenna element is the sum of the voltage required for the column in which a given element is positioned and the voltage required for the row in which the given element is located. Thus, as illustrated in FIGURE 5, the column at the left side of the antenna unit 12 would be delayed by an angle $-\phi$. The column at the right edge of the antenna unit 12 would be delayed by an angle of $+\phi$.

Where the antenna array is one wavelength wide and where the difference between the angle $-\phi$ and $+\phi$ is 360°, the antenna radiation primarily will be at 45° to the face of the antenna. In practice, however, the antenna generally is made many wavelengths wide and many wavelengths high so that narrow beams may be produced. When this is done, it is necessary to produce phase shifts across the face of the antenna which are equal to $N360^\circ$. The factor N may be any integral number with practical values ranging as high as 10 to 15 or more for phase shifts of around 5000° across the antenna.

In FIGURE 7 the controller for generating the horizontal and vertical reference voltages above noted is shown, with the controller for producing the horizontal reference voltages being shown in detail.

In order to point the beam in a given direction, a binary number proportional to the phase shift required for the edge column n , FIGURE 5, is read into an input register 211 of unit 210 from a control source 210c. The register 211 is connected to a switch unit 212. A reference voltage is applied to the switch 212 by way of input channel 213. The digital-to-analog converter of FIGURE 7 may include switch unit 212 which may be the same as in FIGURE 4 which shows the construction of the switch units SW1-SW6 and the connections to the ladder network. The register 211 may be composed of flip-flops as shown in FIGURE 4 or may comprise other binary storage elements. These elements control switches in unit 212 which in turn control the binary weighted resistance ladder of the type commonly used in digital-to-analog converters. Typical of the construction is the resistance network illustrated in the unit 214. The resistance values are chosen so that the voltage at the output is $\frac{1}{2}^k$ the value of the reference voltage on terminal 213 and k is the number of switches in the ladder. When switch S2 is closed to the reference voltage and all the other switches are connected to ground, the output voltage is $\frac{1}{2}^{k-1}$ times the reference voltage, etc. This assumes that the series resistances 214a are not present. Resistances 214a, however, are included for the purpose which will later be explained. In operation the switch for each given ladder position is connected to the reference voltage if the bit in the corresponding register is 1, and to ground if the bit is 0.

The output of the ladder network 214 is applied by way of conductor 215 to a second digital-to-analog unit including switch unit 216 which controls a ladder network 217 and which in turn is controlled by a counter 218. A second counter 219 counts in parallel with counter 218. A decoding logic network 220 is connected to counter 219. Counters 218 and 219 are controlled by a clock 221 which is connected thereto by way of an AND gate 222 and line 227. A control multivibrator 223 controls one input of the AND gate 222. The decoding logic network 220 has output lines i to n with output lines n being connected by way of line 224 to the reset terminal of the multivibrator 223.

A starting unit 225 is connected to the start terminal of the multivibrator 223. The starting unit 225 is also connected to the reset terminal of counter 219 and, by way of an OR gate 226, to the reset terminal of the counter 218.

One control terminal of the OR gate 226 is connected to the output of a comparator 233 which is connected at one input to the output line 229 of the ladder network 217 and at the other input to a comparison reference voltage source 230.

The line 229 is also connected to a bus 231 at the input of a plurality of sample-and-hold units 232i-232n. Line 229 is connected by way of an inverting unit 240 to a bus 241 to sample-and-hold units 242i-242n.

The voltages appearing at the outputs of the sample-and-hold units 232i-232n and 242i-242n are the voltages necessary to shift the beam from antenna unit 12 through a horizontal angle represented by the reference voltage from the numerical input unit 210c.

In a similar manner, a vertical control voltage generator 250 provides output voltages to sample-and-hold units 252i-252n and 262i-262n for shifting the beam from the antenna unit 12 through a vertical angle representative of the magnitude of the reference voltage applied from the reference numerical input voltage source 250c. The voltages from the sample-and-hold units may then be combined for application to the reference input terminals of each module (terminal 35 of FIGURE 4), so that each module in the antenna unit will be adjusted

to shift the phase of the RF antenna excitation pulse in dependence upon the sum of the vertical and horizontal beam angles represented by the voltage on units 210c and 250c. The voltages may be combined from the sample-and-hold units in the manner known in the art, and such as described in "Introduction to Radar Systems," Skolnik, McGraw-Hill (1962), page 312 et seq.

In operation, where a scanning sequence of the antenna is desired, the numbers to be read into the units 210 and 250 from the control sources 210c and 250c come from sequence generators or programmers. The units 210c and 250c may comprise part of a computer if the antenna is to be pointed at some target, as would be the case in a target tracking operation. In either case the voltage output on line 229 will then be proportional to the phase shift desired in the extreme or edge columns of the antenna.

As soon as the phase shift number or signal has been read into the unit 210, a start pulse is applied to the control flip-flop 223. This pulse also resets the counters 218 and 219. As soon as the control unit 223 is set, the AND gate 222 changes state to allow the clock pulse train to pass to the counters 218 and 219. This causes the two counters to advance together. The counter 218 controls the units 216 and 217, with the reference input voltage being the voltage on line 215. As the count in the counter 218 increases, the voltage on line 229 increases in uniform steps.

In the explanation of operation of the reference generator which follows, it will first be assumed that the total phase shift across the face of the antenna is to be less than 360° . Thereafter, operation for a phase shift greater than 360° will be explained.

For a phase shift less than 360° , counter 219 will count in synchronism with counter 218. The state of counter 219 is decoded to provide n indications on n individual output lines 220i-220n. The output voltage on line 229 for each step of counters 218 and 219 is a voltage proportional to the phase shift for each column. That is to say, the first stage of counters 218 and 219 results in a voltage proportional to the phase shift for columns $+i$ and $-i$ of FIGURE 6. The second stage of counters 218 and 219 results in a voltage for columns $+ii$ and $-ii$, and so on. It will be noted from FIGURE 5 that the phase required for column n is the negative of the phase required for column $-n$.

Counters 218 and 219 initially are reset to a state of all zeros. This results in a ladder output voltage on line 229 of zero volts for the first state of the counters. If the number of columns in the antenna is an even number, as shown in FIGURE 1, a reference of zero volts would result in the phase shift introduced in columns i and $-i$ always being zero. This would induce a slight discontinuity in the phase slope across the antenna. To prevent this, the ladder network 214 is provided with resistors 214a. These resistors offset the output of the ladder 214 by an amount equal to one-half step of the output voltage.

The lines 220i-220n, connected to the sample-and-hold units 232i-232n, are sequentially energized to cause storage of a sample voltage in each of the units as the states of the output lines leading from decoder 220 change. Similarly, the other half of the antenna is provided with reference voltages from bus 241 by way of inverter unit 240.

When the output on line 229 equals the reference voltage from source 230, as applied to the comparator 233, the counter 218 is reset. Decoder 220 serves to reset flip-flop 223 at the end of a phase control sequence thus inhibiting clock pulses to counter 219. Counter 219 is reset by the next start pulse. The voltage from reference source 230 is set at a value corresponding with just less than the voltage on line 229 required for 360° phase shift.

Thus far, it has been assumed that the total phase shift required is less than 360° . This generally is not the case and this fact is the basis for including the second counter

219. More particularly, with the output from the voltage ladder 217 fed to the comparator 233 and with the reference voltage from source 230 slightly less than the voltage necessary for a 360° phase shift, when the ladder output voltage exceeds the voltage from source 230, the counter 218 will be reset. However, with the clock pulse being applied thereto, counter 218 will repeat its cycle so long as the clock pulse train is present. In contrast, the counter 219 continues its count until the clock pulse train is stopped by disabling gate 222. In this way, the output of the ladder 217 always indicates a phase shift in the range of 0° to 360°. Counter 219 always contains the number of the columns in binary form for which the voltage being generated at that instant applies.

The sample-and-hold units may be of conventional construction involving closure of a switch in response to a given voltage state on a decoder output line, such as line 220i. This charges a capacitor in the sample-and-hold unit 232i such that the voltage on the output line from unit 232i is equal to the input voltage on bus 231 at the instant of closure of the switch. With a high impedance output buffer-amplifier in the sample-and-hold units, the charge on the condenser will remain unchanged after the input switch is opened. Switches in the sample-and-hold units are controlled by the decoded state of counter 219, as above noted. State 1 of a counter 219 closes the switch in the sample-and-hold units 232i and 242i. Since the inverter 240 is employed to feed bus 241, the two voltages are thus stored as reference voltages for two phase shift units. When the counter 219 reaches its *n*th state, a voltage for each column is stored in the 2*n* sample-and-hold units. The decoded *n*th state of counter 219 also resets unit 223 and ends the process.

The controller 250 for the rows of antenna modules is identical to the controller 210 for the columns of antenna modules. If the rows and columns are the same in number, then the controllers are identical. If the rows and columns are not the same, then the controllers differ only in the number of states produced by the counter 219.

The phase shift reference voltage, for application to a given module, is produced by summing the voltages from two of the sample-and-hold units. This would be accomplished by means of a pair of summing resistances for each element, such as resistances 260 and 261. The output voltage from unit 252i would be separately summed with each of the output voltages from the sample-and-hold units 232i-232*n* and 242i-242*n*.

It is not necessary that the antenna be as shown in FIGURE 6. By omitting elements in the outer rows or columns, the configuration shown in FIGURE 1 may be formed. Entire rows or entire columns may be omitted, depending upon the particular application required. If only one column is employed or if only one row is employed, then either the unit 210 or the unit 250 would be employed to generate the phase control reference voltages.

From the foregoing it will be seen that the system 210 generates control voltages for a given line of phased array antenna elements. A beam index voltage appears at the output of unit 214 which is proportional to the maximum phase shift to be introduced in the antenna. The digital-to-analog converter 216-218 is responsive to the beam index voltage. Counter 219 and the converter are connected in a circuit which includes a clock source and an AND gate 222 for driving the converter and the counter in synchronism. Comparator 233 is connected to the reset terminal of the converter through the OR gate 226. The reference voltage source 230 is connected to one input of the comparator 233. The connection from line 229 at the output of the converter leads to the second input of the comparator. Decoder 220 is connected to the counter 219 and has output states in number dependent upon the number elements in the line of antenna elements. The unit 223 disables the AND gate

222 in response to a final state of the decoder. The sample-and-hold units 232i-232*n*, in response to the decoder, sequentially sample the output of the converter and thus hold a plurality of voltages at voltage levels which are graded from maximum to minimum dependent upon the positions of said elements in said line and the magnitude of the beam index voltage.

While the preferred embodiment of the system involves use of the inverters such as unit 240, it is apparent that the decoder may have built into it twice as many output states so that the unit 210 would generate a single polarity set of stair-stepped voltage suites rather than the two polarity set produced in FIGURE 27.

Having described the invention in connection with certain specific embodiments thereof, it is to be understood that further modifications may now suggest themselves to those skilled in the art and it is intended to cover such modifications as fall within the scope of the appended claims.

What is claimed is:

1. A system for generating control voltages for a given line of phased array antenna elements which comprises:

- (a) means for generating a beam index voltage proportional to the maximum phase shift across said antenna,
- (b) a digital-to-analog converter coupled to said means for control by said index voltage and having an input OR gate,
- (c) a counter,
- (d) a circuit including a clock source and an AND gate leading to said converter and said counter for driving said converter and said counter in synchronism,
- (e) a comparator having an output connected to said OR gate for resetting said converter through said OR gate,
- (f) a reference voltage source connected to one input of said comparator,
- (g) a connection between the output of said converter and the second input of said comparator,
- (h) a decoder connected to said counter having output states in number dependent upon the number of elements in said line,
- (i) means for simultaneously transmitting a start pulse to said counter, to said OR gate, and to enable said AND gate,
- (j) means for disabling said AND gate in response to a final state of said decoder, and
- (k) means responsive to said decoder for sequentially sampling the output of said converter and for holding a plurality of voltages thus sampled at voltage levels graded from maximum to minimum dependent upon the positions of said elements in said line.

2. A system for generating control voltages for a given line of phased array antenna elements which comprises:

- (a) means for generating a beam index voltage proportional to the maximum phase shift across said antenna,
- (b) a digital-to-analog converter for receiving said beam index voltage and having an OR gate control input,
- (c) a counter,
- (d) a circuit including a clock source and an AND gate leading to said converter and said counter for driving said converter and said counter in synchronism,
- (e) a comparator having an output connected to said OR gate for resetting said converter through said OR gate,
- (f) a reference voltage source connected to one input of said comparator,
- (g) a connection between the output of said converter and the second input of said comparator,
- (h) a decoder connected to said counter having out-

- put states in number equal to one-half the number of elements in said line,
- (i) means for simultaneously transmitting a start pulse to said counter, to said OR gate, and to enable said AND gate,
 - (j) means for disabling said AND gate in response to a final state of said decoder, and
 - (k) two sets of means responsive to said decoder for sequentially sampling the output and the inverse of the output of said converter and for holding two sets of voltages at voltage levels graded from maximum to minimum dependent upon the positions of said elements in said line.
3. A system for generating control voltages for a given line of phased array antenna elements which comprises:
- (a) means for generating a beam index voltage proportional to the maximum phase shift across said antenna,
 - (b) a digital-to-analog converter for receiving said beam index voltage,
 - (c) a counter means having output states in number equal to the number of elements in said line,
 - (d) a circuit including a clock source and an AND gate leading to said converter and said counter means for driving said converter and said counter means in synchronism,
 - (e) a comparator having an output circuit including an OR gate connected to reset said converter through said OR gate,
 - (f) a reference voltage source connected to one input of said comparator,
 - (g) a connection between the output of said converter and the second input of said comparator,
 - (h) means for simultaneously transmitting a start pulse to said counter means, to said OR gate, and to enable said AND gate,
 - (i) means for disabling said AND gate in response to a final state of said counter means, and
 - (j) means responsive to said counter means for sequentially sampling the output of said converter and for holding a plurality of voltages at voltage levels graded from maximum to minimum dependent upon the positions of said elements in said line.
4. A system for sequentially generating a plurality of suites of stair-step reference voltages which comprises:
- (a) an analog voltage source of a level greater than the maximum voltage in each said suite,
 - (b) a counter-driven digital-to-analog converter for generating monotonic output voltage,
 - (c) a plurality of sample-and-hold circuits connected to the output of said converter,
 - (d) a counter driven in synchronism with said converter,
 - (e) means for periodically resetting said converter when said monotonic voltage exceeds said maximum voltage, and
 - (f) means responsive to the output of said counter for periodically actuating said sample-and-hold circuits for sampling said output voltage.
5. A system for sequentially generating a plurality of suites of stair-step reference voltages which comprises:
- (a) an analog voltage source of a level greater than the maximum voltage in each said suite,
 - (b) a counter-driven digital-to-analog converter for generating monotonic output voltage,
 - (c) a plurality of sample-and-hold circuits connected to the output of said converter,
 - (d) a counter adapted to be stepped in synchronism with said converter,
 - (e) means for periodically resetting said converter when said monotonic voltage exceeds said maximum voltage, and
 - (f) means responsive to the output of said counter for actuating said sample-and-hold circuits sequentially in synchronism with each change of state of said counter.

6. A system for generating reference voltages from an input voltage proportional in magnitude to the total phase shift across a line of phased array antenna elements where said total phase shift exceeds 360° which comprises:
- (a) a converter responsive to said input voltage for generating a monotonic voltage,
 - (b) means for resetting said converter when said monotonic voltage approaches a magnitude representative of a 360° phase shift,
 - (c) a plurality of sample-and-hold circuits connected to the output of said converter, and
 - (d) means periodically operative in synchronism with said converter sequentially to actuate said sample-and-hold circuits for storing reference voltages for elements of said line of magnitudes lying exclusively between zero and the maximum value of said monotonic voltage.
7. A system for generating control voltages for a given line of $2n$ elements of a phased array antenna which comprises:
- (a) means for generating a beam index voltage proportional to one-half of the total phase shift across said antenna,
 - (b) a digital-to-analog converter responsive to said beam index voltage,
 - (c) a counter operative synchronously with said converter,
 - (d) comparator means connected to the output of said converter for resetting said converter when the output thereof approaches a value representative of a 360° phase shift in one of said elements,
 - (e) a decoder connected to said counter having n output states, and
 - (f) two sets of n means sequentially responsive to said decoder for storing voltages corresponding with the output and the inverse of the output of said converter at each of said n output states.
8. The combination set forth in claim 7 in which means are provided for offsetting the value of said beam index voltage by an amount proportional to one half step in the output of said converter.
9. A system for sequentially generating reference voltages for a line of n elements in a phased array antenna which comprises:
- (a) means for generating an analog voltage proportional in magnitude to the total phase shift across said line,
 - (b) a digital-to-analog converter connected to said generating means and having a first counter as a drive for generating a monotonic output voltage,
 - (c) a plurality of sample-and-hold circuits connected to the output of said converter,
 - (d) a second counter stepped in synchronism with said first counter,
 - (e) means for resetting said first counter each time said output voltage reaches a magnitude just less than that representative of 360° phase shift in one of said n elements whereby a saw-tooth form is superimposed on said monotonic output voltage, and
 - (f) means responsive to each of n changes of state in said second counter for actuating said sample-and-hold circuits for sequential acquisition and storage of said reference voltages.
10. A system for generating reference voltages from two input voltages, one of which is proportional in magnitude to the total phase shift across a row of n elements of a phased array antenna and the other of which is proportional in magnitude to the total phase shift across a column of n' elements of said antenna where one element of said row is one element of said column and where the total phase shift in both said row and said column may exceed 360° which comprises:
- (a) a row control unit having,
 - (i) a first converter responsive to a first of said

13

- input voltages for generating a first monotonic voltage,
- (ii) a first means for resetting said first converter when said first monotonic voltage approaches a magnitude representative of a 360° phase shift, 5
 - (iii) a row of n sample-and-hold circuits connected to the output of said first converter, and
 - (iv) a first control means periodically operative in synchronism with said first converter sequentially to actuate said sample-and-hold circuits in the n row for storing n reference voltages for the n elements of said row of magnitudes lying exclusively between zero and the maximum value of said first monotonic voltage, 10
- (b) a column control unit having, 15
- (i) a converter responsive to a second of said input voltages for generating a second monotonic voltage,
 - (ii) a second means for resetting said second converter when said second monotonic voltage approaches a magnitude representative of a 360° phase shift, 20
 - (iii) a column of n' sample-and-hold circuits connected to the output of said second converter, and 25
 - (iv) a second control means periodically operative in synchronism with said second converter sequentially to actuate said sample-and-hold circuits in the n' column for storing n' reference voltages for n' elements of said column of magnitudes lying exclusively between zero and the maximum value of said second monotonic voltage, and 30
- (c) adding means interconnecting the output of the unit in said row and the output of the unit in said column corresponding with the location in said antenna of said one element for producing a two dimensionally proportional phase shift reference voltage for said one element. 35

14

11. A system for generating phase shift control voltages for a line of n elements in a phased array antenna where the total phase shift across said line exceeds 360° which comprises:
- (a) a first counter-driven digital-to-analog converter adapted to receive an input function representative of the maximum phase shift to be produced across n elements of said line for generating a beam index voltage proportional to said maximum phase shift,
 - (b) a second counter-driven digital-to-analog converter adapted to receive said beam index voltage,
 - (c) a counter,
 - (d) a clock circuit leading to said second converter and said counter for driving said second converter and said counter in synchronism,
 - (e) comparator means connected at its output to the reset terminal of said second converter,
 - (f) a source of reference voltage of magnitude just less than the voltage representative of 360° phase shift connected to one input of said comparator,
 - (g) a connection between the output of said second converter and the second input of said comparator for actuating said comparator to reset said second converter when the output of said second converter exceeds said reference voltage,
 - (h) a decoder responsive to the output of said counter having n output states,
 - (i) means for disabling said counter and said converter in response to a final state of said decoder, and
 - (j) means responsive to said decoder for sequentially acquiring from the output of said converter, and for holding, n voltages at voltage levels corresponding with the output of said second converter at each of said n output states.

No references cited.

RODNEY D. BENNETT, *Primary Examiner*.

T. H. TUBBESING, *Assistant Examiner*.