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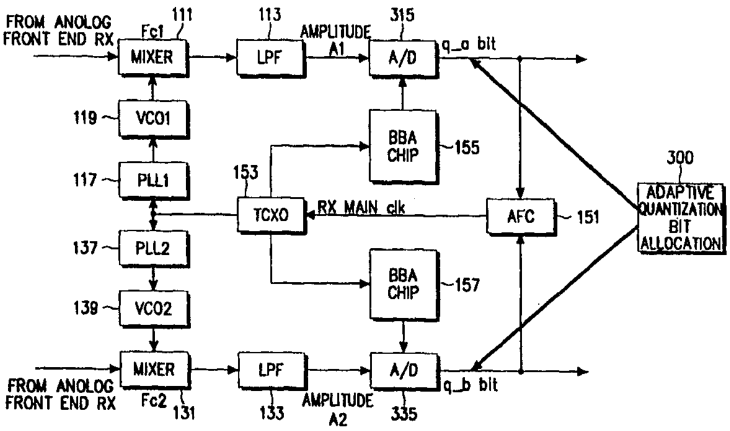


(57) Abstract

An AFC (Automatic Frequency Control) device and a method of controlling reception frequency in a dual-mode terminal. When a dual-mode terminal uses one or two AFC circuits, time required for acquiring tracking synchronization in a PLL circuit for a frequency can be reduced using a test augmentation frequency being an integer multiple of a tracking synchronization acquiring residual frequency of a PLL circuit for another frequency to which the first frequency transits for reliable synchronization acquisition. Errors with respect to an output dynamic range caused by use of two AFCs are reduced and thus the demodulation performance of a receiver is ensured by varying quantization bits of an A/D clock based on the dynamic range of residual errors in a frequency area. The demodulation performance can also be ensured by operating an ACPE circuit for an AFC circuit having many residual frequency errors. In this method, the frequency characteristics of the dual-mode terminal are stabilized and the stability of a demodulator is increased due to a frequency offset. As a result, the stable demodulator performance is ensured.

AFC DEVICE AND METHOD OF CONTROLLING RECEPTION FREQUENCY IN A DUAL-MODE TERMINAL

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates generally to a device and method for controlling the reception frequencies in a terminal in a mobile communication system, and in particular, to a AFC (Automatic Frequency Control) device and method of a dual-mode terminal.

2. Description of the Related Art

Data is generally transmitted by a terminal in a mobile communication system in an FDD (Frequency Division Duplexer) scheme or a TDD (Time Division Duplexer) scheme. The next-generation mobile communication system considers implementing a dual-mode terminal with the advantages of the two schemes. Since the dual-mode terminal uses different frequency bands, it requires oscillators for generating the different frequencies and thus the design of an AFC (Automatic Frequency Controller) for the oscillators is increasingly important. It is difficult to apply different feed-back loops to the two oscillators in a conventional terminal during a synchronization acquisition of different frequencies.

FIG. 1 is a block diagram of an AFC circuit in a receiver of a dual-mode terminal. Referring to FIG. 1, a mixer 111 mixes an input signal RX with an oscillation frequency received from a first voltage-controlled oscillator (VCO1) 119 and outputs a first mixed signal Fc1. A low-pass filter (LPF) 113 low-pass filters the output of the mixer 111. The output of the LPF 113 is the amplitude A1 of the input signal. An analog-to-digital (A/D) converter 115 converts the output of the LPF 113 to digital data q_a bits. A mixer 131 mixes the input signal RX with an oscillation frequency received from a second voltage-controlled oscillator (VCO2) 139 and outputs a second mixed signal Fc2. A LPF 133 low-pass filters the signal received from the mixer 131. The output of the LPF 133 is the amplitude A2 of the input signal. An A/D converter 135 converts the output of the LPF 133 to a digital data q_b bit.

An AFC 151 receives the digital data from the A/D converters 115 and 135 and generates a signal (RX main clock) for automatically controlling a reception frequency. A TCXO (Temperature Compensated Crystal Oscillator) 153 multiplies the output of the AFC 151 to generate an intended RF (Radio Frequency)/IF (Intermediate Frequency). A PLL (Phase Locked Loop) 117 generates a control signal for generating a phase-locked frequency according to the multiplied signal received from the TCXO 153. The oscillator 119 generates the frequency set under the control of the PLL 117 and applies the frequency to the mixer 111. A PLL 137 generates a control signal for generating a phase-locked frequency according to the multiplied signal received from the TCXO 153. The oscillator 139 generates the frequency set under the control of the PLL 137 and applies the frequency to the mixer 131. A BBA circuit 155 generates a sampling clock for the A/D converter 115 in response to the output of the TCXO 153. A BBA (Base Band Analog) circuit 157 generates a sampling clock for the A/D converter 135 in response to the output of the TCXO 153.

The oscillators generate different frequencies through the PLLs in the receiving AFC circuit of the dual-mode terminal as constructed above.

Application of the above conventional AFC circuit to a dual-mode transmission scheme has the following problems. The dual-mode terminal has different RFs/IFs and employs the AFC circuit to stabilize each oscillator when a mode transitions to a different frequency band. Here, the AFC circuit operates to acquire a frequency offset. To do so, it operates a feed-back loop within the range of the amount of residual frequency jitter enough to ensure the demodulation performance at the receiving end, to thereby achieve stable performance. However, it takes a long time to establish a stabilized path by operating the feed-back loop at a mode transition, resulting in the increase of time required to ensure the demodulation performance. As shown in FIG. 1, in the case that different IFs/RFs should be multiplied by one TCXO and controlled by different PLLs, a different control dynamic range is set for each loop. Therefore, the amount of jitter in the phase noise error of each VCO output is different when controlling two different VCOs, thereby decreasing the demodulation performance of the receiver.

FIG. 2 is a graph illustrating the unequal dynamic range characteristics of the receiving AFC circuit in the dual-mode terminal. Referring to FIG. 2, reference numerals 222 and 224 denote two frequency slopes F1_step/V_step and F2_step/V_step of the TCXO 153. Reference numerals 226 and 228 denote the dynamic ranges of the first and second mixed signals Fc1 and Fc2, respectively. Reference numeral 230 denotes the phase-noise margin of the frequencies output from the TCXO 153. As shown in FIG. 2, due to use of the TCXO 153 in the AFC circuit of the conventional dual-mode terminal, the AFC 151 has different control voltage to frequency transform dynamic ranges. Hence, a TCXO exhibiting different slopes, as shown in FIG. 2, is required but difficult to design.

As described above, the receiving AFC circuit of the conventional dual-mode terminal has the problem that either a different operation should be executed at each mode or the frequency error tracking time is extended by use of a single AFC circuit. Another problem is that in the case of using one TCXO having a reference frequency for controlling two RFs/IFs, the dynamic ranges of the phase noise output with respect to the outputs of the two VCOs are different because of the residual phase noise of the TCXO, thereby decreasing the demodulation performance of the receiving end.

SUMMARY OF THE INVENTION

It is, therefore, an object of the present invention to provide an automatic frequency control circuit and a method thereof in a dual-mode terminal, which can stabilize frequency characteristics to increase demodulation performance.

It is another object of the present invention to provide an automatic frequency control circuit and a method thereof in a dual-mode terminal, which can vary the quantization level of digitized data to improve linear frequency transform characteristics.

It is a further object of the present invention to provide an automatic frequency control circuit and a method thereof in a dual-mode terminal, which introduces a forward common phase error compensation scheme to increase demodulation performance.

To achieve the above objects, there is provided an AFC circuit in a dual-mode terminal. According to one aspect of the present invention, the AFC circuit includes a first IF generator having a first frequency oscillator, for generating a first IF by mixing a first input signal with a first oscillation frequency. In the AFC circuit, a first A/D converter receives a first quantization step value, allocates quantization bits to obtain a first linear characteristic, and then converts the first IF to digital data. A second IF generator has a second frequency oscillator, and generates a second IF by mixing a second input signal with a second oscillation frequency. A second A/D converter receives a second quantization step value, allocates quantization bits to obtain a second linear characteristic, and then converts the second IF to digital data. An automatic frequency controller (AFC) receives the first and second digital data and automatically controls the frequency of a main clock based on the linear characteristics of the two input signals. A multiplier multiplies the clock and applies the multiplied clock to the first and second frequency oscillators.

According to another aspect of the present invention, the AFC circuit includes a first IF generator having a first frequency oscillator, for generating a first IF by mixing a first input signal with a first oscillation frequency. A first A/D converter converts the first IF to digital data, a second IF generator has a second frequency oscillator, for generating a second IF by mixing a second input signal with a second oscillation frequency, and a second A/D converter converts the second IF to digital data. An AFC receives the first and second digital data and automatically controls the frequency of the main clock based on the linear characteristics of the two input signals. A first frequency monitor monitors the frequency of the first input signal. A multiplier receives a clock and the outputs of the first frequency monitor and the AFC, multiplies the clock, and applies the multiplied clock to the first and second frequency oscillators. A PDS monitor receives the first IF and PDS information of the multiplier, and generates a PDS monitoring signal. A phase error estimator estimates the phase error from the outputs of the second A/D converter and the PDS monitor, and a multiplier multiplies the phase error by the output of the second A/D converter to thereby correct the phase error.

BRIEF DESCRIPTION OF THE DRAWINGS

The above and other objects, features and advantages of the present invention will become more apparent from the following detailed description when taken in conjunction with the accompanying drawings in which:

FIG. 1 is a block diagram of an AFC circuit in a dual-mode terminal according to the prior art;

FIG. 2 is a graph illustrating the unequal dynamic range in the AFC circuit of the dual-mode terminal shown in FIG. 1;

FIG. 3 is a block diagram of a dual-mode AFC circuit using an adaptive A/D quantization bit assigning method according to an embodiment of the present invention;

FIGs. 4A and 4B are block diagrams of the AFC circuit for bit assignment in the dual-mode terminal shown in FIG. 3; and

FIG. 5 is a block diagram of a dual-mode AFC circuit with a forward common error compensating function according to another embodiment of the present invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

Preferred embodiments of the present invention will be described hereinbelow with reference to the accompanying drawings. In the following description, well-known functions or constructions are not described in detail since they would obscure the invention in unnecessary detail.

The following description is conducted with the appreciation that first and second input signals indicate RX1 and RX2, respectively, first and second IFs indicate Fc1 and Fc2, respectively, and first and second quantization steps indicate F1_step/V_step and F2_step/V_step, respectively.

In a dual-mode terminal using an AFC circuit and a TCXO which can support a dual mode, the AFC circuit and the TCXO generate errors due to different linear characteristics. Therefore, the dual-mode terminal reduces the IF errors caused by the different linear characteristics in two modes by reducing time required for acquiring tracking synchronization of a PLL circuit in a mode using a first frequency by use of a test augmentation frequency which is an integer multiple of a tracking synchronization acquiring residual frequency of a PLL circuit for a second frequency to which the first frequency transitions for reliable synchronization acquisition, so that demodulation performance is ensured. Otherwise, errors with respect to a dynamic range, caused by the different linear characteristics at a mode transition, are reduced by varying the quantization bits of the A/D clock signal based on the dynamic range of residual errors in frequency, to thereby ensure the demodulation performance.

The demodulation performance can also be ensured by operating an ACPE (Advanced Common Phase Error) circuit for an AFC circuit having many residual frequency errors. In this method, the frequency characteristics of the dual-mode terminal are stabilized and the stability of a demodulator is increased due to a frequency offset. As a result, the stable demodulator performance is ensured.

There are three methods of overcoming the problems with use of a single TCXO with respect to a signal having two different RF frequencies in the AFC circuit of the above dual-mode terminal: (1) using a TCXO which can support both modes; (2) appropriately selecting a quantization level to obtain two linear characteristics; and (3) compensating for residual phase errors in one linear characteristic with respect to the other linear characteristic, in a forward direction in the baseband. That is, the TCXO satisfies a linear characteristic at one mode, and a linear characteristic at the other mode is satisfied by compensating for residual phase errors of digitized data. The above three methods of ensuring the stable characteristics of an AFC circuit can be applied to a dual-mode terminal according to the costs involved in configuring the receiving terminal.

Referring to FIGs. 3, 4A, and 4B, there will be given a description of the operation of an AFC circuit in a dual-mode terminal according to an embodiment of the present invention. FIG. 3 is a block diagram of the AFC circuit which improves linear frequency characteristics using an adaptive A/D quantization bit assigning method. FIGs. 4A and 4B are block diagrams of the A/D converters 315 and 335, respectively.

Referring to FIG. 3, the mixer 111 mixes the input signal RX with an oscillation frequency received from the oscillator 119 and outputs the first mixed signal Fc1. The LPF 113 low-pass filters the output of the mixer 111. The output of the LPF 113 is an amplitude A1 of the input signal. The A/D converter 315 converts the output of the LPF 113 to digital data q_a bit. The A/D converter 315 can be configured as shown in FIG. 4A. Referring to FIG. 4A, a maximum amplitude detector 412 detects a maximum amplitude MAX_A1 of the amplitude A1 of the input signal RX received from the LPF 113. A quantization gain controller 416 generates a control signal for controlling quantization gain in response to a first quantization step F1_step/V_step. A quantization bit allocator 414 generates quantization level information according to the maximum amplitude MAX_A1 and the quantization gain control signal received from the quantization gain controller 416. An A/D converter 410 receives the first quantization level information and converts the input signal with the amplitude A to digital data q_a.

The mixer 131 mixes the input signal RX with an oscillation frequency received from the oscillator 139 and outputs the second mixed signal Fc2. The LPF 133 low-pass filters the signal received from the mixer 131. The output of the LPF 133 is an amplitude A2 of the input signal. The A/D converter 135 converts the output of the LPF 133 to digital data q_b bit.

The A/D converter 335 can be configured as shown in FIG. 4B. Referring to FIG. 4B, a maximum amplitude detector 422 detects a maximum amplitude MAX_A2 of the amplitude A2 of the input signal RX received from the LPF 133. A quantization gain controller 426 generates a control signal for controlling quantization gain in response to a second quantization step F2_step/V_step. A quantization bit allocator 424 generates second quantization level information according to the maximum amplitude MAX_A2 and the quantization gain control signal received from the quantization gain controller 426. An A/D converter 420 receives the second quantization level information and converts the input signal with the amplitude Awis to digital data q_b bit.

The AFC 151 receives the digital data q_a bit and q_b bit from the A/D converters 115 and 135 and generates a signal (RX main clock) for automatically controlling a reception frequency. The TCXO 153 multiplies the output of the AFC 151 to generate an intended RF/IF. The PLL1 117 generates a control signal for generating a phase-locked frequency according to the multiplied signal received from the TCXO 153. The oscillator VCO1 119 generates the frequency set under the control of the PLL1 117 and applies the frequency to the mixer 111. The PLL2 137 generates a control signal for generating a phase-locked frequency according to the multiplied signal received from the TCXO 153. The oscillator VCO2 139 generates the frequency set under the control of the PLL2 137 and applies the frequency to the mixer 131. The BBA circuit 155 generates a sampling clock for the A/D converter 115 in response to the output of the TCXO 153. The BBA circuit 157 generates a sampling clock for the A/D converter 135 in response to the output of the TCXO 153.

In order to control the quantization level for the A/D conversion, the slope of a phase detector for the AFC 151 is determined by an input quantization level. That is, input levels of the phase detector should be designed to be different to represent two linear characteristics. The levels of the input signals Fc1 and Fc2 in FIG. 3 should be set to have different linear characteristics so that the AFC 151 can operate with stability. To determine the input levels, the AFC 151 calculates a quantization gain value for A/D conversion by

$$K_q = \frac{2^b}{2A} \quad \ldots\ldots\ldots\ldots (1)$$

where b represents the quantization level for the A/D conversion and A is the maximum amplitude of the received signal.

Since the quantization level is the slope of the phase detector for the AFC 151, the level slopes of inputs of the TCXO 153 can be controlled by varying quantization bits. The quantization level determines a phase compensation resolution, and as the phase compensation resolution decreases, the sensitivity to phase errors increases.

A quantization conversion rate should be considered in determining the quantization level because a noise margin component should be taken into account in A/D conversion. The quantization rate is the ratio of the quantization level of the A/D converter 315 to that of the A/D conveter. The quantization conversion rate is given by

$$K_q = \frac{2^b}{2A} * \frac{R}{100} \dots\dots\dots\dots (2)$$

In Eq.2, quantization data qad_a bit and qad_b bit are generated by determining a quantization level so that the slope of the quantization gain shows the two linear characteristics of the TCXO 153. [IS R THE CONVERSION RATE?]

Therefore, the A/D converters 315 and 335 determine the input levels of the received signal having different linear characteristics. The A/D converters 315 and 335 determine quantization bits so that the slope of quantization gain shows the two linear characteristics of the TCXO 153, and they convert input signals to digital data. Then, the AFC 151 receives the data q_a bit and q_b bit from the A/D converters 115 and 135 and rapidly performs phase synchronization. That is, by appropriately selecting the quantization bits in such a way to obtain the two linear characteristics, the AFC 151 can rapidly acquire phase synchronization. The TCXO 153 multiplies the RX main clock received from the AFC 151 and applies the multiplied RX main clock to the PLLs 117 and 137. Reference numeral 300 indicates that the A/D converters 315 and 335 adaptively allocate quantization bits according to the linear characteristic of each mode.

Now, the operation of a dual-mode automatic frequency control circuit using an ACPE (Advanced Common Phase Error) will be described referring to FIG. 5.

The mixer 111 mixes the input signal RX with an oscillation frequency received from the oscillator 119 and outputs the first mixed signal Fc1. The LPF 113 low-pass filters the output of the mixer 111. The output of the LPF 113 is an amplitude A1 of the input signal. The A/D converter 115 converts the output of the LPF 113 to digital data q_a bit.

The mixer 131 mixes the input signal RX with an oscillation frequency received from the oscillator 139 and outputs the second mixed signal Fc2. The

LPF 133 low-pass filters the signal received from the mixer 131. The output of the LPF 133 is an amplitude A2 of the input signal. The A/D converter 135 converts the output of the LPF 133 to digital data q_b bit.

The AFC 151 receives the digital data q_a bit and q_b bit from the A/D converters 115 and 135 from the A/D converters 115 and 135 and a choice indicator from a terminal control (not shown), and generates a signal (RX main clock) for automatically controlling a reception frequency. A first frequency monitor 511 generates an initial loading frequency error from the output of the AFC 151. Specifically, the first frequency monitor 511 loads a frequency error that the AFC 151 has at the previous mode as an initial value and applies it to the TCXO 153. The TCXO 153 multiplies the output of the AFC 151 and the initial loading frequency error to generate an intended RF/IF. The PLL1 117 generates a control signal for generating a phase-locked frequency according to the multiplied signal received from the TCXO 153. The oscillator VCO1 119 generates the frequency set under the control of the PLL1 117 and applies the frequency to the mixer 111. The PLL2 137 generates a control signal for generating a phase-locked frequency according to the multiplied signal received from the TCXO 153. The oscillator VCO2 139 generates the frequency set under the control of the PLL2 137 and applies the frequency to the mixer 131. The BBA circuit 155 generates a sampling clock for the A/D converter 115 in response to the output of the TCXO 153. The BBA circuit 157 generates a sampling clock for the A/D converter 135 in response to the output of the TCXO 153.

A PDS (Phase Density Spectrum) monitor 153 receives PDS information from the TCXO 153 and the second mixed signal Fc2 from the mixer 131 and monitors a PDS. A phase error estimator 151 measures the phase difference between the PDS signal received from the PDS monitor 513 and the data q_a bit from the A/D converter 135. A multiplier 517 multiplies the outputs of the A/D converter 135 and the phase error estimator 515 and re-compensates the digitized data.

The dual-mode AFC circuit of FIG. 5 compensates for the noise margin of FIG. 2 at the receiving end using the characteristics of the TCXO 153. To do so, the signal Fc1 is first designed to have a small dynamic range, the PDS monitor

513 monitors the PDS characteristic of the TCXO 153, and the phase error estimator 51 estimates a common phase error (CPE) by analyzing the PDS signal. Simultaneously, the first frequency monitor 511 monitors the tracking error component of Fc1 and loads the corresponding frequency error as the initial loading frequency error when the loop of Fc2 operates. Then, when the Fc2 loop starts tracking, the phase error estimator 515 is operated to thereby obtain the CPE value and compensate for the phase error of the AFC 151 based on the CPE value.

More specifically, the initial loading value is set to a stable frequency transition value by the first frequency monitor 511 of Fc1 and then the CPE is obtained.

To obtain the CPE, the PDS characteristic of the TCXO 153 is monitored, an ekda value is determined, and then the PDS of a phase noise is obtained. The PDS is calculated by

$$L_{\Phi N}(f) = 10^{-c} + \begin{bmatrix} 10^{-a} & :|f| < f1 \\ 10^{(f-f1)\frac{b}{f2-f1}} & :f1 < f \\ 10^{(f+f1)\frac{b}{f2-f1}-a} & :f \leftarrow f1 \end{bmatrix} \quad ......(3)$$

where f1 and a are the PLL characteristics frequency and gain, respectively, f2 is a frequency with respect to the noise floor of a characteristic curve, b is the slope of the characteristic curve, and c is a noise floor value.

The above PDS characteristic remains as the residual frequency offset of the phase detector, and a phase noise is obtained in the phase error estimator 515 of FIG. 5 and is compensated for at the next end. The phase error is estimated by

$$\Theta_{E_l} = \frac{\sum_{i=1}^{N_l} \eta_{cl,l} \bullet \theta_{l,cl,l}}{\sum_{i=1}^{N_l} \eta_{cl,l}} \quad ..... (4)$$

where N_L is an observation period, $n_{cl,l}$ is an estimated amplitude value obtained by a channel estimation compensator, and $\theta_{l, cl, l}$ is the phase of the previous symbol. The influence of linear frequency characteristics on residual phase noise can be compensated for by re-compensating the CPE obtained in the above procedure at the next end of the channel estimated value. Therefore, the AFC can be stabilized.

In accordance with the present invention, when a dual-mode terminal uses one or two AFC circuits, the time required for acquiring tracking synchronization in a PLL circuit for a first frequency can be reduced using a test augmentation frequency, which is an integer multiple of a tracking synchronization acquiring residual frequency of a PLL circuit for a second frequency to which the first frequency transitions for reliable synchronization acquisition. Errors with respect to the output dynamic range caused by use of two AFCs are reduced and thus the demodulation performance of a receiver is ensured by varying the quantization bits of the A/D clock based on the dynamic range of residual errors in frequency. The demodulation performance can also be ensured by operating an ACPE circuit for an AFC circuit having many residual frequency errors. In this method, the frequency characteristics of the dual-mode terminal are stabilized and the stability of a demodulator is increased due to a frequency offset. As a result, the stable demodulator performance is ensured.

While the invention has been shown and described with reference to a certain preferred embodiment thereof, it will be understood by those skilled in the art that various changes in form and details may be made therein without departing from the spirit and scope of the invention as defined by the appended claims.

CLAIMS:

1. An Automatic Frequency Control (AFC) device in a dual-mode terminal, comprising:

a first IF (Intermediate Frequency) generator having a first frequency oscillator, for generating a first IF by mixing a first input signal with a first oscillation frequency;

a first analog-to-digital (A/D) converter for receiving a first quantization step value, allocating quantization bits to obtain a first linear characteristic, and then converting the first IF to first digital data;

a second IF generator having a second frequency oscillator, for generating a second IF by mixing a second input signal with a second oscillation frequency;

a second A/D converter for receiving a second quantization step value, allocating quantization bits to obtain a second linear characteristic, and then converting the second IF to second digital data;

an automatic frequency controller for receiving the first and second digital data and automatically controlling the frequency of a main clock based on the first and second linear characteristics; and

a frequency multiplier for multiplying said clock signal and applying the multiplied clock signal to the said first and second frequency oscillators.

2. The AFC device of claim 1, wherein each of the first and second A/D converters comprises:

a maximum amplitude detector for detecting the maximum amplitude value of the IF;

a quantization gain controller for receiving the quantization step value and generating a quantization gain control signal; and

a quantization bit allocator for allocating the quantization bits to the maximum amplitude by using the quantization gain control signal.

3. The AFC device of claim 1, wherein each of the first and second IF generators comprises:

a phase locked loop (PLL) for synchronizing the output of the frequency multiplier with a predetermined frequency in phase;

a mixer for mixing the corresponding input signal with the output of the frequency oscillator; and

a filter for filtering an intended IF band from the output of the mixer;

wherein the frequency oscillator generates an internal oscillation frequency by means of the output of the PLL.

4. The AFC device of claim 2, wherein each of the first and second IF generators comprises:

a phase locked loop (PLL) for synchronizing the output of the frequency multiplier with a predetermined frequency in phase;

a mixer for mixing the corresponding input signal with the output of the frequency oscillator; and

a filter for filtering an intended IF band from the output of the mixer;

wherein the frequency oscillator generates an internal oscillation frequency by means of the output of the PLL.

5. An Automatic Frequency Control (AFC) device in a dual-mode terminal, comprising:

a first Intermediate Frequency (IF) generator having a first frequency oscillator, for generating a first IF by mixing a first input signal with a first oscillation frequency;

a first analog-to-digital (A/D) converter for converting the first IF to digital data;

a second IF generator having a second frequency oscillator, for generating a second IF by mixing a second input signal with a second oscillation frequency;

a second A/D converter for converting the second IF to digital data;

an automatic frequency controller for receiving the first and second digital data and automatically controlling the frequency of a main clock based on a first and second linear characteristics;

a frequency multiplier for receiving a clock signal and the output of said AFC, multiplying the clock signal, and applying the multiplied clock signal to the first and second frequency oscillators;

a PDS monitor for receiving the first IF and PDS information of the multiplier, and generating a PDS monitoring signal;

a phase error estimator for estimating a phase error from the outputs of the second A/D converter and the PDS monitor; and a multiplier for multiplying the phase error by the output of the second A/D converter to thereby correct the phase error.

6. The AFC device of claim 5, wherein each of the first and second IF generators comprises:

a PLL for synchronizing the output of the frequency multiplier with a predetermined frequency in phase;

a mixer for mixing the corresponding input signal with the output of the frequency oscillator; and

a filter for filtering an intended IF band from the output of the mixer;

wherein the frequency oscillator generates an internal oscillation frequency by means of the output of the PLL.

7. The AFC device of claim 5, wherein the AFC further comprises a first frequency monitor for monitoring the frequency of a signal input to the AFC, loading an input frequency error at the previous mode when the mode is transitioned, and outputting the loaded error to the frequency multiplier.

8. The AFC device of claim 7, wherein the frequency multiplier initially loads the first frequency error and multiplies a clock.

9. An automatic frequency controlling method in a dual-mode terminal, comprising the steps of:

generating first and second Intermediate Frequencies (IFs) by mixing first and second input signals with first and second oscillation frequencies;

determining a quantization gain and a transform rate according to the linear characteristics of the first and second IFs and generating first and second digital data;

automatically controlling the frequencies of the first and second digital data and generating a clock signal; and

generating the first and second IFs according to the clock signal.

10. An automatic frequency controlling method in a dual-mode terminal, comprising the steps of:

generating first and second Intermediate Frequencies (IFs) by mixing first and second input signals with first and second oscillation frequencies;

generating first and second digital data according to the linear characteristics of the first and second IFs;

monitoring the tracking error component of the first input signal while estimating a phase error, loading the estimated frequency error value as an initial value to be used in generating a clock signal, and generating the clock signal; and

generating the first and second oscillation frequencies according to the clock signal, estimating a phase error when an automatic control loop for the second input signal starts tracking, and compensating for the phase error.

FIG. 1

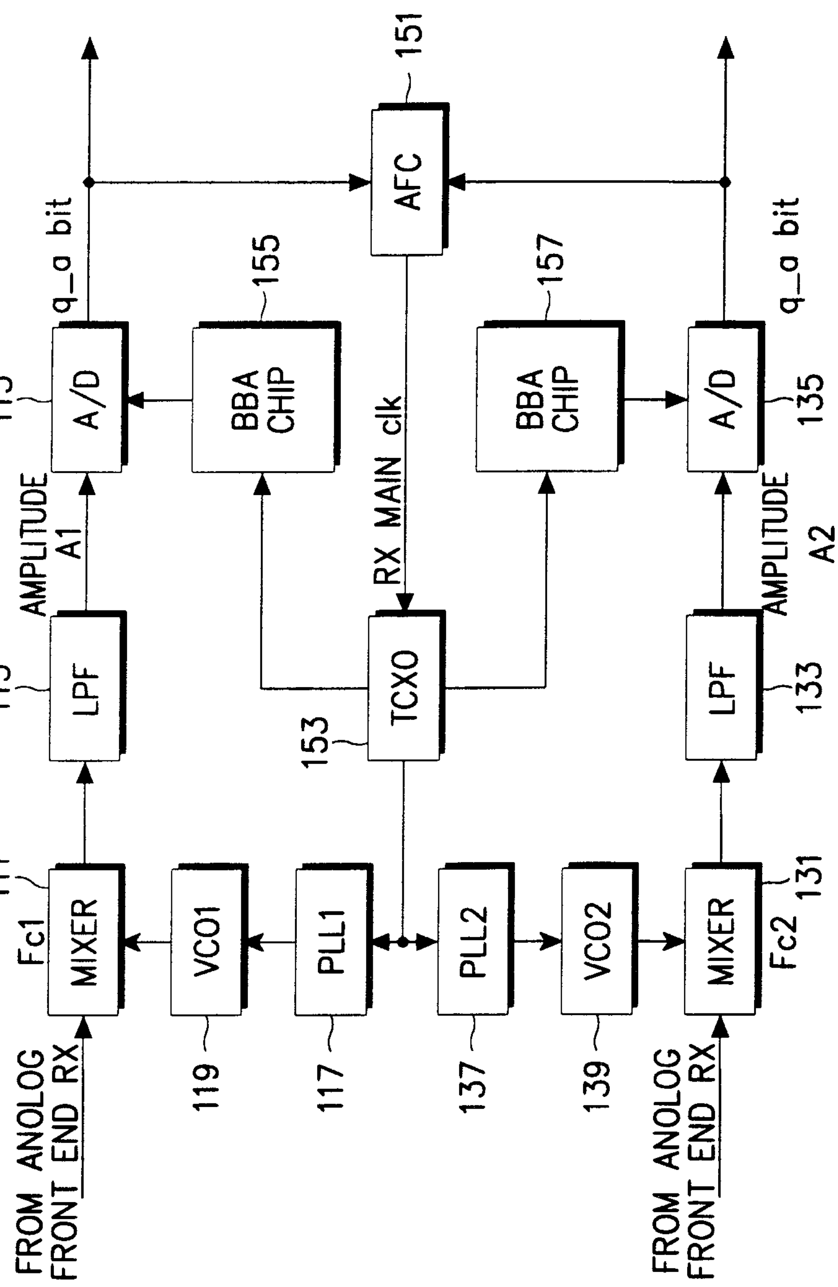

FROM ANOLOG FRONT END RX
Fc1
MIXER
111
LPF
113
AMPLITUDE A1
A/D
115
q_a bit
VCO1
119
PLL1
117
BBA CHIP
155
TCXO
153
RX MAIN clk
AFC
151
PLL2
137
VCO2
139
BBA CHIP
157
FROM ANOLOG FRONT END RX
Fc2
MIXER
131
LPF
133
AMPLITUDE A2
A/D
135
q_a bit

FIG. 2

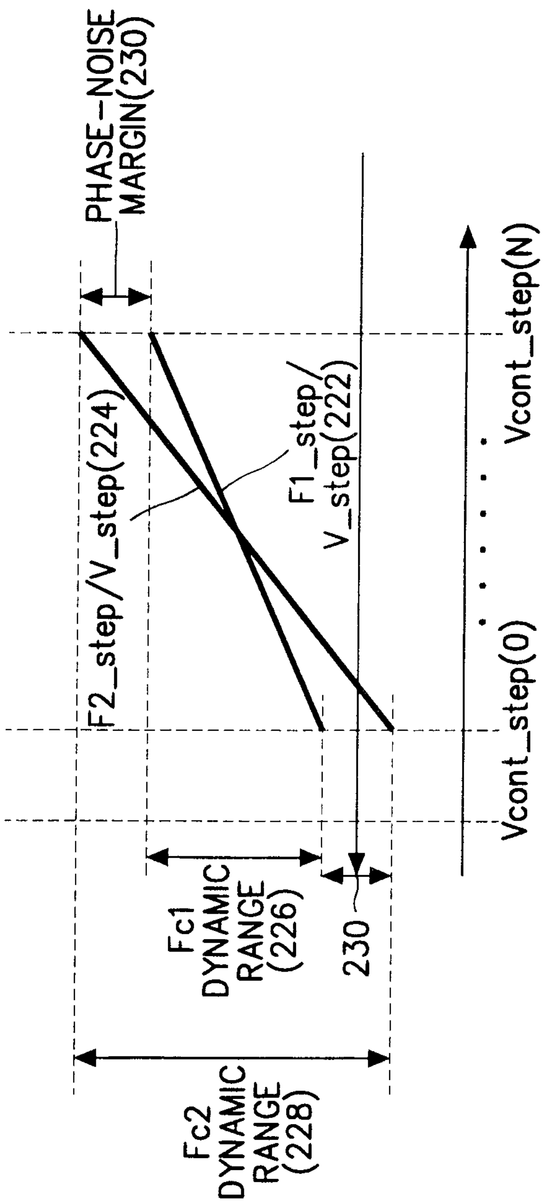
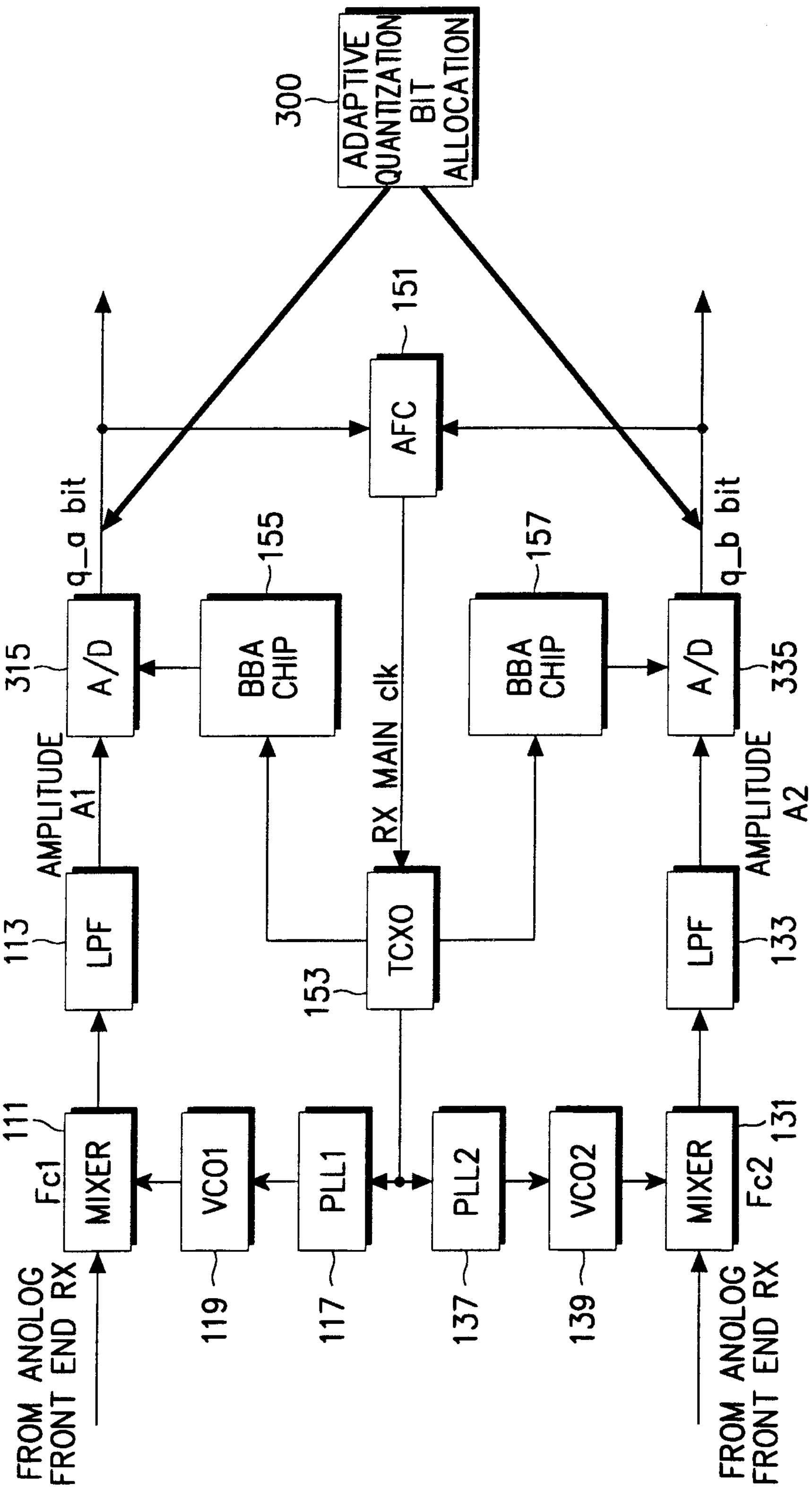

PHASE-NOISE MARGIN(230)
F2_step/V_step(224)
F1_step/ V_step(222)
Vcont_step(N)
Vcont_step(0)
Fc1 DYNAMIC RANGE (226)
230
Fc2 DYNAMIC RANGE (228)

FIG. 3


300
ADAPTIVE QUANTIZATION BIT ALLOCATION
151
AFC
q_a bit
q_b bit
155
BBA CHIP
157
BBA CHIP
315
A/D
335
A/D
RX MAIN clk
AMPLITUDE A1
AMPLITUDE A2
113
LPF
133
LPF
153
TCXO
111
Fc1
MIXER
131
Fc2
MIXER
119
VCO1
117
PLL1
137
PLL2
139
VCO2
FROM ANOLOG FRONT END RX
FROM ANOLOG FRONT END RX

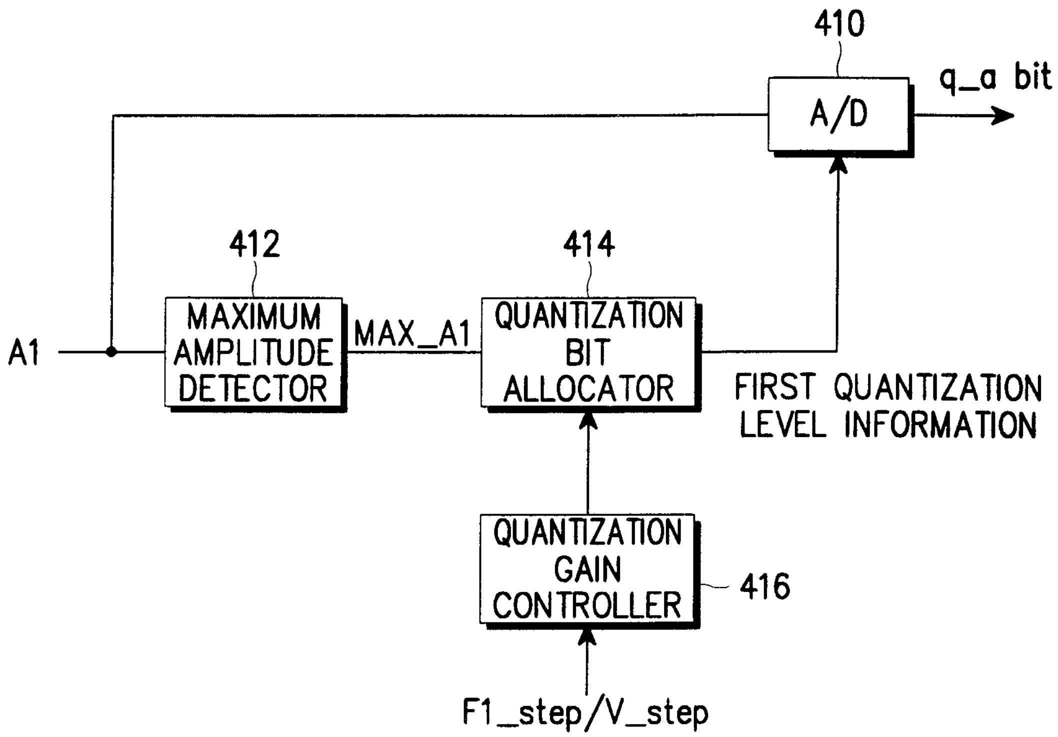

410
q_a bit
A/D
412
414
A1
MAXIMUM AMPLITUDE DETECTOR
MAX_A1
QUANTIZATION BIT ALLOCATOR
FIRST QUANTIZATION LEVEL INFORMATION
QUANTIZATION GAIN CONTROLLER
416
F1_step/V_step

FIG. 4A

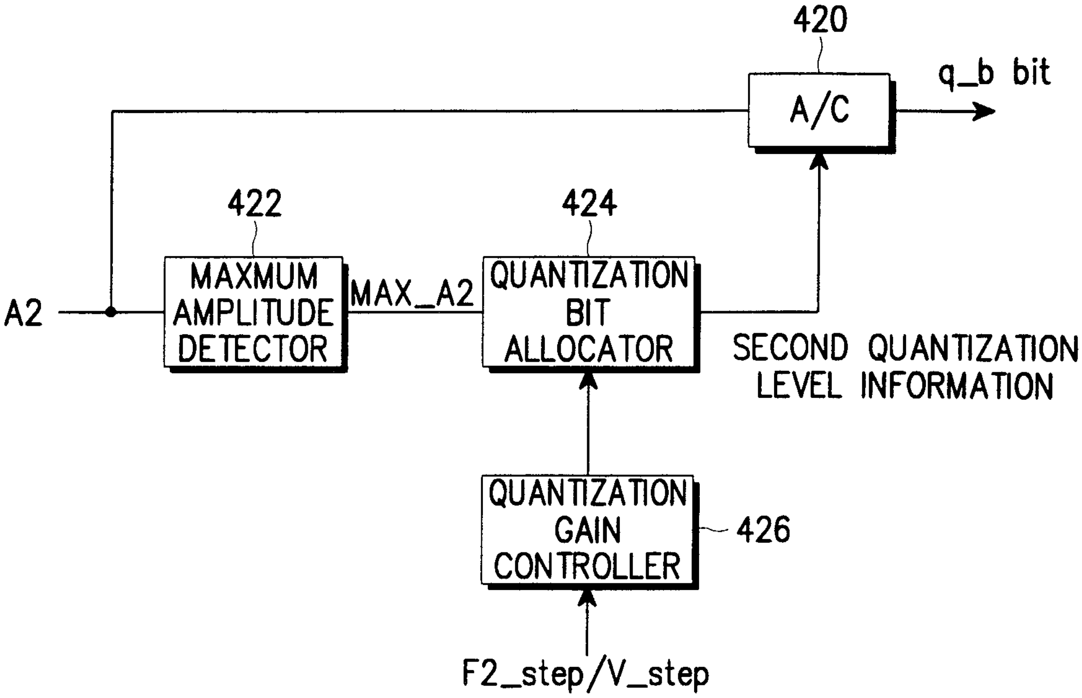

420
q_b bit
A/C
422
424
A2
MAXMUM AMPLITUDE DETECTOR
MAX_A2
QUANTIZATION BIT ALLOCATOR
SECOND QUANTIZATION LEVEL INFORMATION
QUANTIZATION GAIN CONTROLLER
426
F2_step/V_step

FIG. 4B

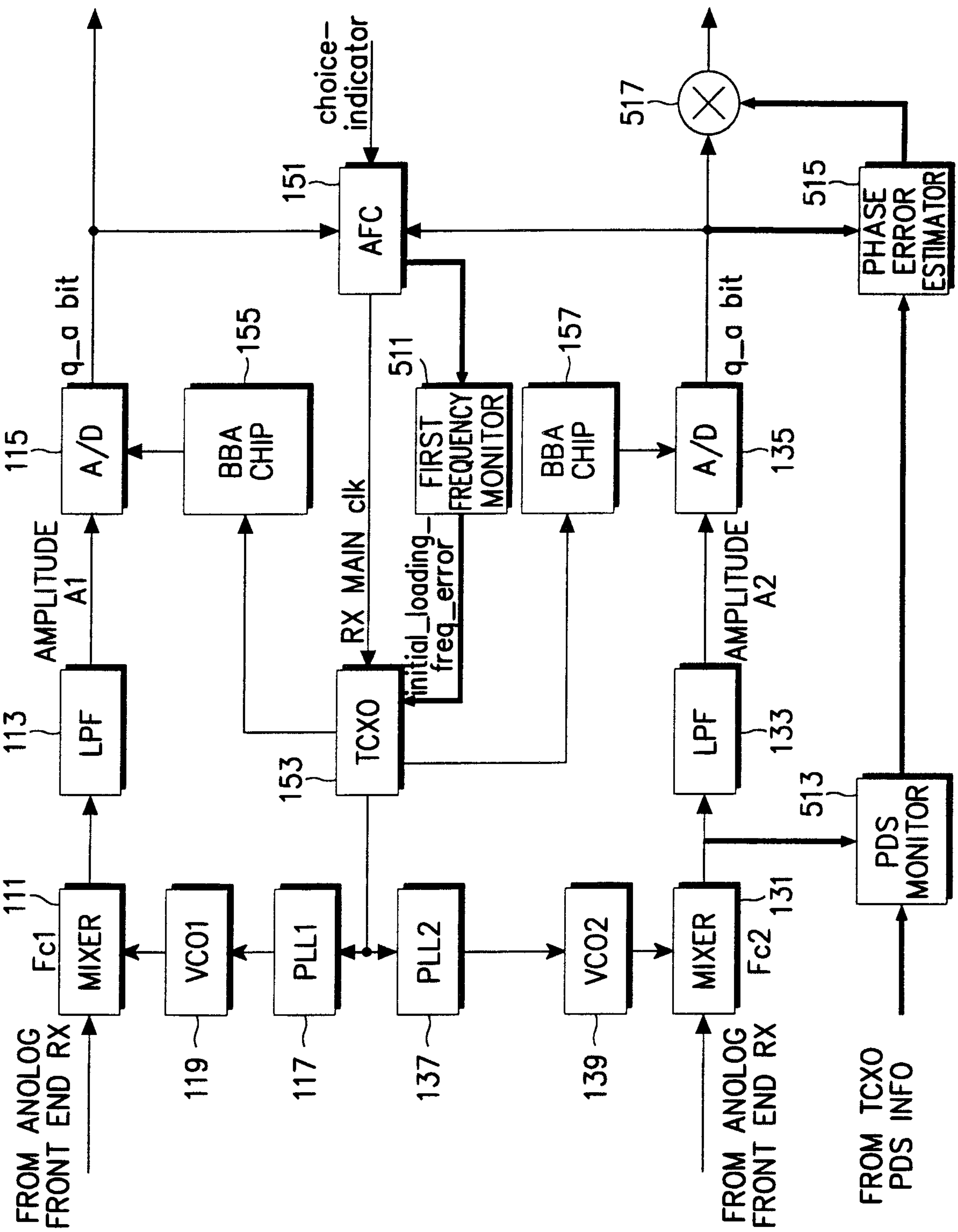

FROM ANOLOG FRONT END RX
Fc1
MIXER
111
119
VCO1
117
PLL1
113
LPF
AMPLITUDE A1
115
A/D
q_a bit
155
BBA CHIP
153
TCXO
RX MAIN clk
initial_loading_freq_error
151
AFC
choice-indicator
511
FIRST FREQUENCY MONITOR
137
PLL2
139
VCO2
157
BBA CHIP
FROM ANOLOG FRONT END RX
Fc2
MIXER
131
133
LPF
AMPLITUDE A2
135
A/D
q_a bit
517
515
PHASE ERROR ESTIMATOR
513
PDS MONITOR
FROM TCXO PDS INFO

FIG. 5