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(54) IMPLANT-CONTROLLED-CHANNEL VERTICAL JFET

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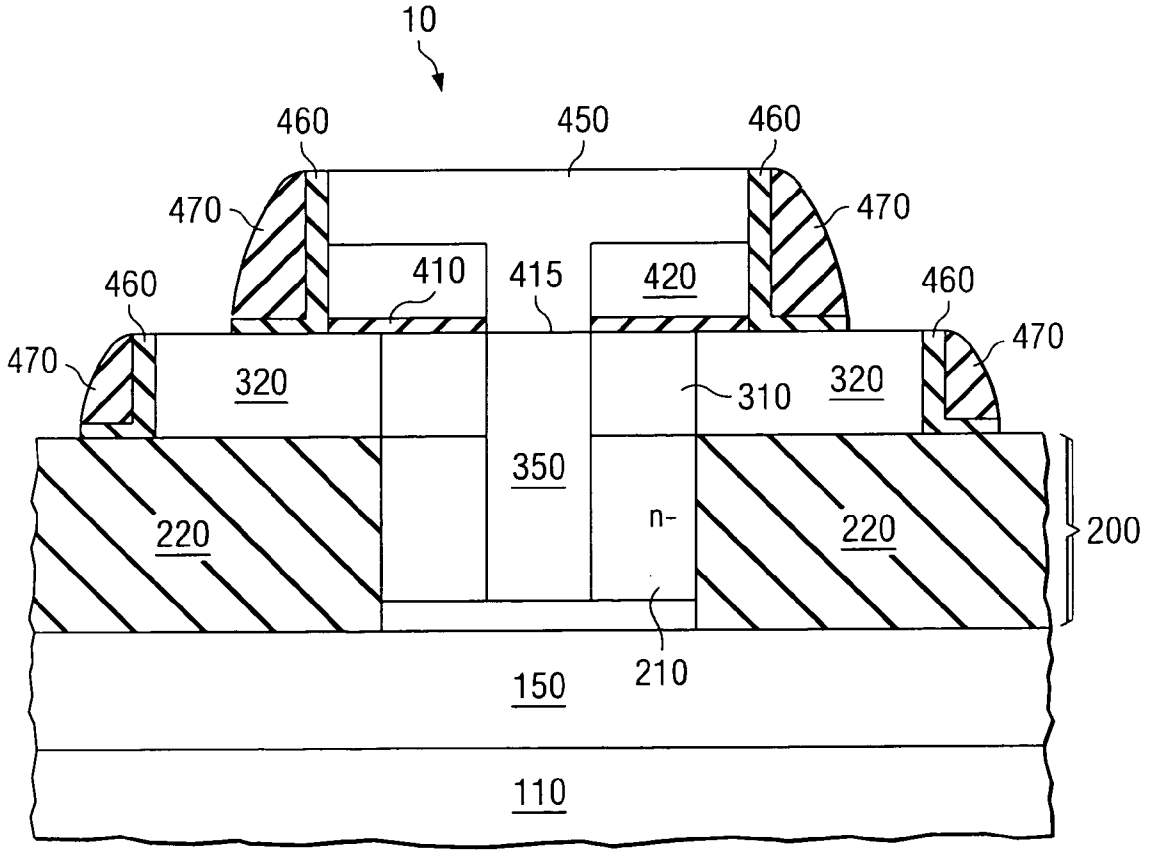
(52) **U.S. Cl.** **257/134**

(57) **ABSTRACT**

We disclose the structure of an electronic device, the method of making the device and the operation of the device. The device is built near the top of a substrate. It has, near the top surface, a buried layer that is electrically communicable to a drain terminal. The device has a body region over the buried layer. A portion of the body region contacts a gate region connected to a gate terminal. The device has a channel region, of which the length spans the distance between the buried layer and a source region, which projects upward from the channel region and is connected to a source terminal. The device current flows in the channel substantially perpendicularly to the top surface of the substrate.



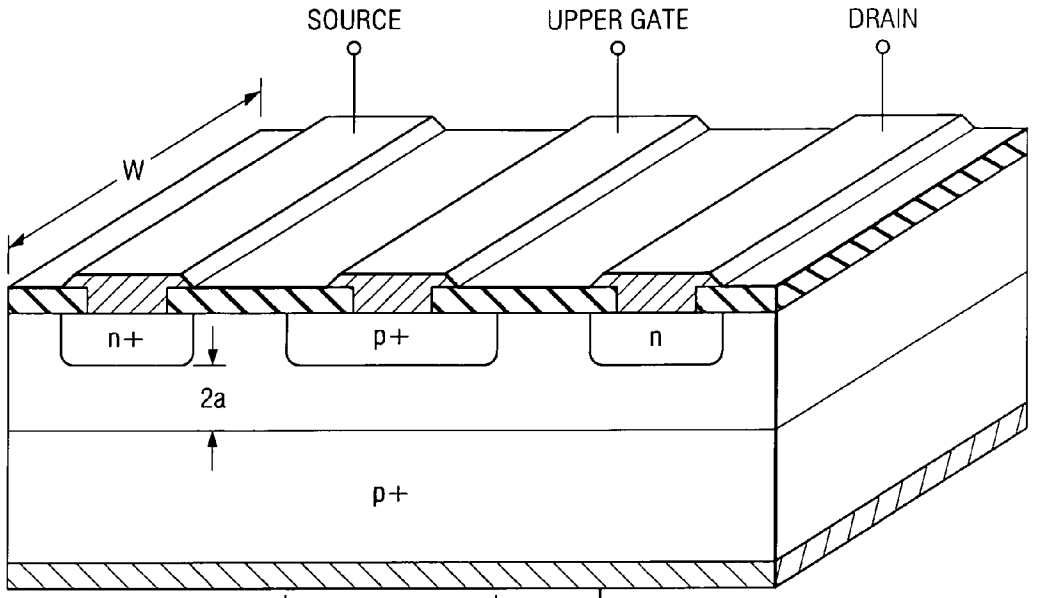


FIG. 1a
(PRIOR ART)

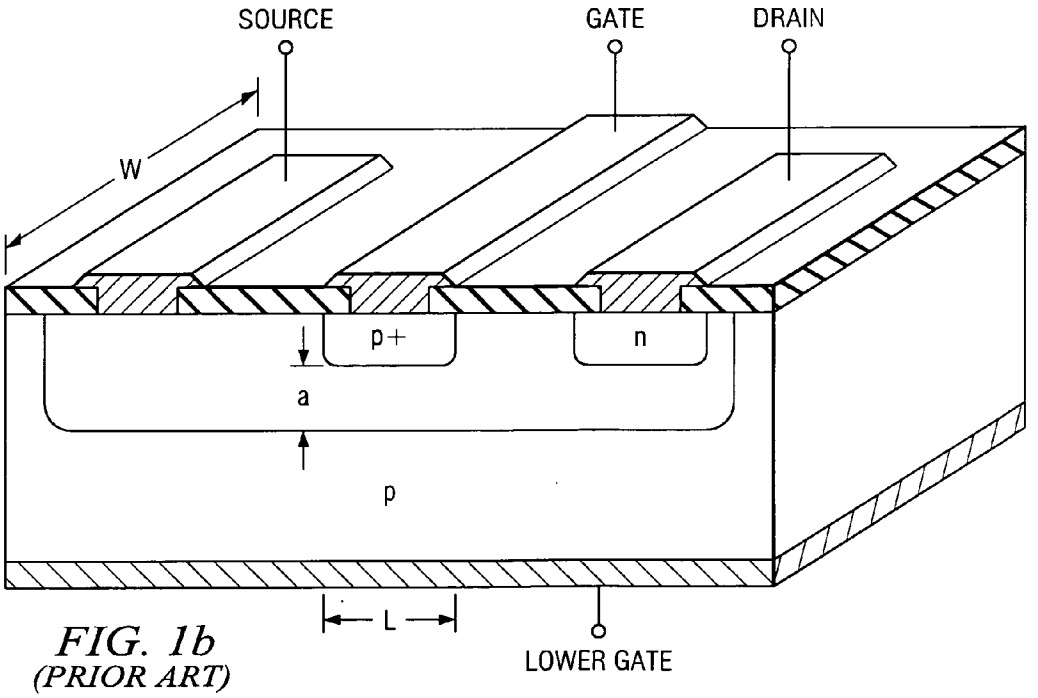


FIG. 1b
(PRIOR ART)

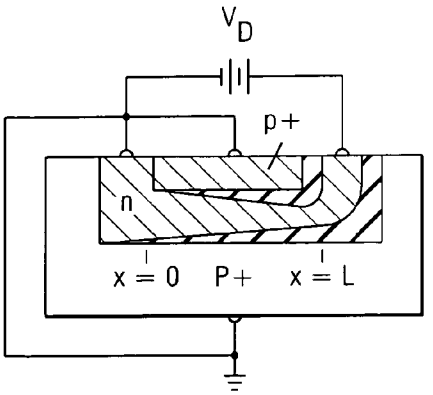


FIG. 1c
(PRIOR ART)

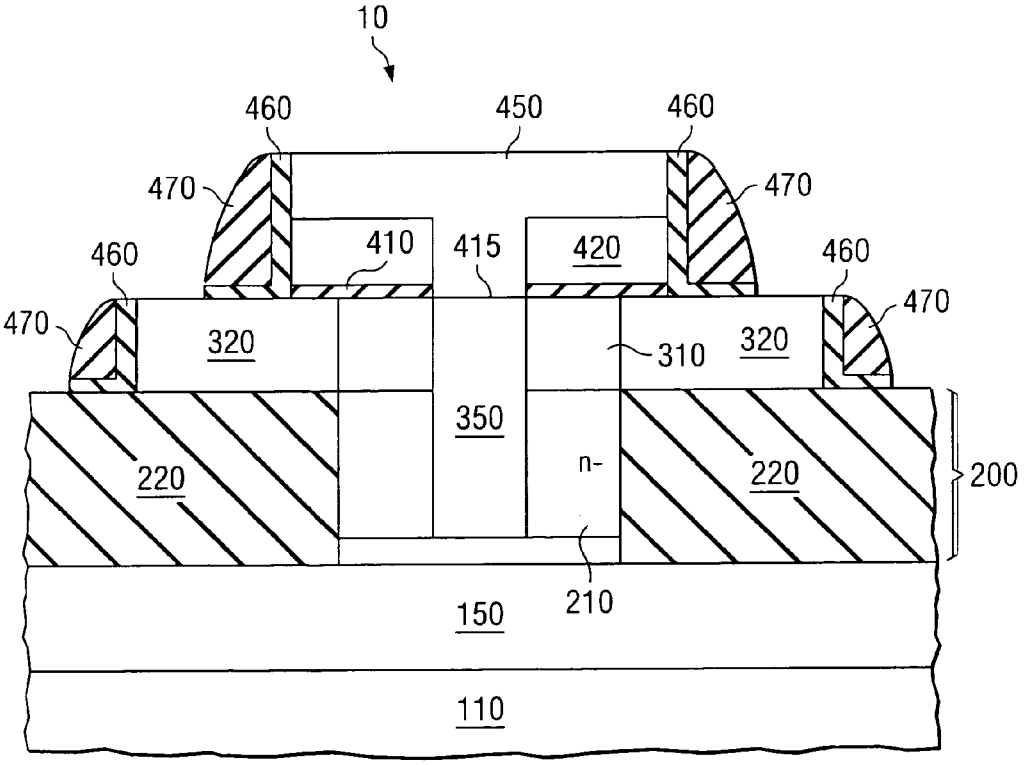


FIG. 2

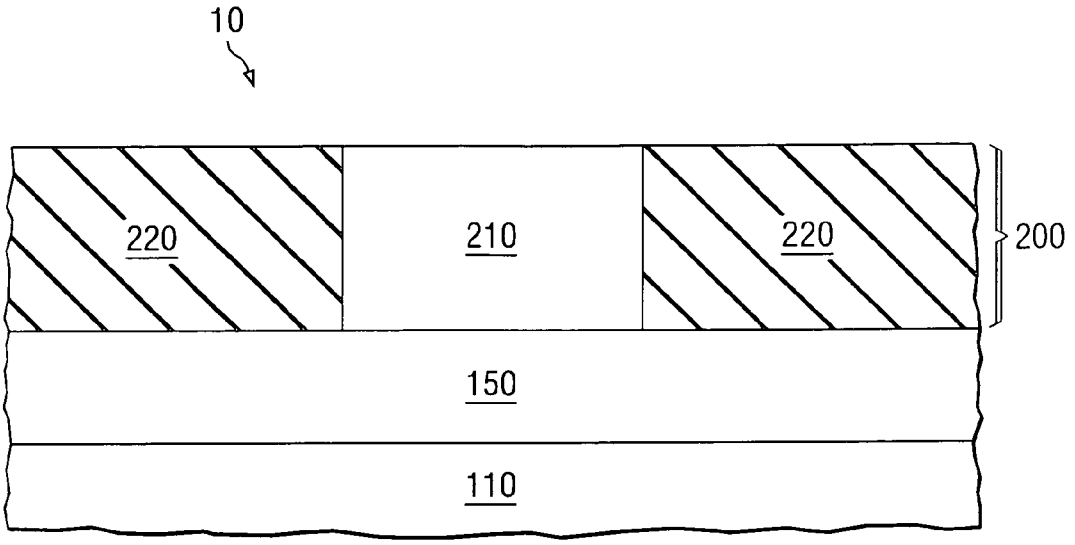

10
220
210
220
200
150
110

FIG. 3

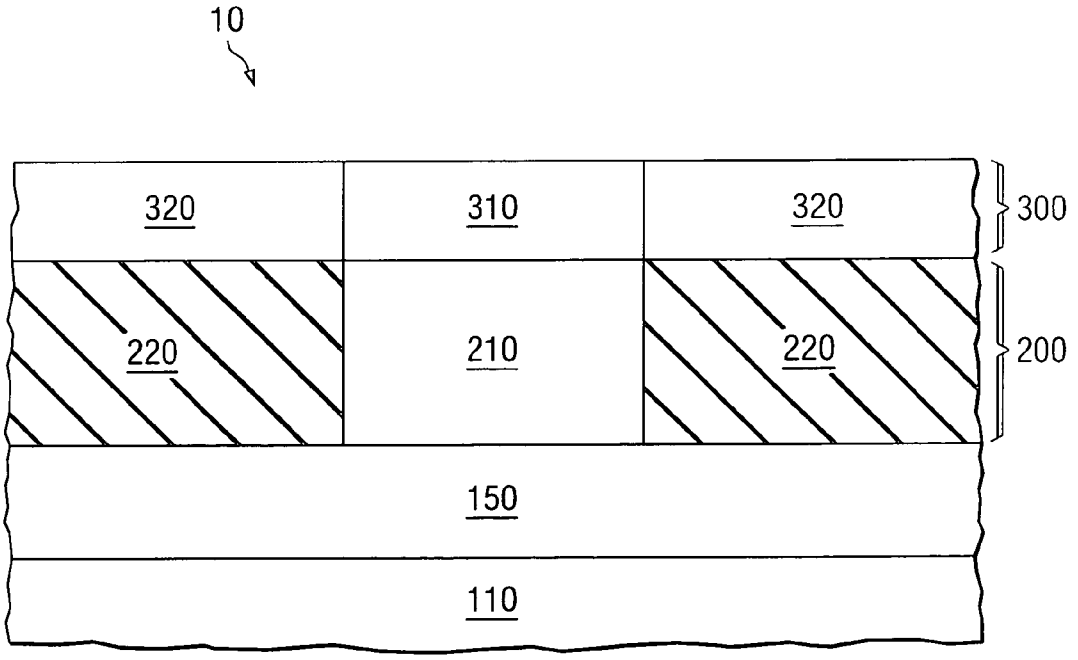

10
320
310
320
300
220
210
220
200
150
110

FIG. 4

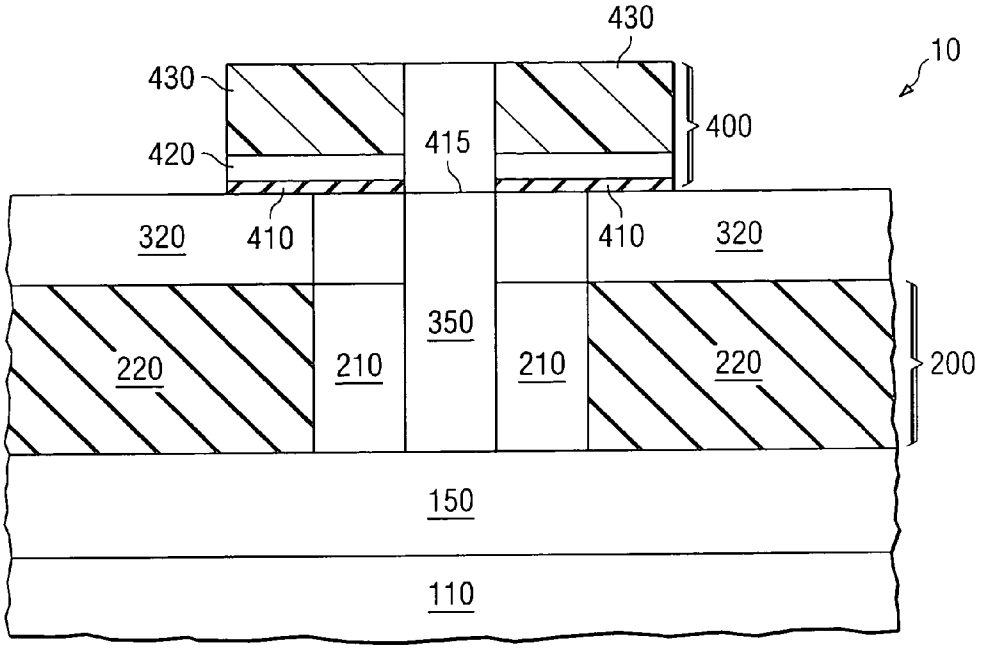

430
10
430
400
420
415
320
410
410
320
350
220
210
210
220
200
150
110

FIG. 5

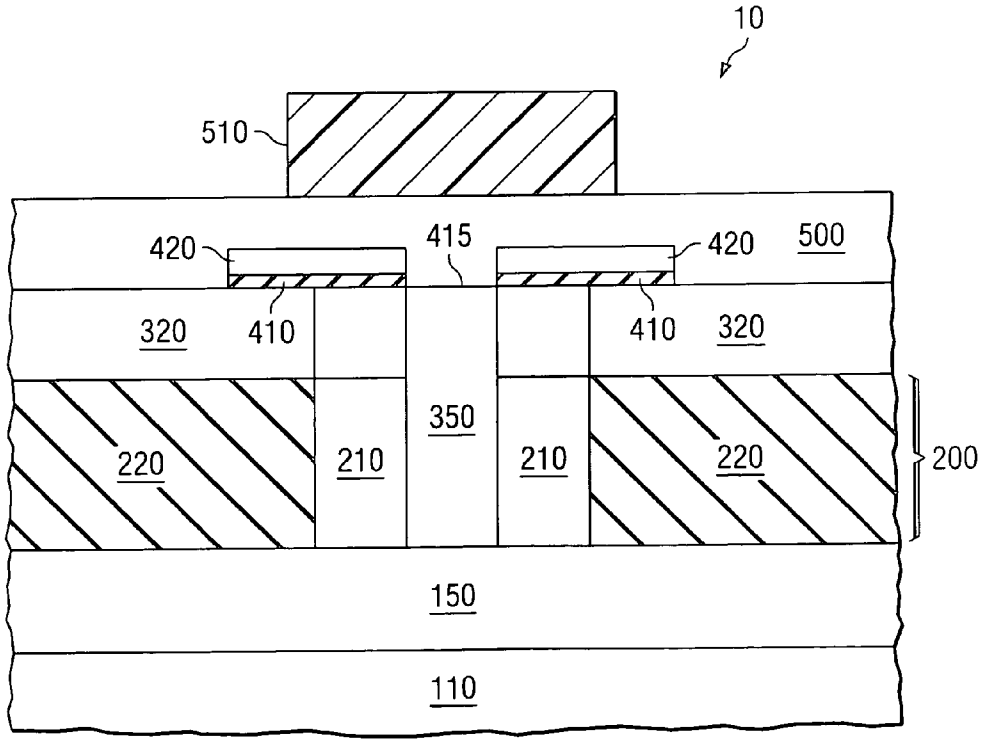

10
510
420
415
420
500
320
410
410
320
350
220
210
210
220
200
150
110

FIG. 6

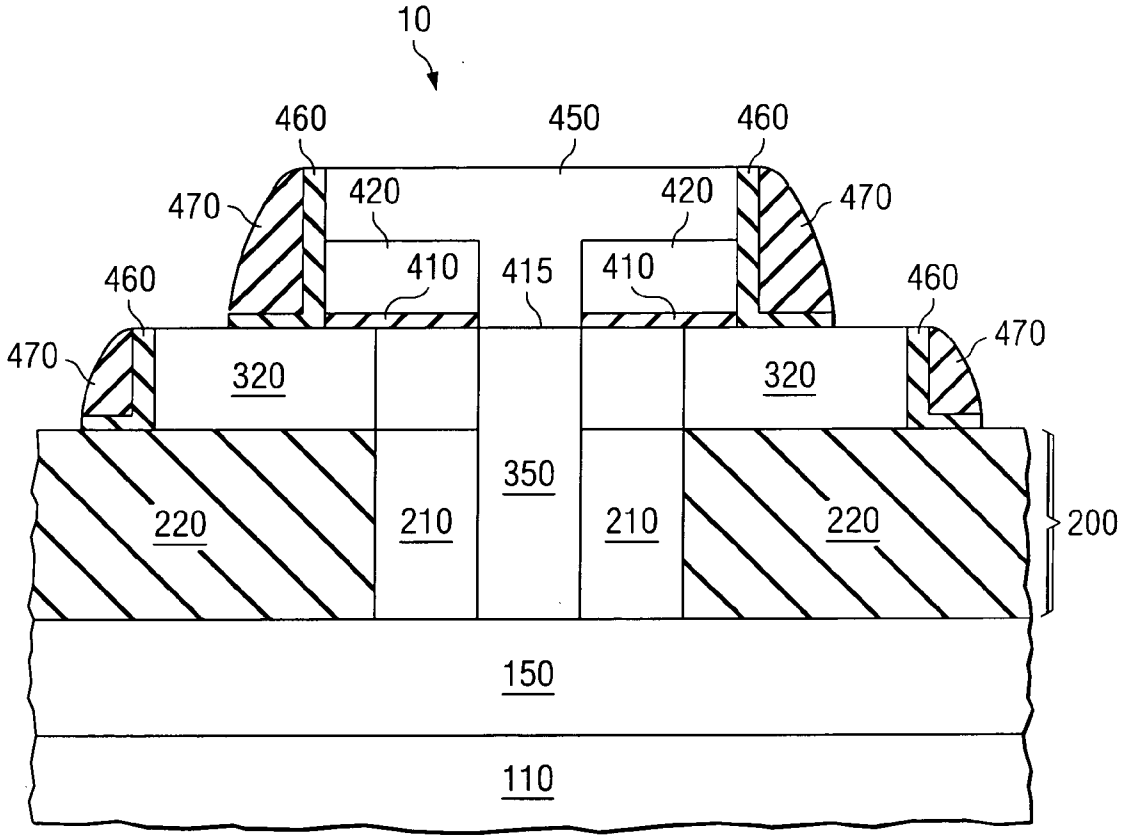

10
460
450
460
470
420
420
470
410
415
410
460
460
470
470
320
320
350
220
210
210
220
200
150
110

FIG. 7

IMPLANT-CONTROLLED-CHANNEL VERTICAL JFET

BACKGROUND OF THE INVENTION

[0001] This invention relates to semiconductor devices and particularly to an improved junction field effect transistor (JFET).

[0002] A conventional JFET is a three-terminal semiconductor device in which a current flowing substantially parallel to the top surface of the semiconductor chip is controlled by an externally applied vertical electric field, as shown in **FIGS. 1***a,* **1***b,* and **1***c.* It can be used as a switch or an amplifier. JFET is known as the unipolar transistor because the current is transported by carriers of one polarity, namely, the majority carriers. This is in contrast with the bipolar junction transistor, in which both majority-and-minority-carrier currents are important.

[0003] A typical n-channel JFET fabricated by the standard planar process is shown in **FIG. 1**. **FIG. 1***a* depicts a JFET built in a semiconductor substrate in an epitaxial layer. **FIG. 1***b* depicts a JFET fabricated by a double-diffused technique in a bulk semiconductor substrate. **FIG. 1***c* is a schematic representation of both JFETs.

[0004] The active region of the JFET consists of a lightly doped n-type channel sandwiched between two heavily doped p^+-gate regions. In **FIG. 1 a**, the lower p^+ region is the substrate, and the upper p^+ region is formed by boron diffusion into the epitaxially grown n-type channel. The p^+ regions are connected either internally or externally to form the gate terminal. Ohmic contacts attached to the two ends of the channel are known as the drain and source terminals through which the channel current flows. Alternatively, the JFET may be fabricated by the double-diffused technique with a diffused channel and an upper gate as illustrated in **FIG. 1***b.* In both cases, the channel and the gate regions run substantially parallel the top surface of the substrate, so does the current flow in the channel.

[0005] When a JFET operates as a switch, without a gate bias voltage, the transistor has a conducting channel between the source and the drain terminals. This is the ON state. To reach the OFF state, a reverse-biasing gate voltage is applied to deplete all carriers in the channel.

[0006] The reverse voltage bias applied across the gate/channel junctions depletes free carriers from the channel and produces space-charge regions extending into the channel. With a gate voltage set between ON and OFF levels, the cross-sectional area of the channel and the channel resistance can be varied. Thus the current flow between the source and the drain is modulated by the gate voltage.

[0007] An important figure of merit of a JFET is its cutoff frequency (f_{co}), which can be represented mathematically as follows:

$$f_{co} \leqq q\ a^2 \mu_n N_d / (4\pi k \epsilon_o L^2),$$

[0008] where q is the electric charge of the charge carriers, a is the channel width, μ_n is the mobility of the charge carriers, N_d is the doping concentration in the channel, k and ϵ_o are the dielectric constant and the electrical permittivity of the semiconductor material and the free space respectively, and L is the channel length.

[0009] Another important figure of merit of a JFET is the noise figure. At lower frequencies the dominant noise source in a transistor is due to the interaction of the current flow and the surface region that gives rise to the 1/f noise spectrum.

[0010] This invention provides a JFET device that has superior f_{co} and 1/f performance over conventional JFETs and a process of making the device.

BRIEF DESCRIPTION OF THE DRAWINGS

[0011] **FIG. 1***a* is a partial sectional depiction of a semiconductor substrate with a JFET device built in it.

[0012] **FIG. 1***b* is a partial sectional depiction of a semiconductor substrate with another JFET device built in it.

[0013] **FIG. 1***c* is a schematical representation of a JFET.

[0014] **FIG. 2** is a partial sectional depiction of a semiconductor substrate with a JFET embodying the invention built in it.

[0015] **FIG. 3** is a cross-sectional depiction of a partially completed JFET **10** embodying this invention.

[0016] **FIG. 4** is a cross-sectional depiction of a further partially completed JFET **10** embodying this invention.

[0017] **FIG. 5** is a cross-sectional depiction of a further partially completed JFET **10** embodying this invention.

[0018] **FIG. 6** is a cross-sectional depiction of a further partially completed JFET **10** embodying this invention.

[0019] **FIG. 7** is a cross-sectional depiction of a further partially completed JFET **10** embodying this invention.

DESCRIPTION OF THE PREFERRED EMBODIMENT

[0020] In **FIG. 2**, an n-channel JFET **10** is shown as a three-terminal device, fabricated near the surface of a semiconductor substrate surface. The semiconductor material in the preferred embodiment is silicon. A JFET embodying this invention can also be fabricated in other semiconductor materials such as germanium, germanium-silicon, gallium arsenide or other compound material. **FIG. 2** depicts a JFET built in a bulk silicon substrate. A JFET embodying this invention can also be fabricated in a substrate of semiconductor-on-insulator such as SIMOX, silicon-on-sapphire, or in bonded wafer. **FIG. 2** depicts an n-channel JFET. A JFET embodying this invention can also be implemented as a p-channel JFET. A JFET may also be one device in an integrated circuit that includes CMOS and Bipolar circuit elements, and passive circuit components.

[0021] The substrate **110** may be either n-type or p-type. In a typical integrated circuit fabricated by a BiCMOS process, the substrate **110** would be a lightly doped, p-type crystalline silicon material. Over a portion of the substrate **110** is an n-type layer **150** of low resistivity that constitutes the drain portion of the JFET. In a BiCMOS structure, a region commonly referred to as "a buried layer" fits this requirement.

[0022] Over a portion of the buried layer **150** is layer **200**. Layer **200** includes several regions of different materials. Among them, region **220** includes primarily dielectric material. In this embodiment, this material is silicon dioxide, fabricated with a STI technique. Region **220** may also be

built with a LOCOS technique or other techniques well known in the art. Element **210** of layer **200** is substantially p-type mono-crystalline silicon. It may be formed by an epitaxial technique.

[**0023**] Elements **320** are gate regions of the JFET, located above layer **200**. They are polycrystalline silicon, heavily doped with p-type dopant. A portion of the p-type dopant diffuses into the adjacent lightly doped p-region **310**, which is mono-crystalline. The combination of elements **310** and **210** makes up a mono-crystalline region that contains the channel region **350** of the JFET.

[**0024**] The channel may be created by implanting n-type ions perpendicular to the substrate surface. The dopant concentration in the channel region is usually not uniform. In fact, it is advantageous to be able to tailor the doping profile, for example, so that the dopant concentration in the channel region near the surface of the substrate is lower than the dopant concentration distant from the surface of the substrate. This dopant profile places the pinch-off region closer to the top of layer **310** and uses the shallow portion of the implanted ions to set the pinch-off voltage of the JFET. Such a profile may be accomplished with a multiple-implant process. The multiple implants may be of various dosages and implant energies. In this embodiment, we employ a three-implant process—one at 220 keV, one at 340 keV and one at 500 keV.

[**0025**] The source region **450** in this embodiment is poly-crystalline. It makes contact to the channel region **350** through an opening **415** etched out through an insulating element that comprises a silicon dioxide element **410** and a silicon nitride element **420**. In the preferred embodiment, there is an absence of native oxide between the source region **450** and the channel region **350** so the source region contacts the channel region and the silicon immediately above the channel region may retain the mono-crystalline structure within a short range. In another embodiment, minute oxide may exist in the vicinity of the opening **450** as result of chemical processes such as a wet chemical cleanup process. The source region **450** is heavily doped with phosphorus, arsenic, or other n-type dopants and it partially overhangs the gate regions **320** and is insulated from the gate region **320** by silicon dioxide elements **410**, silicon nitride elements **420**, oxide elements **460** and nitride elements **470**.

[**0026**] FIGS. **3** to **7** depict the channel portion of a JFET embodying this invention through a fabrication process. The complete fabrication of a functional JFET, in the context of an integrated circuit, involves many well-known processes in addition to those illustrated in the drawings. These well-known processes include creating a drain contact to the buried layer, a source contact to the source region, and a gate contact to the gate region, and wiring the contacts with metallic elements to connect the JFET to the other circuit elements of the integrated circuit.

[**0027**] **FIG. 3** depicts a cross-sectional view of a partially completed JFET **10** embodying this invention. Element **110** is a semiconductor substrate. In this embodiment, the semiconductor material is silicon. Other semiconductor materials suitable to implement this invention include germanium, silicon-germanium, silicon carbide, and gallium arsenide. In this embodiment, the silicon substrate is a bulk substrate. Other type of substrate suitable to implement this invention includes silicon on insulator (SOI).

[**0028**] Substrate **110** may be doped with a p-type or n-type dopants. The dopant concentration may vary from light to heavy as understood by a person with reasonable skill in the art of semiconductor processing.

[**0029**] Element **150** is a heavily doped semiconductor layer partially covering the substrate **110**. In this embodiment, layer **150** is formed by an arsenic or phosphorus implant step followed by a anneal step. In the art of semiconductor processing, this heavily doped region is referred to as "a buried layer".

[**0030**] Layer **200** sits on top of the buried layer. In this embodiment, layer **200** is an epitaxial, lightly doped, p-type mono-crystalline-silicon layer. The thickness of this epi-layer may be between 2000 Å and 7000 Å, preferably about 5000 Å. Layer **200** may be doped in-situ. It may also be doped with a boron implant with a dose between 5×10^{9} to 5×10^{11} ions/cm^2, to a dopant concentration of about 1×10^{15} ions/cm^3.

[**0031**] Layer **200** also includes regions of dielectric material to insulate the JFET electrically from the adjacent circuit elements. The dielectric regions **220** are places in the layer **200** such that the JFET is formed in a mono-crystalline silicon island **210**. In this embodiment, the dielectric material is silicon dioxide and the technique with which the silicon dioxide regions are formed is referred to in the art as the shallow trench isolation (STI) technique.

[**0032**] **FIG. 4** depicts a cross-sectional view of a further partially completed JFET **10**. Features depicted in **FIG. 4** include a layer element **300**. In this embodiment, layer **300** is another lightly doped, p-type, silicon-epi-layer. The thickness of layer **300** may be between 1000 Å and 3000 Å, preferably 2000 Å. Layer **300** may be doped in-situ or it maybe doped with a boron implant with dose between 5×10^{9} and 5×10^{11} ions/cm^2, preferably to a dopant concentration of about 1×10^{15} ions/cm^3.

[**0033**] The portion of epi-layer **300** that is in contact with element **210** is mono-crystalline while the portion that contacts element **220** is poly-crystalline.

[**0034**] **FIG. 5** depicts a cross-sectional view of yet a further partially completed JFET **10** embodying this invention. Features depicted in **FIG. 5** include a region **350** enclosed in the region **210**, and a layer **400** that comprises a patterned photoresist layer **430**, a silicon nitride layer **420**, and a silicon dioxide layer **410**. The nitride and oxide layers are depicted in **FIG. 5** as after a portion, uncovered by the photoresist pattern **430**, has been removed by an etching technique well known in the art of semiconductor processing. The etched portion includes a region **415**. Instead of a silicon-nitride, silicon oxide layer combination in layer **400**, the JFET may also be fabricated by using a single oxide layer, or nitride layer, or oxynitride layer.

[**0035**] The region **350** is the n-channel region of the JFET, it maybe formed by implanting n-type ions into region **210** through the opening **415**. In this embodiment, the channel is formed with a three-step ion-implant process. One implant is at 200 keV, another implant is at 340 keV, and another implant is at 500 keV. Dosages of phosphorus ions that may range from 2×10^{9} to 4×10^{11} ions/cm^2 per implant are used in the 3-step implant—with the higher energy implants typically associate with higher doses. Other n-type ion species

and implant dosages and energies may also be used to tailor the channel doping profile to suit specific circuit requirement.

[0036] **FIG. 6** depicts a cross-sectional view of yet a further partially completed JFET **10** embodying this invention. Features depicted in **FIG. 6** include a layer element **500**. In this embodiment, the layer **500** is polysilicon, with a thickness between 1 kÅ and 3 kÅ. At the vicinity of opening **415**, where layer **500** contacts channel **350**, the crystal may follow the structure of the channel region and remains mono-crystalline.

[0037] **FIG. 6** also depicts a photoresist pattern **510**. This pattern defines the source electrode area and the gate electrode area, as will be further illustrated in **FIG. 7**.

[0038] **FIG. 7** depicts a cross-sectional view of yet a further partially completed JFET **10** embodying this invention. Features depicted in **FIG. 7** include a source element **450**, a gate element **320**, and sidewall elements **460** and **470**.

[0039] In this embodiment, the source element **450** and the gate element **320** are formed with a poly etch process well known in the art of semiconductor processing. The etching action removes the portion of layer **500** that is not protected by the photoresist pattern **510** and the portion of layer **300** that is not protected by oxide element **410** and nitride element **420**. Element **470** and element **460** are referred in the art of semiconductor processing as the sidewalls. They are formed by a technique combining a film deposition and a film etching. The etching action not only removes the newly deposited film but also a portion of the oxide element **410** and nitride element **420** that is not covered by the source element **450** or the sidewall elements **460** and **460**. At the completion of the etching process, the silicon surfaces of the source element **450** and the gate element **320** are uncovered.

[0040] **FIG. 7** also depicts the source and gate implant processes. In this embodiment, the gate-implant species is boron, the dose is 3×10^{15} ions/cm^2, and the implant energy is 20 keV. The source implant species is arsenic, the dose is 1.5×10^{15} ions/cm^2, and the implant energy is 50 keV. Other implant species, dosages and energies maybe used to effect low resistivity in the source and gate-poly-regions.

[0041] Contrary to conventional JFETs, as depicted in **FIGS. 1***a,* **1***b,* and **1***c,* which have their channel substantially parallel and proximate to the top surface of the semiconductor substrate, the JFET embodying this invention has a "vertical" channel.

[0042] It is well known in the art of semiconductor physics that the top surface of the semiconductor substrate is heavily populated with imperfections such as charge traps and surface states. The interaction between the charge carrier in the channel and the surface imperfections is partially responsible for the performance limitation of conventional semiconductor devices in which the current flows parallel to and near the surface.

[0043] In contrast, the "vertical" channel in the present invention channels the flow of the charge carriers in a direction substantially perpendicular to the "surface" of the semiconductor surface. Thus the interaction between the charge carrier and the surface imperfection is substantially reduced, which enables the JFETs embodying this invention to have superior cutoff frequency (f_{co}) and 1/f noise figure.

1-23. (canceled)

24. An method for making an electronic device, comprising

a. providing a semiconductor substrate of a first conductivity, having a top surface and a bottom surface;

b. forming a buried layer of a second conductivity near the top surface;

c. forming a first semiconductor-layer over the buried layer, doping the region with dopant of the first conductivity;

d. forming in the first layer insulation regions that isolate an island of the first-layer material, the insulation regions having substantially the same thickness as the first layer so the insulation regions reaches the buried layer;

e. forming a second semiconductor-layer of the first conductivity over the first semiconductor-layer and the insulation regions, portions of the second layer over the insulation regions being polycrystalline, portions of the second layer over the first layer being mono-crystalline;

f. forming a dielectric layer over the second layer;

g. implanting dopant of the second conductivity into the island of the first semiconductor layer to form a channel-region in the first and the second semiconductor-layer that reaches the buried layer;

h. forming a third semiconductor-layer of the second conductivity over the dielectric layer;

i. patterning and etching the third semiconductor-layer and the dielectric layer to form a gate structure and uncovering a portion of the second semiconductor-layer; and

j. implanting dopant of the first conductivity into the uncovered second semiconductor-regions to form a gate structure.

25. The method in claim 24, in which the semiconductor substrate is silicon.

26. The method in claim 24, in which the insulation regions comprise silicon dioxide formed with a STI technique.

27. The method in claim 24, in which the first semiconductor layer is about 0.5 micrometers thick and the second semiconductor layer is about 0.2 micrometers thick.

28. The method in claim 24, in which the dielectric layer comprises silicon dioxide and silicon nitride.

29. The method in claim 24, in which the implanting into the first semiconductor layer comprises three implant energies and three implant dosages.

30. The method in claim 24, in which a portion of the dopant implanted into the gate structure diffuses into the mono-crystalline portion of the second semiconductor layer.

31. The method in claim 24, in which the first conductivity is p-type.

32. The method in claim 24, in which the first conductivity is n-type.

33. A method for making an n-channel silicon JFET, comprising

a. providing a p-type silicon substrate, having a top surface and a bottom surface;

b. forming a buried layer of mono-crystalline silicon near the top surface, doped with a n-type dopant to a sheet resistance of about 25 ohms per square;

c. forming a 0.5 micrometers silicon mono-crystalline first layer over the buried layer, doping the region with p-type dopant to a concentration of about 1×10^{15} dopant ions per cubic centimeter;

d. forming in the first layer insulation regions that isolate islands of the first-layer material, the insulation regions having substantially the same thickness as the first layer so the insulation regions contact the buried layer;

e. forming a 0.2 micrometer silicon second layer over the first layer and the insulation regions, portions of the second layer over the insulation regions being poly-crystalline silicon, portions of the second layer over the first layer being mono-crystalline silicon, doping the second layer with p-type dopant to a concentration of about 1×10^{15} dopant ions per cubic centimeter;

f. forming a dielectric layer of silicon dioxide and silicon nitride over the second layer;

g. patterning and etching the dielectric layer to form a opening region free of the dielectric material over the second layer;

h. implanting n-type dopant through the opening region to form a n-type channel-region that reaches the buried layer;

i. forming a third n-type silicon layer over the dielectric layer;

j. patterning and etching the third silicon layer and the dielectric layer to form a source structure and uncovering a portion of the second silicon layer; and

k. implanting p-type dopant into the uncovered second-silicon regions to form a gate structure.

* * * * *