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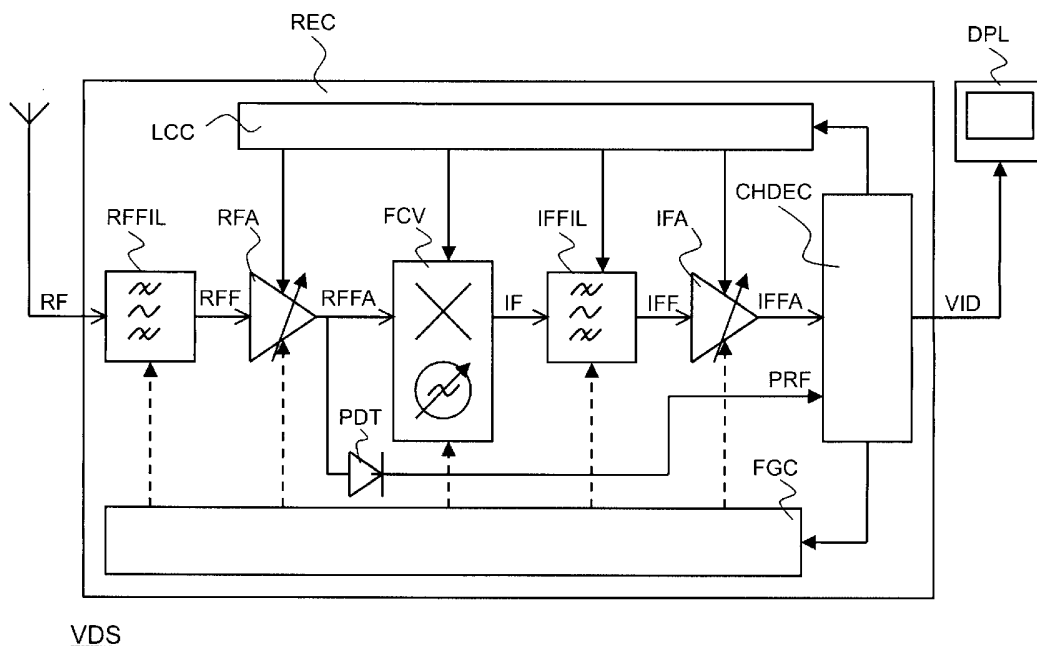
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(54) Title: SIGNAL PROCESSING ARRANGEMENT WITH POWER CONSUMPTION CONTROL



(57) Abstract: A signal processing arrangement (REC) comprises a signal processing circuit (IFA) having a power consumption that is controllable and a degree of linearity that depends on the power consumption. A signal-strength ratio detection (CHDEC, PDT) detects a signal-strength ratio that represents the ratio between the strength of a desired signal present at an input of the signal processing circuit (IFA) and the strength of other signals present at the input. A controller (CHDEC, LCC) controls the power consumption of the signal processing circuit as a function of the signal-strength ratio.

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## Signal processing arrangement with power consumption control

## FIELD OF THE INVENTION

An aspect of the invention relates to a signal processing arrangement that comprises a signal processing circuit having a power consumption that is controllable. The signal processing arrangement may be, for example, a receiver for processing a radio  
5 frequency signal that conveys information in the form of audio, video, or data or any combination of those. Other aspects of the invention relate to a signal processing method, a computer program product for a signal processing arrangement as mentioned hereinbefore, and an information-rendering apparatus that comprises such a signal processing arrangement. The information-rendering apparatus may be, for example, a video display set.

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## BACKGROUND OF THE INVENTION

United States patent 6,498,926 describes a receiver that minimizes power consumption based on measurement of the non-linearity in the output signal from the receiver. The amount of non-linearity is measured by the received signal strength indicator  
15 (RSSI) slope. The RSSI slope is the ratio of the change in the output signal plus intermodulation to the change in the input signal. The input signal level is periodically increased by a predetermined level and the output signal from the receiver is measured. The output signal comprises the desired signal and intermodulation products from non-linearity within the receiver. When the receiver is operating linearly, the output signal level increases  
20 dB per dB with the input signal level. However, as the receiver transitions into non-linear region, intermodulation products due to non-linearity increase faster than the desired signal. By detecting the RSSI slope, the amount of degradation due to non-linearity can be determined. This information is then used to adjust the IIP3 operating point of the amplifiers and mixer to provide the requisite level of performance while minimizing power  
25 consumption.

## SUMMARY OF THE INVENTION

The invention is defined by the independent claims. The dependent claims define advantageous embodiments.

According to an aspect of the invention, a signal processing arrangement has the following characteristics. The signal processing arrangement comprises a signal processing circuit having a power consumption that is controllable and a degree of linearity that depends on the power consumption. A signal-strength ratio detector detects a signal-strength ratio that represents the ratio between the strength of a desired signal present at an input of the signal processing circuit and the strength of other signals present at the input. A controller controls the power consumption of the signal processing circuit as a function of the signal-strength ratio.

The invention takes the following aspects into consideration. A signal processing circuit that is nonlinear to a certain extent may generate spurious signals that interfere with a desired signal. The amount of interference depends on the ratio between the signal strength of the desired signal and that of other signals, which accompany the desired signals. The stronger the other signals are with respect to the desired signal, the more linear the signal processing circuit needs to be in order to ensure a satisfactory signal-to-interference ratio.

In accordance with the aforementioned aspect of the invention, a signal-strength ratio detector detects a signal-strength ratio that represents the ratio between the strength of a desired signal present at an input of the signal processing circuit and the strength of other signals present at the input. A controller controls the power consumption of the signal processing circuit as a function of the signal-strength ratio.

In case that the desired signal is relatively strong with respect to the other signals, the power consumption can be relatively low because a modest degree of linearity will be sufficient to ensure a satisfactory signal-to-interference ratio. In case that the desired signal is relatively weak with respect to the other signals, a relatively high power consumption will be required to ensure a satisfactory signal-to-interference ratio. The invention therefore allows an appropriate adaptation of power consumption that ensures a satisfactory signal-to-interference ratio. Consequently, the invention allows a reduction of power consumption while ensuring signal quality.

An advantage of the invention with respect to the prior art receiver relates to the following aspects. The prior art receiver requires that a circuit whose power consumption is controlled, operates in a nonlinear region or relatively close thereto. Only in that case a signal-distortion measurement can be made, on which measurement the power consumption control is based. The prior art receiver can be regarded to operate in a re-active fashion: some

damage has first to be produced in order to control the damage. By definition, no control is possible unless there is certain damage.

The invention can be considered as a proactive approach. The invention anticipates, as it were, interference on the basis of the detected signal-strength ratio. The invention does not require measurement of interference itself. Therefore, the invention does not require the signal processing circuit to operate in a nonlinear region, contrary to the prior art receiver. Consequently, the invention allows better signal processing quality compared with the prior art receiver.

These and other aspects of the invention will be described in greater detail hereinafter with reference to drawings.

#### BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a block diagram that illustrates a video display set.

Fig. 2A, 2B, and 2C are frequency diagrams that illustrate an intermediate frequency spectrum, an intermediate frequency filter characteristic, and a filtered intermediate frequency spectrum, respectively.

Fig. 3 is a block diagram that illustrates a channel decoder that forms part of the video display set.

Fig. 4 is a flow chart diagram that illustrates operations that the channel decoder carries out.

Fig. 5 is a circuit diagram that illustrates an amplifier having a power consumption that is controllable and a degree of linearity that depends on the power consumption.

#### DETAILED DESCRIPTION

Fig. 1 illustrates a video display set VDS that comprises a receiver REC and a display device DPL. The receiver REC receives a radio frequency spectrum RF and retrieves a video signal VID from a desired signal within the radio frequency spectrum RF. The display device DPL displays the video signal VID.

The receiver REC comprises a radio frequency filter RFFIL, a radio frequency amplifier RFA, a frequency converter FCV, an intermediate frequency filter IFFIL, an intermediate frequency amplifier IFA, and a channel decoder CHDEC. The aforementioned elements constitute a signal processing path that derives the video signal VID from the radio frequency spectrum RF received. The receiver REC further comprises a biasing control

circuit LCC, a signal-strength detector PDT, and a frequency and gain control circuit FGC. These elements, together with the channel decoder CHDEC, control the various elements of the signal processing path.

The radio frequency filter RFFIL filters the radio frequency spectrum RF received. Accordingly, a filtered radio frequency spectrum RFF is obtained, which the radio frequency amplifier RFA receives at an input. The radio frequency amplifier RFA amplifies the filtered radio frequency spectrum RFF. Accordingly, a filtered and amplified radio frequency spectrum RFFA is obtained, which the frequency converter FCV receives at an input. In effect, the frequency converter FCV shifts the filtered and amplified radio frequency spectrum RFF in frequency. Accordingly, an intermediate frequency spectrum IF is obtained, which the intermediate frequency filter IFFIL receives at an input. The intermediate frequency filter IFFIL filters the intermediate frequency spectrum IF. Accordingly, a filtered intermediate frequency spectrum IFF is obtained, which the intermediate frequency amplifier IFA receives at an input. The intermediate frequency amplifier IFA amplifies the filtered intermediate frequency spectrum IFF. Accordingly, a filtered and amplified intermediate frequency spectrum IFFA is obtained, which the channel decoder CHDEC receives at an input. The channel decoder CHDEC further receives a radio frequency signal-strength indication PRF from the signal-strength detector PDT, which measures the power of the filtered and amplified radio frequency spectrum RFFA.

The channel decoder CHDEC carries out several main functions. The channel decoder CHDEC derives the video signal VID from the filtered and amplified intermediate frequency spectrum IFFA. The channel decoder CHDEC further derives commands for the biasing control circuit LCC and the frequency and gain control circuit FGC. On the basis of these commands, the biasing control circuit LCC and the frequency and gain control circuit FGC control the various elements of the signal processing path, which includes the radio frequency amplifier RFA, the frequency converter FCV, the intermediate frequency filter IFFIL, and the intermediate frequency amplifier IFA. This will be explained in greater detail hereinafter.

Fig. 2A illustrates the intermediate frequency spectrum IF. The horizontal axis represents frequency  $F$ , the vertical axis represents signal strength  $P_s$ . There are several small frequency bands, or channels, within the intermediate frequency spectrum IF: a desired channel CC, a first lower adjacent channel LC1, a first upper adjacent channel UC1, a second upper adjacent channel UC2, and a third upper adjacent channel UC3. FIG. 2A illustrates that several signals  $S_1, \dots, S_5$  are present within the intermediate frequency spectrum IF. Signal  $S_1$

lies within the first lower adjacent channel LC1, signal S2 lies within the desired channel CC, signal S3 lies within the first upper adjacent channel UC1, signal S4 lies within the second upper adjacent channel UC2, signal S5 lies within the third upper adjacent channel UC3.

Signal S2, which lies in the desired channel CC, is the desired signal. The other signals S1, S3, S4, and S5 can be regarded as unwanted signals. However, it should be noted that the receiver REC can be tuned differently so that, for example, signal S3 lies within the desired channel CC. In that case, signal S3 is the desired signal and signal S2 is within the first lower adjacent channel LC1 and can then be regarded as an unwanted signal.

Fig. 2B illustrates the characteristics of the intermediate frequency filter IFFIL. The horizontal axis represents frequency F, the vertical axis represents the amplitude characteristic A of the intermediate frequency filter IFFIL. The intermediate frequency filter IFFIL has a pass band that coincides with the desired channel CC. The intermediate frequency filter IFFIL attenuates a signal that lies within in an adjacent channel to a certain extent. The further the adjacent channel is located from the desired channel CC, the greater the attenuation will be.

Fig. 2C illustrates the filtered intermediate frequency spectrum IFF. The filtered intermediate frequency spectrum IFF results from the filter characteristic illustrated in Fig. 2B applied to the intermediate frequency spectrum IF illustrated in Fig. 2A. The filtered intermediate frequency spectrum IFF comprises filtered signals Sf1, ..., Sf5, which are the filtered versions of the signals S1, ..., S5, respectively, illustrated in Fig. 2A.

Fig. 3 illustrates the channel decoder CHDEC. The channel decoder CHDEC comprises an analog-to-digital converter ADC and a digital signal processor DSP. The analog-to-digital converter ADC provides the digital signal processor DSP with a digital representation of the filtered and amplified intermediate frequency spectrum IFFA. The digital signal processor DSP carries out various functions: a channel filtering CHFIL, a demodulation DEM, a frequency spectrum analysis FSPA, a linearity control adjustment LCCA, and a frequency and gain control adjustment FGCA. These functions, which are illustrated as rectangles in Fig. 3, may be implemented in various different manners. The digital signal processor DSP may comprise, for example, a dedicated circuit that carries out a specific function. This can be regarded as a hardware-based implementation. Alternatively, the digital signal processor DSP may comprise a central processing unit that is programmed to carry out various different functions. This can be regarded as a software-based implementation. There are numerous other implementations that can be regarded as a mix of the hardware-based implementation and the software-based implementation.

The channel filtering CHFIL provides a sharp bandpass filter whose pass band has a width that corresponds with any of the channels illustrated in Figs. 2A-2C. The sharp bandpass filter has an amplitude characteristic with relatively steep slopes. Accordingly, the channel filtering CHFIL attenuates to a relatively great extent any signal outside the pass band of the sharp bandpass filter. In order to retrieve the video signal, the channel filtering CHFIL tunes the sharp bandpass filter to the desired channel. Any signal that lies within another channel will be attenuated to a relatively great extent. Referring to Fig. 2C, the channel filtering CHFIL will substantially eliminate the signals Sf1, Sf3, Sf4, and Sf5. Only the signal Sf2 will remain. The digital signal processor DSP then applies the demodulation DEM to signal Sf2 so as to retrieve the video signal VID there from.

Fig. 4 illustrates the frequency spectrum analysis FSPA and the linearity control adjustment LCCA that the channel decoder CHDEC carries out. Steps ST1-ST4 correspond to the frequency spectrum analysis FSPA. Steps ST5-ST8 correspond to the linearity control adjustment LCCA.

In steps ST1-ST4, the channel decoder CHDEC measures the signal strength in each channel within a range of channels. The range of channels may be, for example, comprised between a fifth upper adjacent channel UC5 and a fifth lower adjacent channel LC5, including those channels. Step ST1 is an initialization step. The fifth upper adjacent channel UC5, which constitutes the upper boundary, is set to be a current channel ( $CH = UC5$ ). Steps ST2-ST4 constitute a loop. Steps ST2-ST4 are carried out for each channel that is within the range of channels. In step ST2, the signal strength within the current channel is measured ( $P_s$  ?). This measurement may make use of, for example, the sharp bandpass filter that the channel filtering CHFIL provides. The sharp bandpass filter can be tuned to the current channel so as to eliminate any signal in any other channel.

In step ST3, it is checked whether the current channel is the fifth lower adjacent channel LC5, which constitutes the lower boundary ( $CH = LC5$  ?). Step ST4 is carried out if the fifth lower adjacent channel LC5 is not the current channel. In step ST4, the current channel is set to be the lower neighbor of the channel for which steps ST2 and ST3 have most recently been carried out ( $NXT\ CH = CH - 1$ ). The steps ST2-ST4 are carried out anew. The frequency spectrum analysis FSPA is completed when, in step ST3, it is found that the fifth lower adjacent channel LC5 is the current channel. In that case, the channel decoder CHDEC leaves the loop and proceeds to carry out step ST5, which constitutes the start of the linearity control adjustment LCCA. In steps ST1-ST4, the channel decoder CHDEC thus scans at least a portion of the filtered and amplified intermediate frequency spectrum IFFA,

which is illustrated in Fig. 1, so as to measure the signal strength in each channel that is included in the scan.

In step ST5, the channel decoder CHDEC calculates various signal signal-strength ratios within the filtered intermediate frequency spectrum IFF (CAL(SPR@IFF)), the intermediate frequency spectrum IF (CAL(SPR@IF)), the filtered and amplified radio frequency spectrum RFFA (CAL(SPR@RFFA)), and the filtered radio frequency spectrum RFF (CAL(SPR@RFF)). It should be noted that the channel decoder CHDEC cannot directly scan these frequency spectra. The channel decoder CHDEC can scan the filtered and amplified intermediate frequency spectrum IFFA only. Nevertheless, the channel decoder CHDEC can relatively easily determine respective signal signal-strength ratios in the aforementioned other spectra. For example, the intermediate frequency amplifier IFA provides a signal gain that determines the relation between the filtered and amplified intermediate frequency spectrum IFFA and the filtered intermediate frequency spectrum IFF. The channel decoder CHDEC is involved in controlling this signal gain and, therefore, knows the signal gain that the intermediate frequency amplifier IFA provides. The channel decoder CHDEC may also know the amplitude characteristic of the intermediate frequency filter IFFIL, which is illustrated in Fig. 2B. The amplitude characteristic of the intermediate frequency filter IFFIL may be stored, for example, in a nonvolatile memory that forms part of the channel decoder CHDEC. Accordingly, the channel decoder CHDEC can determine signal signal-strength ratios in the intermediate frequency spectrum IF, which is illustrated in Fig. 2A.

The following example illustrates the aforementioned. Reference is made to Figs. 2A-2C. Let it be assumed, for example, that the intermediate frequency filter IFFIL provides 3 dB attenuation in the desired channel CC and 33 dB attenuation in the first upper adjacent channel UC1. Consequently, the intermediate frequency filter IFFIL attenuates signal S3 in the first upper adjacent channel UC1 30 dB with respect to signal S2 in the desired channel CC. Let it further be assumed that filtered signal Sf3 is 5 dB stronger in terms of signal strength than filtered signal Sf2. That is, the signal signal-strength ratio between these signals is -5dB. The channel decoder CHDEC can relatively easily calculate the signal signal-strength ratio between signal S2 and signal S3 in the intermediate frequency spectrum IF. The channel decoder CHDEC subtracts 30dB from the signal signal-strength ratio of the corresponding filtered signals Sf2 and Sf3 in the filtered intermediate frequency spectrum IFF. The signal signal-strength ratio in the intermediate frequency spectrum IF is thus  $-30-5 = -35$  dB. The signal signal-strength ratio in the filtered radio frequency spectrum

RFF and the filtered and amplified radio frequency spectrum RFFA will substantially be similar. This is because the frequency converter FCV and the radio frequency amplifier RFA, which are illustrated in Fig. 1, do not significantly filter signals compared with the intermediate frequency filter IFFIL.

5                   In step ST5, the channel decoder CHDEC thus determines respective signal strengths of the signals S1, ..., S5 in the intermediate frequency spectrum IF, which is illustrated in Fig. 2C. The channel decoder CHDEC calculates, for example, the ratio between the signal strength of signal S2 and that of signals S3 and S4. The channel decoder CHDEC can calculate signal signal-strength ratios for the corresponding signals in the  
10 filtered and amplified radio frequency spectrum RFFA and the filtered radio frequency spectrum RFF.

                  In step ST6, the channel decoder CHDEC calculates a degree of linearity that the intermediate frequency amplifier IFA should have in order that any interference is at an acceptable level ( $CAL(LIN@IFA)$ ). The intermediate frequency amplifier IFA receives the  
15 filtered intermediate frequency spectrum IFF, which is illustrated in Fig. 2C. A third-order nonlinearity of the intermediate frequency amplifier IFA will cause signals Sf3 and Sf4 to produce intermodulation products that will fall in the desired channel CC. Consequently these intermodulation products will interfere with the desired signal, which is signal Sf2. The third-order intercept point is a figure of merit for the third-order nonlinearity of the circuit.  
20 The higher the third-order intercept point is, the lower the interference due to intermodulation products will be. The interference further depends on the signal signal-strength ratio between signal Sf2 and signals Sf3 and Sf4, which has been calculated in step ST5. The channel decoder CHDEC calculates the third-order intercept point that the intermediate frequency amplifier IFA needs to have in order that the interference is at an acceptable level.

25                   In step ST6, the channel decoder CHDEC carries out similar calculations for the intermediate frequency filter ( $CAL(LIN@IFFIL)$ ), the frequency converter ( $CAL(LIN@FCV)$ ), and the radio frequency amplifier ( $CAL(LIN@RFA)$ ). These calculations are based on signal signal-strength ratios in the intermediate frequency spectrum IF, the filtered and amplified radio frequency spectrum RFFA, and the filtered radio  
30 frequency spectrum RFF, respectively.

                  It should be noted that the degree of linearity that is required not only depends on the relative strength of signals other than the desired signal, but also depends on the respective frequencies of those signals. As mentioned hereinbefore, signals S3 and S4, which are illustrated in Fig. 2A, may produce certain interference in the desired channel CC. Signals

S4 and S5 may also produce certain interference. However, the latter interference will generally be lower compared with the interference that signals S3 and S4 produce for a given degree of linearity. Referring to Fig. 2A, let it be assumed that signal S3 is absent: there is no significant signal within the first upper adjacent channel UC1. Let it further be assumed that a signal comparable to signal S3 is present in a fourth upper adjacent channel, which is not shown in Fig. 2A. In that case, a lower degree of linearity is sufficient compared with the example illustrated in Fig. 2A, although the sum of the respective signal strengths of the other signals is similar in both cases. The channel decoder CHDEC preferably takes into consideration the respective frequencies of the signals other than the desired signal in calculating the required degree of linearity.

In step ST7, the channel decoder CHDEC calculates the control parameter that needs to be applied to the intermediate frequency amplifier IFA in order that the intermediate frequency amplifier IFA has the required degree of linearity ( $CAL(CP@IFA)$ ). The channel decoder CHDEC can carry out this calculation on the basis of, for example, a table that defines a relationship between the degree of linearity of the intermediate frequency amplifier IFA and the control parameter. This table can be stored in a nonvolatile memory. The channel decoder CHDEC carries out similar calculations for the intermediate frequency filter ( $CAL(CP@IFFIL)$ ), the frequency converter ( $CAL(CP@FCV)$ ), and the radio frequency amplifier ( $CAL(CP@RFA)$ ). Accordingly, the channel decoder CHDEC establishes the control parameter that needs to be applied to each of these elements in the signal processing path.

In step ST8, the channel decoder CHDEC issues commands to the biasing control circuit LCC. Each command concerns a specific element in the signal processing path: the intermediate frequency amplifier IFA, the intermediate frequency filter IFFIL, the frequency converter FCV, or the radio frequency amplifier RFA. The command instructs the biasing control circuit LCC to apply to the relevant element, the control parameter that the channel decoder CHDEC has calculated. For example, the channel decoder CHDEC issues a command to the biasing control circuit LCC that concerns the radio frequency amplifier RFA ( $CMD(CP@RFA) \rightarrow LCC$ ). In response to this command, the biasing control circuit LCC will apply to the radio frequency amplifier RFA the control parameter that the channel decoder CHDEC has calculated for this element. This will cause the radio frequency amplifier RFA to have the required degree of linearity in view of the filtered radio frequency spectrum RFF that the radio frequency amplifier RFA receives at its input. The same applies to the other

elements in the signal processing path (CMD(CP@FCV) → LCC, CMD(CP@IFFIL) → LCC, CMD(CP@IFA) → LCC).

The biasing control circuit LCC may comprise, for example, various registers and digital-to-analog converters. A register and a digital-to-analog converter may specifically  
5 be assigned to an element in the signal processing path. The command, which the channel decoder CHDEC issues, may comprise, for example, a binary value. The binary value represents the value of the control parameter that should be applied to the element concerned. The value is stored in the register. The digital-to-analog converter converts the value that is present in the register into an analog control voltage or current. The biasing control circuit  
10 LCC applies the analog control voltage or current to the element concerned.

The channel decoder CHDEC may take into account the radio frequency signal-strength indication PRF that the signal-strength detector PDT provides as illustrated in FIG. 1. The radio frequency signal-strength indication PRF allows the channel decoder CHDEC to determine whether there are relatively strong signals, or not, outside the range of  
15 channels throughout which the scan has been made in steps ST1-ST4. The channel decoder CHDEC can account for the presence of such strong signals in the steps ST5-ST8. For example, the channel decoder CHDEC may increase the required degree of linearity of the various elements in the signal processing path in case the radio frequency signal-strength indication PRF indicates that there are one or more relatively strong signals outside the  
20 scanning range. However, it should be noted the channel decoder CHDEC can provide a satisfactory linearity control without the radio frequency signal-strength indication PRF. That is, the signal-strength detector PDT may be omitted so as to simplify the receiver illustrated in Fig. 1.

In an alternative embodiment, the channel decoder CHDEC does not carry out  
25 the frequency spectrum analysis FSPA. The channel decoder CHDEC measures the signal strength in the desired channel CC only. The channel decoder CHDEC calculates a signal-strength ratio on the basis of the signal strength in the desired channel CC and the radio frequency signal-strength indication PRF that the signal-strength detector PDT provides. The radio frequency signal strength will be relatively high if there are one or more strong adjacent  
30 channel signals, whereas the radio frequency signal strength will be relatively low if adjacent channel signals are relatively weak or even absent. In the first case, the channel decoder CHDEC will instruct the biasing control circuit LCC to control the radio frequency amplifier RFA and the frequency conversion circuit FCV so that these circuits have a relatively high degree of linearity.

The frequency and gain control adjustment FGCA, which the channel decoder CHDEC carries out as illustrated in Fig. 3, preferably comprises a narrowband automatic gain control. The narrowband automatic gain control adjusts respective gains of the radio frequency amplifier RFA, the frequency converter FCV, and the intermediate frequency amplifier IFA on the basis of the signal strength within the desired channel. The narrowband automatic gain control seeks to adjust the respective gains so that the signal strength within the desired channel in the filtered and amplified intermediate frequency spectrum IFFA is at a predetermined level. This allows a satisfactory noise performance. The respective gains will be relatively high if the desired channel in the radio frequency spectrum RF received comprises a relatively weak signal. The receiver REC will have a relatively good noise figure in that case. Conversely, the respective gains will be relatively low if the desired channel in the radio frequency spectrum RF received comprises a relatively strong signal. A relatively good noise figure is not needed in that case. Since the respective gains will be relatively low, internal signals will have relatively modest magnitudes, which prevents overload.

It is possible to establish a signal-strength ratio in a relatively simple manner in case the frequency and gain control adjustment FGCA comprises the aforementioned narrowband automatic gain control. As mentioned hereinbefore, the narrowband automatic gain control causes the signal strength within the desired channel to be at a predetermined level, at least under normal reception conditions. Consequently, there is no need to measure this signal strength. It is sufficient to establish the signal strength within channels other than the desired channel. This can be done on the basis of the radio frequency signal-strength indication PRF that the signal-strength detector PDT provides. In effect, radio frequency signal-strength indication PRF is the sum of the signal strength within the desired channel and the signal strength within the other channels.

The frequency and gain control adjustment FGCA preferably combines the narrowband automatic gain control with a wideband automatic gain control that prevents overload if the radio frequency spectrum RF received comprises relatively strong signals. Such relatively strong signals, which may potentially cause overload, are often referred to as blockers. The wideband automatic gain control may be based on, for example, the radio frequency signal-strength indication PRF that the signal-strength detector PDT provides. The frequency and gain control adjustment FGCA can define a blocker threshold, which the radio frequency signal-strength indication PRF should not exceed. The wideband automatic gain control is not active when the radio frequency signal-strength indication PRF is below the blocker threshold. The wideband automatic gain control may reduce the respective gains that

the radio frequency amplifier RFA and the frequency converter FCV provide if the radio frequency signal-strength indication is above the blocker threshold. In that case, the wideband automatic gain control overrules, as it were, the narrowband automatic gain control.

5                    Fig. 5 illustrates an amplifier AMP having a power consumption that is controllable and a degree of linearity that depends on the power consumption. The amplifier comprises a transistor Q1, first and second impedances Z1, Z2, first and second capacitors C1, C2, and a high-frequency decoupling coil CHK: a so-called choke. The amplifier further comprises an input I, an output O, and supply voltage connections VCC, GND. The transistor  
10 Q1 receives a biasing voltage Vb at its base via the choke CHK.

                    The amplifier AMP has a linear operating region that approximately corresponds to the product of the first impedance Z1 and a biasing current that flows through the transistor Q1 via its emitter and collector. The biasing current varies as a function of the biasing voltage Vb. Consequently, the amplifier AMP has a degree of linearity that varies as  
15 a function of the biasing voltage Vb. Let it be assumed that the biasing voltage Vb is relatively high. In that case, a relatively strong biasing current will flow through the transistor Q1 via its emitter and collector. The product of the first impedance Z1 and the biasing current is relatively large so that the linear operating region is relatively large. Conversely, the  
amplifier AMP will have relatively small linear operating region if the biasing voltage Vb is  
20 relatively low.

                    The amplifier AMP, which is illustrated in Fig. 5, is an example of the following general rule. A relatively high degree of linearity requires relatively a high power consumption. Conversely, power consumption can be relatively low if a relatively low degree of linearity is sufficient.

25                    Let it be assumed that, in the receiver illustrated in Fig. 1, the intermediate frequency spectrum IF is as shown in Fig 2A. In that case, the channel decoder CHDEC will detect a relatively small signal signal-strength ratio: the desired signal is accompanied by other signals that are relatively strong. Consequently, the channel decoder CHDEC will issue a command that indicates that the radio frequency amplifier RFA should have a relatively a  
30 high degree of linearity. The biasing control circuit LCC will control the radio frequency amplifier RFA accordingly. Consequently, the radio frequency amplifier RFA will have relatively high power consumption. The same applies to the other elements in the signal processing path: the frequency converter FCV, the intermediate frequency filter IFFIL, and,

to a lesser extent, the intermediate frequency amplifier IFA. Overall, the receiver will have relatively high power consumption.

Let it now be assumed that the intermediate frequency spectrum IF comprises a signal within the desired channel CC only. There are no adjacent signals. The channel decoder CHDEC will detect a relatively large signal signal-strength ratio: signals other than the desired signal that are relatively weak. Accordingly, the channel decoder CHDEC will calculate a required degree of linearity that is relatively modest. The channel decoder CHDEC will thus issue a command that indicates that the radio frequency amplifier RFA may have a modest degree of linearity. The biasing control circuit LCC will control the radio frequency amplifier RFA accordingly. The same applies to the other elements in the signal processing path: the frequency converter FCV, the intermediate frequency filter IFFIL, and the intermediate frequency amplifier IFA. Overall, the receiver REC will have relatively modest power consumption.

The detailed description hereinbefore with reference to the drawings illustrates the following characteristics. A signal processing arrangement (receiver REC) comprises a signal processing circuit (intermediate frequency amplifier IFA, for example) having a power consumption that is controllable and a degree of linearity that depends of the power consumption. A signal-strength ratio detector detects a signal-strength ratio that represents the ratio between the strength of a desired signal present at an input of the signal processing circuit and the strength of other signals present at the input (filtered intermediate frequency signal IFF, which is illustrated in Fig. 2C, is present at the input of the intermediate frequency amplifier IFA, Sf2 is the desired signal, Sf1, Sf3, Sf4, Sf5 are the other signals; channel decoder CHDEC, which carries out steps ST1-ST5 illustrated in FIG. 4, forms the signal-strength ratio detector, optionally in combination with radio frequency signal-strength detector PDT). A controller controls the power consumption of the signal processing circuit as a function of the signal-strength ratio (channel decoder CHDEC, which carries out steps ST6-ST8, forms the controller in combination with biasing control circuit LCC).

The detailed description hereinbefore further illustrates the following optional characteristics:

- The signal-strength ratio detector comprises a frequency spectrum analyzer (FSPA) arranged to measure signal strength at different frequencies. An advantage of this characteristic is that it allows a more accurate control, which allows further reduction in power consumption.

- The signal-strength ratio detector forms part of a channel decoder (CHDEC) coupled to receive an output signal from the signal processing circuit. An advantage of this characteristic is that it allows cost efficient implementations.

5 - The signal processing arrangement (receiver REC) comprises a filter (intermediate frequency filter IFFIL) for suppressing signals other than the desired signal. The signal-strength ratio detector (channel decoder CHDEC in combination with radio frequency signal-strength detector PDT) is arranged to measure signal strength at an input of the filter and to measure signal strength at an output of the filter. An advantage of this characteristic is that it allows detection of the signal-strength ratio with relatively simple  
10 hardware and software.

- The signal processing arrangement (receiver REC) comprises two signal processing circuits (radio frequency amplifier RFA, intermediate frequency amplifier IFA) each having a power consumption that is controllable. The controller (channel decoder CHDEC, biasing control circuit LCC) is arranged to individually control the power  
15 consumption of one and the other processing circuit. An advantage of this characteristic is that it allows a more accurate control, which allows further reduction in power consumption while ensuring a satisfactory signal-to-interference ratio.

- The controller (channel decoder CHDEC, linearity control circuit LLC) further controls the power consumption of the signal processing circuit (intermediate frequency  
20 amplifier IFA, for example) on the basis of the respective frequencies of the other signals with respect to the desired signal (see the description of step ST6 illustrated in FIG. 4). An advantage of this characteristic is that it allows a more accurate control, which allows further reduction in power consumption.

The aforementioned characteristics can be implemented in numerous different  
25 manners, which fall within the scope of the appended claims. In order to illustrate this, some alternatives are briefly indicated. The signal processor may comprise only a single processing circuit having a power consumption that is controllable. Referring to Fig. 1, the receiver REC may be modified so that the radio frequency amplifier RFA is the only element in the signal processing path whose power consumption is controlled. The amplifier illustrated in Fig. 5 is  
30 merely an example of a signal processing circuit having a power consumption that is controllable. The signal processing circuit may be in the form of, for example, a differential circuit having a controllable tail current. The linearity control circuit LLC and the channel decoder CHDEC may be replaced by a single circuit that performs the functions of the

aforementioned circuits. It is also possible to implement a dedicated circuit that carries out relevant detection and control functions but that does not form part of a channel decoder.

The signal-strength ratio detector can be implemented in numerous different manners. The detailed description hereinbefore merely provides a few examples. As another example, referring to Fig. 1, the receiver REC may be provided with various signal-strength detectors, each of which may be coupled to a different point in the signal processing path that extends between the radio frequency filter RFFIL and the channel decoder CHDEC. The biasing control circuit LCC may control respective elements in the signal processing path on the basis of respective output signals from the respective signal-strength detectors. In such an implementation, these respective signal-strength detectors form part of the signal-strength ratio detector, whereas the channel decoder CHDEC need not form part of the signal-strength ratio detector. The biasing control circuit LCC and the frequency and gain control circuit FGC may be combined into one single circuit that controls, for example, respective bias currents in the respective elements of the aforementioned signal processing path.

It should further be noted that the signal-strength ratio can be expressed in numerous different manners. For example, the signal-strength ratio can be expressed on a linear scale or on a logarithmic scale. The signal-strength ratio may be the quotient of the signal strength of the desired signal and that of one or more other signals. The signal strength ratio may also be the quotient of the signal strength of the desired signal and the signal strength of a combination of various different signals, which includes the desired signal and other signals.

There are numerous different manners to control power consumption in accordance with the invention. Adjusting a bias current, which has been explained with reference to Fig. 5, is merely an example. As another example, it is possible to control power consumption by adjusting a supply voltage. A circuit, which receives a supply voltage, generally has a degree of linearity that depends on the supply voltage. A supply voltage can be adjusted by means of, for example, a controllable voltage regulator, which may be in the form of a so-called DC/DC converter.

Functions may be implemented by means of items of hardware or software, or both. In this respect, the drawings are diagrammatic, each representing only one possible embodiment of the invention. Thus, although a drawing shows different functions as different blocks, this by no means excludes that a single item of hardware or software carries out several functions. Nor does it exclude that an assembly of items of hardware or software or both carry out a function.

The remarks made herein before demonstrate that the detailed description with reference to the drawings, illustrate rather than limit the invention. Any reference sign in a claim should not be construed as limiting the claim. The word "comprising" does not exclude the presence of other elements or steps than those listed in a claim. The word "a" or "an" preceding an element or step does not exclude the presence of a plurality of such elements or steps.

## CLAIMS:

1. A signal processing arrangement (REC) comprising:  
a signal processing circuit (IFA) having a power consumption that is controllable and a degree of linearity that depends on the power consumption;  
a signal-strength ratio detector (CHDEC, PDT) arranged to detect a signal-  
5 strength ratio that represents the ratio between the strength of a desired signal (Sf2) present at an input of the signal processing circuit and the strength of other signals (Sf1, Sf3, Sf4, Sf5) present at the input; and  
a controller (CHDEC, LCC) arranged to control the power consumption of the signal processing circuit as a function of the signal-strength ratio.  
10
2. A signal processing arrangement as claimed in claim 1, wherein the detector comprises a frequency spectrum analyzer (FSPA) arranged to measure signal strength at different frequencies.
- 15 3. A signal processing arrangement as claimed in claim 1, wherein the signal-strength ratio detector forms part of a channel decoder (CHDEC) coupled to receive an output signal from the signal processing circuit.
4. A signal processing arrangement as claimed in claim 1, wherein the signal  
20 processing arrangement comprises a filter (IFFIL) for suppressing signals other than the desired signal, the signal-strength ratio detector (CHDEC, PDT) being arranged to measure signal strength at an input of the filter and to measure signal strength at an output of the filter.
5. A signal processing arrangement as claimed in claim 1, wherein the signal  
25 processing arrangement (REC) comprises two signal processing circuits (RFA, IFA) each having a power consumption that is controllable, the controller (CHDET, LCC) being arranged to individually control the power consumption of one and the other processing circuit.

6. A signal processing arrangement as claimed in claim 1, wherein the controller (CHDEC) further controls the power consumption of the signal processing circuit (IFA) on the basis of the respective frequencies of the other signals (Sf1, Sf3, Sf4, Sf5) with respect to the desired signal (Sf2).

5

7. A signal processing method that employs a signal processing circuit (IFA) having a power consumption that is controllable and a degree of linearity that depends on the power consumption, the signal processing method comprising:

10 a detection step (ST1-ST5) in which a signal-strength ratio is detected that represents the ratio between the strength of a desired signal (Sf2) present an input of the signal processing circuit and the strength of other signals (Sf1, Sf3, Sf4, Sf5) present at the input; and

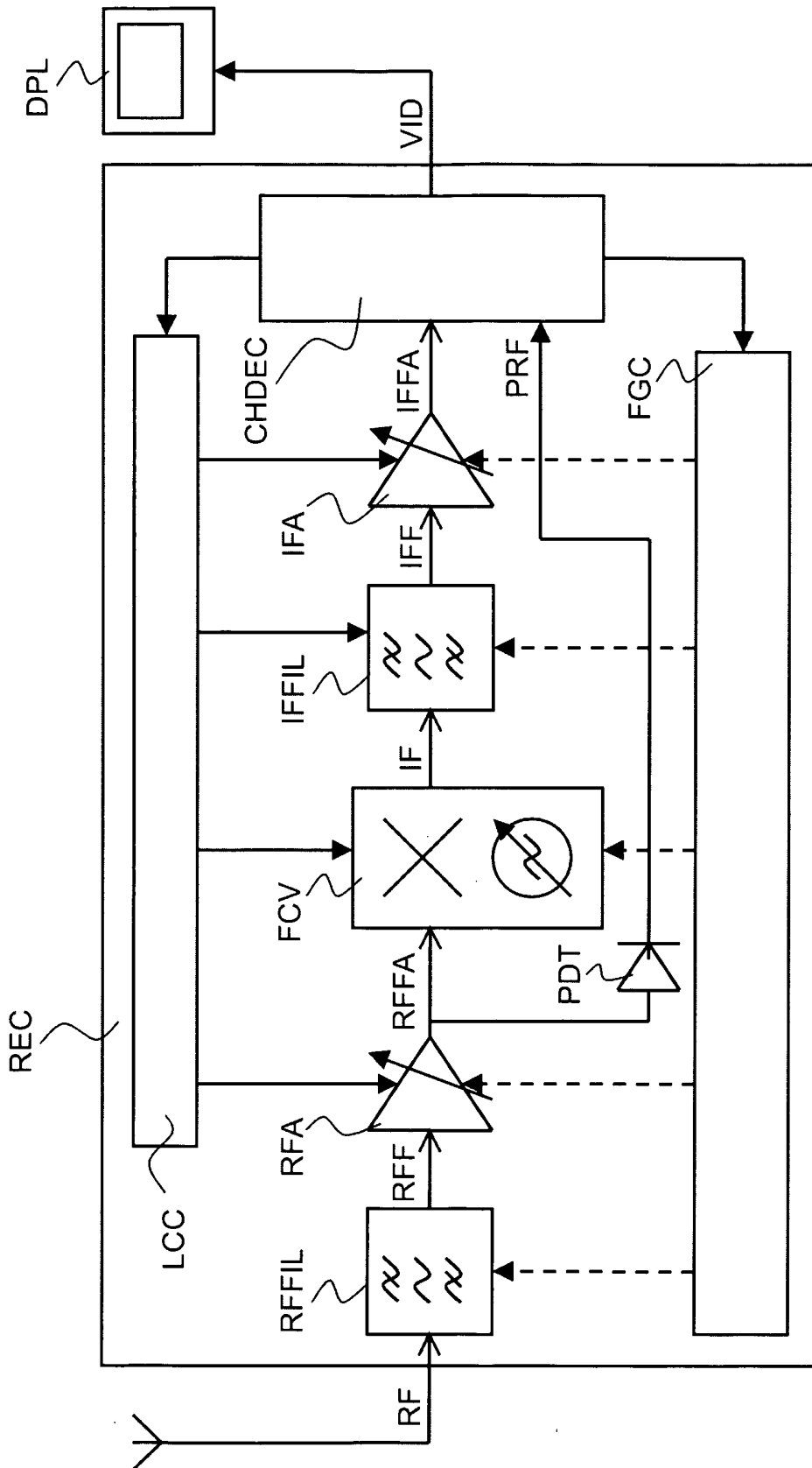
a control step (ST6-ST7) in which the power consumption of the signal-processing circuit is controlled as a function of the signal-strength ratio.

15

8. A computer program product for a signal processing arrangement that comprises a digital processor (CHDEC), the computer program product comprising a set of instructions for, when loaded into the digital processor, enabling the digital processor to carry out the method of claim 7.

20

9. An information-rendering apparatus that comprises a signal processing arrangement (REC) as claimed in claim 1, and an information-rendering device (DPL) for rendering information (VID) that the signal processing arrangement has derived from the desired signal.



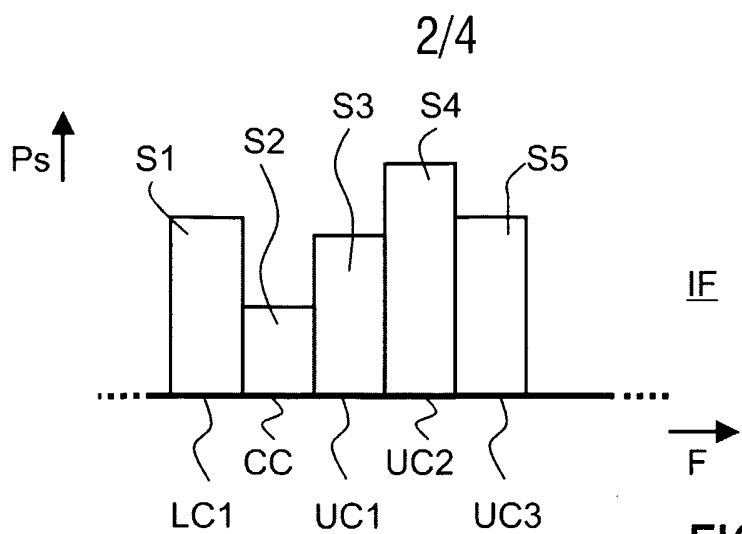


FIG.2A

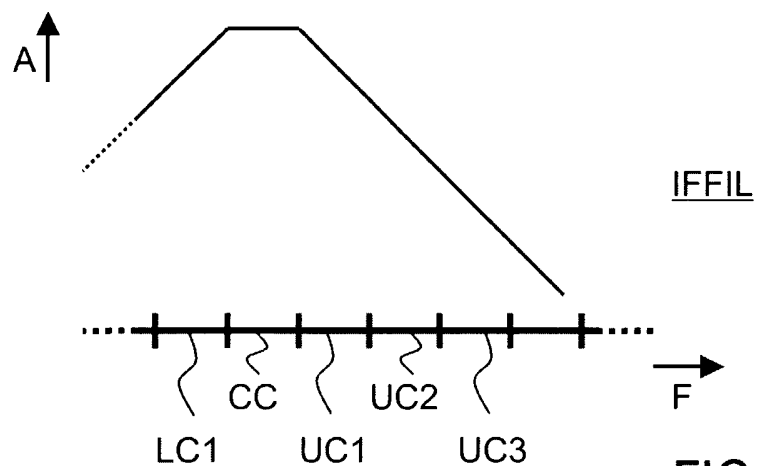


FIG.2B

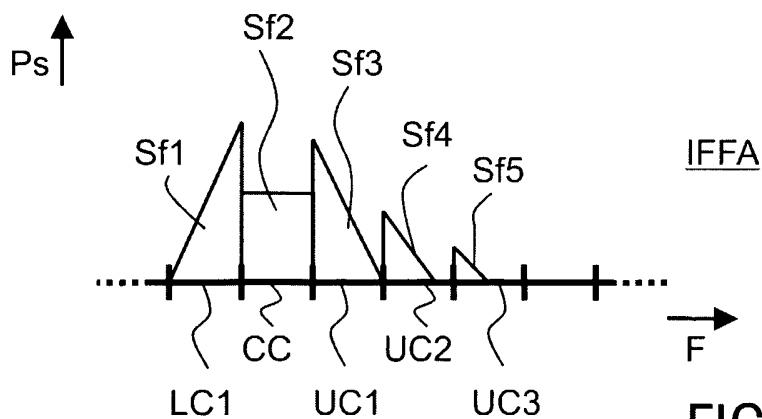


FIG.2C

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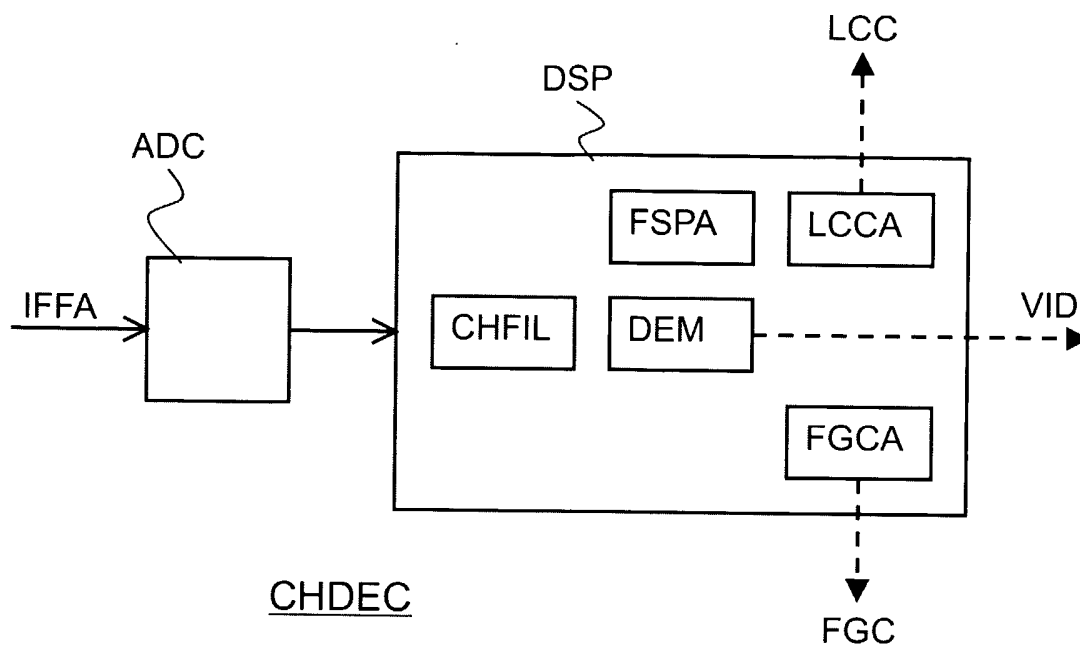


FIG.3

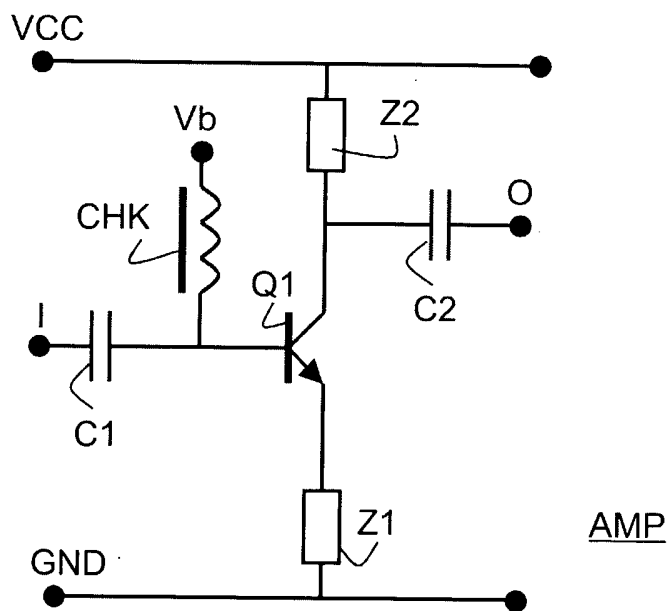


FIG.5

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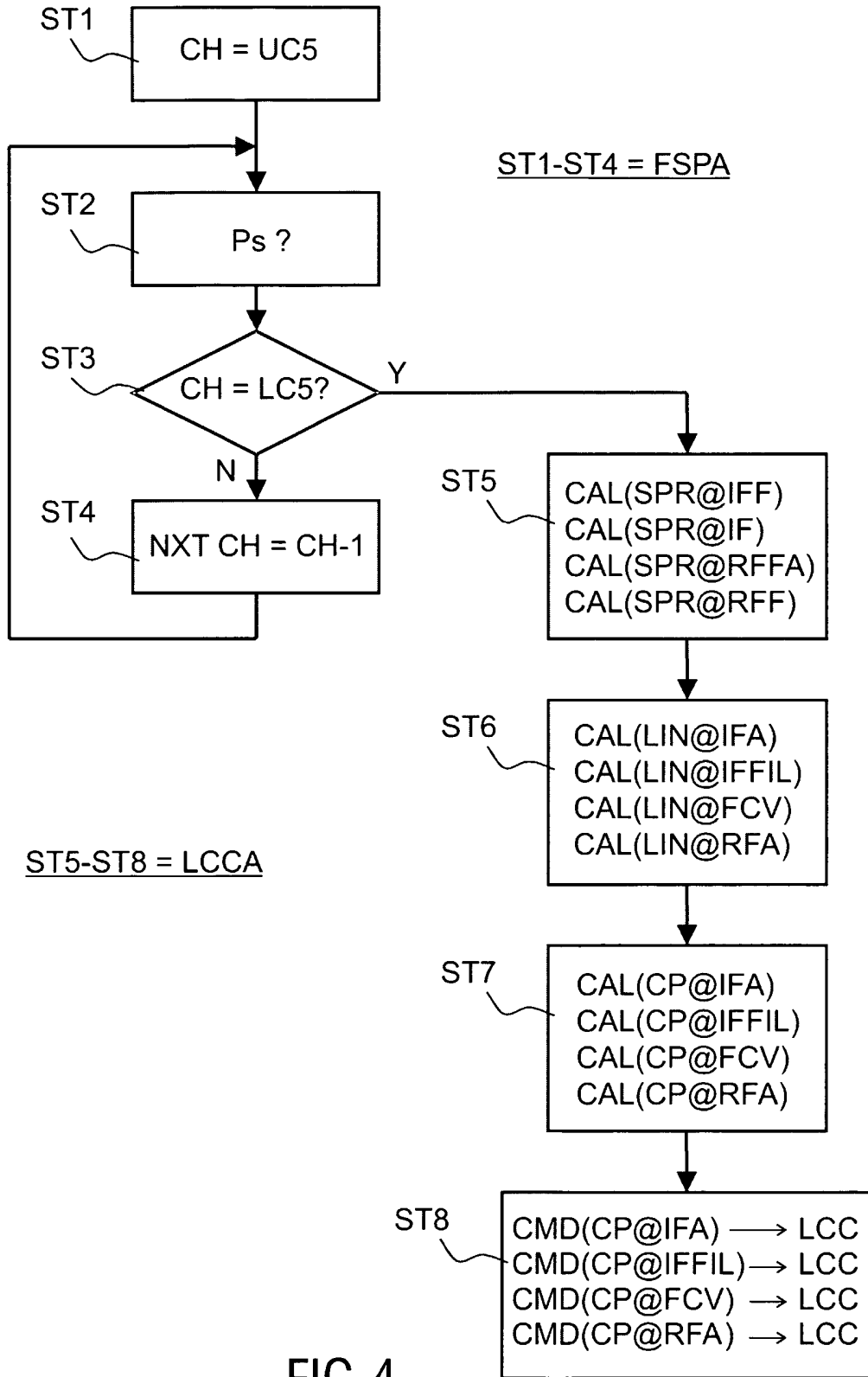


FIG. 4

## INTERNATIONAL SEARCH REPORT

PCT/IB2005/052545

**A. CLASSIFICATION OF SUBJECT MATTER**  
 IPC 7 H03F1/02 H04B1/10

According to International Patent Classification (IPC) or to both national classification and IPC

**B. FIELDS SEARCHED**

Minimum documentation searched (classification system followed by classification symbols)  
 IPC 7 H03F H04B

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

EPO-Internal

**C. DOCUMENTS CONSIDERED TO BE RELEVANT**

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 5 809 400 A (ABRAMSKY ET AL) 15 September 1998 (1998-09-15) figures 1,3	1,3,7-9
X	----- US 5 001 776 A (CLARK ET AL) 19 March 1991 (1991-03-19) figure 1	1,3-5,7
X	----- US 6 564 043 B2 (RAUHALA ANTTI ET AL) 13 May 2003 (2003-05-13) figure 4	1-3,5-7
X	----- US 5 239 683 A (USUI ET AL) 24 August 1993 (1993-08-24) figures 2-4,6	1,2,6,7
	----- -/--	

Further documents are listed in the continuation of box C.

Patent family members are listed in annex.

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Date of the actual completion of the international search

26 October 2005

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## C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
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