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(54) **MULTI-PORT MAGNETIC RANDOM ACCESS MEMORY (MRAM)**

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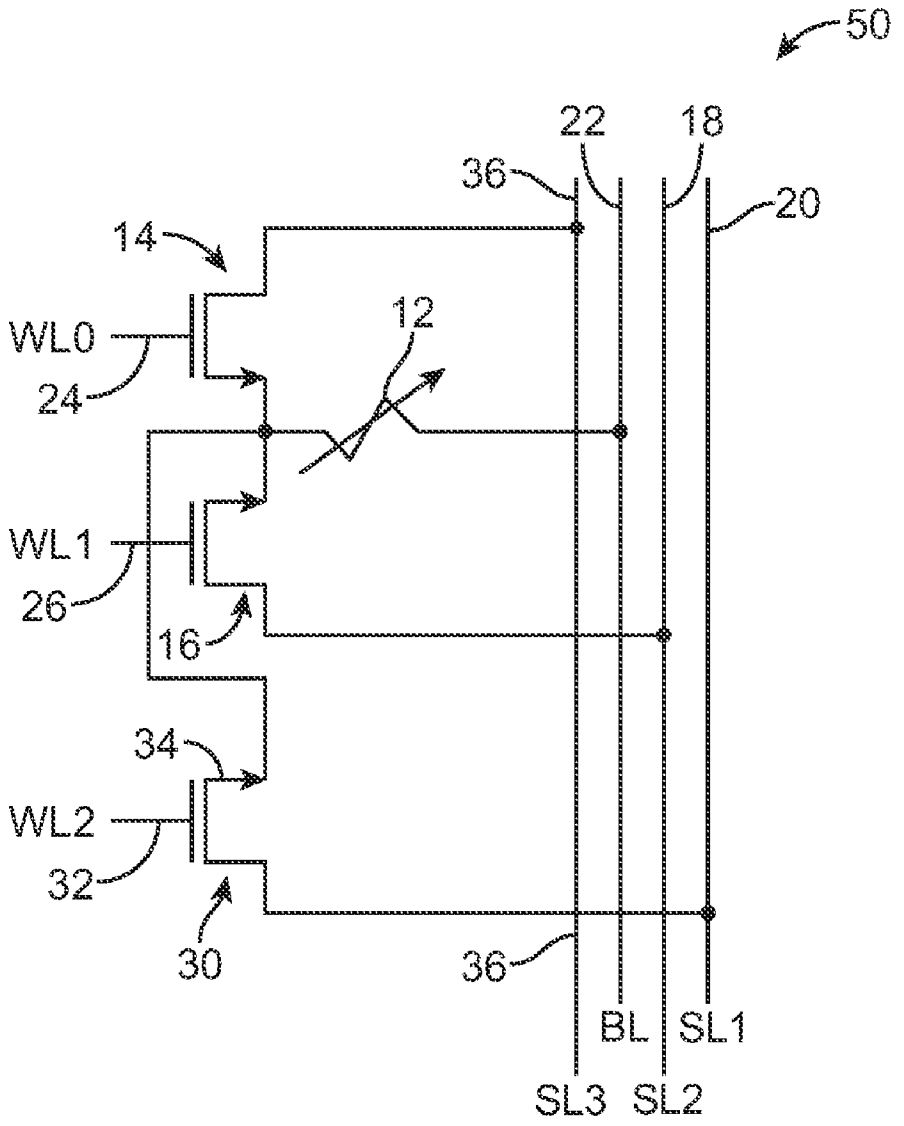
(57) **ABSTRACT**

A memory array is organized into rows and columns of resistive elements and is disclosed to include a resistive element to be read or to be written thereto. Further, a first access transistor is coupled to the resistive element and to a first source line and a second access transistor is coupled to the resistive element and to a second source line, the resistive element being coupled at one end to the first and second access transistors and at an opposite end to a bit line. The memory array further has other resistive elements that are each coupled to the bit line. The resistive element is written to while one or more of the other resistive elements are being read.



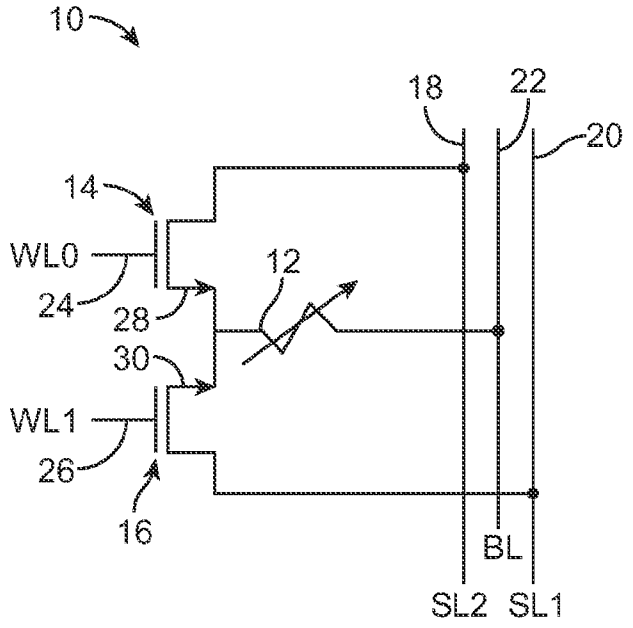

10
18
22
20
14
WL0
24
28
12
30
WL1
26
16
BL
SL2
SL1

FIG. 1

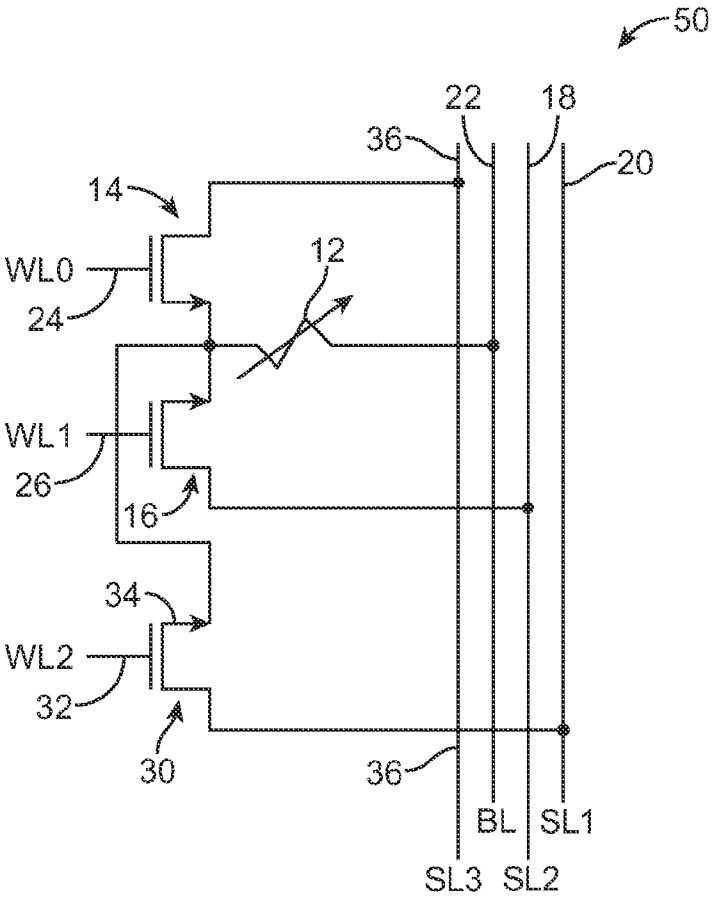

50
22
18
36
20
14
12
WL0
24
WL1
26
16
34
WL2
32
30
36
BL
SL1
SL3
SL2

FIG. 2

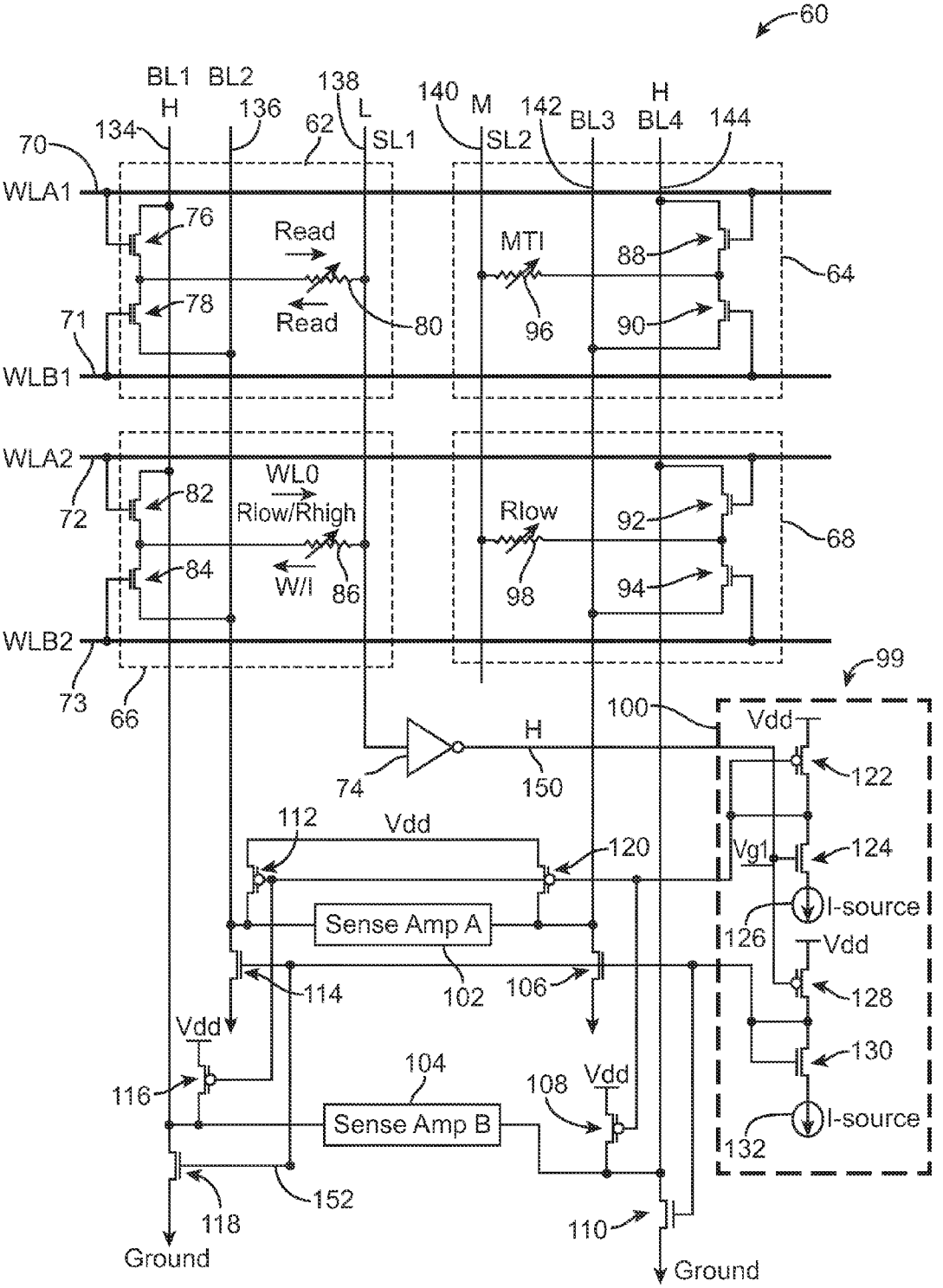

60
BL1
H
BL2
136
138
L
SL1
140
M
SL2
142
BL3
H
BL4
144
134
62
70
WLA1
76
Read
MTI
88
64
78
Read
80
96
90
71
WLB1
WLA2
72
82
WL0
Riow/Rhigh
Riow
92
68
84
W/I
86
98
94
WLB2
73
66
99
100
Vdd
H
74
150
122
112
Vdd
120
Vg1
124
I-source
Sense Amp A
126
Vdd
114
102
106
128
Vdd
130
104
116
108
Vdd
Sense Amp B
I-source
132
152
118
110
Ground
Ground

FIG. 3

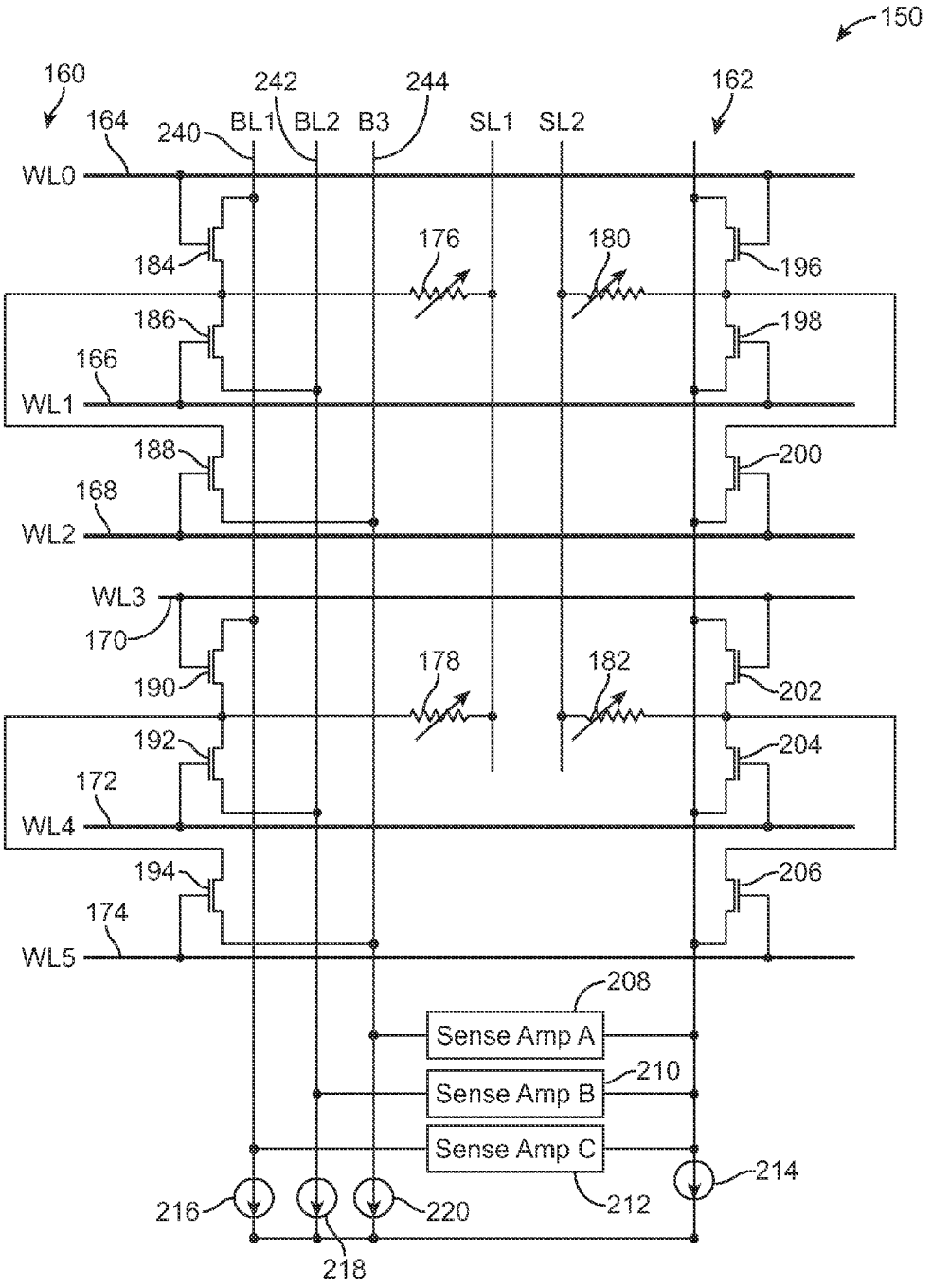

150
160
162
164
240
242
244
BL1
BL2
B3
SL1
SL2
WL0
WL1
WL2
WL3
WL4
WL5
166
168
170
172
174
176
178
180
182
184
186
188
190
192
194
196
198
200
202
204
206
208
210
212
214
216
218
220
Sense Amp A
Sense Amp B
Sense Amp C

FIG. 4

MULTI-PORT MAGNETIC RANDOM ACCESS MEMORY (MRAM)

BACKGROUND OF THE INVENTION

[0001] 1. Field of the Invention

[0002] The invention relates to a magnetic random access memory (MRAM), and, more particularly, to increasing the performance of read and write operations to MRAM cells of a memory array.

[0003] 2. Description of the Prior Art

[0004] Magnetic random access memory (MRAM) shows significant promise in the world of memory and other storage, such as to replace solid state. It is expected that MRAM will replace conventional non-volatile memory and solid state storage and perhaps even other types of storage in the near years ahead. However, great strides are to first be made before wider adoption and popularity of MRAMs, as this type of memory is still in its infancy.

[0005] Among other challenges, memory systems utilizing MRAMs face performance issues during read and write operations. Generally, MRAM, such as magnetic tunnel junction (MTJ) is paired with an access transistor that directs the reading from and writing to the MTJ. The access transistor is typically coupled to a word line of the memory system or array and a bit line and a sense line are coupled to the MTJs of the array for accessing and reading and writing thereof, under the direction of access transistors. However, only one MTJ of a column of MTJs that are all connected to the same bit line can be read and/or written at any given time. When any other MTJ of the same column is to be accessed for reading and writing operations, the MTJ that is being programmed or read must be released prior to programming or reading of any other MTJ that is coupled to a common bit line. In some memory applications it would be beneficial to read and write the same cell via different ports. There could be two or more ports that the memory can be read or written to. As an example one such memory can be read by the CPU while it is being written into by another device. As is appreciated, this would require extra rows and columns in order to access the same cell from different ports.

[0006] Therefore, in light of the foregoing, what is needed is a memory array, made of, at least in part, MRAMs with read and write capability from different ports.

SUMMARY OF THE INVENTION

[0007] To overcome the limitations in the prior art described above, and to overcome other limitations that will become apparent upon reading and understanding the present specification, the invention discloses a method and a corresponding structure for a magnetic memory system including magnetic tunnel junctions (MTJs) and structures and methods for programming and reading the same.

[0008] Briefly, a memory array is organized into rows and columns of resistive elements and is disclosed to include a resistive element to be read or to be written thereto. Further, a first access transistor is coupled to the resistive element and to a first source line and a second access transistor is coupled to the resistive element and to a second source line, the resistive element being coupled at one end to the first and second access transistors and at an opposite end to a bit line. The memory array further has other resistive elements that are each coupled to the bit line. The resistive element can be written to while one or more of the other resistive elements are being read.

[0009] These and other objects and advantages of the present invention will no doubt become apparent to those skilled in the art after having read the following detailed description of the various embodiments illustrated in the several figures of the drawing.

IN THE DRAWINGS

[0010] FIG. **1** shows a portion of a memory array **10** is shown in accordance with an embodiment of the invention.

[0011] FIG. **2** shows a portion of a memory array **50** is shown in accordance with another embodiment of the invention.

[0012] FIG. **3** shows a memory array **60**, organized in rows and columns of memory cells, in accordance with another embodiment of the invention.

[0013] FIG. **4** shows a memory array **150**, in accordance with another embodiment of the invention.

DETAILED DESCRIPTION OF VARIOUS EMBODIMENTS

[0014] In the following description of the embodiments, reference is made to the accompanying drawings that form a part hereof, and in which is shown by way of illustration of the specific embodiments in which the invention may be practiced. It is to be understood that other embodiments may be utilized because structural changes may be made without departing from the scope of the present invention. It should be noted that the figures discussed herein are not drawn to scale and thicknesses of lines are not indicative of actual sizes.

[0015] In accordance with an embodiment of the invention, a memory array is organized into rows and columns of resistive elements and is disclosed to include a resistive element to be read or to be written thereto. Further, a first access transistor is coupled to the resistive element and to a first source line and a second access transistor is coupled to the resistive element and to a second source line, the resistive element being coupled at one end to the first and second access transistors and at an opposite end to a bit line. The memory array further has other resistive elements that are each coupled to the bit line. The resistive element is written to while one or more of the other resistive elements are being read.

[0016] Referring now to FIG. **1**, a portion of a memory array **10** is shown in accordance with an embodiment of the invention. The array **10** is shown to include a resistive element **12**, an access transistor **14**, and an access transistor **16**. Each of the access transistors **14** and **16**, as is well known to those in the art, have a source, a drain, and a gate. Further, a bit line **22** (or "BL") is shown coupled to one end (or "port") of the resistive element **12** and a source line **20** (also referred to herein as "SL**1**") is shown coupled to the source of the transistor **16**. A source line **18** (also referred to herein as "SL**2**") is further shown coupled to the source of the transistor **14**. Another end (or "port") of the resistive element **12**, which is shown opposite to the end thereof that is coupled to the bit line, is shown coupled to the drain of each of the transistors **14** and **16**. Word line **24** (also referred to herein as "WL**0**") is shown coupled to the gate of the access transistor **14** and the word line **26** (also known as "WL**1**") is shown coupled to the gate of the access transistor **16**.

[0017] Each of the transistors **14** and **16** is a n-channel transistor though p-channel transistors are contemplated in which some changes, known to those in the art, to the configuration of the array **10** result.

[0018] In some embodiments, the resistive element **12** is a magnetic tunnel junction memory (MTJ), well know to those in the art. Some such MRAMs are made of magnetic tunnel junctions (MTJs) such as spin transfer torque magnetic random access memory (STTMRAM). Other types of resistive elements, while not listed in the interest of brevity, are nevertheless anticipated.

[0019] In operation, the word line **24** is activated in conjunction with the activation of the source line **18** to access the resistive element **12** for programming and/or reading but at the same time, activation of the word line **26** in conjunction with activation of the source line **20** can be effectuated to allow accessing of the resistive element **12** by another device.

[0020] According, the resistive element **12** is configured to be dual port due to the use of each of the source lines **18** and **20**, in addition to the distinct word lines **24** and **26**, allowing dual access of the resistive element **12** for reading and writing. As such and advantageously, the resistive element **12** can be accessed with two devices at the same time. For example, data that is stored in the resistive element **12** can be read by a processor while another data is being written in another location, substantially simultaneously, of an array made of resistive elements including the resistive element **12**. In the dual port configuration of FIG. **1**, a pair of word lines, a pair of bit lines and a pair of sense amplifiers are required.

[0021] A few exemplary scenarios of reading/writing operations to the element **12** will now be discussed. When performing reading of the element **12** through a single port only, such as the port coupled to the word line **24**, the bit line **22** is fixed to a specific voltage, such as Vs, the word line **24** is driven high, the word line **26** is driven low and the source line **18** is driven by a sense amplifier, which is shown and explained relative to subsequent figures. When reading the element **12** through dual ports, i.e. by two devices simultaneously, the following occurs. The voltage at bit line **22** is fixed at Vs, the word line **24** is driven high, the word line **26** is driven high, the source line **18** is sensed by a sense amplifier and the source line **20** is sensed by a separate sense amplifier, as will be shown and discussed shortly. During a write operation to the element **12**, assuming the word line **24** is used to write or program the element **12**, the voltage at the bit line **22** is set to 0.5 volts, the word line **24** is set high, the word line **26** is set low and if programming is from an anti-parallel to a parallel state, such as in the case where the element **12** is a MTJ, the sense line **18** is set to zero volts and for the case of parallel to anti-parallel programming, the sense line **18** is set to Vdd. "high".

When writing to the element **12** through the word line **26**, the voltage at the bit line **22** is set to Vdd, the voltage of the word line **24** is set low, the voltage at the word line **26** is set high, and if programming is from an anti-parallel to a parallel state, such as in the case where the element **12** is a MTJ, the sense line **20** is set to zero volts and for the case of parallel to anti-parallel programming, the sense line **20** is set to Vdd.

[0022] In the case where writing to the element **12** is done sequentially and using the word line **24**, followed by reading through the word line **26**, the voltage at the bit line **22** is set to 0.5 volts or Vdd, the voltage of the word line **24** is set to a very high value (as an example 1.5V), the voltage at the word line **26** is set low, and in the case where the element **12** is a MTJ and being programmed from an anti-parallel state to a parallel state, the voltage of the sense line **18** is set to zero volts and for the case where the state is being programmed from parallel to anti-parallel, the voltage of the sense line **18** is set to Vdd. During reading, the voltage at the bit line **22** is set to Vx, the voltage of the word line **24** is set to high and the voltage of the source line **20** is sensed by a sense amplifier.

[0023] FIG. **2** shows a portion of a memory array **50** is shown in accordance with another embodiment of the invention. The array **50** is shown to include the resistive element **12**, the access transistor **14**, and the access transistor **16** but because the configuration of the array **50** results in the resistive element **12** being a triple port, another access transistor **30** is shown coupled to the port of the resistive element **12** that is coupled to the transistors **14** and **16**. The transistor **30** is also a n-channel transistor with the understanding that as in the case of the transistors **14** and **16**, the transistor **30** may be an p-channel transistor. The transistor **30** is shown to have a gate **32** that is coupled to a word line **32** (also referred to herein as "WL**2**") and it further has a source coupled to the source line **20** and its drain **34** is shown coupled to the resistive element **12** and the source of each of the transistors **14** and **16**. The resistive element **12** is shown coupled to the transistors **14** and **16** and to the bit line **22**, and the source lines **18** and **20** in the same manner as that shown and discussed relative to the embodiment of FIG. **1**.

[0024] Due to the addition of the transistor **30** and the word line **32** and the sense line **36**, relative to the embodiment of FIG. **1**, the resistive element **12** is triple ported where up to three different devices can access it simultaneously for various operations.

[0025] FIG. **3** shows a memory array **60**, organized in rows and columns of memory cells, in accordance with another embodiment of the invention. In FIG. **3**, the memory array **60** is shown to have four memory cells **62-68**, and memory circuit **99**. While four memory cells are shown in FIG. **3**, it is understood that the memory array **60** can have any number of memory cells and it commonly has many more than shown. Each of the memory cells **62-68** is analogous to the resistive element **12**, and the transistors **14** and **16**, collectively, in that it is a dual port memory cell including a resistive element and two access transistors. For example, the cell **62** is shown to include the resistive element **80** and an access transistor **76** and an access transistor **78** with these transistors coupled to the element **80** in an analogous manner as the configuration of the embodiment of FIG. **1** except that in the case of the embodiment of FIG. **3**, bit line ("BL**1**") **134** and bit line ("BL**2**") **136** are shown coupled to the transistors instead of source lines being coupled to these transistors. Indeed, the use of bit lines and source lines in this manner is an interchangeable one. Accordingly, in FIG. **1**, the source lines **18** and **20** may be bit lines instead in which case the bit line **22** would be a source line. Accordingly, the resistive element **80**, which similar to the element **12** can be a MRAM or other types of resistive element, is shown coupled to the source line **138**, in FIG. **3**.

[0026] Each of the gates of each access transistor **76**, **78**, **82**, **84**, **88**, **90**, **92**, and **94** is shown to be coupled to a word line. For example, the transistor **76** is shown coupled, through its gate, to the word line **70** (also referred to herein as "WLA**1**") and the gate of the transistor **78** is shown coupled to the word line **71** ("WLB**1**"). The gate of the transistor **90** is shown coupled to the word line **71** and the gate of the transistor **88** is shown coupled to the word line **70**. Similarly, the gate of the

transistor **82** is shown coupled to the word line **72** and the gate of the transistor **84** is shown coupled to the word line **73** and the gate of the transistor **94** is shown coupled to the word line **73** and the gate of the transistor **92** is shown coupled to the word line **72**.

[0027] The transistors **76** and **78** allow for a dual port access of the element **80**, as do the transistors **88** and **90** for the element **96** and the transistors **82** and **84** for the element **86** and the transistors **92** and **94** for the element **98**. The transistors **88** and **90** are shown coupled to the bit line **144** ("BL**4**") and the bit line **142** ("BL**3**"), respectively. Similarly, the transistors **92** and **94** are shown coupled to the bit line **144** and the bit line **142**, respectively.

[0028] The circuit **99** is an exemplary embodiment of a memory circuit and many others with varying designs and configurations are contemplated. The circuit **99** is shown to include a driver **100**, an inverter **74**, a sense amplifier **102** (also referred to herein as "sense amp A"), a sense amplifier **104**, transistors **112**, **114**, **118**, **116**, **120**, **106**, **108**, and **110**, which all, with the aid of the word lines **70-73**, cause accessing of the resistive elements **80**, **86**, **96**, and **98** for reading and writing operations. While the word lines **70-73** are driven by row decoders, well known in the industry, the bit lines and source lines of the array **60** are driven by the circuit **99**, as is further discussed below relative to read and write operations.

[0029] In the circuit **99**, the driver **100** is shown to include the transistors **122**, **124**, **128**, and **130**, and the current sources **126** and **132**. The transistors **122** and **128** are shown to be p-channel transistors while the transistors **130** and **124** are shown to be n-channel transistors. It is understood that these transistors may be of opposite types or even other types, in other embodiments.

[0030] Similarly, the transistors **112**, **120**, **116**, and **108** are shown to be p-channel transistors and the transistors **118**, **110**, **114**, and **106** are shown to be n-channel transistors with the understanding that other types of transistors may be used. The sense amplifier **102** is shown coupled to the transistors **120**, **106**, **114**, and **112** and the sense amplifier **104** is shown coupled to the transistors **108**, **110**, **116**, and **118**.

[0031] The invertor **74** is shown coupled to one end (or "port") of each of the elements **80** and **86** and inverts the state thereof and passes on, as its output **150**, the inverted state of these resistive elements to the transistors **124** and **128** of the driver **100**. The gate of the transistor **120** is shown coupled to the drain of the transistor **124** and the source of the transistor **122**. The source of the transistor **124** is shown coupled to the current source **126**. Similarly, the gate of the transistor **110** is shown coupled to the drain of the transistor **130** and the source of the transistor **128**. The source of the transistor **130** is shown coupled to the current source **132**. The source of each of the transistors **110** and **118** is shown coupled to ground and the drain of the transistor **118** is shown coupled to the bit line **134** for driving the same and the drain of the transistor **110** is shown coupled to the bit line **144** for driving the same. The gates of each of the transistors **116** and **112** are shown coupled to each other and the gates of the transistors **108** and **120** are shown coupled to each other. The source of the transistor **116** and the source of the transistor **108** are each shown coupled to the voltage level, Vdd, well known in the art. The source of the transistors **112** and **120** are shown coupled to each other.

[0032] The gates of the transistors **114**, **106**, **152**, and **110** are shown coupled to each other. The source of the transistors **112** and **120** are coupled to each other and to Vdd.

[0033] Due to each memory cell of the array **60** including two access transistors, two sense amplifiers are utilized in the circuit **99**. Thus, the sense amplifier **102** senses the bit line **136** and the bit line **142** and the sense amplifier **104** senses the bit lines **134** and **144**. In a three-port configuration, such as that of the embodiment of FIG. **2**, three sense amplifiers are required.

[0034] As the case of the embodiment of FIG. **1**, each of the resistive elements of the array **60** is read or written to by accessing it through two different access transistors and two word lines. Accordingly, two different resistive elements that are coupled to the same bit lines can be read at the same time by using two different sense amplifiers.

[0035] An exemplary read operation is now discussed relative to the array **60**. The upper resistive elements, such as the elements **76**, **82**, **88**, or **92** is accessed by activating the word line **70**, which in the current example is setting the word line **70** to a high state, or WLA**1**=high. The lower resistive element, elements **78**, **90**, **84**, or **94** is accessed by activating the word line **73**, which in the current example amount to setting the word line **73** to a high state, or WLB**2**=high. The rest of the word lines, such as the word lines **71** and **72**, are grounded. The source lines **138** and **140** are grounded (the active and also the reference select lines). These cause the output of the inverter **74** to go high, which causes the p-channel pull ups (or transistors **112**, **120**, **116**, and **108**) to turn on. Current flows through these transistors and through the bit lines **134**, **136**, **142**, and **144** and through the resistive elements **80**, **86**, **96**, and **98**. The sense amplifiers **102** and **104** each compare the voltage values of their respective inputs and switch accordingly. The size of the current sources **126** and **132** are the same in the embodiment of FIG. **3**, accordingly, the size of the P (and N) channel devices on the reference side are slightly larger to increase the voltage on the reference side when both the active and reference resistive elements have the same resistance value. Now let us consider the case when the bottom resistive element is being written into while the upper resistive element is being read. If, for example, the resistive element, in the case where it is a MTJ is switching from a parallel state to an anti-parallel state when being programmed, then the bit line **134** is at a high state, e.g. 1.2V and the source line **138** is at 0V, while the word line **72**, WLA**2**, is high. Since the voltage of the source line **138** is at zero, the P-channels current sources are on and the top MTJ is fed through the bit line **136**, while the word line **71**, WLB**1**, is high and all other word lines are at ground. In this scheme the voltage appearing at the sense amp A, sense amplifier **102**, determines the status of upper MTJ, such as the element **80** or **96**. Now if we are converting the status of the lower MTJ, or the element **86** or **98**, from anti-parallel (AP) to parallel (P), then the bit line **134** is at zero volts (BL**1**=0 V) and the source line **138** is at 1.2V. In this configuration the p-channels in the current sources are off and n-channels are on. On the upper MTJ current will go through the MTJ and is controlled by the N-channel current source. The voltages appear at two ends of the sense amp will indicate the status of the MTJ.

[0036] To read the state of the MTJ by sense amp A, sense amplifier **102**, the power line is powered up, while the word line **70**, WLA**1**, is high and the rest of the word lines are grounded. The current I pass through the MTJ and the voltage is compared to the voltage of the reference current resulting in 0 or 1 depending on the value of the MTJ resistance. Same MTJ can also be read by powering up the word line WLB**1** and grounding the rest of the word lines. MTJ programming

can easily be done by selecting the MTJ by either word or bit lines and passing proper current through it. One can reverse the direction of the current and change the resistance value of the selected MTJ.

[0037] As can be appreciated, multi-port MRAM is realized, in accordance with various embodiments and methods of the invention, by increasing the number of select transistors, word lines, bit lines and sense amplifiers.

[0038] FIG. **4** shows a memory array **150**, in accordance with another embodiment of the invention. The array **150** includes three-port resistive elements, analogous to that of the embodiment of FIG. **2**. In accordance therewith, several MTJs are sensed substantially at the same time.

[0039] In FIG. **4**, the array is shown to include MTJs **176** and **178** that are generally located on the left side of FIG. **2**, at **160**, and reference MTJs **180** and **182**, generally located at the right side of FIG. **4**, at **162**. Further shown as a part of the array **150**, are access lines, such as word lines **164-174** (also known as "WL**0**" through "WL**5**"). Further, the array **150** is shown to include access transistors **184-194**, which are shown coupled to the MTJs **176** and **178** and access transistors **196-206**, which are shown coupled to the reference MTJs **180** and **182**. The array **150** is also shown to include sense amplifiers **208-212** and current sources **216-220**.

[0040] The access lines on the left side of FIG. **4**, at **160**, such as the WL**0** through WL **5**, couple the each of the two MTJs to a distinct one of the sense amplifiers **208-212**, i.e. the sense amplifiers A through C. Further details of the coupling of various elements or structures with each other, shown in FIG. **4**, are not discussed because they are analogous to that of embodiments of prior figures. That is, the MTJs **176-178** are accessed through the different word lines WL**0**-WL**5**. The reference MTJs **180-182** on the right side of FIG. **4**, serve as references when reading from and writing to the MTJs **176-78** but advantageously, only one reference voltage is required to read all the MTJs. The right side of all of the sense amplifiers **208-212** use the same voltage as those required by the reference MTJs **180-182** to sense the MTJs **176-178** when being read. The difference between two-port resistive elements, such as the embodiment **10**, vs. three-port resistive elements, such as the embodiment **50** or **150**, is that a dual-port MTJ can be accesses by two different routes, while in a triple-port MTJ arrangement, the same MTJ can be accessed via 3 different routes. In the embodiment of FIG. **4**, three sense amplifiers can sense 3 different MTJs at the same time but they are compared to the same reference voltage, i.e. the reference voltage of the MTJs **180-182**, appearing on the right side of the FIG. **4**.

[0041] It is understood that while two MTJs **176** and **178** are shown in the embodiment of FIG. **4**, additional MTJs may be employed requiring additional reference MTJs. The operation of the array **150** is analogous to that of embodiments discussed herein relative to prior figures.

[0042] Although the invention has been described in terms of specific embodiment, it is anticipated that alterations and modifications thereof will no doubt become apparent to those more skilled in the art. It is therefore intended that the following claims be interpreted as covering all such alterations and modification as fall within the true spirit and scope of the invention.

What is claimed is:

1. (canceled)

2. (canceled)

3. (canceled)

4. (canceled)

5. (canceled)

6. (canceled)

7. (canceled)

8. A memory array organized into rows and columns of resistive elements, the memory array comprising:

a first pair of access transistors coupled to each other and a first and second word lines;

a first resistive element coupled to the first pair of access transistors and to a first sense line;

a second pair of access transistors coupled to each other and a third and fourth word lines;

a second resistive element coupled to the second pair of access transistors and to the first sense line;

a first pair of reference access transistors coupled to each other and the first and second word lines;

a first reference resistive element coupled to the first pair of reference access transistors and to a second sense line;

a second pair of reference access transistors coupled to each other and the third and fourth word lines;

a second reference resistive element coupled to the second pair of reference access transistors and to the first sense line,

wherein the first resistive element is written to while the second resistive element is read.

9. The memory array of claim **8**, wherein the first pair of access transistors is further coupled to a first and second bit lines.

10. The memory array of claim **9**, wherein the second pair of access transistors is further coupled to a third and fourth bit lines.

11. The memory array of claim **10**, further including a first sense amplifier coupled to the second bit line and the third bit lines.

12. The memory array of claim **11**, further including a second sense amplifier coupled to the third bit line and the fourth bit lines.

13. The memory array, as recited in claim **8**, wherein the resistive element is a magnetic random access memory (MRAM).

14. The memory array, as recited in claim **8**, wherein the resistive element is a magnetic tunnel junction (MTJ).

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