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(54) Title: METHOD AND SYSTEM FOR MITIGATING WRITE AMPLIFICATION IN A PHASE CHANGE MEMORY-BASED STORAGE DEVICE

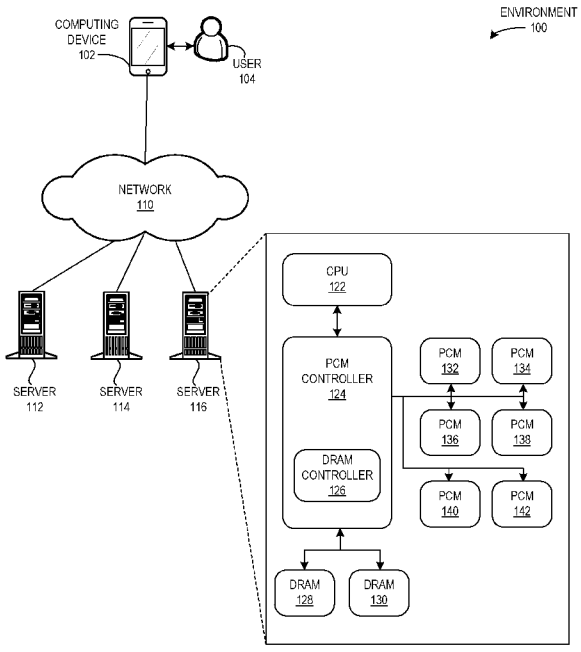


FIG. 1

(57) Abstract: One embodiment facilitates mitigating write amplification in a phase change memory-based storage device. During operation, the system receives, by a controller of the storage device, data to be stored in a phase change memory (PCM) of the storage device. The system writes, by the controller, the data to a sector of a volatile memory of the same storage device to obtain an updated portion of the sector. In response to detecting a predetermined condition, the system writes the updated portion to the PCM.

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METHOD AND SYSTEM FOR MITIGATING WRITE AMPLIFICATION IN A PHASE CHANGE MEMORY-BASED STORAGE DEVICE

BACKGROUND

Field

[0001] This disclosure is generally related to the field of data storage. More specifically, this disclosure is related to a method and system for mitigating write amplification in a phase change memory-based storage device.

Related Art

[0002] The proliferation of the Internet and e-commerce continues to create a vast amount of digital content. Various storage systems have been created to access and store such digital content. One such storage system uses phase change memory (PCM), which is a type of non-volatile random access memory. PCM uses a specific type of glass and can hold multiple bits in a single cell (or sector). A standard PCM-based storage device typically writes data using a relatively large block or sector size (e.g., 4 kilobytes (KB)). In a situation with frequent I/O updates with small block sizes, the standard PCM-based storage device can suffer significant write amplification (e.g., when the actual amount of information physically written to storage media is a multiple of the logical amount intended to be written).

[0003] For example, given a sector with a size of 4 KB and a single update (e.g., a write) of only 128 bytes of data, the standard PCM-based storage device system must perform the following three operations: 1) read out the entire 4 KB sector from PCM; 2) modify the read-out sector with the updated 128 bytes; and 3) write back the entire 4 KB sector with the updated 128 bytes. This single update with three operations may result in a latency that is 2-3 times higher than a direct overwriting of data. Furthermore, the resulting write amplification has a high value of 32 (i.e., 4 KB / 128 bytes). Given that PCM media may have an approximate lifespan of 10^{-7} program cycles (in that a cell is worn out after being written to 10^{-7} times), the lifespan of a standard PCM-based device may be a limiting factor in the design and deployment of a storage system. Thus, both the write amplification and the higher latency can decrease the efficiency of the storage system.

SUMMARY

[0004] One embodiment mitigates write amplification in a phase change memory-based storage device. During operation, the system receives, by a controller of the storage device, data to be stored in a phase change memory (PCM) of the storage device. The system writes, by the controller, the data to a sector of a volatile memory of the same storage device to obtain an updated portion of the sector. In response to detecting a predetermined condition, the system writes the updated portion to the PCM. In some embodiments, the system writes the updated portion to the PCM without writing an entirety of the sector to the PCM.

[0005] In some embodiments, the sector includes original data and original parity bits. The system writes the updated portion to the PCM by: comparing the data in the updated portion of the sector with the corresponding original data to obtain a first difference; aligning the first difference by pre-pending and appending zeros to the first difference; encoding the aligned first difference to obtain a second difference; comparing the original parity bits with the second difference to obtain new parity bits; and writing the updated portion and the new parity bits to the PCM.

[0006] In some embodiments, the predetermined condition is based on one or more of: reaching a predetermined timeout or expiration period for the updated portion; reaching a predetermined capacity threshold of the volatile memory; executing an instruction to write data from the volatile memory to the PCM; a loss in power; and detecting a predetermined time interval or frequency for writing data from the volatile memory to the PCM.

[0007] In some embodiments, writing the updated portion to the PCM is in response to determining that a length of the updated portion is less than a predetermined length.

[0008] In some embodiments, the system writes the data to the sector of the volatile memory in response to determining that a length of the received data is less than a predetermined length corresponding to a block size for the PCM. Furthermore, in response to determining that the length of the received data is not less than the predetermined length corresponding to the block size for the PCM, the system writes the received data to the PCM.

[0009] In some embodiments, prior to writing the updated portion to the PCM, the system: determines data which has been written to a plurality of sectors; aggregates the data into a second sector; and in response to detecting the predetermined condition, writes the aggregated data to the PCM.

[0010] In some embodiments, the system determines the data which has been written to the plurality of sectors based on one or more of: a frequency of access; a predetermined

frequency of access; a preferential mapping algorithm; an observable condition; and a predetermined condition.

[0011] In some embodiments, prior to writing the aggregated data to the PCM, the system: generates parity bits for the aggregated data; and includes the generated parity bits with the aggregated data.

[0012] Another embodiment mitigates write amplification in a phase change memory-based storage device. During operation, the system receives, by a controller of the storage device, a request to read data. The system retrieves, by the controller, the requested data from a phase change memory (PCM) of the storage device, wherein the requested data has been previously written to the PCM from a volatile memory of the same storage device. In response to detecting a predetermined condition, the system writes, by the controller, the retrieved data to the volatile memory.

[0013] In some embodiments, the retrieved data corresponds to a first portion of a first sector of the PCM. The system writes the retrieved data to the volatile memory by: determining a second sector of the volatile memory, wherein the second sector corresponds to the first sector; writing the first portion to the second sector; aligning the first portion in the second sector based on a length of the first portion and a length of the second sector to obtain a new codeword; returning, by the controller, the first portion from the new codeword.

[0014] In some embodiments, the system retrieves the requested data from the PCM in response to determining that the requested data is not stored in the volatile memory. Furthermore, in response to determining that the requested data is stored in the volatile memory, the system returns the requested data from the volatile memory.

[0015] In some embodiments, the predetermined condition is based on one or more of: performing a caching algorithm; detecting a user-generated or host-configured condition; determining that the requested data is to be written to the volatile memory; analyzing statistics associated with access of the data; determining that a likelihood of the requested data to be requested or accessed is greater than a predetermined threshold; and an observable condition associated with the requested data.

BRIEF DESCRIPTION OF THE FIGURES

[0016] FIG. 1 illustrates an exemplary environment that facilitates mitigating write amplification in a phase change memory (PCM)-based storage device, in accordance with an embodiment of the present application.

[0017] FIG. 2 illustrates an exemplary flow for accumulating updated user data in volatile memory and for writing the updated user data to PCM, in accordance with an embodiment of the present application.

[0018] FIG. 3A presents a flowchart illustrating a method for writing data in a PCM-based storage device, in accordance with an embodiment of the present application.

[0019] FIG. 3B presents a flowchart illustrating a method for writing data in a PCM-based storage device, in accordance with an embodiment of the present application.

[0020] FIG. 4 presents a flowchart illustrating a method for determining a predetermined condition for flushing data to PCM, in accordance with an embodiment of the present application.

[0021] FIG. 5A presents a flowchart illustrating a method for reading data in a PCM-based storage device, in accordance with an embodiment of the present application.

[0022] FIG. 5B presents a flowchart illustrating a method for reading data in a PCM-based storage device, in accordance with an embodiment of the present application.

[0023] FIG. 6A illustrates an exemplary distribution of user data in volatile memory, based on a statistically hot uneven distribution, in accordance with an embodiment of the present application.

[0024] FIG. 6B illustrates an exemplary distribution of user data in volatile memory, based on a statistically hot even distribution and a method for reshuffling data, in accordance with an embodiment of the present application.

[0025] FIG. 7 illustrates an exemplary computer system that facilitates mitigating write amplification in a phase change memory (PCM)-based storage device, in accordance with an embodiment of the present application.

[0026] FIG. 8 illustrates an exemplary apparatus that facilitates mitigating write amplification in a phase change memory (PCM)-based storage device, in accordance with an embodiment of the present application.

[0027] In the figures, like reference numerals refer to the same figure elements.

DETAILED DESCRIPTION

[0028] The following description is presented to enable any person skilled in the art to make and use the embodiments, and is provided in the context of a particular application and its requirements. Various modifications to the disclosed embodiments will be readily apparent to those skilled in the art, and the general principles defined herein may be applied to other embodiments and applications without departing from the spirit and scope of the present disclosure. Thus, the embodiments described herein are not limited to the embodiments shown,

but are to be accorded the widest scope consistent with the principles and features disclosed herein.

Overview

[0029] The embodiments described herein solve the problem of mitigating write amplification in a PCM-based storage device by adding volatile memory to the PCM-based storage device, along with a controller module to manage the data path. A standard PCM-based storage device typically writes data using a relatively large block or sector size (e.g., 4 KB). However, in the case of frequent I/O updates with small block sizes, the standard PCM-based storage device can suffer significant write amplification. For example, given a 4 KB sector and an update of only 128 bytes, the standard PCM-based storage device can experience a write amplification of 32 (4,024 bytes / 128 bytes). The write amplification can result in a shorter overall lifespan for the PCM media. Furthermore, because a single update in a standard PCM-based storage device can require three operations (i.e., read out, modify, and write back), the standard PCM-based storage device may incur a higher latency than a direct overwriting operation. Both the write amplification and the increased latency can decrease the efficiency of the storage system.

[0030] The embodiments described herein facilitate mitigating write amplification in a PCM-based storage device ("PCM device") by including volatile memory (such as DRAM) in the PCM device. The PCM device incrementally stores and updates smaller data blocks in its internal DRAM and, based on a predetermined condition for flushing the data from DRAM to PCM, writes the updated blocks into the PCM media in a single operation (e.g., as a single codeword encoded with an error code correction (ECC)). The PCM device can also include a controller which manages the data path to/from the volatile memory (e.g., DRAM) and the PCM media, as well as a power-loss detecting circuit. The controller can determine the predetermined flushing condition, which can be based on, e.g., a timeout, a capacity of the data buffer, an explicit host instruction, a loss in power, and an update frequency.

[0031] Thus, the embodiments described herein provide a system which improves the efficiency of a storage system, where the improvements are fundamentally technological. The improved efficiency can include mitigating write amplification for I/O operations associated with a PCM-based storage device. The system provides a technological solution (i.e., a PCM-based storage device which places the volatile memory and the PCM media on the same storage device, and includes a controller module to manage the data path) to the technological problem of reducing latency in I/O tasks, increasing the lifespan of the PCM media, and improving the overall efficiency of the system.

[0032] The term "storage server" refers to a server which can include multiple drives and multiple memory modules.

[0033] The term "phase change memory-based storage device" or "PCM-based storage device" or "PCM device" refers to a device, as described herein, which includes volatile memory, a controller module, and PCM on the same device. A PCM device of the prior art is referred to herein as a "standard PCM-based storage device."

[0034] The term "volatile memory" refers to computer storage which can lose data quickly upon removal of the power source, such as DRAM.

[0035] The term "phase change memory" or "PCM" refers to a type of non-volatile random access memory, which can be used for long-term persistent computer storage.

[0036] The term "ECC-encoding" refers to encoding data based on an error correction code, while the term "ECC-decoding" refers to decoding data based on the error correction code.

[0037] The term "PCM controller" refers to a module located in a PCM-based storage device, and includes logic which controls data access to/from the PCM on the storage device. The term "DRAM controller" refers to a module located in the PCM controller, and includes logic which controls data access to/from the volatile memory (e.g., DRAM) on the same storage device as the PCM controlled by the PCM controller. In the embodiments described herein, the controllers are situated in the data path between the volatile memory and the PCM. The DRAM controller also includes a data buffer, into which data is written for temporary storage, and subsequently written or flushed into the PCM. The controller's data buffer can also include data which is being processed by the controller, including being compared, aligned, and ECC-encoded/decoded, as described below in relation to FIGs. 2 and 3B.

Exemplary System

[0038] FIG. 1 illustrates an exemplary environment 100 that facilitates mitigating write amplification in a phase change memory (PCM)-based storage device, in accordance with an embodiment of the present application. Environment 100 can include a computing device 102 which is associated with a user 104. Computing device 102 can include, for example, a tablet, a mobile phone, an electronic reader, a laptop computer, a desktop computer, or any other computing device. Computing device 102 can communicate via a network 110 with servers 112, 114, and 116, which can be part of a distributed storage system. Servers 112-116 can include a storage server, which can include a phase change memory (PCM)-based storage device. For example, server 116 can include a CPU 122, which communicates with a PCM controller 124. PCM controller 124 can communicate with phase change memory media (such as PCMs 132, 134, 136, 138, 140, and 142), and can further include a DRAM controller 126. DRAM controller

126 can communicate with volatile memory (such as DRAMs 128 and 130), and can further include a data buffer (not shown).

[0039] By including CPU 122, DRAM controller 126, and DRAMs 128 and 130 in PCM-based storage device 116, the embodiments described herein can avoid frequent transmission of data through a host fabric, such as a Peripheral Component Interface Express (PCIe) bus. DRAM controller 126 can read old data directly from local PCMs 132-142 into its own data buffer, make the modification, and write the data back. Because the entirety of these operations occur inside PCM-based storage device 116, the system can avoid the cost associated with transmitting and reading data via a PCIe bus.

[0040] Thus, server 116 depicts an exemplary architecture of a PCM-based storage device, as in the embodiments described herein. A general data flow is described below in relation to FIG. 2. An exemplary data flow in a write operation is described below in relation to FIGs. 3A, 3B, and 4, and an exemplary data flow in a read operation is described below in relation to FIGs. 5A and 5B.

Exemplary Flow for Processing Data from Volatile Memory to PCM

[0041] FIG. 2 illustrates an exemplary flow for accumulating updated user data in volatile memory and for writing the updated user data to PCM, in accordance with an embodiment of the present application. To ensure the security of stored data, the system may perform error correction code (ECC) encoding on data before storing the data in the PCM. At a time T0 210, a sector of data in volatile memory (e.g., DRAM) can include original user bits 202 and original parity bits 204. Original parity bits 204 can be the bits which are added to original user bits 202 upon an ECC-encoding.

[0042] In the embodiments described herein, the system can incrementally update blocks in a single sector in the volatile memory, before processing the data and flushing the processed data to the PCM. For example, at a time T1 211, user data 220 can be written to a portion of the sector. At a time T2 212, user data 222 can be written to the sector. At a time T3 213, user data 224.1 and 224.2 can be written to the sector. New user data which is written to the sector simply overwrites the corresponding portion of the sector. Thus, at a time T4 214, the sector includes an unchanged portion 240, an updated portion 242, and an unchanged portion 244. Updated portion 242 can include: user data 224.1; user data 230 (which is the portion of user data 220 not overwritten by subsequent user data); user data 224.2; and user data 232 (which is the portion of user data 222 not overwritten by subsequent data).

[0043] The system can detect a predetermined condition to write the updated portion from the DRAM to the PCM. Exemplary conditions are described below in relation to FIG. 4.

The system can compare updated portion 242 with a corresponding portion of original user bits 250 (of original user bits 202) to obtain a user delta 260 (via an XOR operation 236 and a result 252). Thus, at a time T5 215, user delta 260 is the difference between original user bits 250 and updated portion 242.

[0044] At a time T6 216, the system can align user delta 260 with the original sector size (align function 252). For example, based on the length of user delta 260 and the length of original user bits 202, the system can prepend and append user delta 260 with zeroes, which forms a vector 264 (or an aligned and updated user bits 264). Vector 264 can include an aligned portion 266, user delta 260, and an aligned portion 268. The system can encode vector 264 (via encode operation 270) to obtain a parity delta 272. Subsequently, the system can write to the PCM media the entire updated sector (including parity delta 272 appended to vector 264).

[0045] Thus, by accumulating small block sized user updates in internal DRAM, and by flushing the accumulated blocks to the PCM based on a predetermined condition, the embodiments described herein provide a PCM-based storage device which facilitates mitigating write amplification, and thus results in a more efficient storage system.

Exemplary Communication During a Write Operation

[0046] FIG. 3A presents a flowchart 300 illustrating a method for writing data in a PCM-based storage device, in accordance with an embodiment of the present application. During operation, the system receives, by a controller of the storage device, data to be stored in a phase change memory (PCM) of the storage device (operation 302). If the length of the data is not less than 4 KB (decision 304), the system writes the entire 4 KB unit of data to the PCM (operation 306), and the operation continues at operation 342 of FIG. 3B. If the length of the data is less than 4 KB (decision 304), the system writes, by the controller, the data to a sector of a volatile memory of the same storage device to obtain an updated portion of the sector (operation 308). The system determines whether the updated portion replaces a previous version of the data (decision 310). If it does not, the system waits to receive incoming data for an I/O merge (operation 312), and the operation returns to operation 302.

[0047] If the system does determine that the updated portion replaces a previous version of the data (decision 310), the system maps, by the controller, a logical address of the sector and an offset of the updated portion to a physical block address of the PCM (operation 314). The system accumulates the updated portion and any other updated portions in the sector by overwriting the previous versions (operation 316). If the system does not detect a predetermined condition to flush data from the volatile memory to the PCM (decision 318), the operation returns to operation 302. If the system does detect a predetermined condition to flush data from the

volatile memory to the PCM (decision 318), the operation continues as described at Label A of FIG. 3B.

[0048] FIG. 3B presents a flowchart 330 illustrating a method for writing data in a PCM-based storage device, in accordance with an embodiment of the present application. During operation, the system compares the data in the updated portion of the sector with the corresponding original data to obtain a first difference, wherein the sector includes original data and original parity bits (operation 332). The system aligns the first difference by pre-pending and appending zeros to the first difference (operation 334) (e.g., based on a length of the first difference and a length of the sector). The system encodes the aligned first difference to obtain a second difference (operation 336). The system compares the original parity bits with the second difference to obtain new parity bits (operation 338). The system writes the updated portion and the new parity bits to the PCM (operation 340). The system verifies that the data is securely written to the PCM (operation 342), and the operation returns.

Detecting Trigger Conditions for Flushing Data from DRAM to PCM

[0049] FIG. 4 presents a flowchart 400 illustrating a method for determining a predetermined condition for flushing data to PCM, in accordance with an embodiment of the present application. If the system reaches a predetermined timeout for the updated portion (decision 402), the system writes the updated portion in the data buffer to the PCM (operation 412). If not, and if the system reaches a predetermined capacity threshold of the volatile memory (decision 404), the system writes the updated portion in the data buffer to the PCM (operation 412). If not, and if the system determines to execute a specific instruction (e.g., from a host) (decision 406), the system writes the updated portion in the data buffer to the PCM (operation 412). If not, and if the system detects (e.g., by a power-loss detecting circuit in the PCM-based storage device) a loss in power (decision 408), the system writes the updated portion in the data buffer to the PCM (operation 412). If not, and if the system detects a predetermined time interval or frequency for flushing data (decision 410), the system writes the updated portion in the data buffer to the PCM (operation 412). If not, the operation returns.

[0050] Note that while decisions 402-410 are depicted in a specific order in flowchart 400, the controller can perform operation 412 upon detecting any of the predetermined conditions represented by decisions 402-410.

Exemplary Communication During a Read Operation

[0051] FIG. 5A presents a flowchart 500 illustrating a method for reading data in a PCM-based storage device, in accordance with an embodiment of the present application. During

operation, the system receives, by a controller of the storage device, a request to read data (operation 502). If the requested data is stored in a volatile memory of the storage device (decision 504), the operation continues as described at operation 528 of FIG. 5B. If the requested data is not stored in the volatile memory of the storage device (decision 504), the system retrieves, by the controller, the requested data from a phase change memory (PCM) of the storage device, wherein the requested data has been previously written to the PCM from the volatile memory of the same storage device (operation 506). If the system determines not to update the volatile memory with the retrieved data (decision 508), the operation continues as described at operation 528 of FIG. 5B. If the system does determine to update the volatile memory with the retrieved data (decision 508), the operations continues at Label B of FIG. 5B.

[0052] FIG. 5B presents a flowchart 520 illustrating a method for reading data in a PCM-based storage device, in accordance with an embodiment of the present application. During operation, the system determines a second sector of the volatile memory, wherein the retrieved data corresponds to a first portion of a first sector of the PCM, and wherein the second sector corresponds to the first sector (operation 522). The system writes the first portion to the second sector (operation 524). The system aligns the first portion in the second sector based on a length of the first portion and a length of the second sector to obtain a new codeword (operation 526). The system returns, by the controller, the requested data or the first portion from the new codeword (operation 528), and the operation returns.

Exemplary Use Cases Showing Data Distribution; Reshuffling Method

[0053] FIG. 6A illustrates an exemplary distribution 600 of user data in volatile memory, based on a statistically hot uneven distribution, in accordance with an embodiment of the present application. Distribution 600 includes six sectors: sector A 610 includes original user bits 611 and original parity bits 612; sector B 620 includes original user bits 621 and original parity bits 622; sector C 630 includes original user bits 631 and original parity bits 632; sector D 640 includes original user bits 641 and original parity bits 642; sector E 650 includes original user bits 651 and original parity bits 652; and sector F 660 includes original user bits 661 and original parity bits 662. The statistically uneven hot distribution 600 shown in FIG. 6A results in a preferred distribution for the embodiments described herein. New blocks of user data (i.e., updated data) are written to only two of the depicted six sectors, which results in a need for fewer overall write operations (e.g., flushing the updated data). Three blocks of new user data (new data A 614, 616, and 618) are written to sector A in the original user bits 611, overwriting the previous bits as shown, and as described above in relation to FIG. 2. Three other blocks of new

user data (new data E 654, 656, and 658) are written to sector E in the original user bits 651, similarly overwriting the previous bits as shown.

[0054] In contrast, a statistically even hot distribution can result in flushing sectors even when only one small data block has been updated in each sector. FIG. 6B illustrates an exemplary distribution 670 of user data in volatile memory, based on a statistically hot even distribution and a method for reshuffling data, in accordance with an embodiment of the present application. Six blocks of new user data are written to each of the six sectors: new data A 672 is written to sector A 610; new data B 674 is written to sector B 620; new data C 676 is written to sector C 630; new data D 678 is written to sector D 640; new data E 680 is written to sector E 650; and new data F 682 is written to sector F 660. The controller of a PCM-based storage device can monitor the frequency of access of data blocks A-F (i.e., 672-682), and allocate a new physical location for these frequently updated blocks, e.g., by a using a preferential mapping algorithm. Rather than inefficiently (and frequently) performing six separate writes to the PCM, where each update is only for a small block of data, the controller can aggregate or group the frequently accessed blocks into a single sector and perform only one write to the PCM. For example, the controller can detect or determine the frequently accessed data blocks A-F, reshuffle these determined blocks A-F (reshuffle operation 690), and place them as reshuffled user data 691 in a new sector M 670, along with new parity bits 692. In this way, the system can perform only one write instead of six, resulting in a more efficient storage system with both an increased latency and an increased lifespan for the PCM.

[0055] Another advantage to employing such a preferential mapping algorithm is that the system need no longer wait for a natural expiration of any of blocks A-F in order to write the data to the PCM. Instead, the system can place frequently accessed blocks of data together in one physical location and write the entire block to the PCM in one operation. The system may base the block selection (e.g., the preferential mapping algorithm) not only on frequency of access but also on any other observable or preconfigured condition detected by the controller.

Exemplary Computer System and Apparatus

[0056] FIG. 7 illustrates an exemplary computer system 700 that facilitates mitigating write amplification in a phase change memory (PCM)-based storage device, in accordance with an embodiment of the present application. Computer system 700 includes a processor 702, a volatile memory 704, a controller 705, a phase change memory (PCM) 706, and a storage device 708. Computer system 700 may be a client-serving machine. Volatile memory 704 can include, e.g., RAM, that serves as a managed memory, and can be used to store one or more memory pools. PCM 706 can include persistent storage that is accessed via controller 705. Furthermore,

computer system 700 can be coupled to a display device 710, a keyboard 712, and a pointing device 714. Storage device 708 can store an operating system 716, a content-processing system 718, and data 732.

[0057] Content-processing system 718 can include instructions, which when executed by computer system 700, can cause computer system 700 to perform methods and/or processes described in this disclosure. Specifically, content-processing system 718 can include instructions for receiving and transmitting data packets, including a request to write or read data, and data to be processed (e.g., encoded, aligned, or compared) and stored. Content-processing system 718 can further include instructions for receiving, by a controller of a storage device, data to be stored in a phase change memory (PCM) of the storage device (communication module 720). Content-processing system 718 can include instructions for writing, by the controller, the data to a sector of a volatile memory of the same storage device to obtain an updated portion of the sector (volatile memory-accessing module 722). Content-processing system 718 can include instructions for, in response to detecting a predetermined condition, writing the updated portion to the PCM (condition-detecting module 728 and PCM-accessing module 724).

[0058] Content-processing system 718 can include instructions for processing data to be written to the PCM, including: comparing the data in the updated portion of the sector with the corresponding original data to obtain a first difference; aligning the first difference by pre-pending and appending zeros to the first difference; encoding the aligned first difference to obtain a second difference; comparing the original parity bits with the second difference to obtain new parity bits; and writing the updated portion and the new parity bits to the PCM (sector-processing module 726).

[0059] Content-processing system 718 can include instructions for determining data which has been written to a plurality of sectors, and aggregating the data into a second sector (data-shuffling module 730).

[0060] Content-processing system 718 can include instructions for receiving, by a controller of a storage device, a request to read data (communication module 720). Content-processing system 718 can include instructions for retrieving, by the controller, the requested data from a phase change memory (PCM) of the storage device (PCM-accessing module 724). Content-processing system 718 can include instructions for, in response to detecting a predetermined condition, writing, by the controller, the retrieved data to the volatile memory (condition-detecting module 728 and volatile memory-accessing module 722).

[0061] Data 732 can include any data that is required as input or that is generated as output by the methods and/or processes described in this disclosure. Specifically, data 732 can store at least: data to be written, read, stored, or accessed; processed or stored data; encoded or

decoded data; an error correction code (ECC) encoding or decoding; a codeword; parity bits; an indicator of whether data is stored in volatile memory or PCM; a block; a sector; a logical block address; a physical block address; a buffer for data in volatile memory; a condition to flush data from volatile memory to PCM; a pre-determined condition for writing, storing, or flushing data; a level of power; a loss in power level; a sector; a portion of a sector; data; aligned portions; a vector; a difference which is the result of a comparison; a timeout; an expiration period; a percentage of a capacity of a data buffer; a capacity threshold; an instruction; a threshold; a timeout; an expiration; a frequency; a length of data, a block, or a sector; a frequency of access; a preferential mapping algorithm; a reshuffling method; an observable condition; and a configured condition.

[0062] FIG. 8 illustrates an exemplary apparatus 800 that facilitates mitigating write amplification in a phase change memory (PCM)-based storage device, in accordance with an embodiment of the present application. Apparatus 800 can comprise a plurality of units or apparatuses which may communicate with one another via a wired, wireless, quantum light, or electrical communication channel. Apparatus 800 may be realized using one or more integrated circuits, and may include fewer or more units or apparatuses than those shown in FIG. 8. Further, apparatus 800 may be integrated in a computer system, or realized as a separate device which is capable of communicating with other computer systems and/or devices. Specifically, apparatus 800 can comprise units 802-812 which perform functions or operations similar to modules 720-730 of computer system 700 of FIG. 7, including: a communication unit 802; a volatile memory-accessing unit 804; a PCM-accessing unit 806; a sector-processing unit 808; a condition-detecting unit 810; and a data-shuffling unit 812.

[0063] The data structures and code described in this detailed description are typically stored on a computer-readable storage medium, which may be any device or medium that can store code and/or data for use by a computer system. The computer-readable storage medium includes, but is not limited to, volatile memory, non-volatile memory, magnetic and optical storage devices such as disk drives, magnetic tape, CDs (compact discs), DVDs (digital versatile discs or digital video discs), or other media capable of storing computer-readable media now known or later developed.

[0064] The methods and processes described in the detailed description section can be embodied as code and/or data, which can be stored in a computer-readable storage medium as described above. When a computer system reads and executes the code and/or data stored on the computer-readable storage medium, the computer system performs the methods and processes embodied as data structures and code and stored within the computer-readable storage medium.

[0065] Furthermore, the methods and processes described above can be included in hardware modules. For example, the hardware modules can include, but are not limited to, application-specific integrated circuit (ASIC) chips, field-programmable gate arrays (FPGAs), and other programmable-logic devices now known or later developed. When the hardware modules are activated, the hardware modules perform the methods and processes included within the hardware modules.

[0066] The foregoing embodiments described herein have been presented for purposes of illustration and description only. They are not intended to be exhaustive or to limit the embodiments described herein to the forms disclosed. Accordingly, many modifications and variations will be apparent to practitioners skilled in the art. Additionally, the above disclosure is not intended to limit the embodiments described herein. The scope of the embodiments described herein is defined by the appended claims.

What Is Claimed Is:

1. A computer-implemented method for mitigating write amplification in a phase change memory-based storage device, the method comprising:

receiving, by a controller of the storage device, data to be stored in a phase change memory (PCM) of the storage device;

writing, by the controller, the data to a sector of a volatile memory of the same storage device to obtain an updated portion of the sector; and

in response to detecting a predetermined condition, writing the updated portion to the PCM.

2. The method of claim 1, wherein the sector includes original data and original parity bits, and wherein writing the updated portion to the PCM further comprises:

comparing the data in the updated portion of the sector with the corresponding original data to obtain a first difference;

aligning the first difference by pre-pending and appending zeros to the first difference;

encoding the aligned first difference to obtain a second difference;

comparing the original parity bits with the second difference to obtain new parity bits; and

writing the updated portion and the new parity bits to the PCM.

3. The method of claim 1, wherein the predetermined condition is based on one or more of:

reaching a predetermined timeout or expiration period for the updated portion;

reaching a predetermined capacity threshold of the volatile memory;

executing an instruction to write data from the volatile memory to the PCM;

a loss in power; and

detecting a predetermined time interval or frequency for writing data from the volatile memory to the PCM.

4. The method of claim 1, wherein writing the updated portion to the PCM is in response to determining that a length of the updated portion is less than a predetermined length.

5. The method of claim 1, wherein writing the data to the sector of the volatile

memory is in response to determining that a length of the received data is less than a predetermined length corresponding to a block size for the PCM, and wherein the method further comprises:

in response to determining that the length of the received data is not less than the predetermined length corresponding to the block size for the PCM, writing the received data to the PCM.

6. The method of claim 1, wherein prior to writing the updated portion to the PCM, the method further comprises:

determining data which has been written to a plurality of sectors;

aggregating the data into a second sector; and

in response to detecting the predetermined condition, writing the aggregated data to the PCM.

7. The method of claim 6, wherein determining the data which has been written to the plurality of sectors is based on one or more of:

a frequency of access;

a predetermined frequency of access;

a preferential mapping algorithm;

an observable condition; and

a predetermined condition.

8. The method of claim 6, wherein prior to writing the aggregated data to the PCM, the method further comprises:

generating parity bits for the aggregated data; and

including the generated parity bits with the aggregated data.

9. A computer-implemented method for mitigating write amplification in a phase change memory-based storage device, the method comprising:

receiving, by a controller of the storage device, a request to read data;

retrieving, by the controller, the requested data from a phase change memory (PCM) of the storage device, wherein the requested data has been previously written to the PCM from a volatile memory of the same storage device; and

in response to detecting a predetermined condition, writing, by the controller, the retrieved data to the volatile memory.

10. The method of claim 9, wherein the retrieved data corresponds to a first portion of a first sector of the PCM, and wherein writing the retrieved data to the volatile memory further comprises:

determining a second sector of the volatile memory, wherein the second sector corresponds to the first sector;

writing the first portion to the second sector;

aligning the first portion in the second sector based on a length of the first portion and a length of the second sector to obtain a new codeword;

returning, by the controller, the first portion from the new codeword.

11. The method of claim 9, wherein retrieving the requested data from the PCM is in response to determining that the requested data is not stored in the volatile memory, and wherein the method further comprises:

in response to determining that the requested data is stored in the volatile memory, returning the requested data from the volatile memory.

12. The method of claim 9, wherein the predetermined condition is based on one or more of:

performing a caching algorithm;

detecting a user-generated or host-configured condition;

determining that the requested data is to be written to the volatile memory;

analyzing statistics associated with access of the data;

determining that a likelihood of the requested data to be requested or accessed is greater than a predetermined threshold; and

an observable condition associated with the requested data.

13. A computer system for mitigating write amplification in a phase change memory-based storage device, the system comprising:

a processor; and

a memory coupled to the processor and storing instructions, which when executed by the processor cause the processor to perform a method, the method comprising:

receiving, by a controller of the storage device, data to be stored in a phase change memory (PCM) of the storage device;

writing, by the controller, the data to a sector of a volatile memory of the same storage device to obtain an updated portion of the sector; and

in response to detecting a predetermined condition, writing the updated portion to the PCM without.

14. The computer system of claim 13, wherein the sector includes original data and original parity bits, and wherein writing the updated portion to the PCM further comprises:

comparing the data in the updated portion of the sector with the corresponding original data to obtain a first difference;

aligning the first difference by pre-pending and appending zeros to the first difference;

encoding the aligned first difference to obtain a second difference;

comparing the original parity bits with the second difference to obtain new parity bits; and

writing the updated portion and the new parity bits to the PCM.

15. The computer system of claim 13, wherein the predetermined condition is based on one or more of:

reaching a predetermined timeout or expiration period for the updated portion;

reaching a predetermined capacity threshold of the volatile memory;

executing an instruction to write data from the volatile memory to the PCM;

a loss in power; and

detecting a predetermined time interval or frequency for writing data from the volatile memory to the PCM.

16. The computer system of claim 13, wherein writing the updated portion to the PCM is in response to determining that a length of the updated portion is less than a predetermined length.

17. The computer system of claim 13, wherein writing the data to the sector of the volatile memory is in response to determining that a length of the received data is less than a predetermined length corresponding to a block size for the PCM, and wherein the method further comprises:

in response to determining that the length of the received data is not less than the predetermined length corresponding to the block size for the PCM, writing the received data to the PCM.

18. The computer system of claim 13, wherein prior to writing the updated portion to

the PCM, the method further comprises:

determining data which has been written to a plurality of sectors;

aggregating the data into a second sector; and

in response to detecting the predetermined condition, writing the aggregated data to the PCM.

19. The computer system of claim 18, wherein determining the data which has been written to the plurality of sectors is based on one or more of:

a frequency of access;

a predetermined frequency of access;

a preferential mapping algorithm;

an observable condition; and

a predetermined condition.

20. The computer system of claim 18, wherein prior to writing the aggregated data to the PCM, the method further comprises:

generating parity bits for the aggregated data; and

including the generated parity bits with the aggregated data.

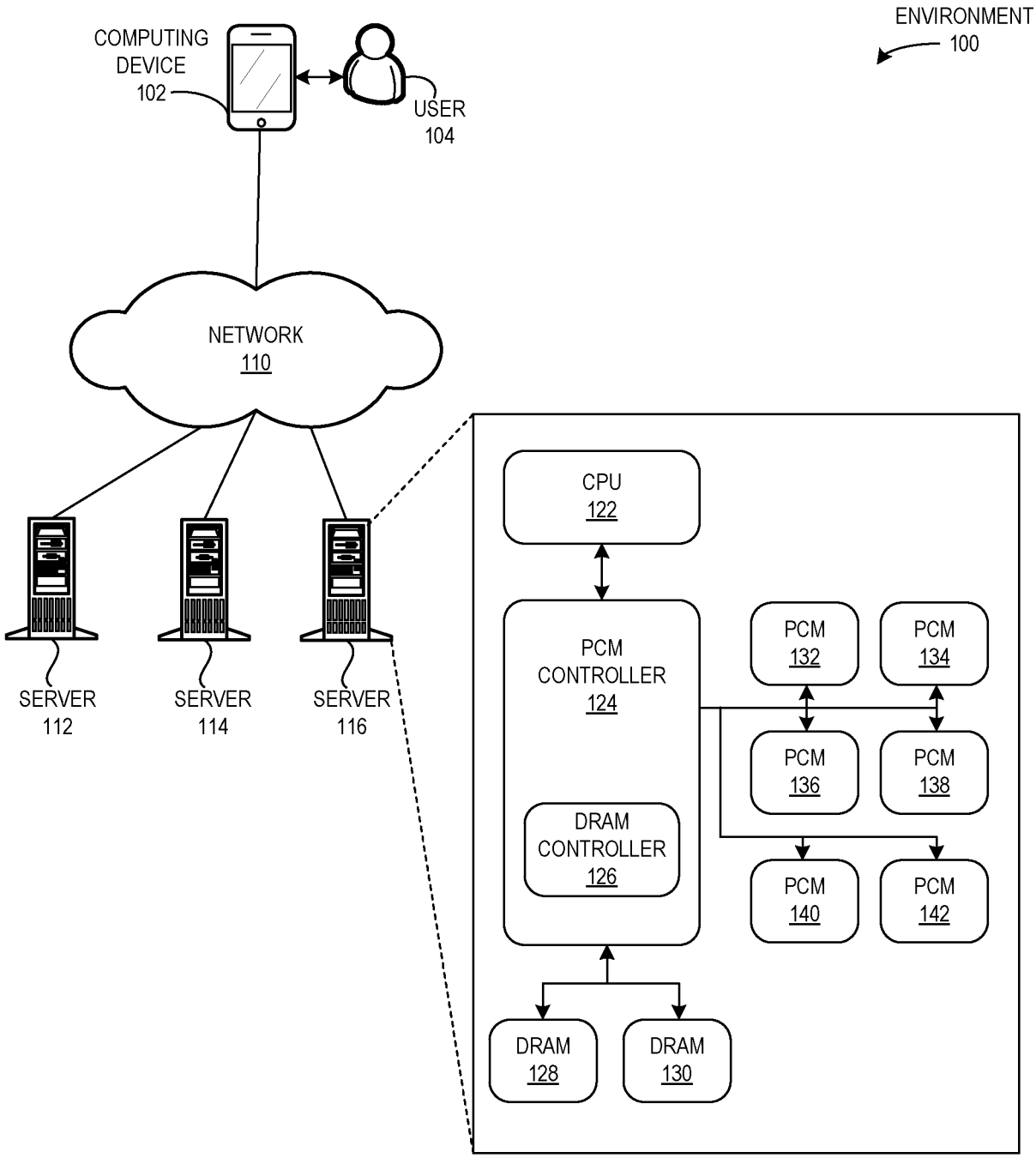

ENVIRONMENT
100
COMPUTING DEVICE
102
USER
104
NETWORK
110
SERVER
112
SERVER
114
SERVER
116
CPU
122
PCM CONTROLLER
124
DRAM CONTROLLER
126
PCM
132
PCM
134
PCM
136
PCM
138
PCM
140
PCM
142
DRAM
128
DRAM
130

FIG. 1

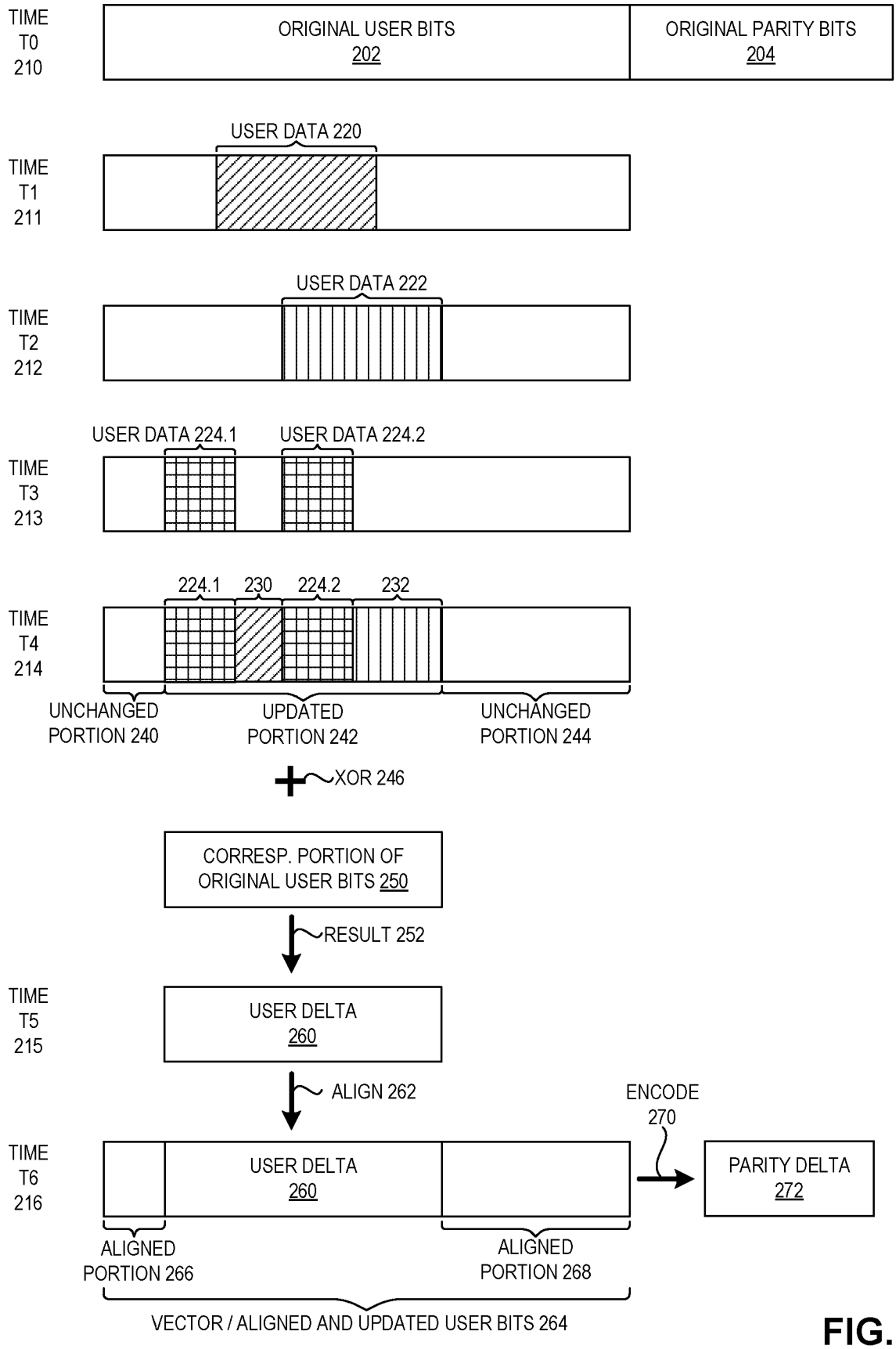

TIME T0 210
ORIGINAL USER BITS 202
ORIGINAL PARITY BITS 204
TIME T1 211
USER DATA 220
TIME T2 212
USER DATA 222
TIME T3 213
USER DATA 224.1
USER DATA 224.2
TIME T4 214
224.1
230
224.2
232
UNCHANGED PORTION 240
UPDATED PORTION 242
UNCHANGED PORTION 244
XOR 246
CORRESP. PORTION OF ORIGINAL USER BITS 250
RESULT 252
TIME T5 215
USER DELTA 260
ALIGN 262
ENCODE 270
TIME T6 216
USER DELTA 260
PARITY DELTA 272
ALIGNED PORTION 266
ALIGNED PORTION 268
VECTOR / ALIGNED AND UPDATED USER BITS 264

FIG. 2

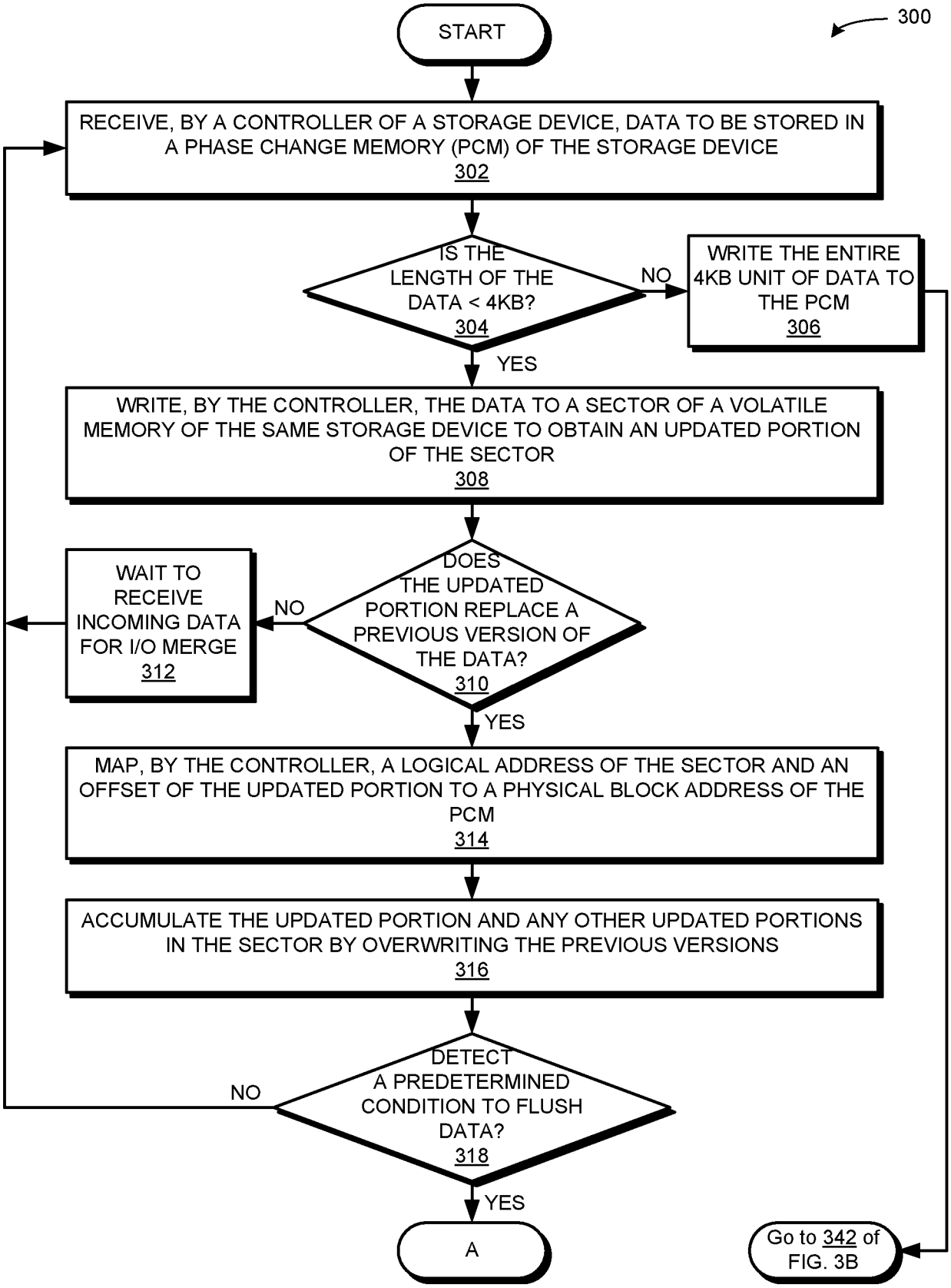

300
START
RECEIVE, BY A CONTROLLER OF A STORAGE DEVICE, DATA TO BE STORED IN A PHASE CHANGE MEMORY (PCM) OF THE STORAGE DEVICE
302
IS THE LENGTH OF THE DATA < 4KB?
304
NO
WRITE THE ENTIRE 4KB UNIT OF DATA TO THE PCM
306
YES
WRITE, BY THE CONTROLLER, THE DATA TO A SECTOR OF A VOLATILE MEMORY OF THE SAME STORAGE DEVICE TO OBTAIN AN UPDATED PORTION OF THE SECTOR
308
DOES THE UPDATED PORTION REPLACE A PREVIOUS VERSION OF THE DATA?
310
NO
WAIT TO RECEIVE INCOMING DATA FOR I/O MERGE
312
YES
MAP, BY THE CONTROLLER, A LOGICAL ADDRESS OF THE SECTOR AND AN OFFSET OF THE UPDATED PORTION TO A PHYSICAL BLOCK ADDRESS OF THE PCM
314
ACCUMULATE THE UPDATED PORTION AND ANY OTHER UPDATED PORTIONS IN THE SECTOR BY OVERWRITING THE PREVIOUS VERSIONS
316
DETECT A PREDETERMINED CONDITION TO FLUSH DATA?
318
NO
YES
A
Go to 342 of FIG. 3B

FIG. 3A

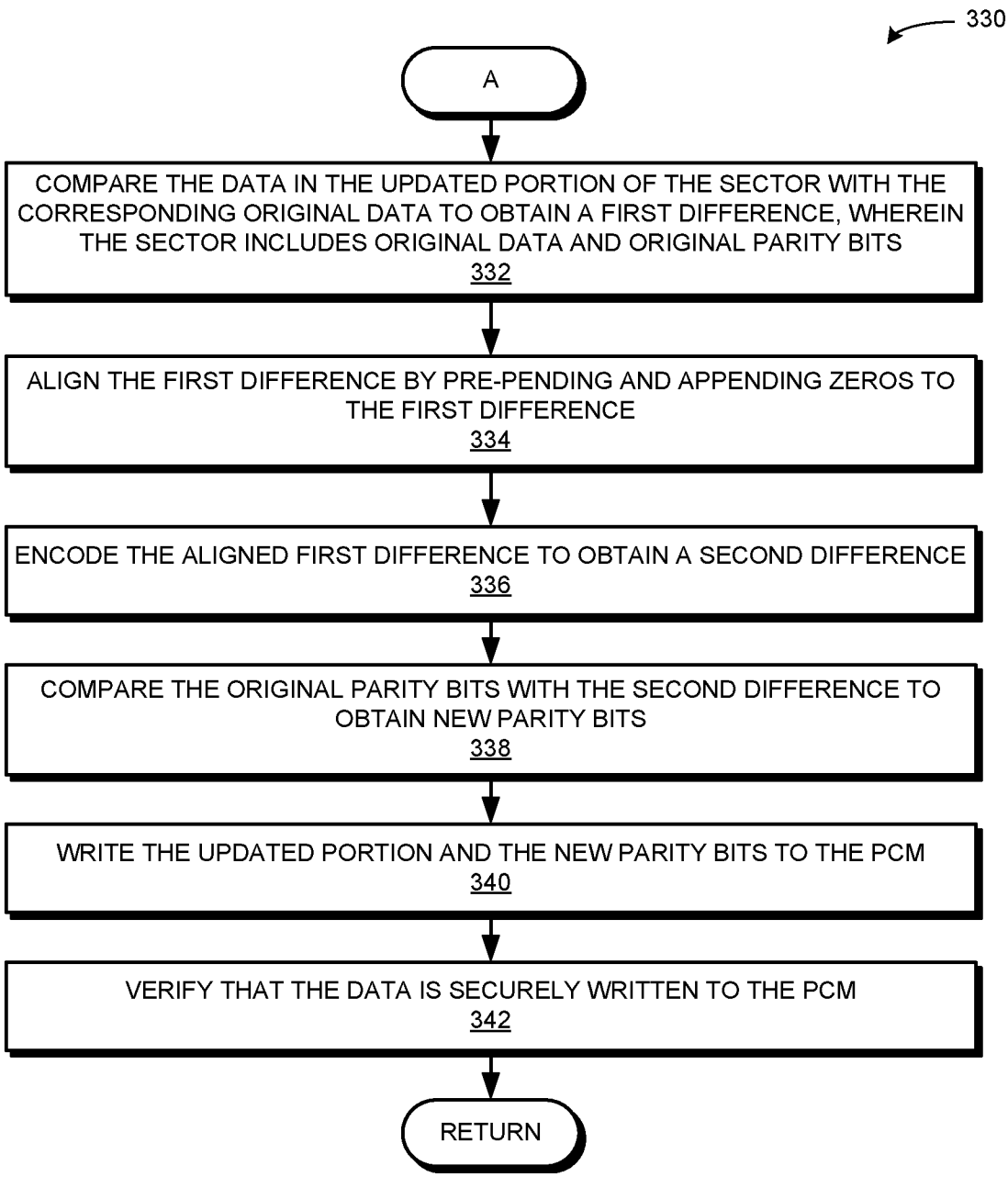

330
A
COMPARE THE DATA IN THE UPDATED PORTION OF THE SECTOR WITH THE CORRESPONDING ORIGINAL DATA TO OBTAIN A FIRST DIFFERENCE, WHEREIN THE SECTOR INCLUDES ORIGINAL DATA AND ORIGINAL PARITY BITS
332
ALIGN THE FIRST DIFFERENCE BY PRE-PENDING AND APPENDING ZEROS TO THE FIRST DIFFERENCE
334
ENCODE THE ALIGNED FIRST DIFFERENCE TO OBTAIN A SECOND DIFFERENCE
336
COMPARE THE ORIGINAL PARITY BITS WITH THE SECOND DIFFERENCE TO OBTAIN NEW PARITY BITS
338
WRITE THE UPDATED PORTION AND THE NEW PARITY BITS TO THE PCM
340
VERIFY THAT THE DATA IS SECURELY WRITTEN TO THE PCM
342
RETURN

FIG. 3B

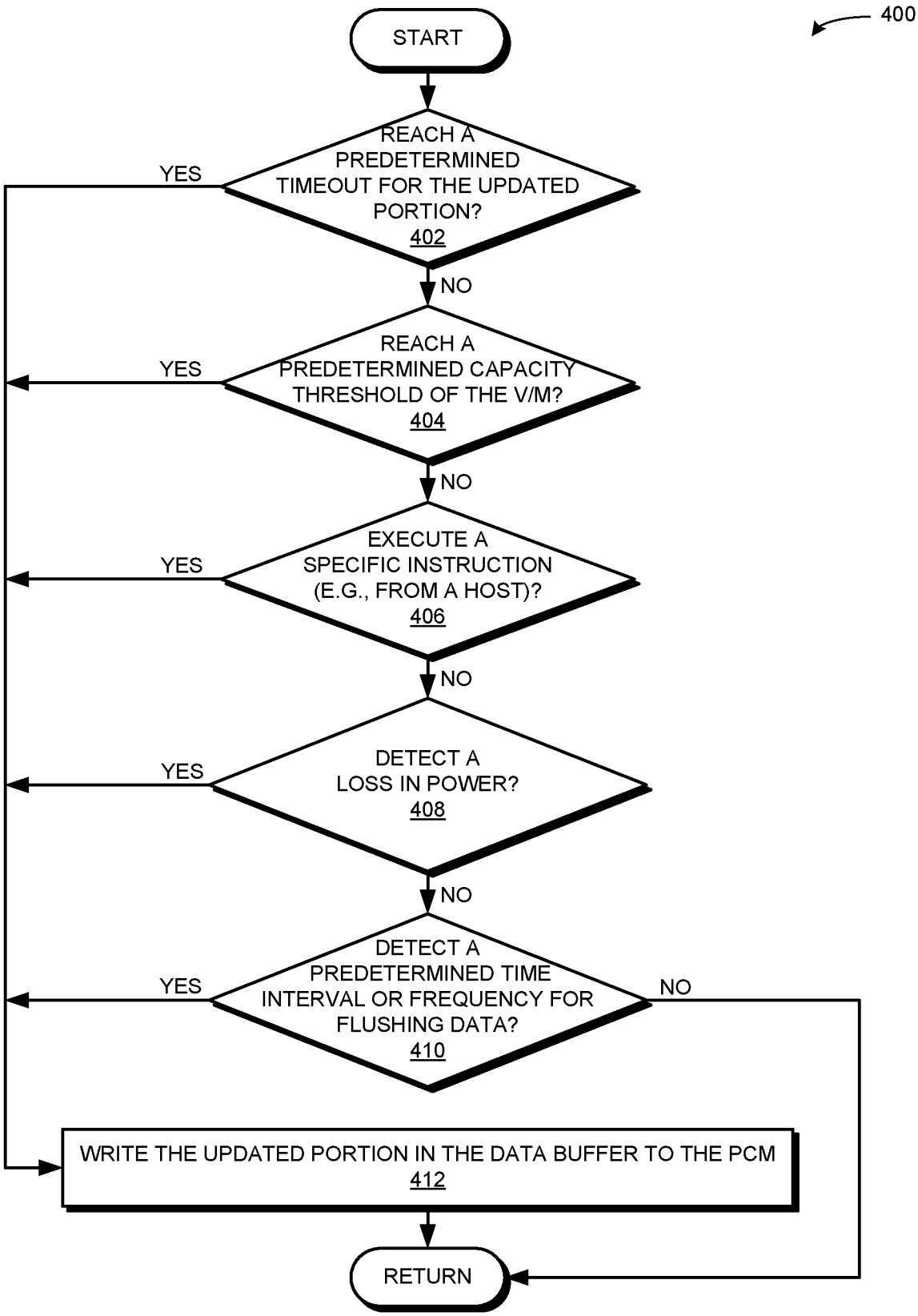

400
START
REACH A PREDETERMINED TIMEOUT FOR THE UPDATED PORTION?
402
YES
NO
REACH A PREDETERMINED CAPACITY THRESHOLD OF THE V/M?
404
YES
NO
EXECUTE A SPECIFIC INSTRUCTION (E.G., FROM A HOST)?
406
YES
NO
DETECT A LOSS IN POWER?
408
YES
NO
DETECT A PREDETERMINED TIME INTERVAL OR FREQUENCY FOR FLUSHING DATA?
410
YES
NO
WRITE THE UPDATED PORTION IN THE DATA BUFFER TO THE PCM
412
RETURN

FIG. 4

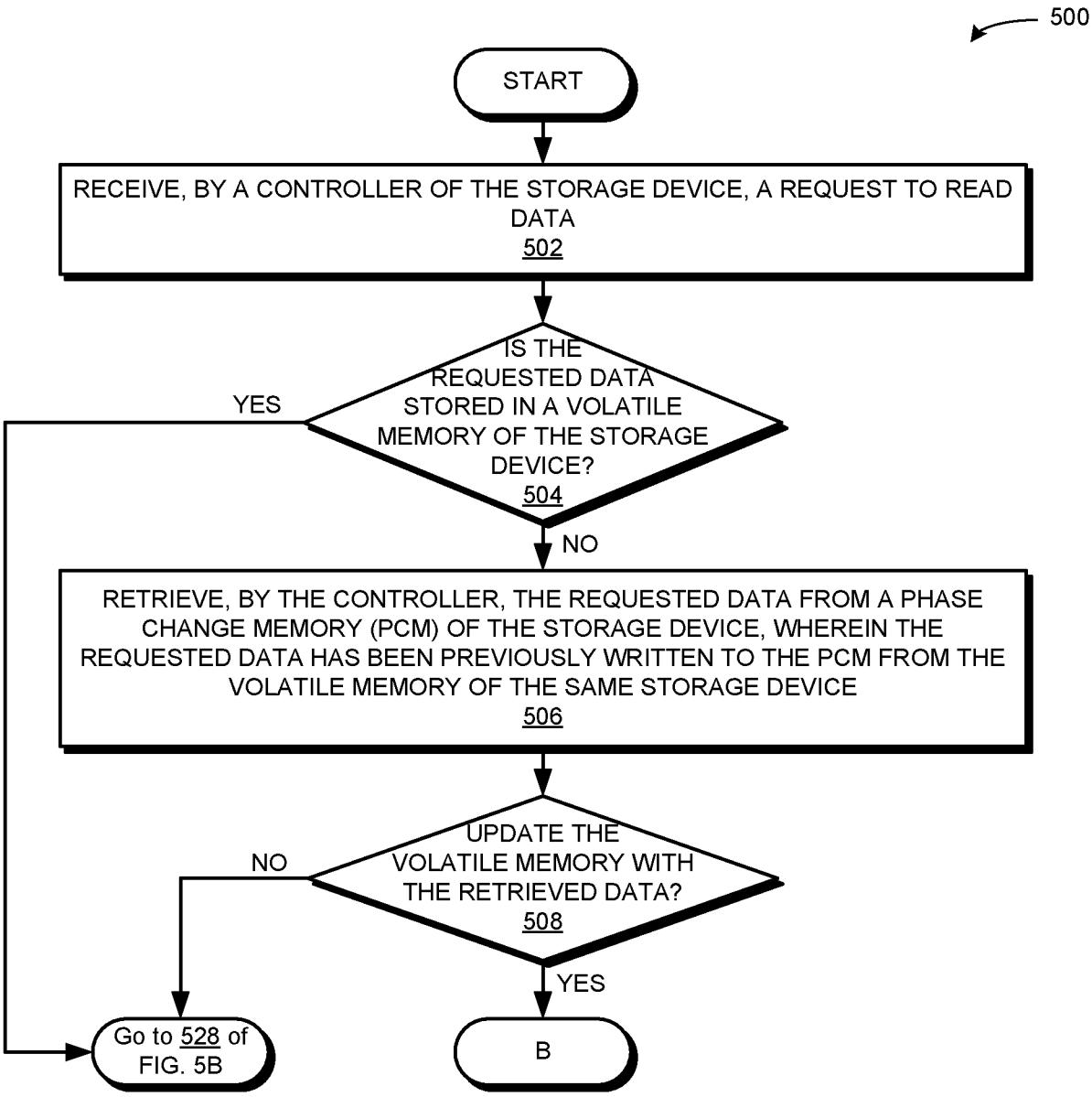

500
START
RECEIVE, BY A CONTROLLER OF THE STORAGE DEVICE, A REQUEST TO READ DATA
502
IS THE REQUESTED DATA STORED IN A VOLATILE MEMORY OF THE STORAGE DEVICE?
504
YES
NO
RETRIEVE, BY THE CONTROLLER, THE REQUESTED DATA FROM A PHASE CHANGE MEMORY (PCM) OF THE STORAGE DEVICE, WHEREIN THE REQUESTED DATA HAS BEEN PREVIOUSLY WRITTEN TO THE PCM FROM THE VOLATILE MEMORY OF THE SAME STORAGE DEVICE
506
UPDATE THE VOLATILE MEMORY WITH THE RETRIEVED DATA?
508
NO
YES
Go to 528 of FIG. 5B
B

FIG. 5A

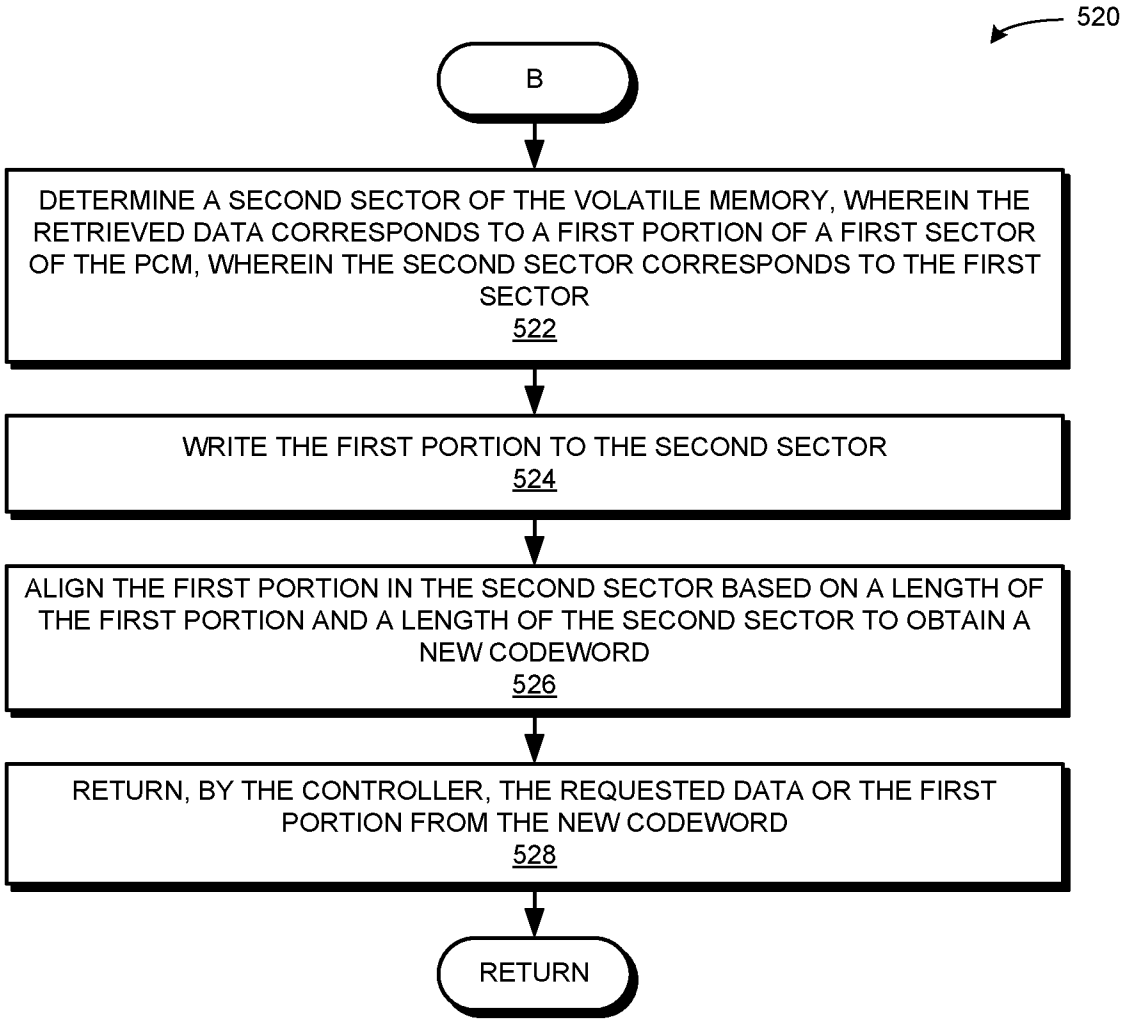

520
B
DETERMINE A SECOND SECTOR OF THE VOLATILE MEMORY, WHEREIN THE RETRIEVED DATA CORRESPONDS TO A FIRST PORTION OF A FIRST SECTOR OF THE PCM, WHEREIN THE SECOND SECTOR CORRESPONDS TO THE FIRST SECTOR
522
WRITE THE FIRST PORTION TO THE SECOND SECTOR
524
ALIGN THE FIRST PORTION IN THE SECOND SECTOR BASED ON A LENGTH OF THE FIRST PORTION AND A LENGTH OF THE SECOND SECTOR TO OBTAIN A NEW CODEWORD
526
RETURN, BY THE CONTROLLER, THE REQUESTED DATA OR THE FIRST PORTION FROM THE NEW CODEWORD
528
RETURN

FIG. 5B

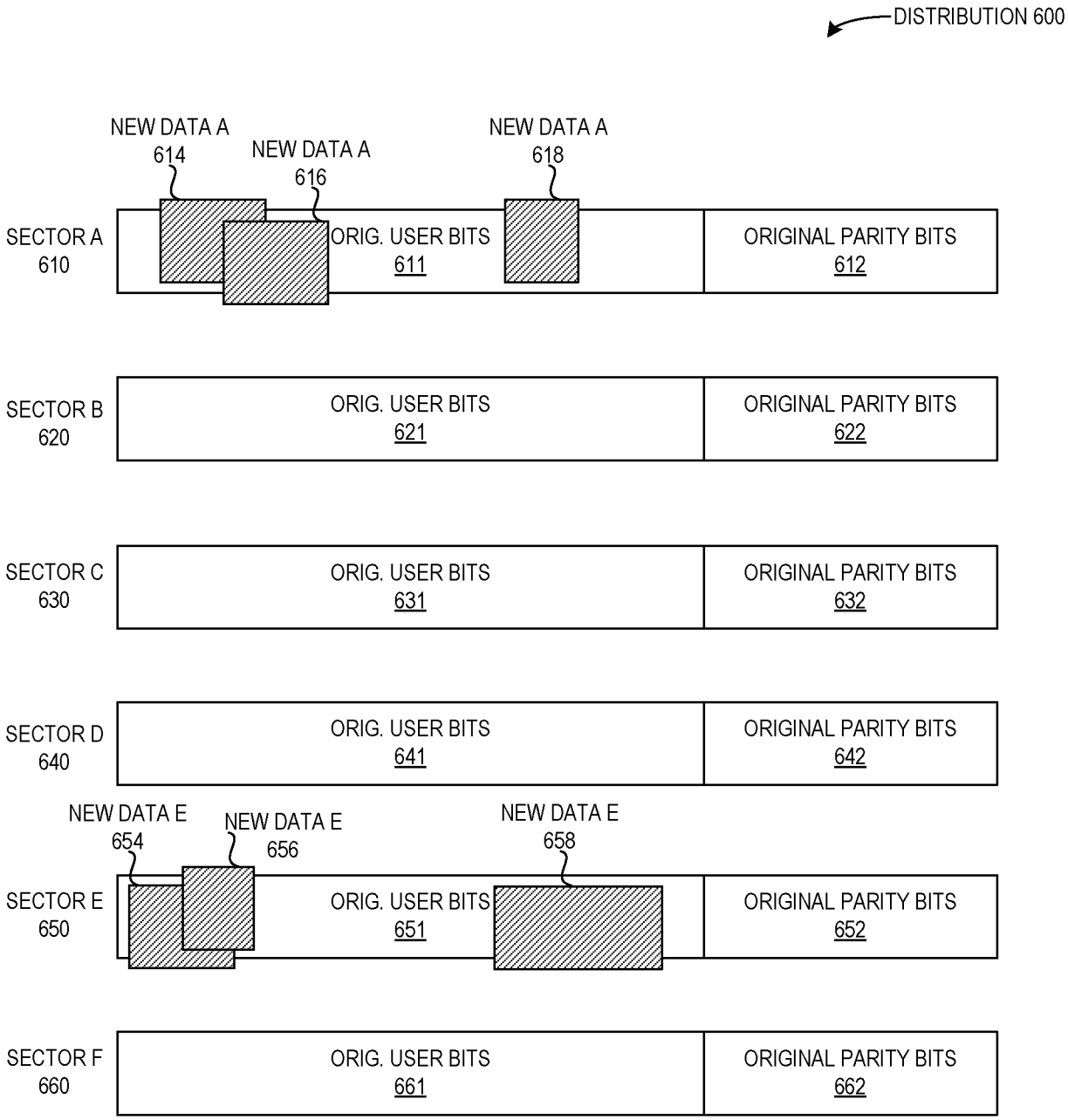

DISTRIBUTION 600
NEW DATA A
614
NEW DATA A
616
NEW DATA A
618
SECTOR A
610
ORIG. USER BITS
611
ORIGINAL PARITY BITS
612
SECTOR B
620
ORIG. USER BITS
621
ORIGINAL PARITY BITS
622
SECTOR C
630
ORIG. USER BITS
631
ORIGINAL PARITY BITS
632
SECTOR D
640
ORIG. USER BITS
641
ORIGINAL PARITY BITS
642
NEW DATA E
654
NEW DATA E
656
NEW DATA E
658
SECTOR E
650
ORIG. USER BITS
651
ORIGINAL PARITY BITS
652
SECTOR F
660
ORIG. USER BITS
661
ORIGINAL PARITY BITS
662

FIG. 6A

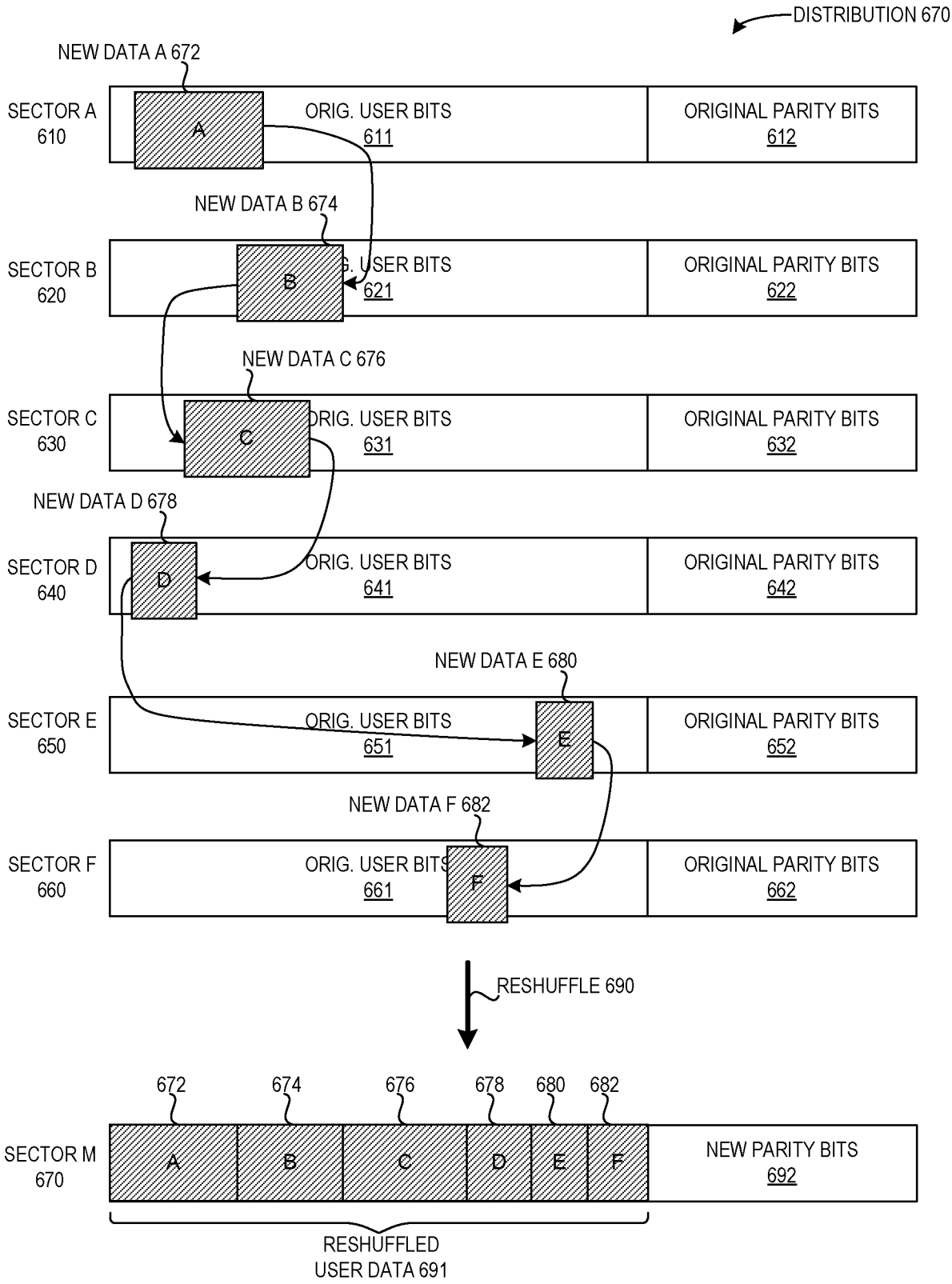

DISTRIBUTION 670
NEW DATA A 672
SECTOR A 610
A
ORIG. USER BITS 611
ORIGINAL PARITY BITS 612
NEW DATA B 674
SECTOR B 620
B
ORIG. USER BITS 621
ORIGINAL PARITY BITS 622
NEW DATA C 676
SECTOR C 630
C
ORIG. USER BITS 631
ORIGINAL PARITY BITS 632
NEW DATA D 678
SECTOR D 640
D
ORIG. USER BITS 641
ORIGINAL PARITY BITS 642
NEW DATA E 680
SECTOR E 650
ORIG. USER BITS 651
E
ORIGINAL PARITY BITS 652
NEW DATA F 682
SECTOR F 660
ORIG. USER BITS 661
F
ORIGINAL PARITY BITS 662
RESHUFFLE 690
672
674
676
678
680
682
SECTOR M 670
A
B
C
D
E
F
NEW PARITY BITS 692
RESHUFFLED USER DATA 691

FIG. 6B

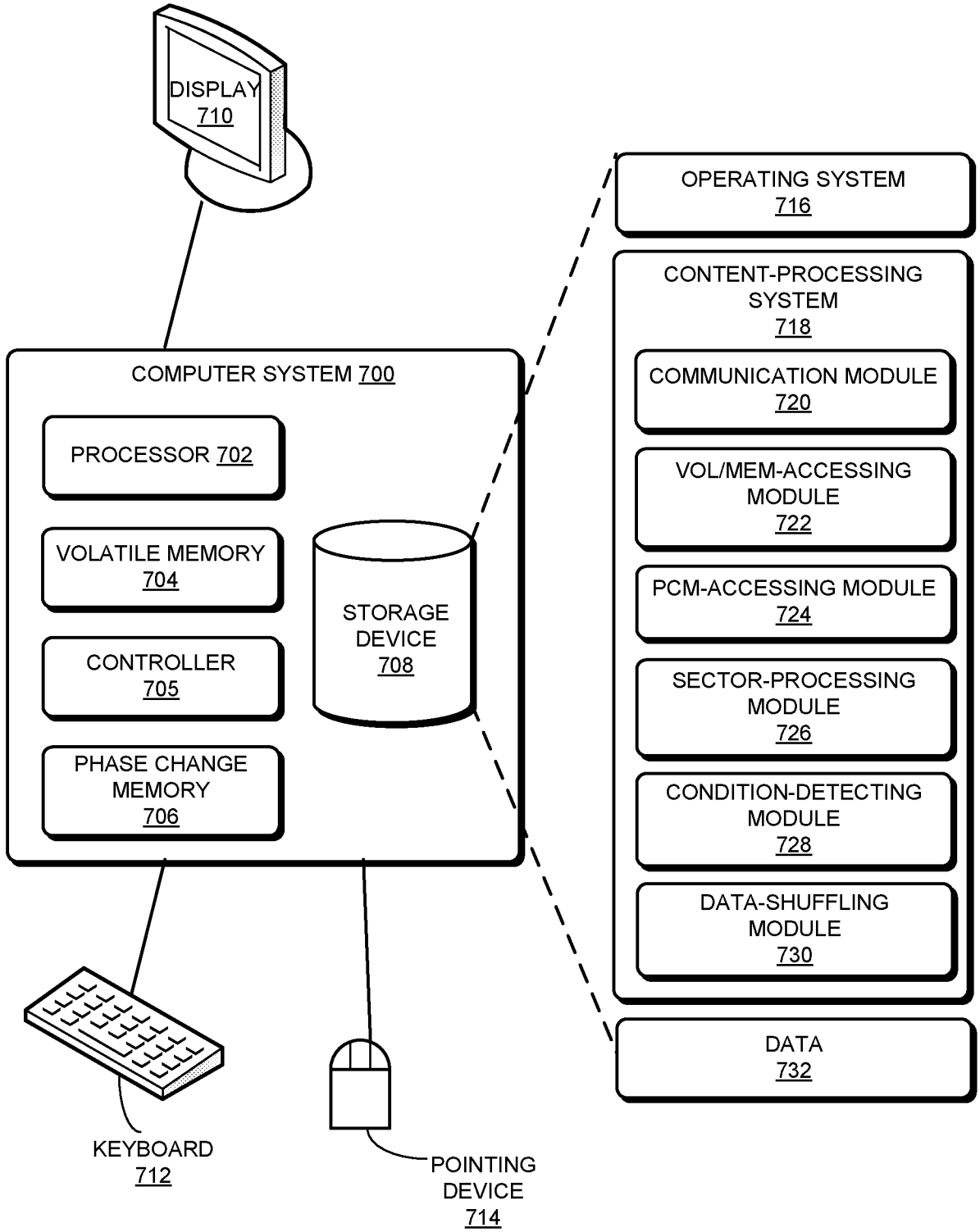

DISPLAY
710
OPERATING SYSTEM
716
CONTENT-PROCESSING SYSTEM
718
COMMUNICATION MODULE
720
VOL/MEM-ACCESSING MODULE
722
PCM-ACCESSING MODULE
724
SECTOR-PROCESSING MODULE
726
CONDITION-DETECTING MODULE
728
DATA-SHUFFLING MODULE
730
COMPUTER SYSTEM 700
PROCESSOR 702
VOLATILE MEMORY
704
CONTROLLER
705
PHASE CHANGE MEMORY
706
STORAGE DEVICE
708
DATA
732
KEYBOARD
712
POINTING DEVICE
714

FIG. 7

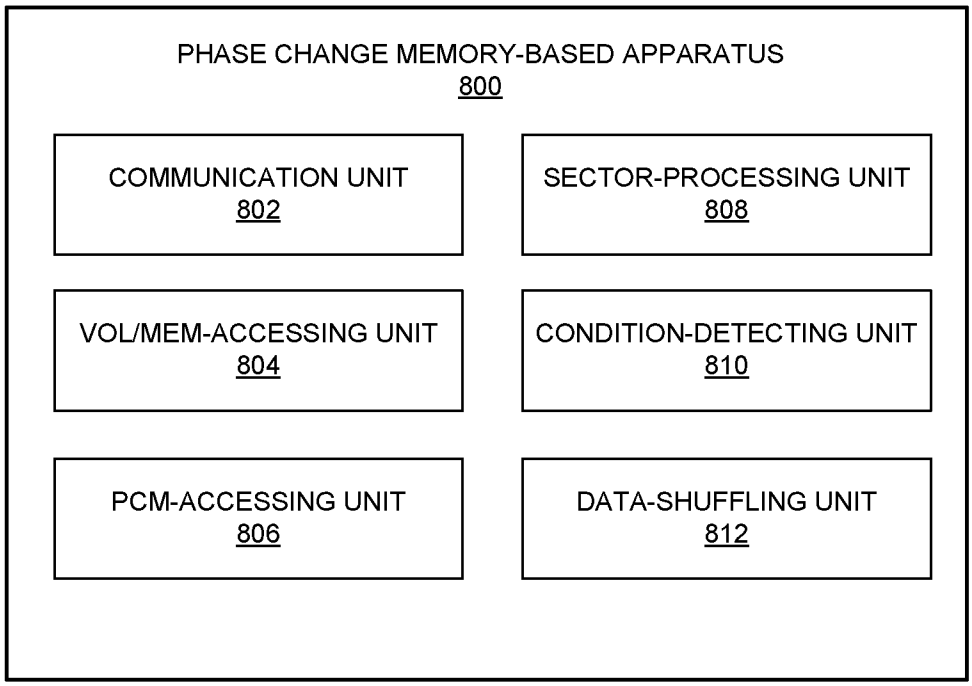

PHASE CHANGE MEMORY-BASED APPARATUS
800
COMMUNICATION UNIT
802
SECTOR-PROCESSING UNIT
808
VOL/MEM-ACCESSING UNIT
804
CONDITION-DETECTING UNIT
810
PCM-ACCESSING UNIT
806
DATA-SHUFFLING UNIT
812

FIG. 8

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US 18/39813

Box No. II Observations where certain claims were found unsearchable (Continuation of item 2 of first sheet)

This international search report has not been established in respect of certain claims under Article 17(2)(a) for the following reasons:

1. ☐ Claims Nos.:
because they relate to subject matter not required to be searched by this Authority, namely:

2. ☐ Claims Nos.:
because they relate to parts of the international application that do not comply with the prescribed requirements to such an extent that no meaningful international search can be carried out, specifically:

3. ☐ Claims Nos.:
because they are dependent claims and are not drafted in accordance with the second and third sentences of Rule 6.4(a).

Box No. III Observations where unity of invention is lacking (Continuation of item 3 of first sheet)

This International Searching Authority found multiple inventions in this international application, as follows:
This application contains the following inventions or groups of inventions which are not so linked as to form a single general inventive concept under PCT Rule 13.1.

Group I: Claims 1-8, 13-20, directed to writing data to volatile memory to obtain an updated portion of a sector and writing that portion to phase change memory in response to detecting a condition.

Group II: Claims 9-12, directed to retrieving requested data from phase change memory that had been previously stored in volatile memory, and writing the retrieved data to volatile memory.

1. ☐ As all required additional search fees were timely paid by the applicant, this international search report covers all searchable claims.

2. ☐ As all searchable claims could be searched without effort justifying additional fees, this Authority did not invite payment of additional fees.

3. ☐ As only some of the required additional search fees were timely paid by the applicant, this international search report covers only those claims for which fees were paid, specifically claims Nos.:

4. ☒ No required additional search fees were timely paid by the applicant. Consequently, this international search report is restricted to the invention first mentioned in the claims; it is covered by claims Nos.:
1-8, 13-20

Remark on Protest

☐ The additional search fees were accompanied by the applicant's protest and, where applicable, the payment of a protest fee.

☐ The additional search fees were accompanied by the applicant's protest but the applicable protest fee was not paid within the time limit specified in the invitation.

☐ No protest accompanied the payment of additional search fees.

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US 18/39813

A. CLASSIFICATION OF SUBJECT MATTER
IPC(8) - G11C 11/00 (2018.01)
CPC - G11C 13/0004, G11C 13/0069, G11C 11/5678, G11C 2213/79, G11C 13/004

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
See Search History Document

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
See Search History Document

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
See Search History Document

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X -- Y	US 2017/0160978 A1 (SAMSUNG ELECTRONICS CO., LTD.) 08 June 2017 (08.06.2017), entire document, especially abstract and para [0039], [0041], [0045]-[0049], [0067], [0079], [0096], Fig. 1, Fig. 8, Fig. 12.	1, 3-8, 13, 15-20 ---------- 2, 14
Y	US 2009/0232158 A1 (FRANK et al.) 17 September 2009 (17.09.2009), entire document, especially abstract and para [0046], [0051].	2, 14

☐ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

* Special categories of cited documents:
"A" document defining the general state of the art which is not considered to be of particular relevance
"E" earlier application or patent but published on or after the international filing date
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
15 October 2018	30 OCT 2018
Name and mailing address of the ISA/US Mail Stop PCT, Attn: ISA/US, Commissioner for Patents P.O. Box 1450, Alexandria, Virginia 22313-1450 Facsimile No. 571-273-8300	Authorized officer: Lee W. Young PCT Helpdesk: 571-272-4300 PCT OSP: 571-272-7774

Form PCT/ISA/210 (second sheet) (January 2015)