PATENT SPECIFICATION (11) 1 590 044

1 590 044

(21) Application No. 39431/77 (22) Filed 21 Sep 1977

(31) Convention Application No. 7628765 (32) Filed 24 Sep 1976 (19) in

(33) France (FR)

(44) Complete Specification Published 28 May 1981

(51) INT. CL.[3] G11C 11/24

(52) Index at Acceptance H3T 2C 2T2X 2T3F 2W2 3J CAS MBV H1K 11A3 11B4 11C1B 11C4 11D3 11D 1BD 1DE 1FE 1FJ 4C11 4C14 4C1R 9C2 GAX

(54) A NON-VOLATILE, LONG MEMORY FOR FAST SIGNALS

(71) We, THOMSON-CSF, a French Body Corporate of 173, Boulevard Haussmann, 75 - PARIS (8e) FRANCE, do hereby declare the invention for which we pray that a patent may be granted to us, and the method by which it is to be performed, to be particularly described in and by the following statement:

The present invention covers a non-volatile, long memory for fast electric signals.

In certain applications it is necessary to have memories which enable data to be stored for a very long time (several months for example) on the one hand and which, on the other, have a sufficiently short recording time to allow fast signals to be recorded. Finally, it is preferable that such a memory be non-volatile, i.e. that it retains its contents when the power supply is cut off.

Known solid state, non-volatile, long life memory systems, among which may be mentioned in particular MNOS type (Metal – Nitride – Oxide – Semiconductor) structures, are not generally very useful for fast signals, of the order of a nanosecond for example, because their recording time are too long.

According to the present invention, there is provided a non-volatile, long memory for fast signals, comprising at least a first storage stage, comprising a capacitor (C) with two terminals (P and Q) and a diode (D) having two terminals (U and P), connected in series, said fast signal being applied to the terminals of said first storage stage; a second storage stage with an MIIS element (E); said first storage stage being arranged such that when said fast signal is applied to the terminals of said first storage stage a quantity of electric charges which quantity is a function of the amplitude of said fast signal, is accumulated and is stored in said first storage stage for a time at least equal to the time required said second stage to store said signal, said storage in said second stage being done by means of the accumulation at least of a fraction of said quantity of charges at the terminals of the MIIS element.

The invention will be better understood with the help of the following description, which is given as a non-limiting example and is illustrated by the drawings attached that show:

Figures 1, 2 and 3 equivalent electrical circuits of different embodiments of a memory device in accordance with the invention;

Figures 4a, 4b and 4c, ways of producing the MIIS element used in the device in accordance with the invention;

Figures 5a, 5b, 5c and 6a, 6b, actual embodiments of the equivalent circuits of Figures 1 and 2;

Figure 7, an actual embodiment of the equivalent circuit of Figure 3;

Figure 8 an actual embodiment of the equivalent circuit of Figure 3, which uses elastic surface waves.

In these various figures, the same references are used for the same elements.

Figure 1 shows the equivalent electrical circuit of one embodiment of a device in accordance with the invention. The diagram is made up as follows:

In series with an input terminal 11 there is a switch T_1, a first connection point U, a diode D, a second connection point P, a second switch T_2 and an output terminal 21. At the point P are connected in parallel a capacitor C on the one hand, and a resistor R in series with an MIIS type structure E on the other. These two parallel branches are connected at a point Q, which is itself connected to a second input terminal 12 and a second output terminal 22. With the polarities adopted on the diagram (diode D going from terminal 11 to point P), the direction of connection of the MIIS element is such that its semiconductor part is connected to point Q.

It may be remembered that an MIIS structure is formed by a layer of metal covered by an insulating layer, which is itself covered by a very thin (a few tens of Angströms thick) second insulating layer and finally by a semiconducting layer. A special case of such a structure is known under the initials MNOS, i.e. Metal – Nitride (of silicon) – Oxide (of silicon) – Semiconductor (silicon). When a

positive voltage with respect to the semiconductor is applied to the metal, electrons coming from the semiconductor pass through the thin insulating layer under a tunnel effect and are trapped at the interface of the two insulating layers. The recording thus obtained can be maintained for a very long time, about a year. Erasure can be obtained by applying a voltage in the opposite direction for example.

In operation, the signal V_s to be recorded is applied between terminals 11 and 12, switch T_1 being closed and switch T_2 open. Voltage Vs thus applied, charge capacitor C through diode D. This forms the first phase of the recording, in which the time to record may be very short, i.e. the signal V_s may be very short, about a nanosecond for example.

After this first phase, part of the charges distribute themselves in the MIIS element E. The electric field they produce between the metal and the semiconductor tends to transfer these same charges from the semiconductor to the interface between the two insulating layers where they are recorded. This MIIS element forms the second stage of the device in accordance with the invention, giving a long, non-volatile recording of the electrical charges in a quantity proportional to the amplitude of the input signal V_s.

As far as the resistor R is concerned, its value is chosen such that quantitatively only capacitor C is concerned in the first phase of recording. Also, the value of capacitor C can then be chosen to be adpated to the characteristics of signal V_s, independantly of the MIIS element.

Reading takes place between terminals 21 and 22 by closing switch T_2, for example by using an MOS type (Metal – Oxide – Semiconductor) field effect transistor. In this case, this transistor's grid capacity may act the role of the capacitor C.

Signal V_s applied to input terminals 11 and 12 may be sampled first, the opening of switch T_1 then enclosing the sample to be recorded. Sampling can also be carried out directly by switch T_1.

Erasure of the information stored in the MIIS element is obtained by the application of a reverse electrical field, i.e. directed from the semiconductor to the metal, thanks to a signal applied to terminals 11 and 12 for example.

It may be noted that, in this embodiment, on the one hand signal V_s must always have the same sign (positive in the case in the figure) and, on the other, the charging time for capacitor C is a function of the amplitude of V_s. This embodiment is therefore more especially adapted to digital signals.

Figure 2 shows the equivalent electrical circuit of another embodiment of the recording device in accordance with the invention.

On this diagram, there is the capacitor C in parallel with resistor R and the MIIS element E connected in the same direction as in Figure 1. The signal V_s to be recorded is applied between terminals 11 and 12, terminal 12 being connected to point Q as before. Terminal 11 is connected, when a switch T is in the position T_1., to point P through a capacitor C_1. Output terminals 21 and 22 are connected respectively to capacitor C_1 when switch T is in position T_2, and to point Q. Diode D, a connection point U, a voltage source E_1, two connection points N and M and a coupling device 33 enabling a signal V_e to be introduced into the circuit, are also connected in series between points P and Q.

A capacitor, a voltage source and a switch in series are also shown dotted in Figure 2. They are either connected between points P and Q (C_{a1}, V_{a1} and T_{a1}), or C_{a2}, V_{a2} and T_{a2}) connected to the terminals of a capacitor C_{a3} placed between points M and N; their role will be discussed later.

In operation, the signal to be recorded V_s, applied between terminals 11 and 12, polarizes diode D more or less according to its amplitude. If the capacity of C_1 is greater than that of diode D, signal V_s is practically at the terminals P and Q of capacitor C. Voltage E_1 can be introduced in series with D so that, no matter what the positive or negative amplitude of the signal diode D is always polarized in the reverse direction. When a pulse of amplitude V_e greater than that of V_s is applied to element 33 in a direction such that it causes diode D to conduct, the voltage V_e (or $V_e - E_1$) is found at the terminals of capacitor C.

As previously , after this first phase, part of the charges are distributed in the MIIS element E and the electric field thus produced tends to transfer these same charges to the interface of the two insulating layers where they are recorded.

The recording process during the second phase can be controlled with advantage by the auxiliary voltage V_a, either to increase the speed or prevent an increase or again to eliminate the charges already stored, i.e. to erase.

As was said above, voltage V_a can be introduced into the circuit in two ways:

– either between points P and Q, the purpose of capacitor C_{a1} being to prevent the drift of the charges accumulated towards the source V_{a1};

– or between points M and N, the link MN being replaced by a high value capacitor C_{a3} and the source V_{a2} being placed at the terminals of C_{a3}, capacitor C_{a2} having the same role as capacitor C_{a1} previously.

In either case, an electric field is produced in the MIIS, from the metal towards the semiconductor, after the first recording phase (switch T_a then being closed) and an insulator-insulator interface charging current appears. The MIIS element E being previously more or less charged depending on the amplitude of

signal V_s the electric field appearing in the MIIS is a function of V_s and hence of the quantity of charges trapped.

It may be noted that, for small values of said quantity of charges trapped, this function is linear. The role of voltage V_a, which must then be much greater than the potential difference induced by signal V_s, is essentially to accelerate the process and make the effects linear. Finally, on the diagram is shown a direction for voltage V_a such that it makes the recording process easier; evidently, by reversing the direction of V_a, the inhibition of the recording process or even the erasure of the data stored can be obtained.

In the diagram of Figure 2, reading can be done as in the case of Figure 1 at terminals 21 and 22, switch T being in the position T_2.

Erasure is obtained by subjecting the MIIS element to a reverse electric field (directed towards the metal) by the application of a potential difference between points P and Q, the circuit then being cut between points M and N.

This embodiment enables a quantity of charges proportional to the signal to be stored, no matter what the sign of this signal, and in that way is adapted to the case of analog signals. Sampling is here carried out by the writing pulse V_e.

Figure 3 shows the equivalent electrical circuit of a third embodiment of the recording device in accordance with the invention.

This embodiment is identical to that of Figure 2 except for what concerns the MIIS element E and resistor R. These are connected in Figure 3 between points P and N, the metallic part of the MIIS being placed on the side of point P and the semi-conductor part on the side of point N.

The operation in two phases is analogous to that of the device in Figure 2 and, in the same way, it is possible to control the second phase by the addition of an auxiliary voltage V_a.

As far as erasure of the data stored in the MIIS element is concerned, this cannot be obtained by the application of a positive potential difference V_{N-P} because diode D is then short-circuiting the MIIS element. Then, the lighting of the MIIS can be used to accelerate the output of electrons from the insulator-insulator interface traps.

Figures 4a, 4b and 4c show ways of producing the MIIS element E.

On Figure 4a is shown a silicon substrate 1 covered with a thin oxide layer 2 on which a silicon nitride layer 3 forming the second insulating layer is deposited, followed by a layer of metal 4. An MNOS element is thus obtained.

Another method is shown in Figure 4b. A silicon substrate 7 is covered with a thick layer of silicon oxide in which is produced, e.g. by ion implant, a zone 6 as trap for the charge carriers. That zone is created to a depth controlled by the energy of the implanted ions and such that the oxide thickness between zone 6 and the silicon 7 is small. The oxide 8 is then covered with a metallic layer 5. The silicon 7 may be, for example, of polycrystalline silicon doped with type P impurities.

A third method is shown in Figure 4c. It consists in oxidizing (layer 6) a highly doped sub strate of silicon 9 and then in implanting low energy ions to produce a trap area 10 near the oxide surface 6. Then a semiconductor layer 41 is deposited, type P polycristalline silicon for example. The silicon 9 here plays the role of the metallic layers (4 and 5) in the preceding figures.

Figures 5a and 5b show a first mode of integrated production of the devices of Figures 1 and 2, Figure 5c being their equivalent electrical circuit.

The device in Figure 5a is formed by a semiconductor substrate 13, of type N silicon for example, covered successively by:

- an insulating layer 14, silicon oxide for example, except in a zone 15 which is covered with a conducting deposit, platinium for example, which forms with substrate 131 a Schottky junction;
- a conducting layer 16 such as very slightly resistive polycrystalline silicon, preferably of type P, which covers layer 14 and area 15;
- an insulating layer 17, of silicon oxide for example, which covers layer 16 except where an electrical connection point P is made on the latter. An area 20 which forms a trap area for the charge carriers as described in Figure 4b, is made by ion implantation in layer 17 at the level of area 15;
- a metallic layer in two parts, 18 and 19, part 19 being above areas 15 and 20 and forming the connection Q and part 18 being outside areas 15 and 20 and forming a connection A. Figure 5b represents the device of the preceding figure in which electrode A has been suppressed.

Figure 5c is the equivalent electrical circuit of the Figure 5a and 5b. It shows that the MIIS element E (formed by layers 16, 17, 20 and 19) is connected in series with diode D (formed by the Schottky type junction between layers 13 and 15). In the case of Figure 5a, the device further comprises a capacitor C_{al} (formed by layers 16, 17 and 18) connected to common point P (formed by layer 16) between diode D and element E.

As can be seen from the figures, it is a way of producing the diagrams of Figures 1 and 2, between points U, P and Q, the MIIS element E also playing the role of capacitor C. It may be noted that, because of the types of conductivity chose, diode D is conducting from P towards U and the element E is inversed, which requires an adaptation of the polarities of the voltage sources shown in Figures 1 and

2.

Capacitor C_{a1} between point P and A is only required when the auxiliary voltage V_a is applied between points P and Q.

Figures 6 show a varient of Figures 5 which contain a capacitor C distinct from that of the MIIS element.

Figure 6a is identical to Figure 5b except for the areas 16 and 20 on the latter. Layer 23 (Figure 6a), which replaces layer 16 on Figure 5b is still formed by polycristalline silicon but its resistivity is higher than that of layer 16. As for area 20 of traps for charge carriers in Figure 5b, it is replaced by an area 24 on Figure 6a of the same type but extending in ring fashion around layer 15.

Figure 6b shows the equivalent circuit of this device which contains:

- capacitor C, connected between points P and Q, formed by layer 15, insulator 17 and conductor 19 above the area 15;
- element E, connected between the same points P and Q, formed in rings by layers 23, 24, 27 and 19; resistor R in series with element M is obtained by the use of layer 23 of polycrystalline silicon of higher resistivity;
- diode D connected between P and U in the same direction as for Figure 5, formed by layer 15 and substrate 13.

The device of Figure 6a appears then as a variant of Figure 5b. It is also possible to adapt it to obtain a variant similar to Figure 5a with its capacitor C_{a1}.

As was said above, an MOS type (Metal – Oxide – Semi-conductor) field effect transistor, or MOSFET transistor, can be used for reading, and integrated in the devices of Figures 5 and 6 for this purpose. It is then the electrode Q which acts as gate for the MOSFET transistor.

Figure 7 shows a mode of integrated production of the circuit in Figure 3.

On this figure can be seen:

- a semiconductor substrate, e.g. of silicon, doped N^+ in its lower part 28 and N in its upper part 27;
- an insulating layer 25, of silicon oxide for example, deposited on substrate 28;
- a conducting layer 26, forming the connection point Q, deposited on insulating layer 25;
- insulating layer 14, that covers layer 27 except in area 15 and in area 29 where, as layer 27 does not exist, insulating layer 14 covers directly substrate 28;
- the metallic deposit on area 15, which forms a Schottky junction with substrate 27;
- the area 24 of traps for charge carriers which spreads as a ring round area 15;
- the layer 23 of polycrystalline silicon covering area 15 and its immediate neighbourhood;
- insulating layer 17 covering layer 23;
- conducting layer 19 covering layer 17 and forming connection point M in Figure 3.

In the dip 29 and above insulator 14 a metallic electrode 30 is deposited, which has to be connected to switch T (see Figure 3).

Referring to the diagram in Figure 3, it may be seen that it really is the equivalent electrical circuit of the device in Figure 7 in which:

- the MIIS element E is formed by layers 27, 14, 24 and 23;
- resistor R, in series with it, has its value fixed by the resistivity of the polycrystalline silicon 23;
- diode D, connected in parallel with the preceding elements is formed in layers 15 and 27;
- capacitor C is formed by substrate 28, insulator 25 and electrode 26;
- point P is formed by substrate 28 (or 27);
- capacitor C_1 is formed by substrate 28, insulator 25 and electrode 30.

To end up, the device in Figure 7 has no voltage source E_1 but has between M and N a capacitor such as C_{a2} (shown on Figure 2) which is formed by layers 23, 17 and 19.

In a variant of this device, electrode Q can be placed on top using the same method as that for electrode 30.

Figure 8 shows another embodiment of the circuit in Figure 3, which is adapted to the recording of a signal carried by elastic surface waves.

It comprises:

- a piezoelectric substrate 34 on whose surface elastic wave trains S, which represent the data to be recorded, may be propagated,
- a flat electrode 35 covering the lower surface of substrate 34 when the elastic waves S are moving on the upper face, the electrode forming connection point Q in Figure 3,
- a semiconductor substrate 39, of type N silicon for example, plated opposite the upper surface of substrate 34 but not in contact with it, the upper surface of substrate 39 forming connection point N.

The lower surface of substrate 39 is covered with an insulating layer 37, of silicon oxide for example, which leaves the areas 40 that are covered with a metallic layer to form the Schottky junctions, and then by a low resistively polycristalline layer 36 which overlaps layer 37. As before a trap area 38 for charge carriers is made in insulating layer 37 by ion implantation for example, to give MIIS structures formed by part of the deposits 36, area 38, layer 37 and substrate 39.

The capacitor C is formed by the space between layer 36 and electrode 35.

In operation, writing pulse V_e is applied as shown in Figures 3 and 8, i.e. between point Q (piezoelectric substrate 34) and point N (semiconductor substrate 39). When the elastic wave has passed, a quantity of charges is stored in each diode which is a function of the electric field associated with the elastic wave that acts as voltage V_s in the diagram of Figure 3. This process is analogous to that

which is described in the British Patent Applications No 54 558 74 and 23 972 75 held by THOMSOM-CSF.

During the second phase of recording, i.e. the charging of the MIIS element, signal S no longer exists and the three elements D, E and C produce an electric field at the terminals of the MIIS element which, in accordance with the same procedure as before, enables charges to be transferred to area 38.

Reading is obtained between semiconductor substrate 39 and electrode 35 by using another elastic wave, called the read wave, which induces an electromotive force whose amplitude is a function of the number of charges stored, between these elements.

WHAT WE CLAIM IS:

1. A non-volatile, long memory for fast signals, comprising at least a first storage stage, comprising a capacitor (C) with two terminals (P and Q) and a diode (D) having two terminals (U and P), connected in series, said fast signal being applied to the terminals of said first storage stage; a second storage stage with an MIIS element (E); said first storage stage being arranged such that when said fast signal is applied to the terminals of said first storage stage a quantity of electric charges, which quantity is a function of the amplitude of said fast signal, is accumulated and is stored in said first storage stage for a time at least equal to the time required for said second stage to store said signal, said storage in said second stage being done by means of the accumulation at least of a fraction of said quantity of charges at the terminals of the MIIS element.

2. A memory as claimed in Claim 1, wherein said diode (D) and said capacitor (C) are connected in series at the first terminal (P) of said capacitor (C) and of said diode, said fast signal (V_s) being applied between the second terminal (U) of said diode and the second terminal (Q) of said capacitor, which are the terminals of said first stage, said second stage being connected to the terminals (P and Q) of said capacitor (C).

3. A memory as claimed in Claim 1, wherein said diode (D) and said capacitor (C) are connected in series at the first terminal (P) of said capacitor and of said diode, their other terminals (U and Q) forming the terminals of said first stage, said first stage further comprising a further capcitor (C_1) and a switch (T), said further capacitor (C_1) being connected between the first terminal (P) of said capacitor (C) and said switch (T), said fast signal (V_s) being applied between the second terminal (Q) of the capacitor (C), which forms the second terminal of the first stage, and said switch (T), said second stage being connected in parallel to terminals (P and Q) of said capacitor (C), the storing in said first stage being obtained by the application of a write signal (V_e) to terminals (U and Q) of said first stage, and the reading of the signal stored in said second stage being obtained between said switch (T) and said second terminal (Q) of the capacitor (C).

4. A memory as claimed in Claim 1, wherein said diode (D) and said capacitor (C) are connected in series at the first terminal (P) of said capacitor and of said diode, their other terminals (U and Q) forming the terminals of said first stage, the latter further comprising a switch (T) and a further capacitor (C_1), connected,between the first terminal (P) of said capacitor (C) and said switch (T), said fast signal (V_s) being applied between the second terminal (Q) of said capacitor (C), which forms the second terminal of said first stage, and said switch (T), the second stage being connected in parallel to the terminals (U and P) of said diode (D), the storing in said first stage being obtained by the application of a write signal (V_e) between the terminals (U and Q) of said first stage and the reading of the signal stored in said second stage being obtained between said switch (T) and said second terminal (Q) of said capacitor (C).

5. A memory as claimed in Claim 3, wherein said first stage further comprises a voltage source (E_1) for polarizing said diode (D), connected in series with the latter.

6. A memory as claimed in Claim 3, further comprising an auxiliary assembly formed by a voltage source (V_a) in series with a capacitor (C_a) connected between the terminals (P and Q) of said capcitor (C).

7. A memory as claimed in Claim 3, further comprising an auxiliary assembly formed by a voltage source (V_a) in series with a capacitor (C_a) connected between the terminals of a third capacitor (C_{a3}) which is connected between the first terminal (U) of the first stage and the said diode (D).

8. A memory as claimed in Claim 1, wherein said second stage further comprises a resistor (R) in series with the MIIS element (E).

9. A memory as claimed in Claim 1, wherein said capacitor (C) is formed by said MIIS element (E).

10. A memory as claimed in Claim 2 or 3, formed by a semi-conducotr substrate (13) covered with a first insulating layer (14) except in an area of said substrate (13) which is covered with a metallic layer (15) that forms with said substrate (13) a Schottky junction, said first insulating layer (14) and said metallic layer (15) being covered with a layer of semiconductor material (16) bearing a connection (P) which forms the first terminal of said capacitor (C), said semiconductor layer (16) being covered with a second insulating layer (17) containing an area (20) of traps for charge carriers right above said metallic layer (15), said second insulating layer (17) being covered with a conducting layer (19), which forms the second terminal (Q) of said capacitor (C).

11. A memory as claimed in Claim 2 or 3,

formed by a semiconductor substrate (13) covered with a first insulating layer (14), except in an area of said substrate which is covered with a metallic layer (15) forming with said substrate (13) a Schottky junction, said first insulating layer (14) and said metallic layer (15) being covered with a layer of semiconductor material (23) bearing a connection (P), which forms the first terminal of said capacitor (C), said semiconductor layer (23) being covered with a second insulating layer (17) containing an area (24) of traps for charge carriers placed in ring fashion around said metallic layer (15), said second insulating layer (17) being covered with a conducting layer (19) above said metallic layer (15) and said trap area (24), which forms the second terminal (Q) of said capacitor (C).

12. A memory as claimed in Claim 6 and one of Claims 10 and 11, further comprising a further conducting layer (18) on said second insulating layer, not in contact with said conducting layer (19), forming with said second insulating layer (17) and said semiconductor layer (16) the capacitor (C_a) of the said auxiliary assembly.

13. A memory as claimed in Claim 4, formed by a semiconductor substrate (27, 28) having on its lower surface a first insulating layer (25) covered with a first conducting layer (26) which forms the second terminal (Q) of said capacitor (C), said substrate having on its upper surface a second insulating layer (14), except in an area of the substrate which is covered with a metallic layer (15) that forms with said substrate a Schottky junction, said second insulating layer (14) having an area (24) of traps for charge carriers, placed in ring fashion around said metallic layer (15), and having on the one hand, a layer of semiconductor material (23) above said trap area (24) and said metallic mayer (15) and, on the other, a second conducting layer (30), which is not in contact with said semiconductor layer (23) and forms a connection joined to said switch (T), said semiconductor layer (23) being covered in succession with a third insulating layer (17) and a third metallic layer (19) forming the first terminal of said first stage.

14. A memory as claimed in Claim 4, comprising:

— a piezoelectric substrate (34) on which elastic waves may be propagated that represent the said fast signal (V_s), the lower surface of said substrate (34) being covered with an electrode (35) forming the second terminal (Q) of said capacitor (C).

— a semiconductor substrate (39) placed opposite the upper surface of said piezoelectric substrate (34), that has a connection forming the first terminal of said first stage, and on its lower surface an insulating layer (37), except in areas of the semiconductor substrate (39) which are each covered with a metallic layer (40) that forms with said semiconductor substrate (39) a Schottky junction, said insulating layer (37) having an area (38) of traps for charge carriers, said metallic layers (40) being covered with a semiconductor layer (36); reading being carried out between said semiconductor substrate (39) and said electrode (35) using an elastic read wave.

15. A memory as claimed in one of Claims 10 to 14, wherein said semiconductor substrate is formed of type N silicon, said insulating layers by silicon oxide, said semiconductor layer by polycrystalline silicone, said trap areas for charge carriers being made by an insulating layer with ion implantation therein.

16. A memory substantially as hereinbefore described with reference to any of the following, Modified by any one of Figures 4; optionally as Figure 1, or Figure 1 and Figure 5*a* optionally and Figure 5*c*; or Figure 2, or Figure 2 and Figure 5*b* optionally and Figure 5*c*; or either Figure 1 or Figure 2 and Figure 6*a* optionally and Figure 6*b*; or Figure 3 optionally and Figure 7 or Figure 8 of the accompanying drawings.

HASELTINE, LAKE & CO.,
Chartered Patent Agents,
Hazlitt House,
28, Southampton Buildings,
Chancery Lane, London, WC2A 1AT
Agents for the Applicants

Printed for Her Majesty's Stationery Office by MULTIPLEX techniques ltd., St. Mary Cray, Kent. 1981. Published at the Patent Office, 25 Southampton Buildings, London WC2 1AY, from which copies may be obtained.

1590044 COMPLETE SPECIFICATION

5 SHEETS *This drawing is a reproduction of the Original on a reduced scale*

Sheet 1

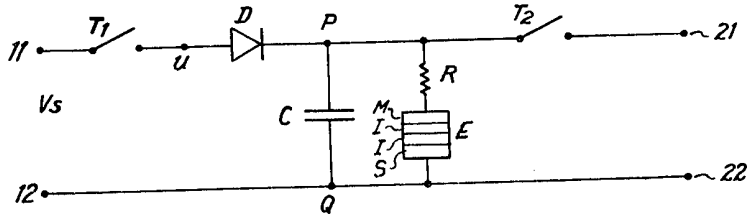


FIG. 1

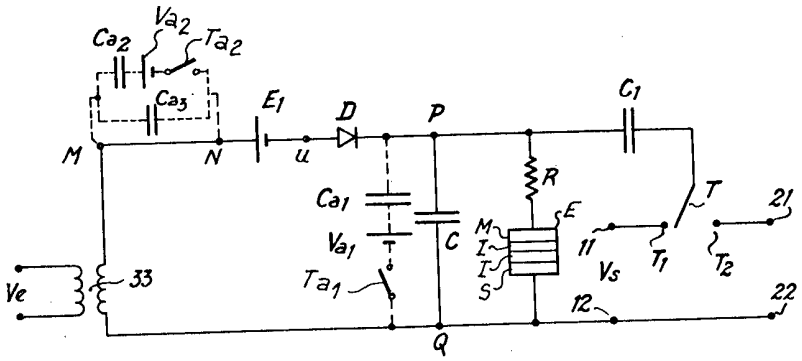


FIG. 2

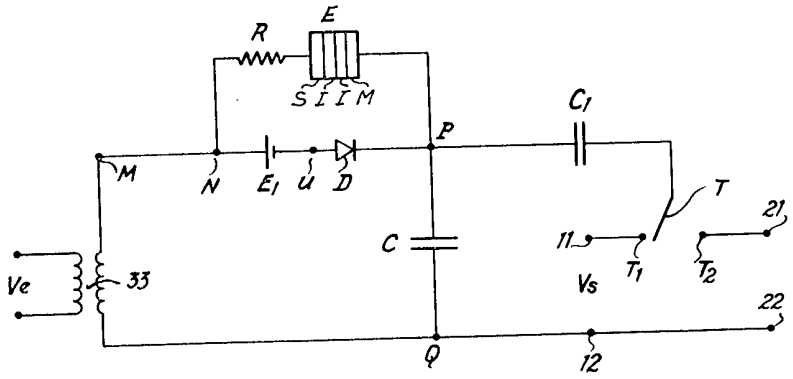


FIG. 3

1590044 COMPLETE SPECIFICATION
5 SHEETS *This drawing is a reproduction of the Original on a reduced scale*
Sheet 2

FIG. 4 (a)

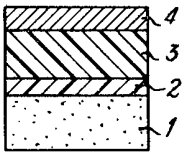
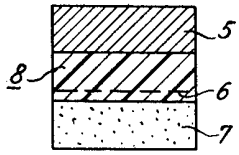


FIG. 4 (b)



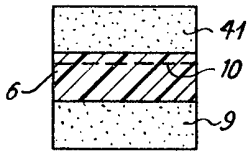
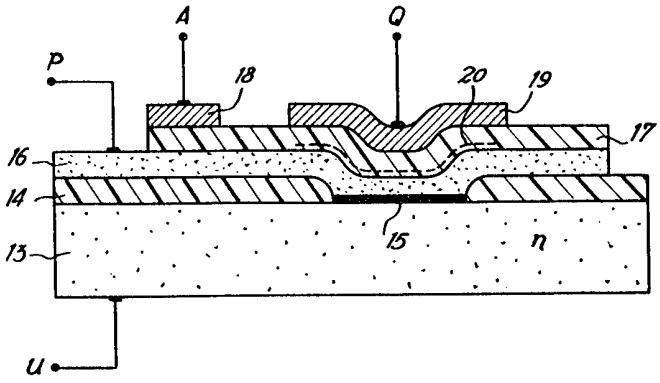
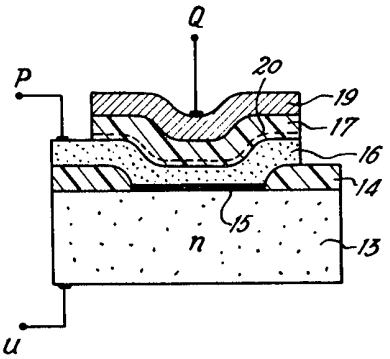


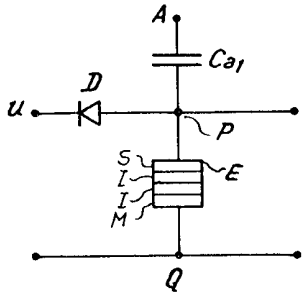
FIG. 4 (c)



FIG·5a



FIG·5b



FIG·5C

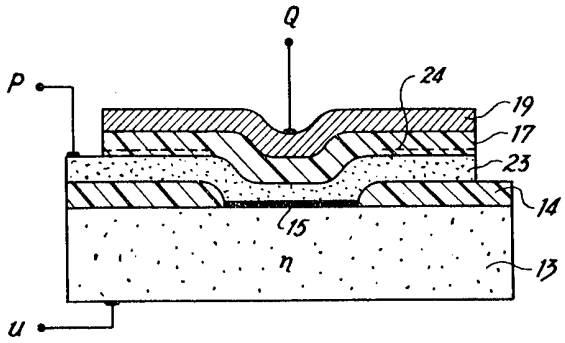


FIG. 6a

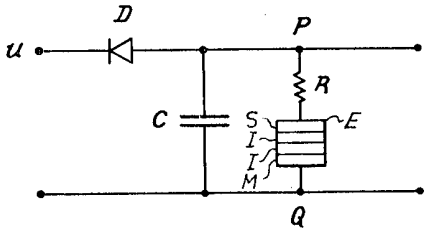


FIG. 6b

1590044 COMPLETE SPECIFICATION
5 SHEETS This drawing is a reproduction of the Original on a reduced scale
Sheet 5

FIG. 7

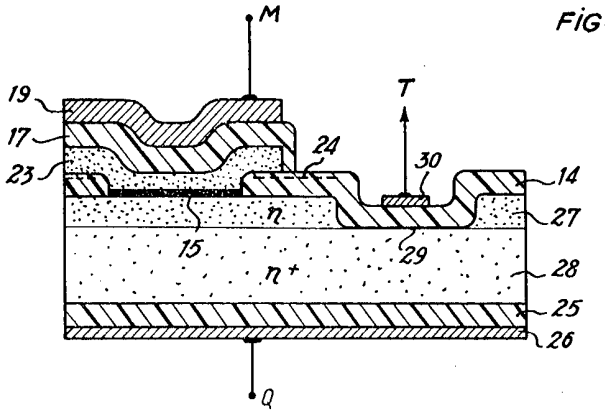


FIG. 8