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(54) Title: AN ENERGY-EFFICIENT FLIPDAC SWITCHING TECHNIQUE FOR CAPACITIVE DAC IN SAR ADCs

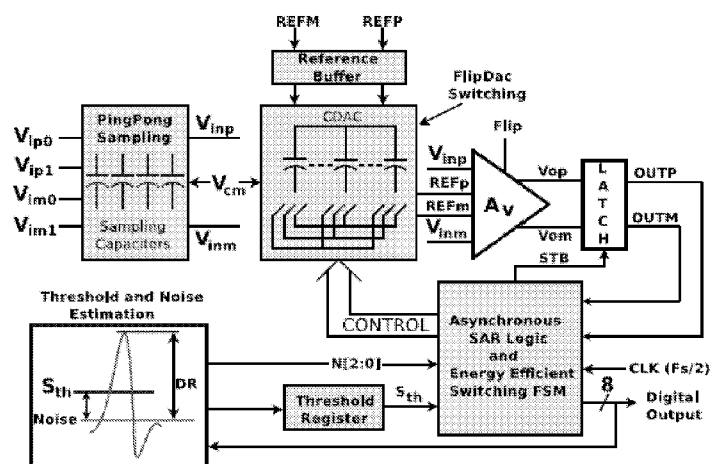


Fig. 1

(57) Abstract: Embodiments of the disclosure relate to a system and method to optimise energy consumption in an analog to digital converter (ADC). The system is an 8 bit SAR ADC with input and reference buffer. The ADC resolution may be adjusted from 8 to 1 bit linearly based on the dynamic range requirement. An energy efficient digital to analog converter (DAC) switching discourages the discharging of the DAC and consumes less energy than the conventional methods. The use of ping-pong input sampling in the ADC reduces the bandwidth requirement of the input buffer and clock speed by a factor of two. The conversion process is only enabled through the in-built background noise rejection logic to ensure that the noise is not processed. The conversion process reduces both power consumption and output data rate.



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AN ENERGY-EFFICIENT FLIPDAC SWITCHING TECHNIQUE FOR CAPACITIVE DAC IN SAR ADCs

TECHNICAL FIELD

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Embodiments of the present disclosure relate to analog to digital convertors (ADC). More particularly, the embodiments relate to switching of digital to analog convertors (DAC) used in ADCs to reduce the power consumption.

10 BACKGROUND

Presently, there has been a lot of interest in energy efficient digital to analog convertors (DAC) switching techniques for capacitive DAC. It has been shown that the digitization of the input voltages involving more number of DOWN transitions than UP
15 transitions are energy in-efficient. The power consumed or energy drawn from the reference voltage is more.

In one prior art, stepwise charging technique uses adiabatic charging of the capacitors by reducing effective voltage drop across the switch. It trade-offs conversion
20 time with energy which can hamper the speed of the operation of the SAR analog to digital convertors (ADC).

In another prior art, Vcm based switching is currently the most energy-efficient DAC switching scheme which is implemented on Silicon. But the DOWN transitions are
25 still energy inefficient due to the large MSB capacitors connected to the reference. The change in the direction of the polarization of the capacitors adds to the energy inefficiency.

Also, known in the art is that ADCs are reconfigured resolution by switching out
30 larger capacitors with the reduction in resolution. This saves power exponentially with the resolution, as power consumption was dominated by the CDAC, but increases layout-cum-logic complexity.

Hence, there is a need of a solution which can reduce the number of DOWN
35 transitions and thereby reducing the power consumption of ADCs. Further, the solution needs to be energy efficient, simple and minimal hardware usage.

SUMMARY

The shortcomings of the prior art are overcome and additional advantages are provided through the provision of methods and systems of the present disclosure.

The present disclosure solves limitations of existing techniques by providing energy efficient DAC switching technique which consumes less power.

Additional features and advantages are realized through various techniques provided in the present disclosure. Other embodiments and aspects of the disclosure are described in detail herein and are considered as part of the claimed disclosure.

In one embodiment, the disclosure provides a system to optimise energy consumption in an analog to digital converter (ADC). The system comprises a reference buffer to provide predefined clean voltages to capacitor digital to analog convertor (CDAC). Also, the system comprises a capacitive digital to analog convertor (CDAC) to convert digital feedback data into analog to compare with the input and implement binary search technique. The CDAC includes plurality of capacitors arranged in a predetermined fashion. Further, the system comprises a comparator to compare the magnitude of CDAC voltage with a predefined input voltage and generate a decision. The system also includes successive approximation register (SAR) block to control capacitors of the capacitive DAC based on the comparator output, to flip DAC input voltages of the comparator based on the output magnitude of the comparator during second MSB (most-significant-bit) decision, thereby reducing the energy consumption of the ADC.

In another embodiment, the disclosure provides a method of optimising energy consumption in an analog to digital converter (ADC). The method comprising sampling input data signals using a sampling block for providing input to capacitor digital to analog convertor (CDAC). An analog data output is generated by the CDAC. Next, estimating magnitude of the output of the CDAC is performed using a comparator. The method also includes performing flip operation on the CDAC to interchange input voltages to comparator for reducing number of down transitions in the CDAC, thereby reducing the power consumption in the ADC.

The foregoing summary is illustrative only and is not intended to be in any way limiting. In addition to the illustrative aspects, embodiments, and features described above, further aspects, embodiments, and features will become apparent by reference to the drawings and the following detailed description.

BRIEF DESCRIPTION OF THE ACCOMPANYING DRAWINGS

The novel features and characteristic of the disclosure are set forth in the appended claims. The embodiments of the disclosure itself, however, as well as a preferred mode of use, further objectives and advantages thereof, will best be understood by reference to the following detailed description of an illustrative embodiment when read in conjunction with the accompanying drawings. One or more embodiments are now described, by way of example only, with reference to the accompanying drawings wherein like reference numerals represent like elements and in which:

Fig. 1 shows a block diagram of the SAR ADC, in accordance with an embodiment;

Fig. 2a shows a CDAC switching in a 3 bit ADC for conventional technique;

Fig. 2b shows a CDAC switching in a 3 bit ADC for FlipDac switching technique, , in accordance with an embodiment;

Fig. 3 illustrates FlipDac switching technique for a 4-bit SAR ADC and energy cost comparison for each step in the binary search tree, in accordance with an embodiment of the present disclosure;

Fig. 4 illustrates a timing diagram for FlipDac switching technique, in accordance with an embodiment;

Fig. 5 shows a comparison of CDAC switching energy for a 10 bit SAR ADC;

Fig. 6a shows sampling in SAR ADC for a traditional method or Traditional sampling;

Fig. 6b shows sampling in SAR ADC for ping-pong input sampling;

Fig. 7 shows architecture of ping-pong input sampling technique;

Fig. 8a shows an effective activity factor for a spike approximated as a triangular waveform;

Fig. 8b shows an effective activity factor for an important spike features that should be preserved;

Fig. 9 shows schematic diagram of the preamplifier switch states 1 and 2 which are determined by Flip input to the preamplifier, in accordance with an embodiment;

Fig. 10 shows the Flip Logic by switching rails implementation, in accordance with an embodiment;

5 Fig. 11 shows an asynchronous logic Variable resolution is implemented using the MUX setting controlled by $N2 - N0$;

Fig. 12 shows timing diagram of depicting asynchronous operation;

Fig. 13 shows architecture of 8 bit CDAC with separate sub-DACs;

Fig. 14 shows architecture of VGA for even or odd numbered channel;

10 Fig. 15 shows OTA sharing between even and odd numbered channel;

Fig. 16 (a) shows measured SNDR Vs F_{in} for -1 dBFS input at 1 MS/s speed.;

Fig. 16 (b) shows 16384 point FFT of the ADC output for -1 dBFS input at $F_{in} = 62.439$ KHz;

Fig. 17 shows measured digital output of the activity dependent ADC, the X-axis and Y-axis represent the time in μsec and the output code respectively; and

15 Figs. 18a and 18b show relative reduction in power consumption and ODR respectively.

The figures depict embodiments of the disclosure for purposes of illustration only. One skilled in the art will readily recognize from the following description that
20 alternative embodiments of the structures and methods illustrated herein may be employed without departing from the principles of the disclosure described herein.

DETAILED DESCRIPTION

25 The foregoing has broadly outlined the features and technical advantages of the present disclosure in order that the detailed description of the disclosure that follows may be better understood. Additional features and advantages of the disclosure will be described hereinafter which form the subject of the claims of the disclosure. It should be appreciated by those skilled in the art that the conception and specific embodiment
30 disclosed may be readily utilized as a basis for modifying or designing other structures for carrying out the same purposes of the present disclosure. It should also be realized by those skilled in the art that such equivalent constructions do not depart from the spirit and scope of the disclosure as set forth in the appended claims. The novel features which are believed to be characteristic of the disclosure, both as to its organization and method

of operation, together with further objects and advantages will be better understood from the following description when considered in connection with the accompanying figures. It is to be expressly understood, however, that each of the figures is provided for the purpose of illustration and description only and is not intended as a definition of the limits of the present disclosure.

Exemplary embodiments of the present disclosure provide system and method to optimize energy consumption in an analog to digital converter (ADC)

One embodiment of the present disclosure is a system to optimise energy consumption in an analog to digital converter (ADC). The system comprises a reference buffer to provide predefined clean voltages to capacitor digital to analog convertor (CDAC). Also, the system comprises a capacitive digital to analog convertor (CDAC) to convert digital feedback data into analog to compare with the input and implement binary search technique. The CDAC includes plurality of capacitors arranged in a predetermined fashion. Further, the system comprises a comparator to compare the magnitude of CDAC voltage with a predefined input voltage and generate a decision. The system also includes successive approximation register (SAR) block to control capacitors of the capacitive DAC based on the comparator output, to flip DAC input voltages of the comparator based on the output magnitude of the comparator during second MSB (most-significant-bit) decision, thereby reducing the energy consumption of the ADC.

Another embodiment of the present disclosure is a method of optimising energy consumption in an analog to digital converter (ADC). The method comprising sampling input data signals using a sampling block for providing input to capacitor digital to analog convertor (CDAC). An analog data output is generated by the CDAC. Next, estimating magnitude of the output of the CDAC is performed using a comparator. The method also includes performing flip operation on the CDAC to interchange input voltages to comparator for reducing number of down transitions in the CDAC, thereby reducing the power consumption in the ADC.

Fig. 1 shows a block diagram of successive approximation register (SAR) ADC, in accordance with an embodiment of the present disclosure. Fully differential input and

reference voltages are used. The reference DAC and sampling capacitors are segregated to gain advantages. An on-chip reference buffer is implemented to provide clean and stable voltage reference to the ADC. The V_{cm} rail is not buffered as ideally no charge is required from this rail owing to the symmetric switching scheme. A master clock of only half the sampling speed is used, saving power in clock buffers by 2X and reducing total system power. Spike threshold S_{TH} is calculated based on the background noise and is stored in registers. The dynamic range (DR) decides the resolution setting (N2-N0) of the ADC. An energy efficient switching technique FlipDac is used to make DAC power consumption very small.

FlipDac switching is an energy efficient DAC switching techniques for CDAC. The digitization of the input voltages involving more number of DOWN transitions than UP transitions is energy in-efficient. The extra work done by the reference in discharging the CDAC during DOWN transitions dominates the energy consumption. The energy drawn from the reference can be reduced if it is possible to resolve an input through fewer DOWN transitions. Even if the number of DOWN transitions is not smaller than that of UP transitions, the energy consumption can be reduced by pushing their occurrences towards the LSBs.

Fig. 2a shows the switching technique for a 3-bit SAR ADC for $V_{ip} > V_{in}$, in accordance with an embodiment of the present disclosure. The DOWN transition draws more energy from the reference compared to the UP transition. Fig. 2b presents the switching technique proposed by us for a 3 bit ADC. For the DOWN transition step, the energy drawn from the reference is 5X smaller than that in Fig. 2a. This is achieved by discouraging the reduction of individual CDAC voltage inputs to the comparator during the DOWN transition. The inputs V_{ip} and V_{in} , are interchanged to preserve the comparator logic. The scheme is also overall 33 % more energy efficient than Fig. 2a.

Fig. 3 illustrates the switching scheme for a 4-bit ADC for $V_{ip} > V_{in}$, in accordance with an embodiment. The second MSB capacitor (2C) is the replica of the remaining two LSB capacitors. First DOWN transition as shown in Fig. 3 illustrates FlipDac switching technique. The FlipDac step does not take any extra clock cycle and hence speed is not compromised. Fig. 4 shows the timing diagram for the FlipDac switching technique, in accordance with an embodiment. If b2 is detected as logic HIGH,

VC2-VC3 as shown in Fig. 3, tracks Vip-Vin in the conventional way. However, if b2 is detected as logic LOW, Flip goes high and, VC2 and VC3 interchange their roles. The residual tracking of the input Vip-Vin is then carried out by VC3-VC2 which helps in reducing the number of times CDAC is discharged, especially during the MSBs. As shown in Fig. 4, output 1001 is resolved indirectly by tracking 1110 by the CDAC. This results in fewer discharging steps than in the case when CDAC resolves 1001 directly.

In one embodiment, the flipping of the CDAC is performed only for the first DOWN transition by making use of the symmetric structure of the CDAC, for both UP and DOWN transitions, from this node. The splitting of (MSB-1)th capacitor helps in implementing binary search, after flipping, without incurring extra time and switching. The energy consumption during various steps for a 4-bit ADC is also compared with in Fig. 3. The number in the circle represents the total number of unit capacitors connected to Vref. The relative energy costs are shown on the arrows. The energy drawn from the reference for each UP ($\Delta V_{DAC} > 0$) and DOWN ($\Delta V_{DAC} < 0$) transitions may be calculated as:

$$E_{UP} = (C_{sw} \cdot (V_{ref} - V_{cm}) - (C_{ref} + C_{sw}) \cdot (\Delta V_{DAC})) \cdot V_{ref}$$

$$E_{DOWN} = ((C_{ref} - C_{sw}) \cdot |\Delta V_{DAC}|) \cdot V_{ref}$$

where C_{sw} is the capacitance switched, C_{ref} is the total capacitance connected to V_{ref} before this step, ΔV_{DAC} is the change in CDAC reference voltage in that step.

Fig. 5 illustrates a comparison of the energy drawn from the reference for each code in a 10 bit SAR ADC and FlipDac switching technique. The switching technique achieves minima at output code 511 and 512 compared to maxima in, which happens because code 511 and code 512 are resolved by tracking code 0 and code 1023 respectively, by the CDAC, which have no DOWN transitions. Table-I compares the FlipDac switching technique with the recent CDAC switching techniques or schemes for a 10 bit ADC which shows the savings achieved over them. This scheme necessitates the use of separate sampling capacitors which upon investigation is found favourable in reducing the power consumption.

Table-I DAC switching energy comparison for 10 bit SAR ADC

Spec.	[19]	[18]	[13]	This scheme
Energy ($C \cdot V_{ref}^2$)	142	255.5	170	106
Saving	25.3 %	58.6 %	37.5 %	-

One embodiment of the present disclosure is Ping-Pong input sampling Fig. 6a shows the timing diagram of a conventional 8 bit SAR ADC. Typically 2-3 clock cycles or equivalent delay (T_{vga}) is dedicated to the tracking of the input on the CDAC (C_{DAC}). It is then followed by 8 bit-cycles for the digitization of the sample. It demands large bandwidth or current in the input buffer (VGA). The power consumption in the VGA may be reduced by giving more time for the input tracking but it contradicts with the design of the reference buffer in the sampling approach. In this ADC, ping-pong sampling technique is employed which relaxes the design of both VGA and the reference buffer.

In one embodiment, Figs. 7b and 8 illustrate the sampling technique used or employed in the ADC. In this technique, inputs are sampled on capacitors C_{in0} and C_{in1} rather than C_{DAC} . There are two sets of sampling capacitors of which when one is tracking the input, the other is used in the digitization of the previous sample, which enables the use of the complete sample period TS as shown in the Fig. 6b, for the input tracking which relaxes the bandwidth requirement of the VGA stage. This also reduces the power consumption in the reference buffer as comparatively more time is available for bit cycling. The Ping-pong sampling in the ADC enables the use of two half rate clocks for even and odd-numbered channels. Also, the ping-pong sampling alleviates the clock requirement by 2X over asynchronous schemes employing clocks equal to that of the sampling rate which saves power in the clock buffers.

One embodiment of the present disclosure is about power saving in VGA. Considering, if $T_{vga} = \alpha_{vga} \cdot TS$, the N bit settling error may be given by the following equation,

$$V_{err1} = \frac{V_{ref}}{2^N} = V_{ref} \cdot \exp\left(\frac{-T_{vga}}{R_{eq} \cdot C_{DAC}}\right) \quad (1)$$

Assuming output resistance $R_{eq} = \beta/I_D$ where β is a constant dependent on the architecture of the driver and I_D is the current consumed in the driver,

$$I_{D,vga,1} = \frac{N \cdot \ln(2) \cdot \beta_{vga} \cdot C_{DAC}}{\alpha_{vga} \cdot T_S} \quad (2)$$

Now for ping-pong input sampling $\alpha_{vga} = 1$,

$$I_{D,vga,2} = \frac{N \cdot \ln(2) \cdot \beta_{vga} \cdot C_{DAC}}{T_S} \quad (3)$$

The percentage power saving may be calculated as,

$$\frac{I_{D,vga,1} - I_{D,vga,2}}{I_{D,vga,1}} = (1 - \alpha_{vga}) \cdot 100\% \quad (4)$$

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Another embodiment of the present disclosure is power saving in reference buffer: Let $T_{ref} = \alpha_{ref} \cdot T_S$, the N bit settling error due to the reference buffer may be given as,

$$V_{err2} = \frac{V_{ref}}{2^N} = V_{ref} \cdot \exp\left(\frac{-(T_{ref})/2N}{R_{eq} \cdot C_{eq}}\right) \quad (5)$$

10 where C_{eq} is the equivalent capacitance seen by the reference buffer and 50 % of each bit cycle (T_{ref}/N) is given for CDAC settling.

$$I_{D,ref,1} = \frac{N \cdot \ln(2) \cdot \beta_{ref} \cdot C_{eq}}{\alpha_{ref} \cdot T_S} \cdot 2N \quad (6)$$

For ping-pong input sampling $\alpha_{ref} = 1$,

$$I_{D,ref,2} = \frac{N \cdot \ln(2) \cdot \beta_{ref} \cdot C_{eq}}{T_S} \cdot 2N \quad (7)$$

15 The percentage power saving can be calculated as,

$$\frac{I_{D,ref,1} - I_{D,ref,2}}{I_{D,ref,1}} = (1 - \alpha_{ref}) \cdot 100\% \quad (8)$$

Therefore, an 8 bit ADC with 2 cycles given for sampling in the conventional approach, $\alpha_{vga} = 0.2$ and $\alpha_{ref} = 0.8$. Hence 80 % power can be saved in the VGA and 20% power can be saved in the reference buffer by using ping pong sampling technique.

20 Actually, the power saving in the VGA is more as the sampling capacitors are much smaller than C_{DAC} as shown in the Fig. 7. The drawback of this architecture is the use of extra sampling capacitors. But as the sizes of capacitors are determined by thermal noise and not matching the area penalty is not significant for moderate resolution ADCs. The

architecture also requires good matching between two sampling paths for a single channel application and may need calibration. But no such requirement is imposed for multichannel input, as in NRS, where each channel either even or odd, traverses a fixed path every time. Also, this alleviates the concern of duty cycle distortion due to the half-rate clocking as even and odd numbered channels are sampled by two different non overlapping clocks.

One embodiment of the present disclosure is Activity dependent ADC. There is a great need to reduce the amount of data to be transmitted to enable chronic recording from a number of channels. The information in neural Extracellular Action Potential (EAP) is essentially encoded in the spike time-stamps but the amplitude information in the EAPs is also important for spike sorting purpose. Simple thresholding is found to be equally effective as other complex spike detection algorithms. However, representing a spike as a point event causes loss of information required for spike sorting as shown in Fig. 8b. For this reason, an activity dependent ADC technique or method or scheme is employed to obviate the processing of the background noise. The digitization process is only enabled when the input is found larger than the spike detection threshold S_{TH} which is shown in Fig. 2. The spike detection threshold S_{TH} is decided based on the magnitude of the background noise (σ_n), $S_{TH} = k \cdot \sigma_n$ where $k = 3-4$, so that the probability of the false detection of the noise as a spike is very small. The ADC is programmable to operate either in this mode or free running mode to transmit raw data.

Fig. 8a illustrates the activity dependent ADC technique. The spike is approximated as a triangular waveform with maximum amplitude A_{max} and spike duration T_{spike} . The slope the spike as shown in the Fig. 8a is calculated as,

$$m = \frac{dV}{dt} = \frac{2 \cdot A_{max}}{T_{spike}} = \frac{k \cdot \sigma_n}{x} \quad (9)$$

Hence,
$$x = \frac{k \cdot \sigma_n \cdot T_{spike}}{2 \cdot A_{max}}$$

In one embodiment, if the total number of spikes in time T_{exp} is $\alpha = S_R \cdot T_{exp}$ where S_R is the spike rate in spikes/sec, the effective time (T_{eff}) for which the N bit ADC operates is given by,

$$T_{eff} = \alpha(T_{spike} - 2.x) + \frac{(T_{exp} - \alpha(T_{spike} - 2.x))}{N + 1} \quad (10)$$

The second term in the equation 10 indicates that the ADC operates only for one cycle for spike detection and is idle for remaining N bit cycles if the spike is not detected. The effective activity factor (EAF) of as N bit ADC working on activity based A/D scheme can be given by,

$$EAF = \frac{T_{eff}}{T_{exp}} = \frac{1}{N + 1} + \frac{N}{N + 1} \cdot SR \cdot T_{spike} \cdot \left(1 - \frac{S_{TH}}{A_{max}}\right) \quad (11)$$

The equation 11 represents the effective time for which an activity dependent ADC may be working when compared to a free running ADC. Also, the equation represents the reduction in power consumption of the ADC and output data rate (ODR) of the system. As an example, the typical values of T_{spike} is 1msec and SR is 100 spikes/sec. Assuming $S_{TH}/A_{max} = 0.2$, EAF for an 8 bit ADC can be calculated from Eqn. 11 as approximately 0.18 which saves 82 % energy and ODR over a free running ADC. The logic is in-built in the ADC and CDAC is reused for this purpose which obviates the use of separate DAC for each channel. The spike detection threshold (S_{TH}) can be increased to reduce EAF and to provide more immunity against the background noise but may cause loss of information. Hence the value of S_{TH} should be decided based spike sorter's requirement in addition to the background noise.

In one embodiment, the ADC is designed with reconfigurable resolution to mitigate unnecessary processing in case of smaller dynamic range. The previous state-of-the-art ADCs reconfigured resolution by switching out larger capacitors with the reduction in resolution which saves power exponentially with the resolution. As the power consumption was dominated by the CDAC, but increases layout-cum-logic complexity. However, the CDAC power consumption is very small compared to the digital switching power by using the FlipDac switching technique. Hence, the resolution is reduced by simply halting the binary search algorithm in-between based on the resolution requirement. It enables the resolution reconfiguration from 8 bit to 1 bit at 1 bit step. Thus, the technique of variable resolution saves power linearly with the resolution and is limited by the static power consumption in the ADC.

In an embodiment a preamplifier is used before the clocked latch and the use of a preamplifier is preferred for offset and kickback noise mitigation. Kickback noise is an important concern due to the use of small sampling capacitors. The preamplifier in SAR ADC is subjected to step input only and needs to amplify the error just enough for the detection of the sign by the clocked latch, which relaxes the settling requirement in the preamplifier. If $A_v(s) = A_{v0}/(1 + s/p)$, for an input V_{in} , $u(t)$ and initial condition at output as $V_o(0^-)$, the output v_o is,

$$v_o(t) = A_{v0} \cdot V_{in} (1 - \exp(-\omega_p t)) + V_o(0^-) \exp(-\omega_p t) \quad (12)$$

The second term in equation 12 may be eliminated by resetting output before enabling CDAC output. The output of the preamp, after a delay T_d from CDAC output is calculated and effective amplification $A_{v,eff}$ is given by,

$$A_{v,eff} = A_{v0} (1 - \exp(-\omega_p T_d)) \quad (13)$$

Fig. 10 shows a schematic diagram of preamplifier. The input transistors for REFP and REFM inputs are interchangeable to implement the Flip logic. A partial positive feedback is used to reduce the effective output conductance. The load transistors are sized, such that $W2 < W1$, to prevent the effective output conductance from becoming negative, even in the presence of any mismatch. If $W2 = \eta \cdot W1$, the dc voltage gain A_{v0} and the bandwidth ω_p , for a load capacitance C_L , may be calculated as:

$$A_{v0} = \frac{g_{m,in}}{g_{m,w1}} \frac{1}{1 - \eta} \quad \text{and} \quad \omega_p = \frac{g_{m,w1} \cdot (1 - \eta)}{C_L}$$

By increasing η towards unity, more voltage gain may be achieved but it makes the preamplifier more sluggish. As an example, let $\eta = 0.8$ as a trade-off between voltage gain, speed and stability. The obtained results or values are $A_{v0} = 14$ and $\omega_p = 8$ MHz.

One embodiment of the present disclosure is FlipDac switching technique. During the first DOWN transition, flipping of the C_{DAC} is done to save energy. However, it may lead to the interchanging of V_{DACp} and V_{DACn} inputs to the preamplifier, which is compensated internally in the preamplifier which is as shown in Fig. 10. For implementing the flip logic, reference rails in the CDAC are also interchanged as illustrated in the Fig. 10. Rails V and G are shorted together to V_{cm} input and V_{cm1} , V_{cm2} rails is shorted to REFP or REFM based on the sign of the input.

Fig. 11 illustrates asynchronous technique employed in CDAC. The timing diagram for the same is illustrated in Fig. 12. The individual bit cycling phases are generated once a decision is made by the comparator after STB and is detected by a NAND gate. A shift register of depth equal to 11 is used to progress a pulse, after each decision, to enable the extraction of the next bit, where the first flip-flop is asynchronously preset by SOC to start. Programmable delay line (PDL) is used to generate STB RST and STB PST signals to respectively reset and preset STB by introducing delays D1 and D2. The input HS controls PDL to modulate delays for operating at higher speed. Once the pulse reaches the final flip-flop the conversion halts until the next SOC. The position of the final flip-flop is decided based on the resolution requirement ($N_2 - N_0$) through a digital MUX. It implements variable resolution, without complicating the layout and logic, and prevents unnecessary conversion steps to happen. Two extra flip-flops are used to include the logic for STH which can be bypassed for the free running mode.

Fig. 13 shows the architecture of the 8 bit CDAC used in the ADC, as one embodiment. Separate sub-DACs for DOWN and UP transitions are used. As the linearity of a CDAC is determined by total capacitance switched, indifferent of its position, this structure does not compromise the linearity performance of the CDAC.

One embodiment is VGA and Reference Buffer of the VGA. The architecture of the VGA is shown in Fig. 14. VGA comprises of two stages VGA1 and VGA2 in which VGA1 may be put in sleep mode if detectable signal amplitude is large. Switch S1 and S2 are selected based on the total gain requirement to fully traverse the ADC dynamic range. The architecture of the VGA block is illustrated in Fig. 15. The OTA is shared between the two sets of capacitors for employing ping-pong input sampling. The OTA is a two-stage trans-conductance amplifier which consumes about 3 μ A driving 1 MS/s 8-bit SAR ADC. Any noise on the reference voltage will directly appear at the output of the ADC and will deteriorate its dynamic performance, especially in a SOC environment. Hence, an on-chip reference buffer is used. The OTA designed for the reference buffer is a two-stage trans-conductance amplifier consuming 4 μ A and is load compensated.

Figs. 16a and 16b illustrate measured SNDR for different input frequencies. The ADC achieves a SNDR of about 48.1 dB for a near Nyquist input of 499.939 KHz which

translates to ENOB of 7.7. The ADC consumes total power of $8.8 \mu\text{W}$ with $V_{DD} = 1 \text{ V}$. Based on parasitic extracted simulations, CDAC consumes only $0.4 \mu\text{W}$ and preamp consumes $1.5 \mu\text{W}$ which is approximately 5% and 17% of the total power consumption respectively. The power consumption is dominated by the digital switching approximately 78 %. As the power consumption is dominated by the digital switching, it reduces linearly with the decrease in the resolution.

Fig. 17 illustrates activity dependent A/D represents the measured output of the ADC working under activity dependent ADC method at 1 MS/s speed. The values of S_{TH} and EAF are shown in Fig. 17, where the first bit S is the sign bit. The ADC takes two extra cycles for the spike detection and purging of the CDAC. If S_{TH} is set as 0, the ADC behaves as a free running ADC and consumes $10.7 \mu\text{W}$. Figs. 18(a) and 18(b) show the relative reduction in power consumption and ODR as a function of S_{TH} under different noise conditions. An experiment is conducted with the spike input to the ADC is approximated by a triangular waveform with noise. Based on the value of input noise σ_n , a proper value of S_{TH} may be found which reduces power consumption and ODR but preserves three important spike features of Fig. 8(b), i.e. A_{max} the maximum positive spike amplitude, A_{min} the minimum negative spike amplitude and T_{pp} the time between A_{max} and A_{min} .

In one embodiment, VGA can only be characterized at low frequencies of approximately 1 KHz, as it is not designed to drive large capacitance i.e. approximately 5pF at higher frequencies. The low frequency voltage gain matches the expected 8-35 dB. Table II shows the comparison of the VGA with two previous state-of-the-art NRSs and shows the advantage gained due to the bandwidth relaxation by the ping pong input sampling.

Table II Shows VGA comparison.

Spec.	[2]	[10]	This work
Gain	17-20 dB	5.7-20.5 dB	8-35 dB
ADC	9b, 640 KS/s	10b, 8 Ksps/ch.	8b, 1 MS/s
VGA	$40.6 \mu\text{A}$	$0.55 \mu\text{A}$	$3 \mu\text{A}$

One embodiment of the present disclosure is a 8-to-1 bit, 1 MS/s SAR ADC in UMC $0.13 \mu\text{m}$ CMOS technology. Energy efficient DAC switching technique is used which

consumes lowest power compared to the conventional techniques, without using extra capacitors or clock cycles. The DAC switching technique consumes about 37 % less energy than the present state-of-the-art techniques. For multichannel input, use of ping-pong input sampling is emphasized to save power in VGA and reference buffer. Also,
5 the SAR ADC consumes lower power in clock buffers as we employ clock of half of the sampling speed. The resolution of the ADC can be varied based on the dynamic range required to avoid unnecessary processing and save power.

The FlipDac switching techniques makes energy consumption in the DAC which is
10 approximately 5 %, that is negligible compared to digital switching energy which is approximately 78 %. The DAC switching technique will be more beneficial in higher resolution and higher speed SAR ADCs where the DAC switching energy is more comparable to the digital switching energy.

15 The present disclosure is not to be limited in terms of the particular embodiments described in this application, which are intended as illustrations of various aspects. Many modifications and variations can be made without departing from its spirit and scope, as will be apparent to those skilled in the art. Functionally equivalent methods and apparatuses within the scope of the disclosure, in addition to those enumerated
20 herein, will be apparent to those skilled in the art from the foregoing descriptions. Such modifications and variations are intended to fall within the scope of the appended claims. The present disclosure is to be limited only by the terms of the appended claims, along with the full scope of equivalents to which such claims are entitled. It is also to be understood that the terminology used herein is for the purpose of describing particular
25 embodiments only, and is not intended to be limiting.

With respect to the use of substantially any plural and/or singular terms herein, those having skill in the art can translate from the plural to the singular and/or from the singular to the plural as is appropriate to the context and/or application. The various
30 singular/plural permutations may be expressly set forth herein for sake of clarity.

In addition, where features or aspects of the disclosure are described in terms of Markush groups, those skilled in the art will recognize that the disclosure is also thereby

described in terms of any individual member or subgroup of members of the Markush group.

5 While various aspects and embodiments have been disclosed herein, other aspects and embodiments will be apparent to those skilled in the art. The various aspects and embodiments disclosed herein are for purposes of illustration and are not intended to be limiting, with the true scope and spirit being indicated by the following claims.

We claim:

1. A system to optimise energy consumption in an analog to digital converter (ADC) comprising:

5 reference buffer to provide predefined clean voltages to capacitor digital to analog convertor (CDAC);

 capacitive digital to analog convertor (CDAC) to convert digital feedback data into analog to compare with the input and implement binary search technique, said CDAC comprises capacitors arranged in a predetermined fashion;

10 comparator to compare the magnitude of CDAC voltage with a predefined input voltage and generate a decision;

 successive approximation register (SAR) block to control capacitors of the capacitive DAC based on the comparator output, to flip DAC input voltages of the comparator based on the output magnitude of the comparator during 2nd (most-significant-bit) MSB decision, thereby reducing the energy consumption of the ADC.

2. The system as claimed in claim 1, wherein the SAR block flips the DAC input voltages of the comparator if the output magnitude is negative value during the 2nd MSB.

20 3. The system as claimed in claim 1, wherein the CDAC comprises capacitors arranged in a symmetric structure to generate differential values as input to the comparator.

4. The system as claimed in claim 1, wherein the SAR block decreases number of down transitions of the CDAC to reduce power consumption of the ADC.

25 5. The system as claimed in claim 1, wherein the comparator is connected to a latch to store the output data of the comparator.

6. The system as claimed in claim 1, wherein a master clock is used in the ADC to trigger all blocks with half the sampling frequency to reduce power consumption.

7. A method of optimising energy consumption in an analog to digital converter (ADC) comprising:

sampling inputs data signal using a sampling block for providing input to capacitor digital to analog convertor (CDAC), wherein analog data output is generated by the CDAC;

estimating magnitude of the output of the CDAC using a comparator;

5 performing flip operation on the CDAC to interchange input voltages to comparator to reduce number of down transitions in the CDAC, thereby reducing the power consumption in the ADC.

10 8. The method as claimed in claim 7, wherein the flipping operation in CDAC is performed using successive approximation register (SAR) logic block.

9. The method as claimed in claim 7, wherein a master clock is used in the ADC to trigger all blocks with half the sampling frequency to reduce power consumption.

10. The method as claimed in claim 7 or 8, wherein SAR block decreases down transition of the CDAC to reduce power consumption of the ADC.

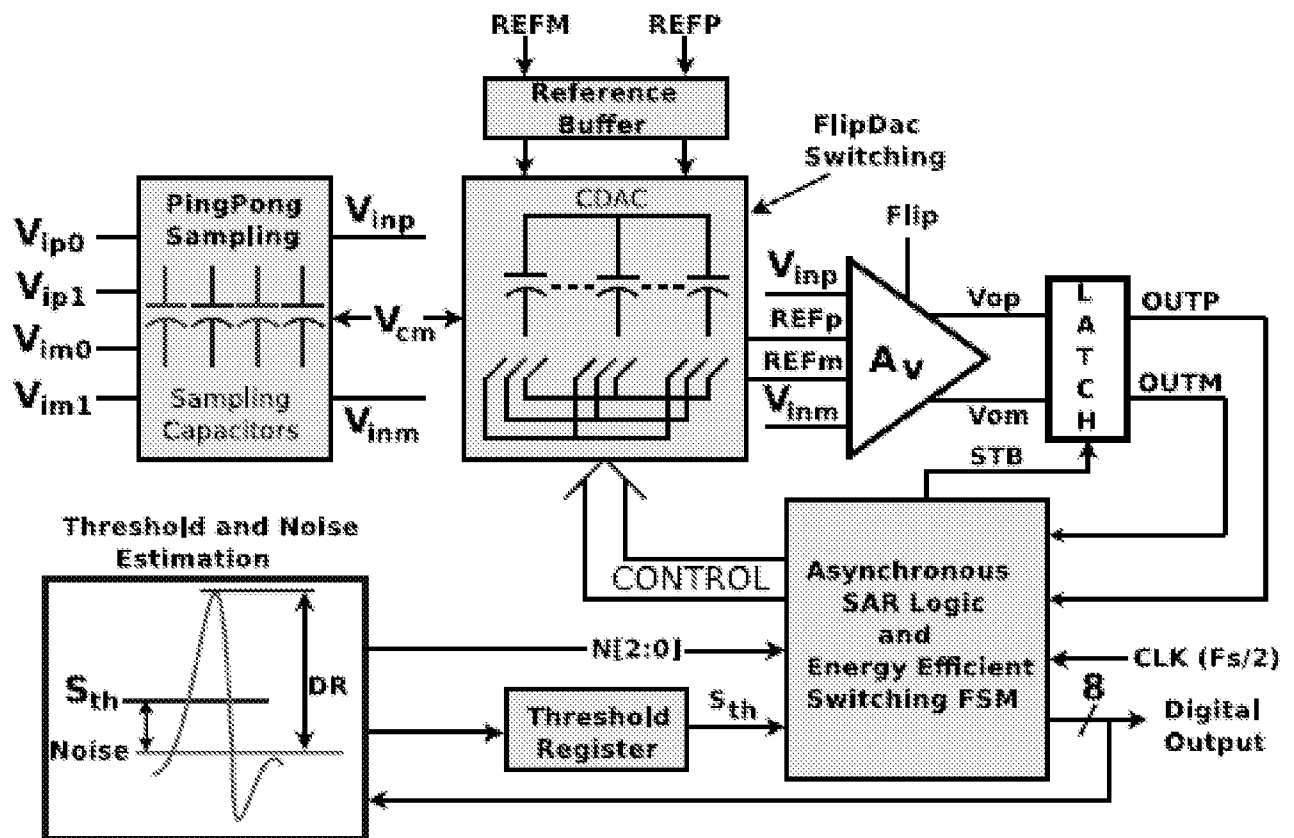


Fig. 1

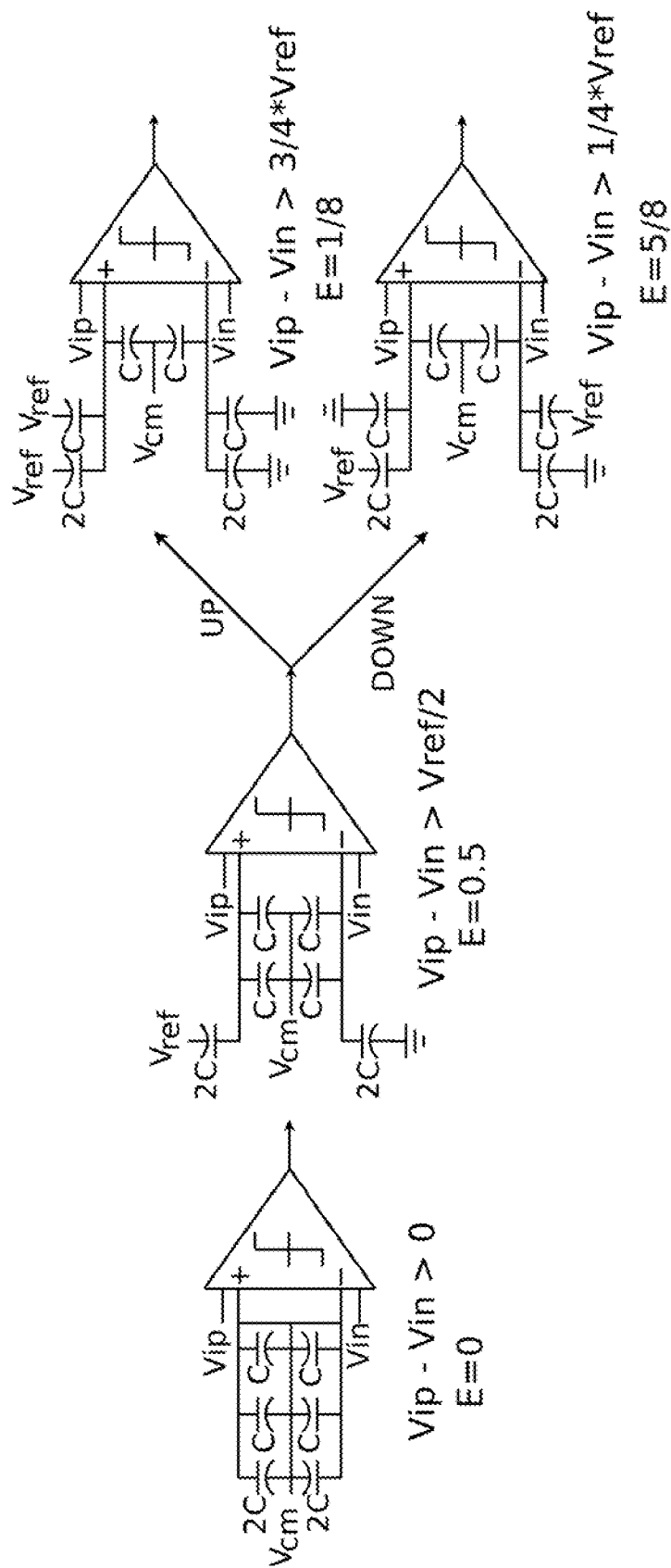


Fig. 2a

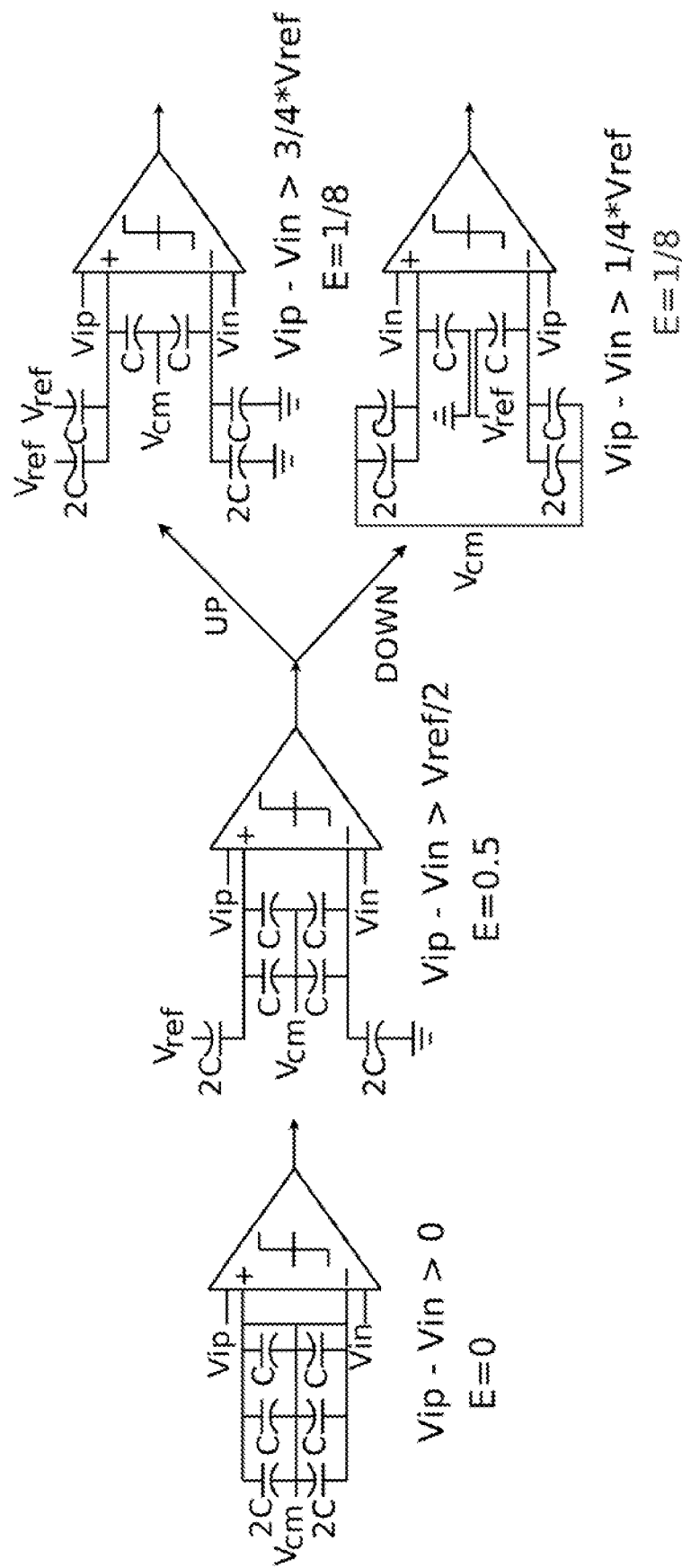
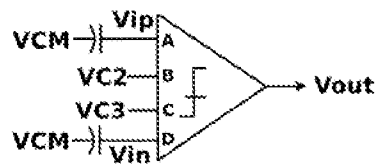
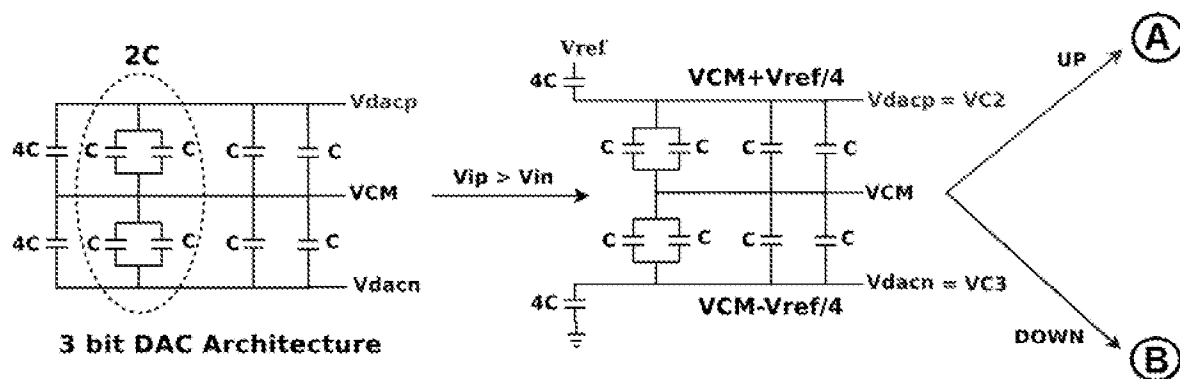


Fig. 2b



Comparator Architecture



Energy Cost Comparison with [13]

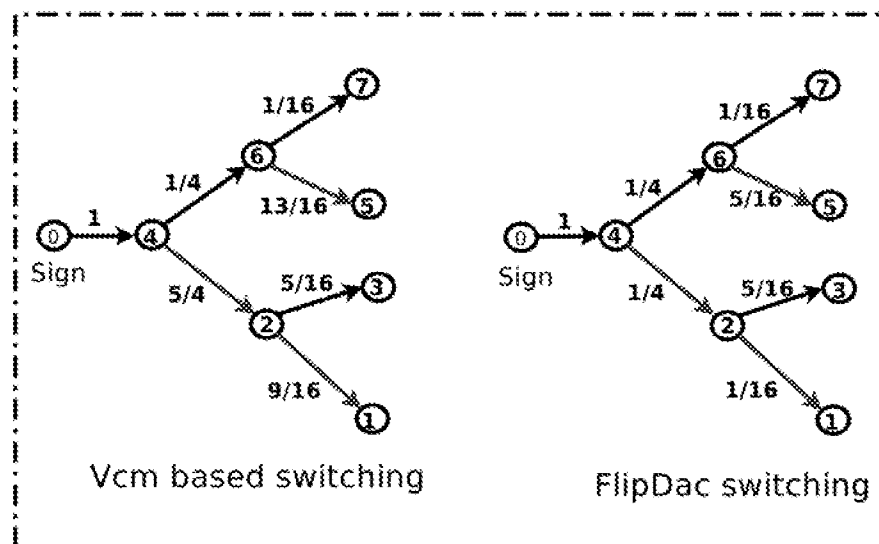


Fig. 3

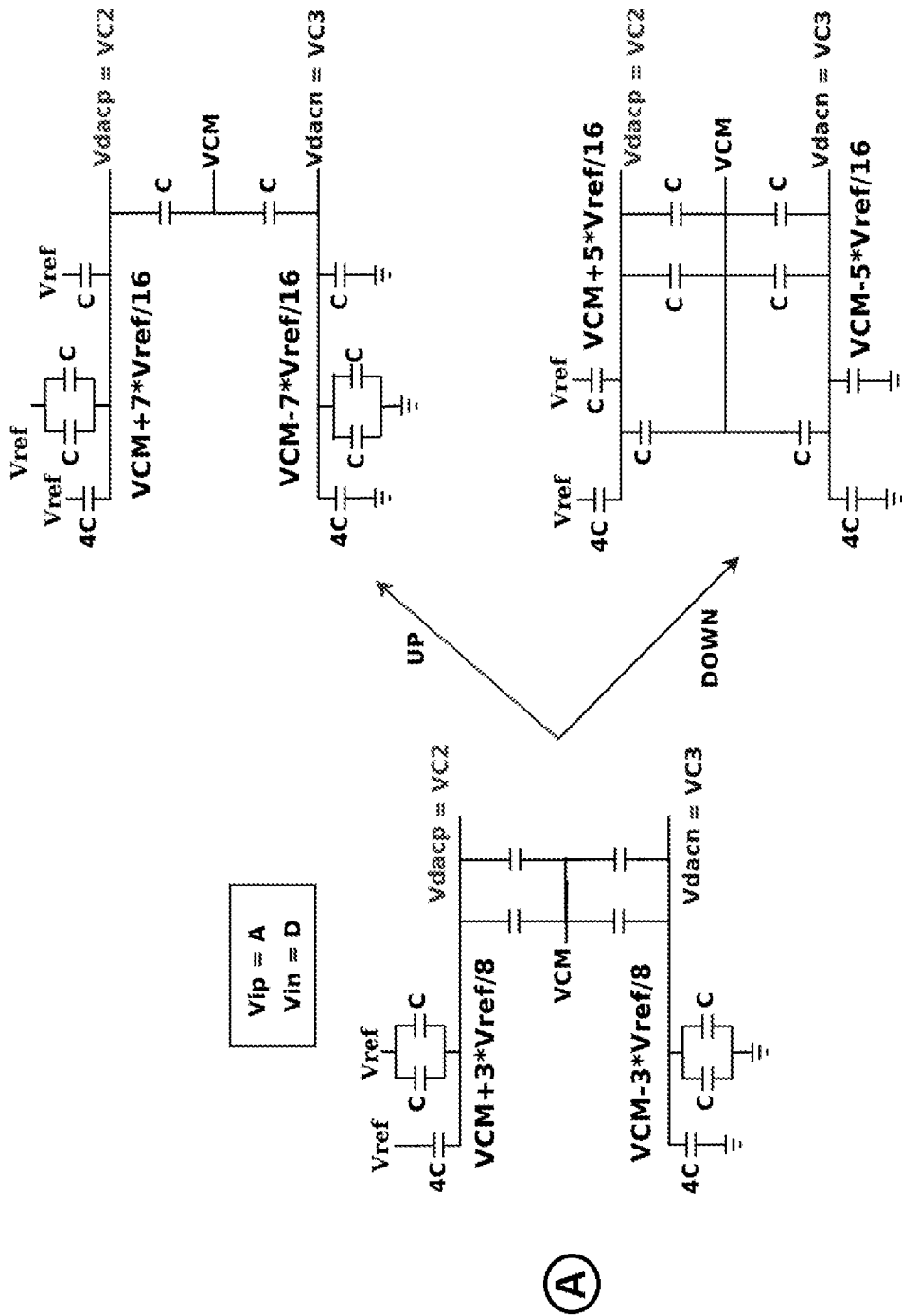


Fig. 3 (Continued)

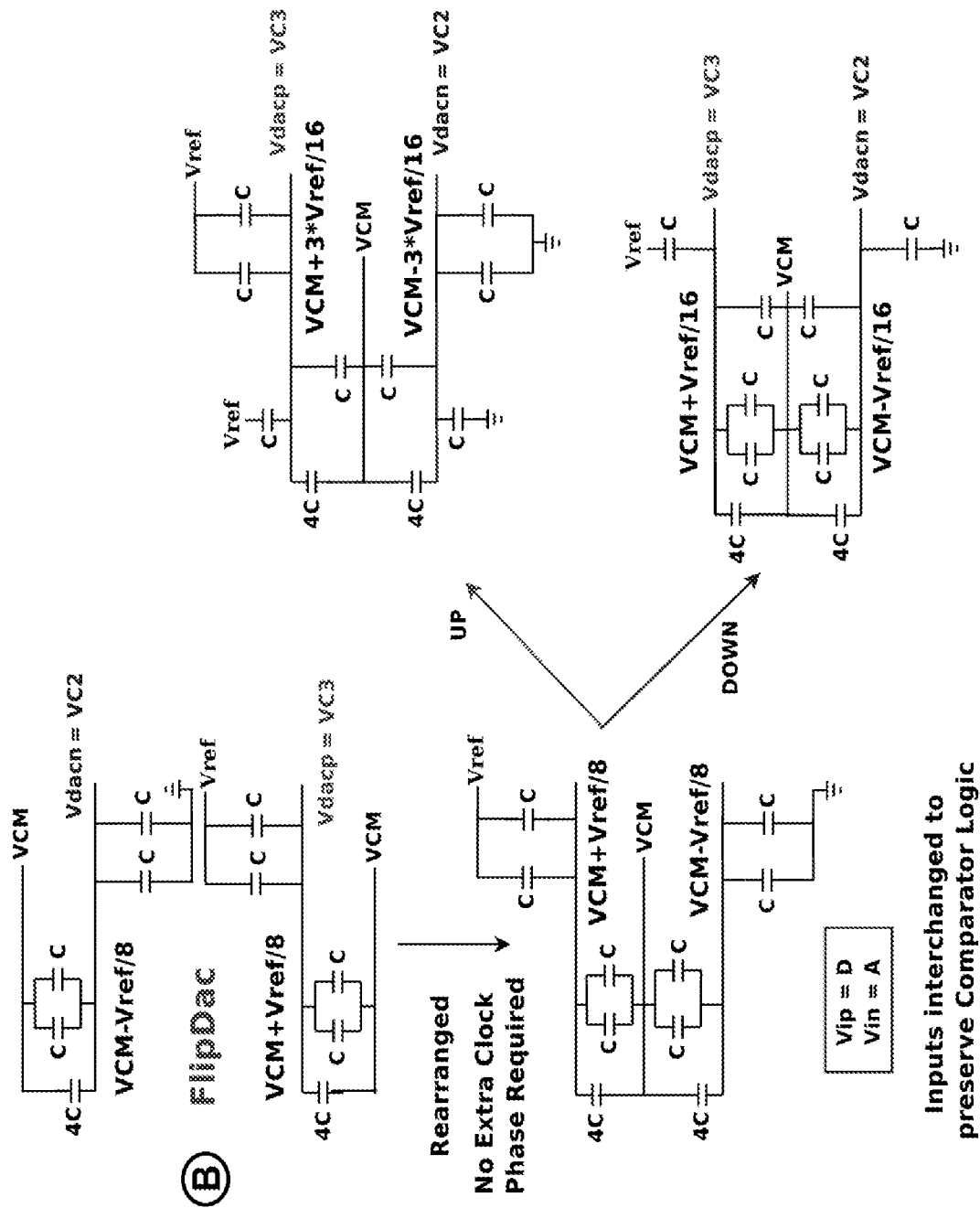


Fig. 3 (Continued)

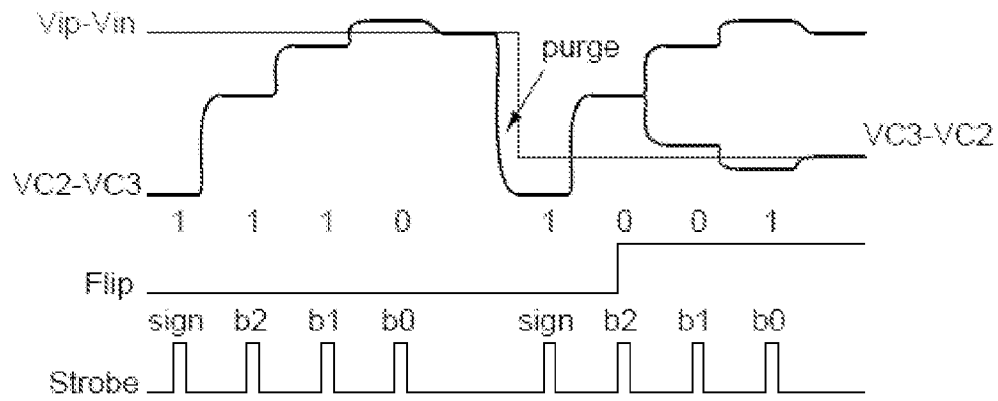


Fig. 4

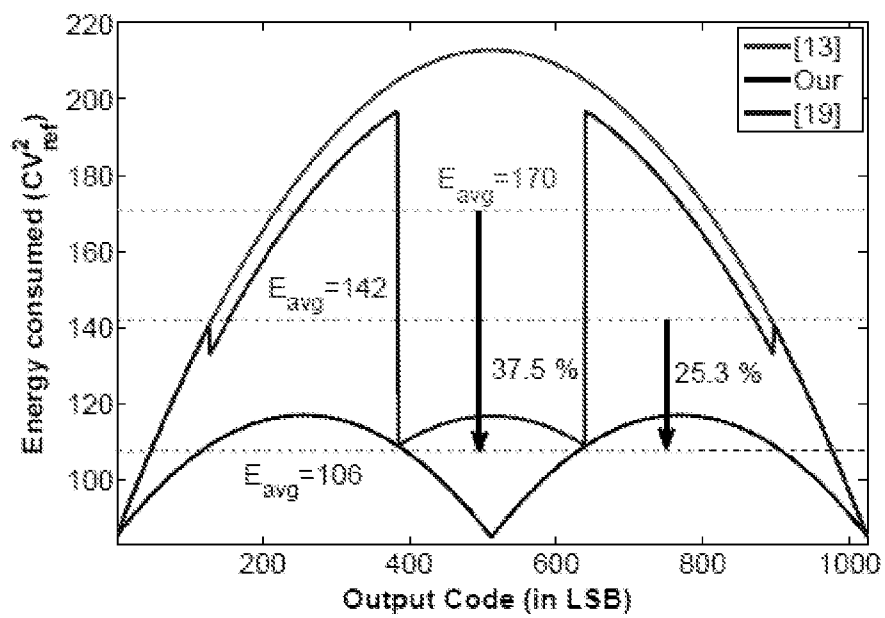


Fig. 5

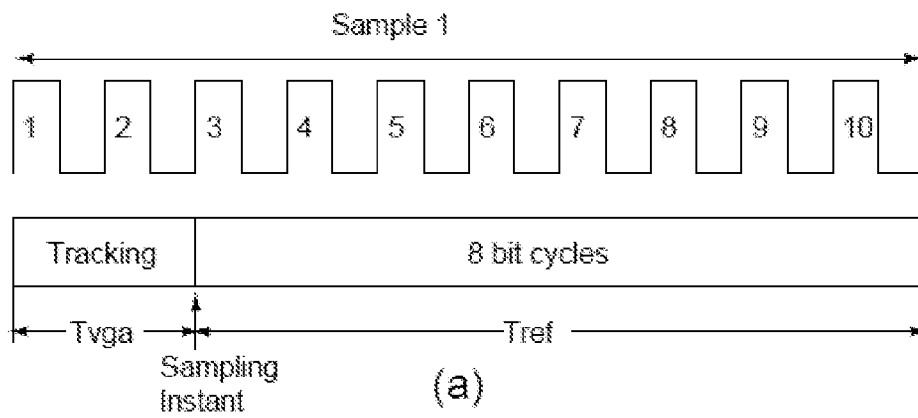


Fig. 6a

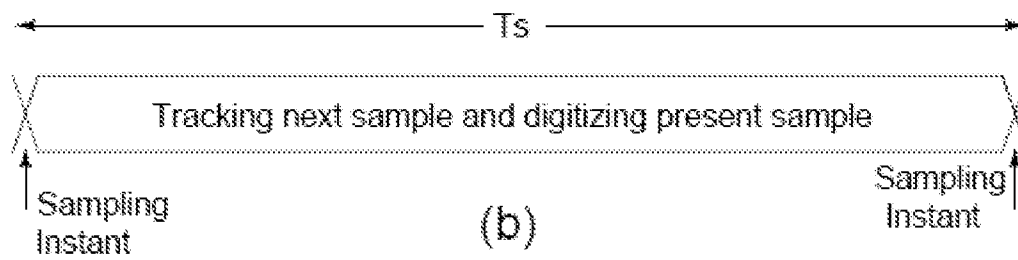


Fig. 6b

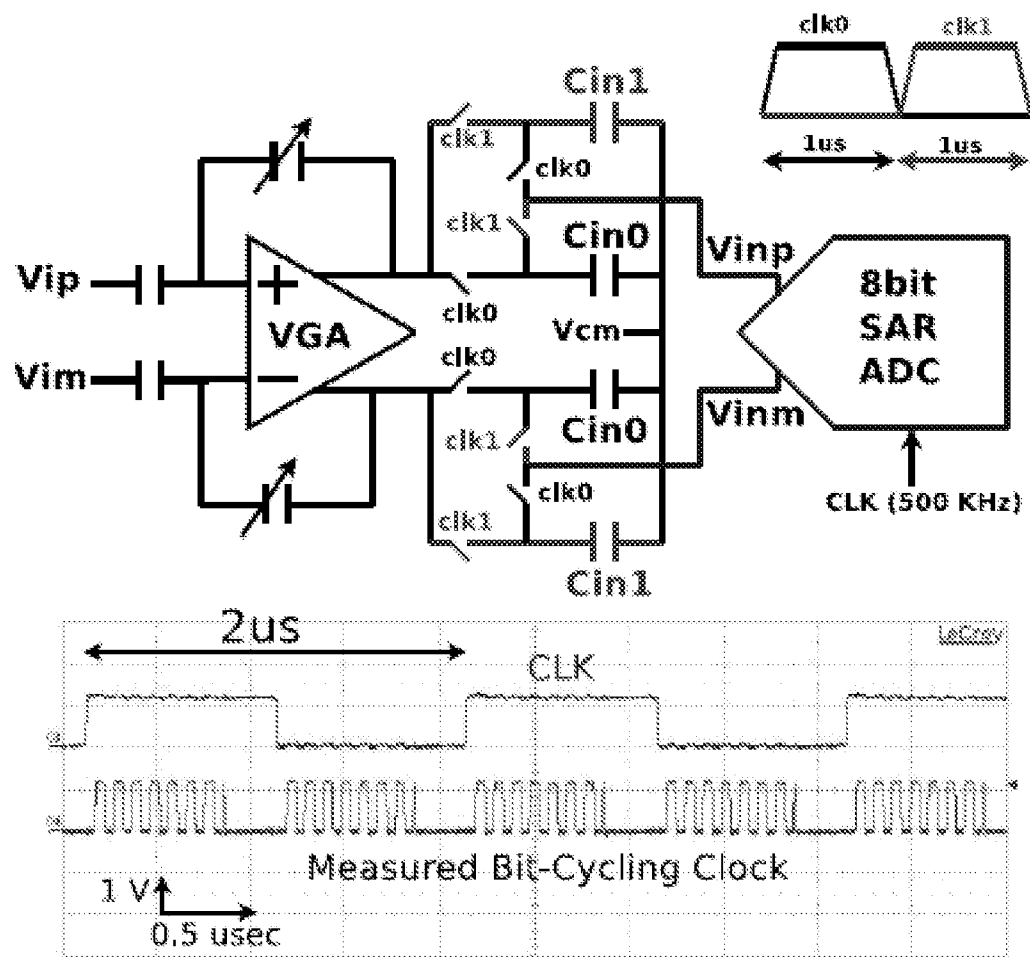


Fig. 7

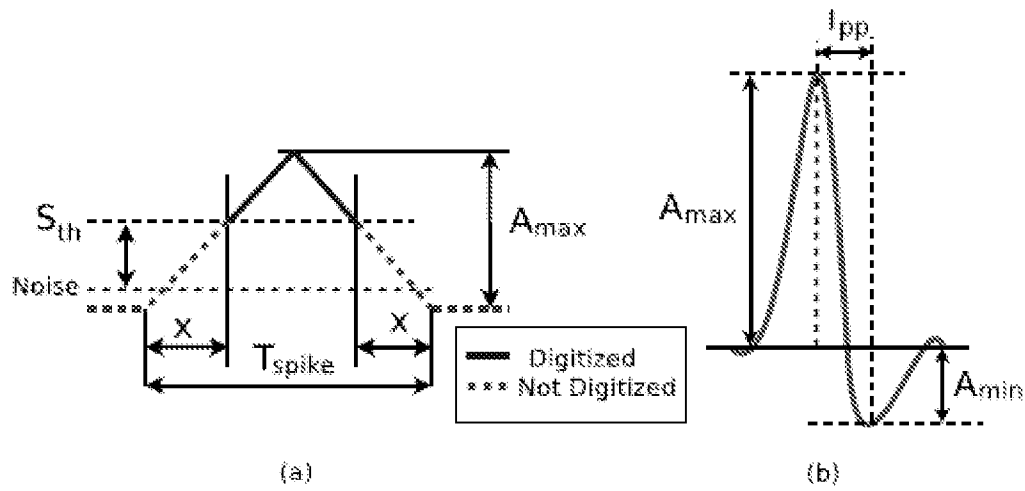


Fig. 8a

Fig. 8b

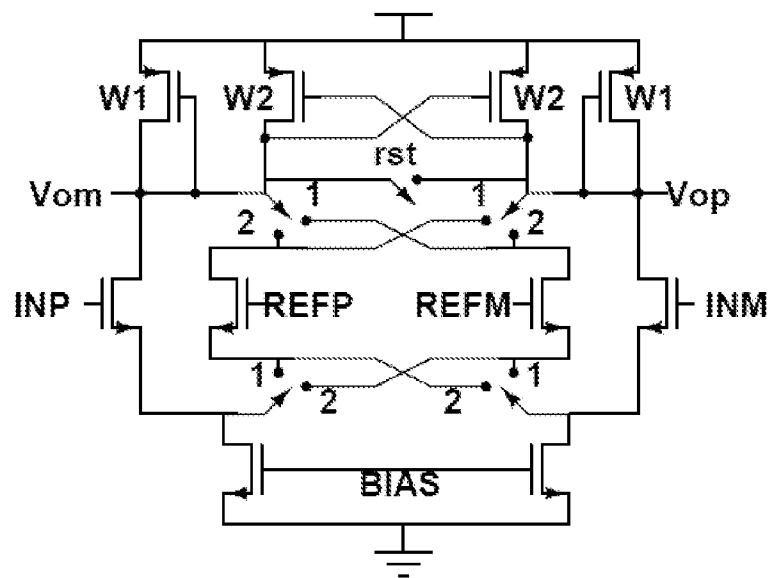


Fig. 9

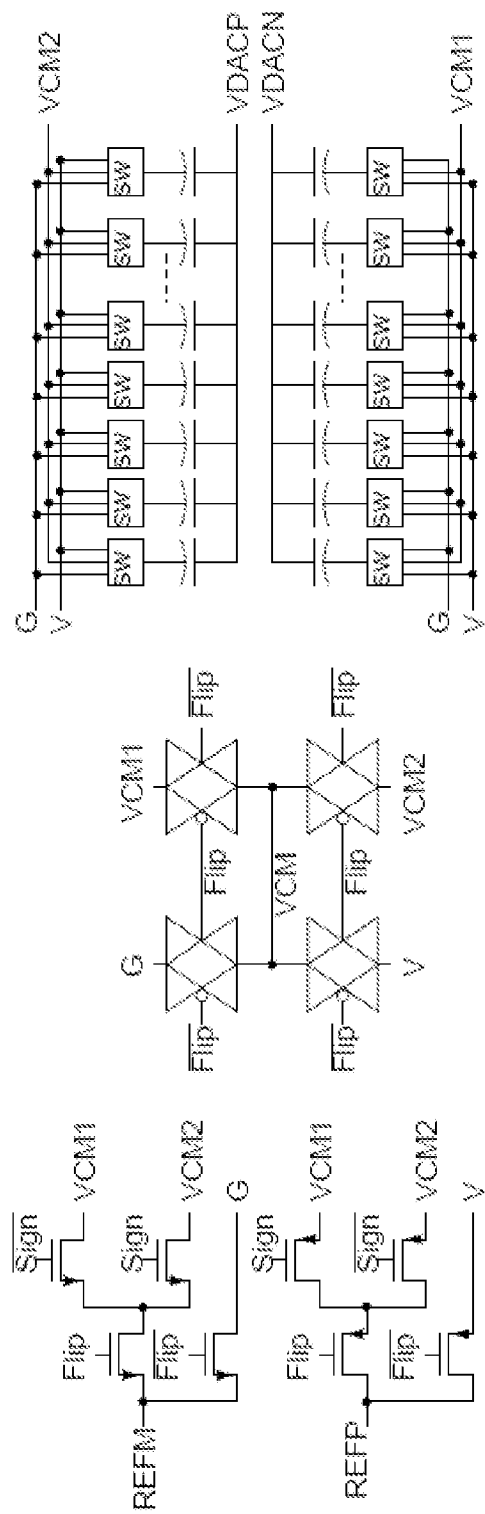


Fig. 10

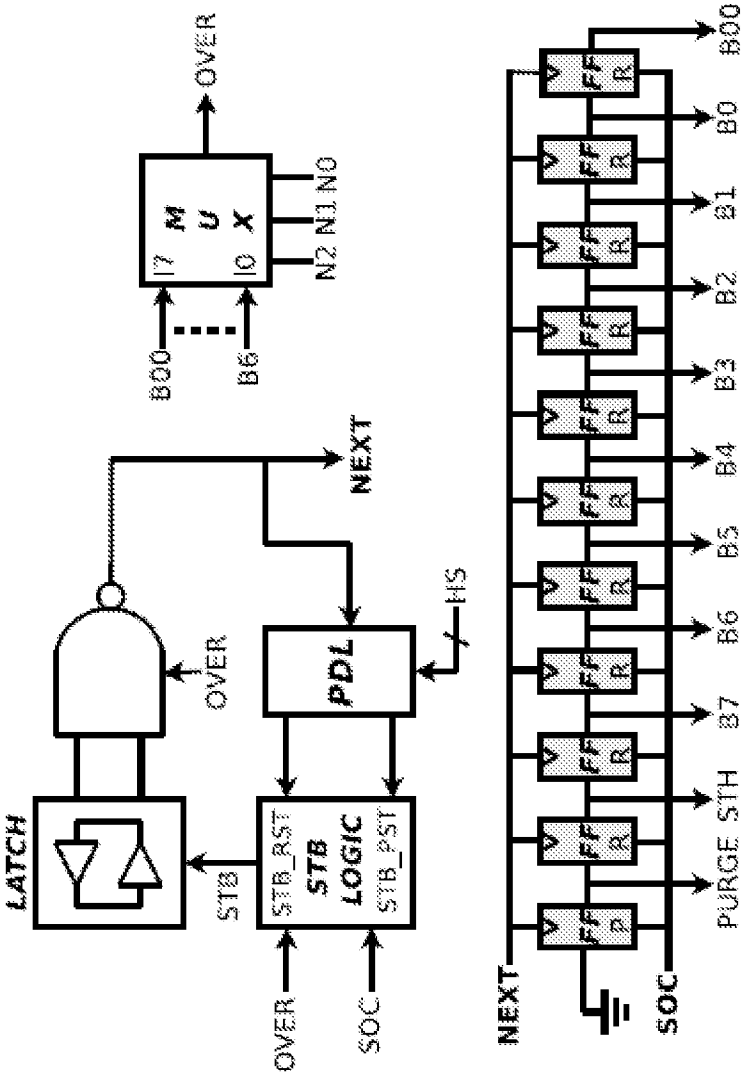


Fig. 11

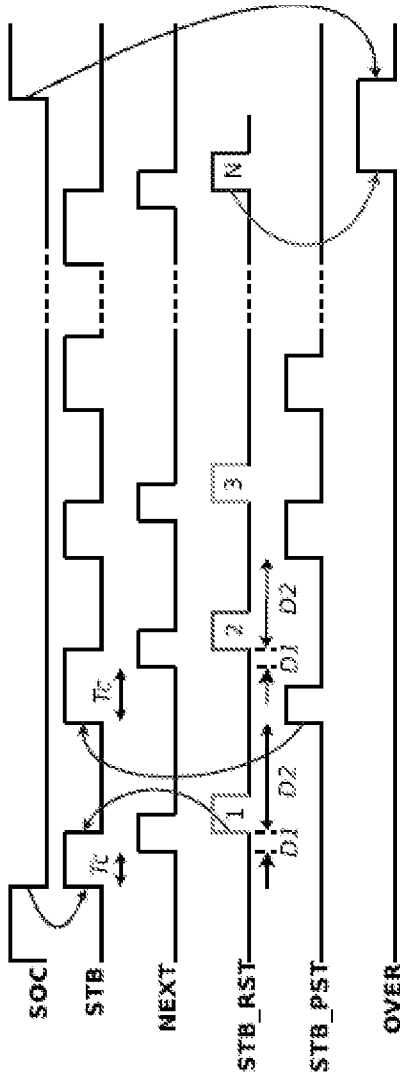


Fig. 12

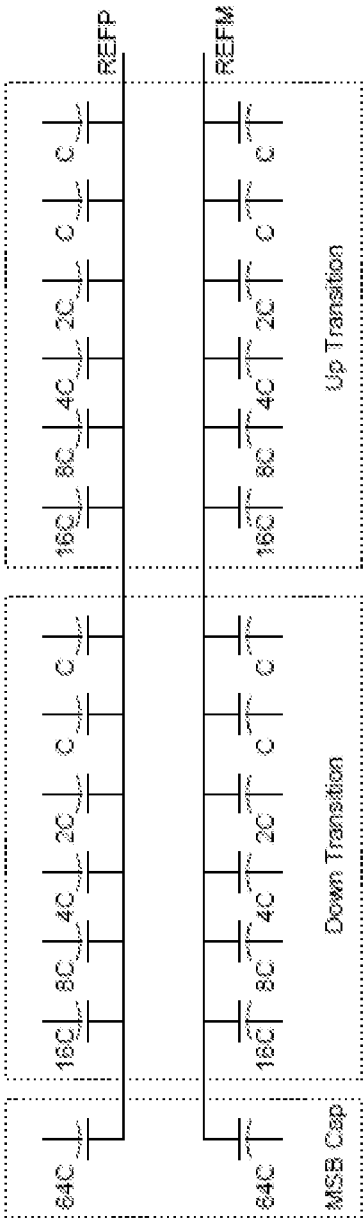


Fig. 13

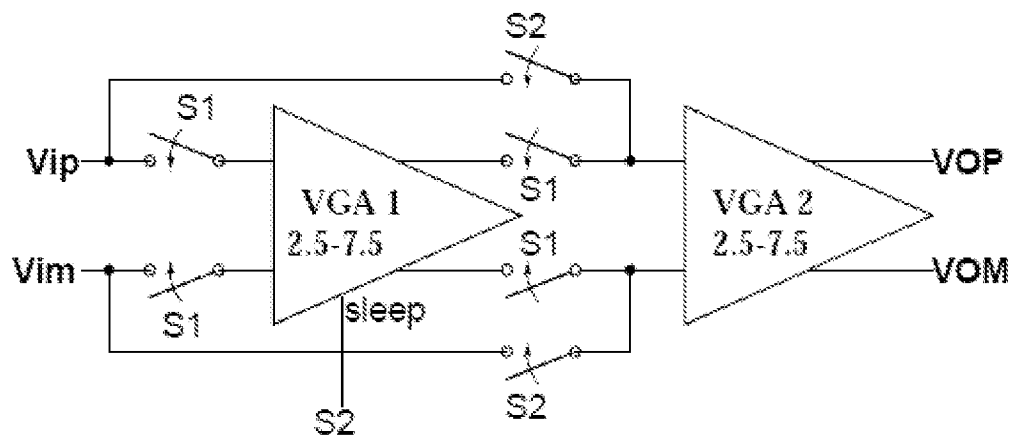


Fig. 14

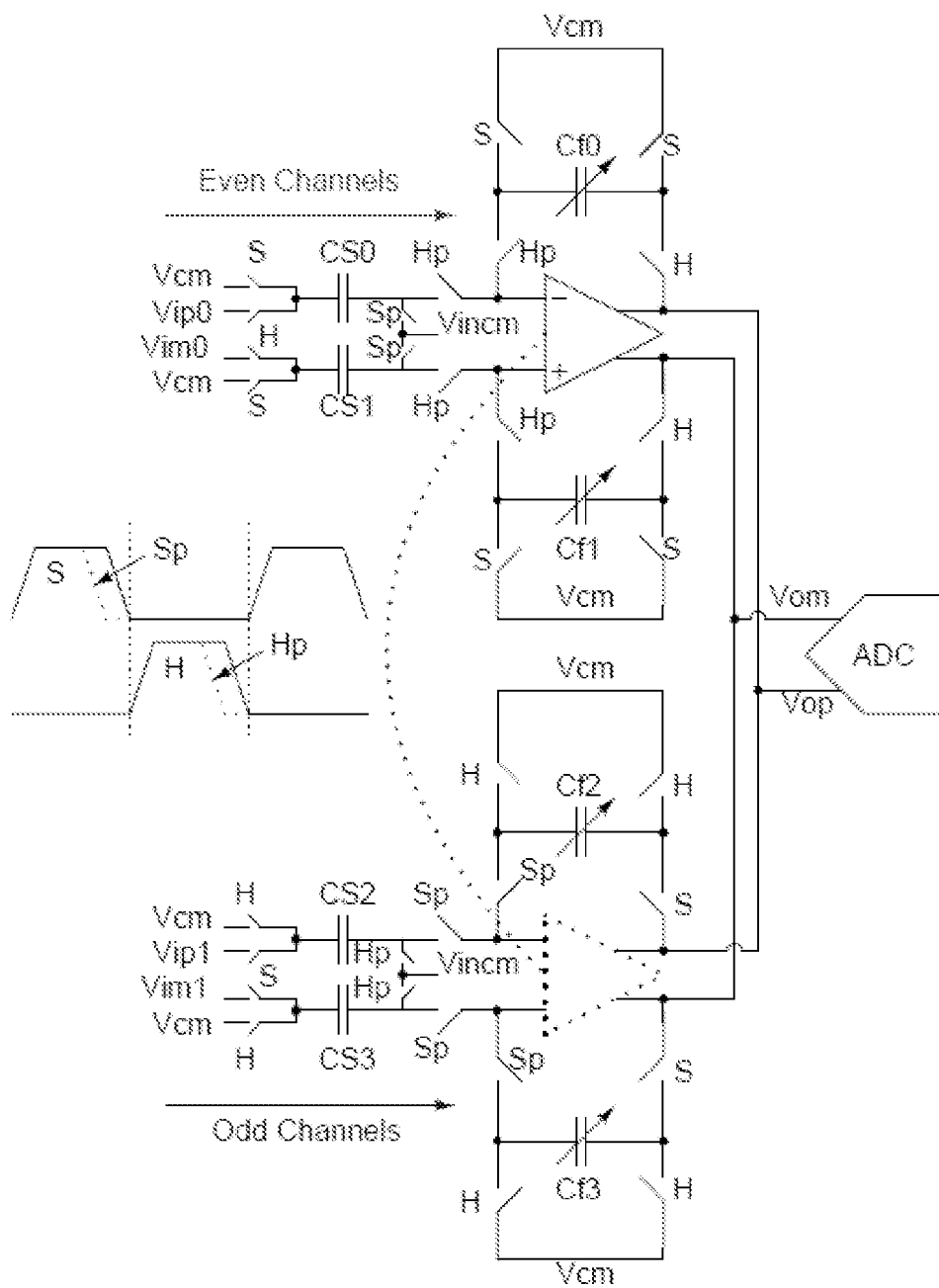


Fig. 15

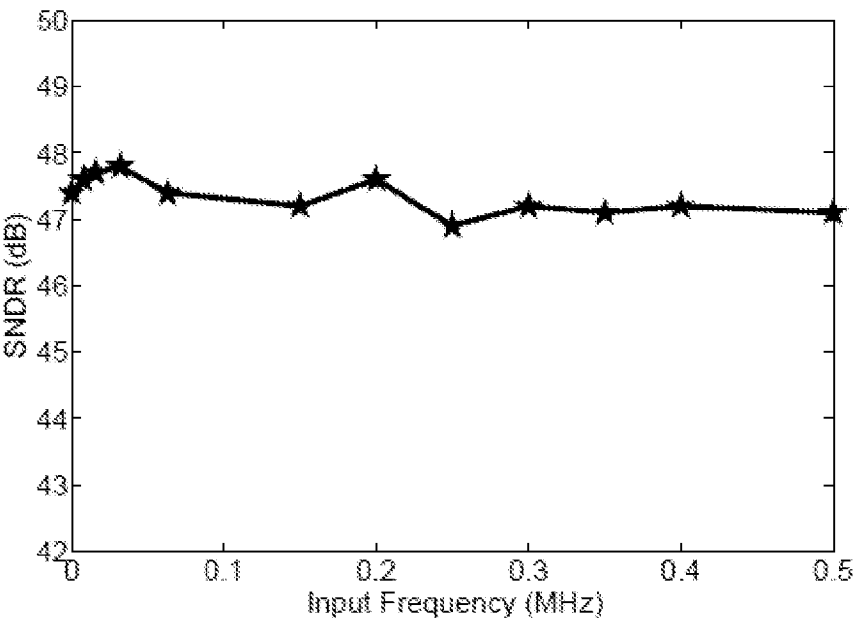


Fig. 16a

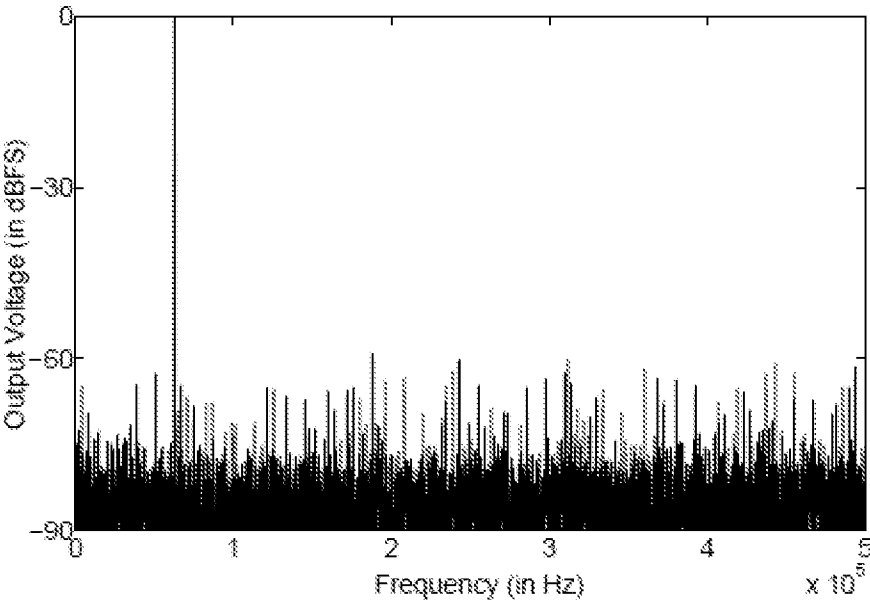


Fig. 16b

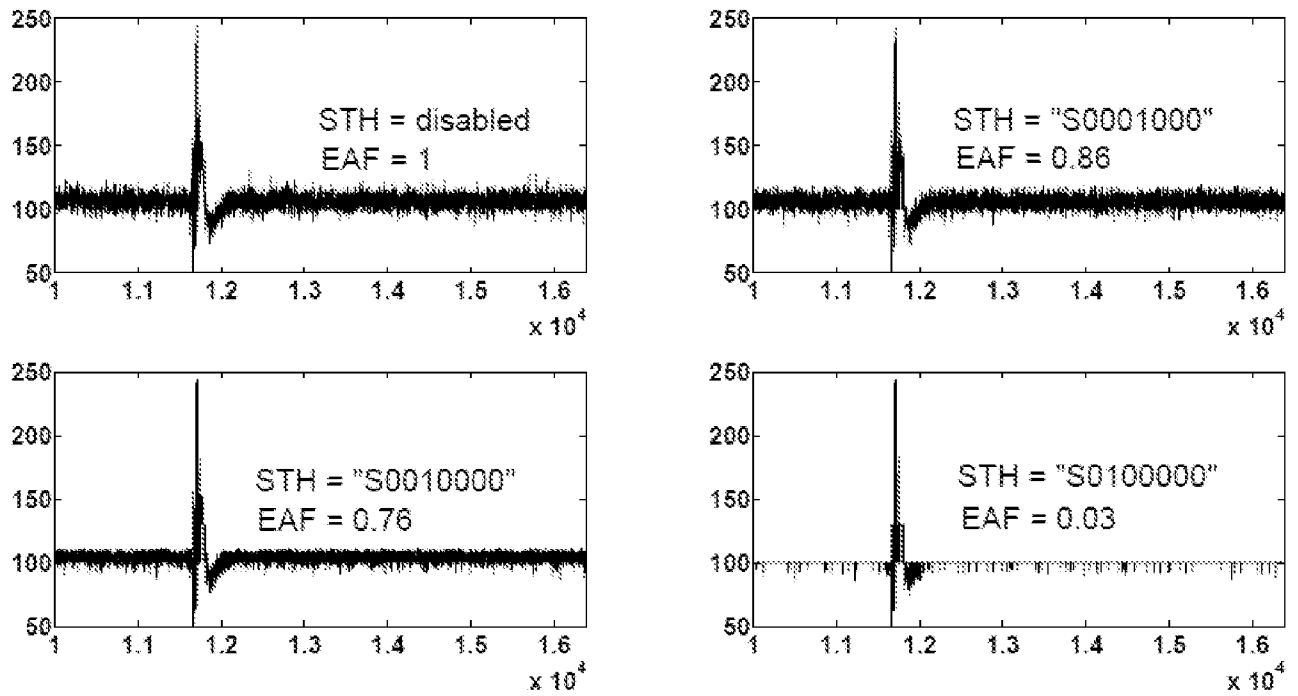


Fig. 17

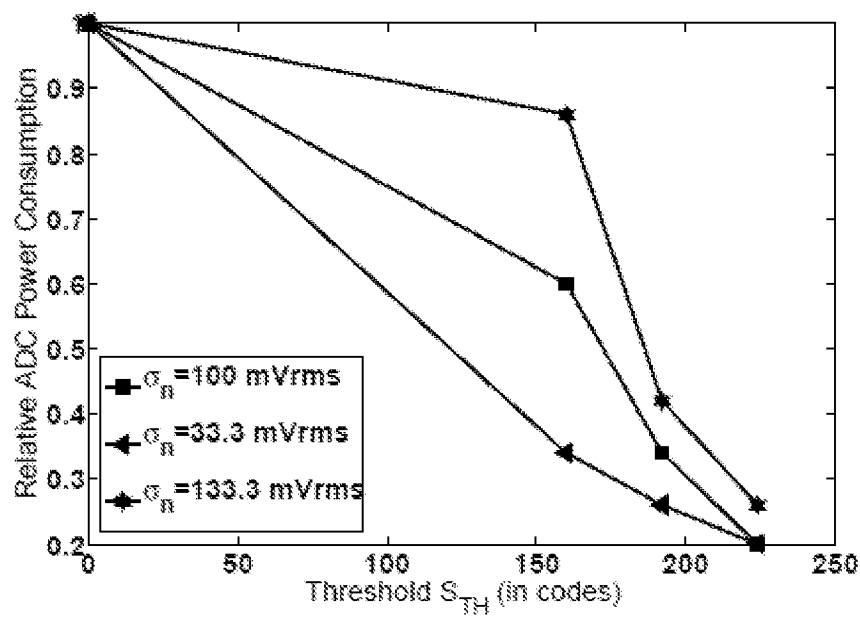


Fig. 18a

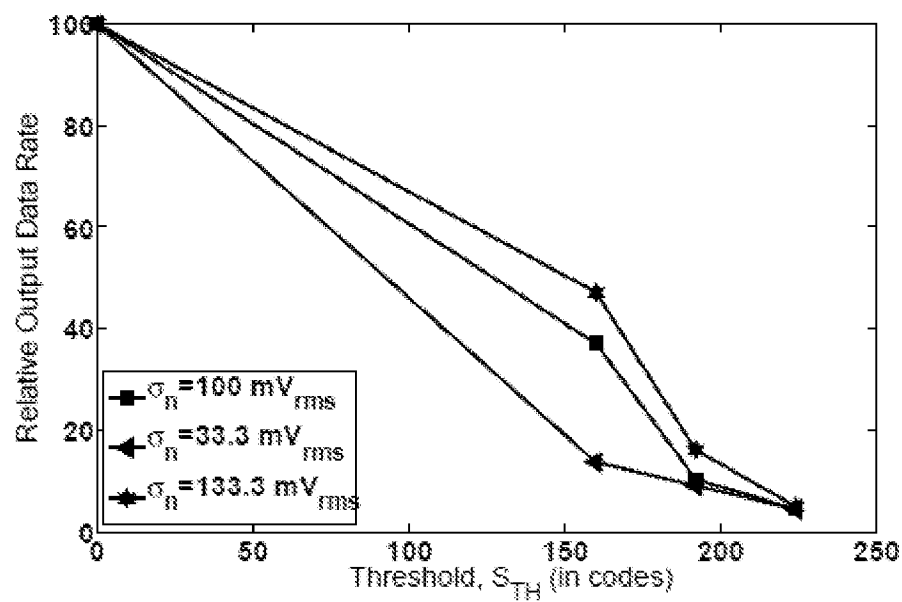


Fig. 18b

INTERNATIONAL SEARCH REPORT

International application No
PCT/IB2012/057456

A. CLASSIFICATION OF SUBJECT MATTER

INV. H03M1/00

ADD. H03M1/46 H03M1/80

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

H03M

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

EPO-Internal

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	ANAND T ET AL: "Energy efficient asymmetric binary search switching technique for SAR ADC", ELECTRONIC LETTERS, THE INSTITUTION OF ENGINEERING AND TECHNOLOGY, vol. 46, no. 22, 28 October 2010 (2010-10-28), pages 1487-1488, XP006037061, ISSN: 1350-911X, DOI: 10.1049/EL:20102691 Introduction figures 2,3 ----- -/--	1-10



Further documents are listed in the continuation of Box C.



See patent family annex.

* Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

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Date of the actual completion of the international search

31 May 2013

Date of mailing of the international search report

07/06/2013

Name and mailing address of the ISA/

European Patent Office, P.B. 5818 Patentlaan 2
NL - 2280 HV Rijswijk
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Fax: (+31-70) 340-3016

Authorized officer

Rocha, Daniel

INTERNATIONAL SEARCH REPORT

International application No
PCT/IB2012/057456

C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT		
Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	GINSBURG B P ET AL: "An Energy-Efficient Charge Recycling Approach for a SAR Converter With Capacitive DAC", CONFERENCE PROCEEDINGS / IEEE INTERNATIONAL SYMPOSIUM ON CIRCUITS AND SYSTEMS (ISCAS) : MAY 23 - 26, 2005, INTERNATIONAL CONFERENCE CENTER, KOBE, JAPAN, IEEE SERVICE CENTER, PISCATAWAY, NJ, 23 May 2005 (2005-05-23), pages 184-187, XP010815508, DOI: 10.1109/ISCAS.2005.1464555 ISBN: 978-0-7803-8834-5 the whole document	1-10
A	----- YAN ZHU ET AL: "A 10-bit 100-MS/s Reference-Free SAR ADC in 90 nm CMOS", IEEE JOURNAL OF SOLID-STATE CIRCUITS, IEEE SERVICE CENTER, PISCATAWAY, NJ, USA, vol. 45, no. 6, 9 June 2010 (2010-06-09), pages 1111-1121, XP011311113, ISSN: 0018-9200, DOI: 10.1109/JSSC.2010.2048498 the whole document	1-10
A	----- CHUN-CHENG LIU ET AL: "A 10-bit 50-MS/s SAR ADC With a Monotonic Capacitor Switching Procedure", IEEE JOURNAL OF SOLID-STATE CIRCUITS, IEEE SERVICE CENTER, PISCATAWAY, NJ, USA, vol. 45, no. 4, 24 March 2010 (2010-03-24), pages 731-740, XP011305775, ISSN: 0018-9200, DOI: 10.1109/JSSC.2010.2042254 the whole document -----	1-10