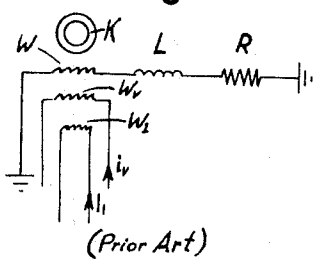
Oct. 10, 1961 E. BADER 3,004,172

SWITCH CORE MATRIX

Filed July 2, 1959 4 Sheets-Sheet 1

Fig. 1a



(Prior Art)

Fig. 1b

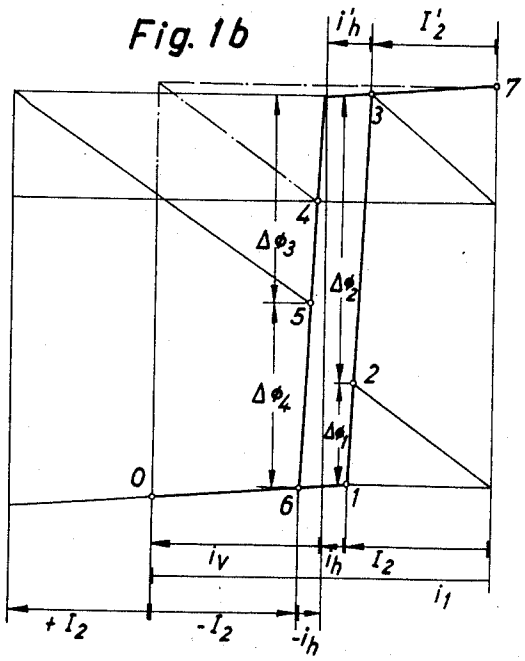


Fig. 1c

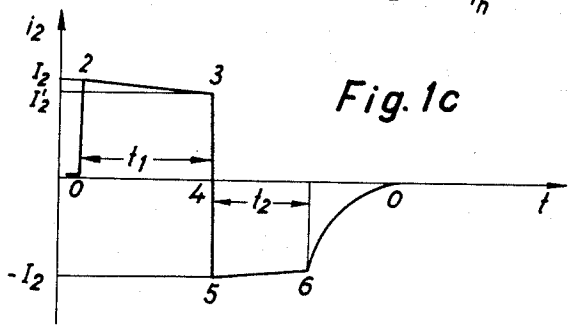
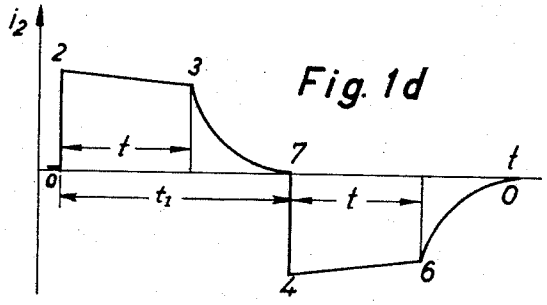


Fig. 1d



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SWITCH CORE MATRIX

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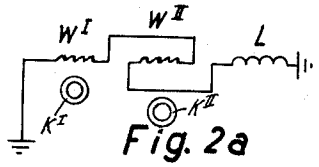
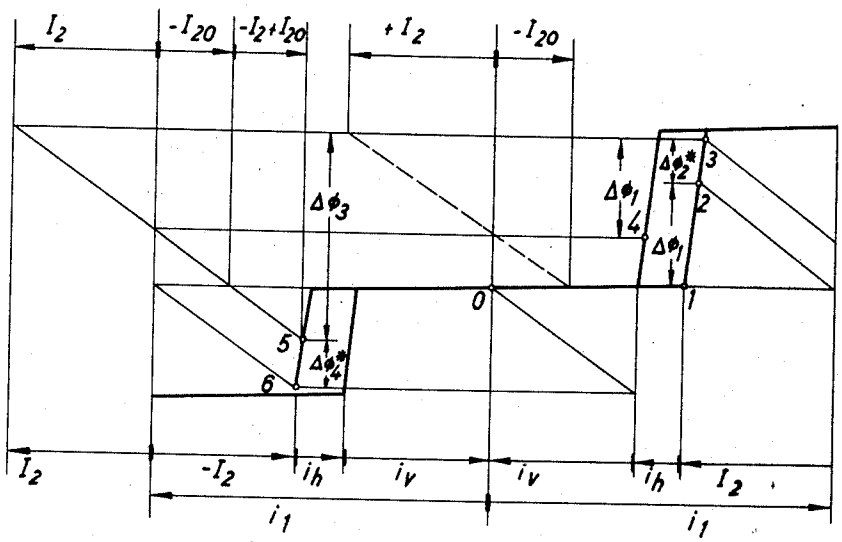


Fig. 2a

Fig. 2b



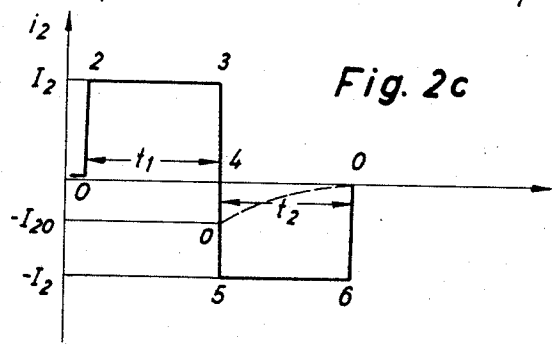


Fig. 2c

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SWITCH CORE MATRIX

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Fig. 3

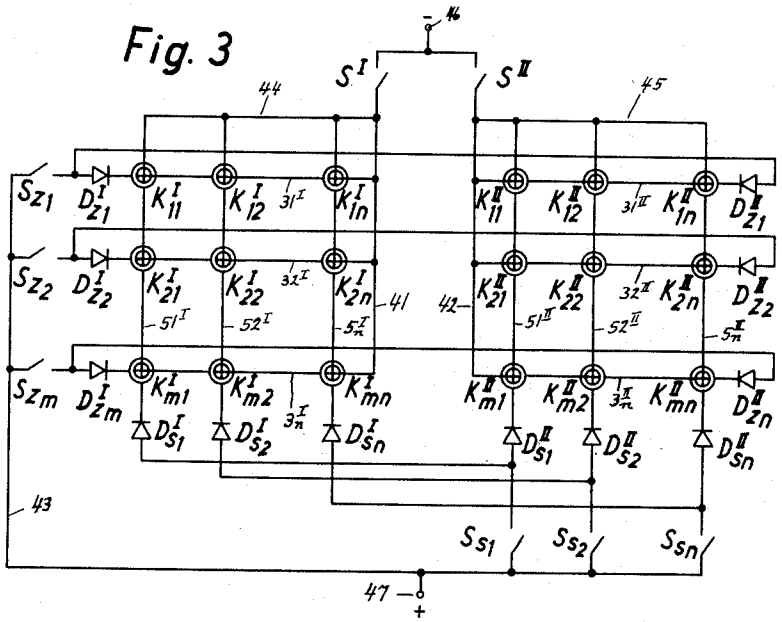
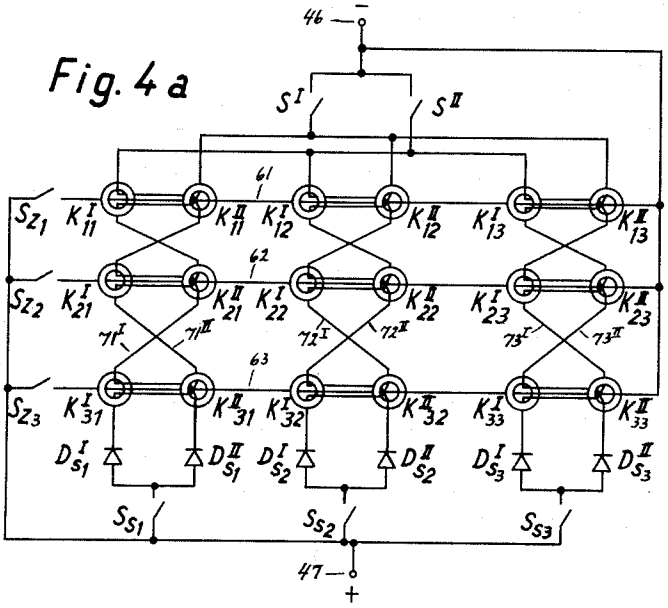


Fig. 4a



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Oct. 10, 1961 E. BADER 3,004,172

SWITCH CORE MATRIX

Filed July 2, 1959 4 Sheets-Sheet 4

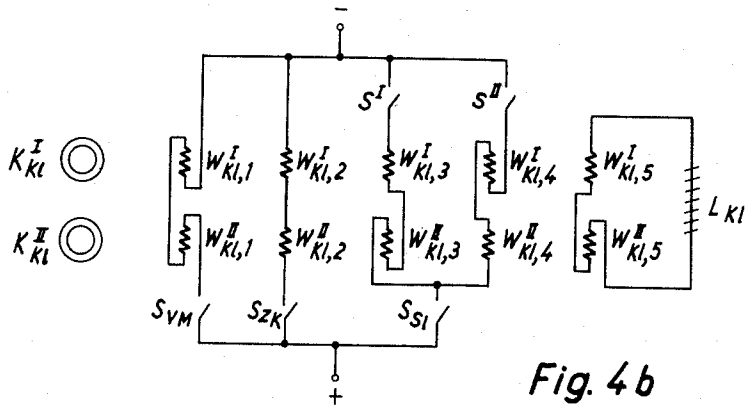

Fig. 4b

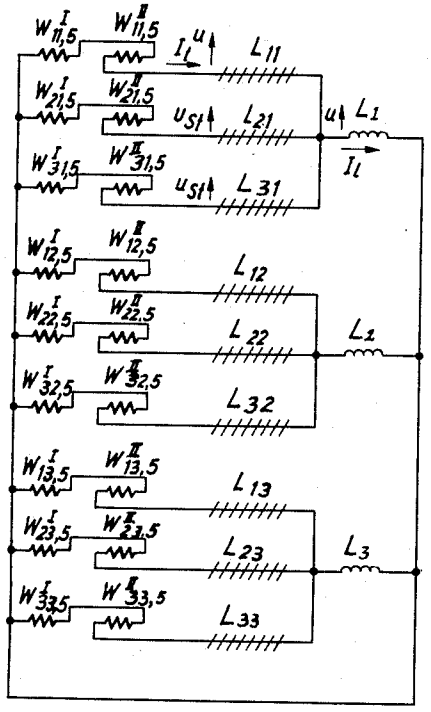

Fig. 5

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United States Patent Office 3,004,172 Patented Oct. 10, 1961

3,004,172

SWITCH CORE MATRIX

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Filed July 2, 1959, Ser. No. 824,505
Claims priority, application Germany July 3, 1958
5 Claims. (Cl. 307—88)

The present invention relates to a switch core matrix having cores made of magnetizable material of approximately rectangular hysteresis curves. At every cross point of such matrix hereinafter referred to as intersections of the columns and rows, a positive and a negative current pulse is to be produced and to be conveyed to an associated load, which load may be the row or the column wire of a storage matrix.

The switch core matrices known in the art have a single switch core at each intersection, and this core has an output winding connected to an associated load. A core is excited upon column and row coincidence and a positive and a negative output pulse succession is produced, provided the output circuit contains an appreciable ohmic component besides the inductive component. The impedance of a storage matrix thus controlled by a switch core matrix is predominantly inductive when either one of its row or its column wires is excited at about half of the current necessary for saturation. Thus, in the switch core matrices known per se, every output switch matrix circuit (which is an input circuit for the storage matrix) must contain an additional ohmic resistance. Further disadvantages of the known switch core matrices will be discussed later.

It is an object of the present invention to provide a novel and improved switch core matrix.

It is another object of the invention to provide a novel and improved wiring circuit for the excitation of cores in a switch core matrix.

It is a further object of the invention to provide a switch core matrix using cores of considerably smaller saturation flux than the flux required for saturation of the cores in known switch core matrices.

It is a still further object of the invention to reduce the power input requirements of switch core matrices.

It is another object of the invention to reduce noise pulses in the output circuits of switch core matrices.

It is a further object of the invention to reduce the time interval between operation cycles in switch core matrices.

It is an additional object of the invention to equalize the positive and the negative pulse lengths in the output circuits of switch core matrices.

It is another object of the invention to improve the shape of output pulses of a switch core matrix.

According to a primary embodiment of the invention, each intersection in a switch core matrix is provided with a pair of cores, whereby one core produces the positive pulse and the other one produces the negative pulse, and the common output load of the two cores is almost exclusively inductive.

Still further objects and the entire scope of applicability of the present invention will become apparent from the detailed description given hereinafter; it should be understood, however, that the detailed description and specific examples, while indicating preferred embodiments of the invention, are given by way of illustration only, since various changes and modifications within the spirit and scope of the invention will become apparent to those skilled in the art from this detailed description.

In the drawings:

FIGURE 1*a* is a circuit diagram of a single core used in a prior art switch core matrix;

FIGURE 1*b* is a diagram of the hysteresis curve of the core used in FIGURE 1*a*;

FIGURE 1*c* is a diagram of the output pulse succession of the circuit shown in FIGURE 1*a*, plotted against time;

FIGURE 1*d* is another diagram of the output pulse succession of the circuit shown in FIGURE 1*a*, operated in another way than shown in FIGURE 1*c*, also plotted against time;

FIGURE 2*a* is a circuit diagram of a pair of cores used in a switch core matrix in accordance with the present invention;

FIGURE 2*b* is a diagram showing the combined hysteresis loops of the cores shown in FIGURE 2*a*;

FIGURE 2*c* is a diagram showing the output of the circuit shown in FIGURE 2*a*, plotted against time;

FIGURE 3 illustrates schematically a switch core matrix in accordance with the invention;

FIGURE 4*a* illustrates schematically a modified switch core matrix in accordance with the invention;

FIGURE 4*b* shows the winding circuits on a pair of cores used in a switch core matrix as shown in FIGURE 4*a*;

FIGURE 5 shows an arrangement of the output circuits of the pairs of cores shown in FIGURE 4*a*, to attenuate noise pulses.

Referring in detail to the drawings, in FIGURE 1*a*, W is an output winding of a switch core K, said winding being connected in series with an inductance L and an additional ohmic resistor R. The core K may be biased magnetically by means of a current i_v flowing through a winding W_v connected to an appropriate voltage source. The core is thus pre-saturated, as indicated by O in FIGURE 1*b*.

Upon coincidence of the actuation of the row and the column of the matrix to which the core K pertains, a resultant current i_1 is passing through a common winding W_1 and the core K is thus energized. This current which actually is a resultant of row and column excitation overcomes the bias current i_v and produces the hysteresis loss current i_h and the secondary current i_2 in the winding W. (In FIGURE 1*b*, an equal number of windings of W, W_v and W_1 is assumed.) In order to produce a current I_2 in the inductive load L, the core must produce a flux $\Delta\Phi=L\cdot I_2$, bringing the saturation of the core up to point 2 (See FIGURE 1*b*), whereby the secondary current i_2 reaches this value I_2 (see FIGURE 1*c*). During the time interval of a positive current pulse in the winding W_1, i.e., during the time from the initiation of a current flow in W_1 until the current i_1 is turned off (interval t_1 in FIGURE 1*c*) the core must supply a flux $\Delta\Phi_2=I_2\cdot R\cdot t_1$ in order to produce the current energy loss in the resistance R. Upon reversal of the excitation current i_1, a flux $\Delta\Phi_3\cong 2\Delta\Phi_1$ is necessary to reduce the current I_2 flowing in the load and to produce a current of equal magnitude but of opposite polarity: $-I_2$. The remaining flux $\Delta\Phi_4=-I_2\cdot R\cdot t_2$ produces the energy loss in the resistance R during the time of the negative current flow $-I_2$. This remaining flux $\Delta\Phi_4$ thus determines the length of the time interval t_2 of the negative current pulse. When the magnetic condition of the core reaches point 6 on the hysteresis loop, the current fades along an exponential function in time containing the time constant L/R. This effects an undesired prolongation of the duration of the cycle of the entire system by approximately three times the time constant value L/R.

With $\Delta\Phi_1=L\cdot I_2$ and $\Delta\Phi_2=I_2\cdot R\cdot t_1$, there is obtained for the time interval t_1 the equation

$$t_1=\frac{\Delta\Phi_2}{\Delta\Phi_1}\cdot\frac{L}{R}$$

The time interval t_2 can be calculated from

$$\Delta\Phi_1 = L \cdot I_2$$

and

$$|\Delta\Phi_4| = |\Delta\Phi_2 - \Delta\Phi_1| = |I_2| \cdot R t_2$$

This results in t_2,

$$t_2 = \left(\frac{\Delta\Phi_2}{\Delta\Phi_1} - 1\right)\frac{L}{R} = t_1 - \frac{L}{R}$$

In other words, in such an arrangement as shown in FIGURE 1*a*, the time interval t_2 of the negative current pulse is always shorter than the time interval t_1 of the positive current pulse, and the difference is precisely the amount of the time constant L/R.

The ratio of these pulse widths is given by

$$\frac{t_2}{t_1} = \frac{\Delta\Phi_2 - \Delta\Phi_1}{\Delta\Phi_2}$$

It is therefore necessary, for such arrangements, that a finite resistance R be used in order to make it possible to obtain a negative pulse.

If, for example, this ratio shall have at least a value of

$$\frac{t_2}{t_1} = \frac{2}{3} \text{ or } \frac{4}{5}$$

the total flux between saturation $\Delta\Phi_1 + \Delta\Phi_2$ must be twice (or three times) the value of the flux $2 \cdot \Delta\Phi_1$, necessary solely for the purpose of reversing the current in the indutance L from $+I_2$ to $-I_2$. In other words, if

$$\frac{t_2}{t_1} = \frac{2}{3}$$

is required, 50% of the entire flux changes produced by the core is a loss. If

$$\frac{t_2}{t_1} = \frac{4}{5}$$

the loss amounts even to 67% of the total flux $\Delta\Phi_1 + \Delta\Phi_2$. Thus, if

$$\frac{t_2}{t_1}$$

approaches 1, the loss increases considerably.

The ratio of the inductance L_s of a saturated switch core to the predetermined load L determines the primary voltage drop across the half-excited switch cores, i.e., those cores through which flows, besides the biasing current i_v, only a row current or a column current $i_1/2$. This occurs when the column to which the particular core pertains is selected but not the row, or vice versa. The ratio L_s/L also determines the noise current in the secondary windings. But with a given magnetic material being used for a core,

$$\frac{\Delta\Phi}{i_h} \sim L_s$$

where the total flux $\Delta\Phi = \Delta\Phi_1 + \Delta\Phi_2$. Furthermore, the current efficiency

$$2I_2/i_1 = \frac{1}{1 + I_2/i_h}$$

as well as the current I_2 itself are predetermined, so that $L_s \sim \Delta\Phi$. Thus, the larger the total flux of the switch core, the larger must be the power delivered by the primary driving stages. This power is determined by the product of the maximum voltage and the maximum current at a given time for the current increase. Also, the larger the total flux of the switch core, the higher will be the secondary noise current pulses which the half-excited cores supply to the corresponding row or column wires of the storage matrix.

If the pulse width ratio is

$$\frac{t_2}{t_1} = \frac{2}{3}\left(\text{or } \frac{4}{5}\right)$$

the flux difference between saturation of the switch cores is to be four times (or six times) the flux $\Delta\Phi_1$ required to satisfy the power requirement of the inductive load L. This rule for proportioning the core circuits results in a considerable increase of the primary driving power and in a considerable increase in the height of the disturbance pulses.

The irreversible branches of the hysteresis loop have a finite slope. Thus, the hysteresis loss current increases from i_h to i'_h during the time of a positive current pulse (when the flux changes by $\Delta\Phi_2$. At the same time, the current in the winding W decreases from I_2 to I'_2. The latter decrease is the greater the higher the flux variation $\Delta\Phi_2$ during this time interval t_1. In the example above, $\Delta\Phi_2$ is three times (five times) the flux $\Delta\Phi_1$ required by the inducance L when the pulse width ratio is

$$\frac{t_2}{t_1} = \frac{2}{3}\left(\text{or } \frac{4}{5}\right)$$

The thus produced slope of the output pulse is very undesirable because of the very narrow tolerance of half of the excitation current for a storage matrix.

In another mode of operation of a known switch core matrix, having but one switch core at each of its intersections, every core is designed in such a manner, that it becomes demagnetized completely upon every positive current pulse and it will be re-magnetized upon the following negative current pulse.

FIGURE 1*d* shows the secondary current i_2 through the inductive load L during the time of one cycle. In a manner similar to the mode of operation explained above, a flux $\Delta\Phi_1 = LI_2$ is produced first by the core upon a coincidence of row and column excitation. This is to produce a current I_2 in the inductive load L. During the time interval t_1 of the positive current pulse, the core first changes its magnetization along the irreversible branch of its hysteresis loop up to point 3, thereby producing a flux $\Delta\Phi_2 = I_2 \cdot R \cdot t$. Thereafter, still during a portion of the interval t_1, the magnetization of the core is shifted into the reverse branch of the hysteresis loop designating the saturation of the core. During the latter portion of the time interval t_1, the current in the inductance L fades out from I_2 (or, more exactly, from I_2') in accordance with an exponential function having the time constant L/R. After a time period which is approximately $3 \cdot L/R$, the current is almost zero and the core has a saturation indicated at 7. At that time, the primary current i_1 is shut off. As a result, the magnetization of the core is shifted to point 4 of the hysteresis loop, and it produces the flux $\Delta\Phi_1$, whereby a current $-I_2$ flows through the inductive load L. The remaining flux $\Delta\Phi_4$ equals the flux $\Delta\Phi_2$. Thus, in this mode of operation, the negative current pulse has a width equal to the width of the positive current pulse. Upon a magnetization indicated by 6 in the hysteresis loop, the current again fades out along exponental function in the inductive load and, after approximately

$$3 \cdot \frac{L}{R}$$

has a magnitude of about zero.

As one can see from this second mode of operation of a device as shown in FIGURE 1*a*, there is a loss in time of about

$$3 \cdot \frac{L}{R}$$

after the positive current pulse. Thus, for a similar flux difference between saturation $\Delta\Phi_1 + \Delta\Phi_2$ of the core, the cycle here is even longer than in the first mode of operation, as explained above. Or, when in the second mode of operation, the cycle equals the cycle of the first mode of operation, the flux difference $\Delta\Phi_1 + \Delta\Phi_2$ must be higher in the former than in the latter. This means a still higher

driving stage power and higher disturbance pulses from a half-way excited core and, furthermore, there would be a steeper slope of the output pulse at the beginning thereof.

Turning now to the matrix in accordance with the present invention, there is shown in FIGURE 2*a* a core circuit thereof and the diagrams of FIGURES 2*c* and 2*b* illustrate its mode of operation. In FIGURE 2*a*, K^{I} and K^{II} are two cores positioned at each intersection of a switch core matrix. There are two output windings W^{I} and W^{II}, each positioned on one core. The input excitation windings are not shown, but their effect will be described explicitly in the following. The output windings W^{I} and W^{II} are connected in series. Each core is provided with a premagnetization winding and primary excitation windings (not shown). An example of a complete circuit will be explained with reference to FIGURE 4*b*; it will be understood, however, that the means to produce particular fluxes, as called for in the following, can be carried out with conventional windings positioned on a core. An inductance L is connected in series with the windings W^{I} and W^{II}. The bias causes both cores to have the magnetization indicated with O in FIGURE 2*b*. During the time interval t_1, incident to the occurrence of the positive current pulses in the excitation windings occurring upon line and row coincidence, the total excitation current for the cores shifts the flux in the core K^{I} by $\Delta\Phi_1=LI_2$, thereby inducing a current I_2 in the winding W^{I} to flow through the inductance load L. During the time interval t_1, the core K^{I} has its magnetization shifted from point **2** to point **3**, whereby a flux $\Delta\Phi_2{}^{*}=I_2\cdot r\cdot t_1$ is produced to cover the energy losses of the ohmic resistance r of the windings, themselves, which cannot be avoided. After the time interval t_1 has elapsed, the exciter current i_1 of the core K^{I} is turned off and the exciter current i_1 for the core K^{II} is turned on. Both of the cores produce the flux $\Delta\Phi_3=2\Delta\Phi$ necessary to reverse the current in the inductive load L from $+I_2$ to $-I_2$. The core K^{I} produces the flux $\Delta\Phi_1+\Delta\Phi_2{}^{*}$ and attenuates thereby the current $+I_2$ causing a current $-I_{20}$ to flow through the inductance (dashed lines in FIGURES 2*b* and 2*c*). Thus, the core K^{II} only needs to produce a flux of $\Delta\Phi_1-\Delta\Phi_2{}^{*}$ to negatively increase the current in the inductance L from $-I_{20}$ to $-I_2$, whereby the magnetization of the core K^{II} is shifted to point **5** of the hysteresis loop. During the time interval $t_2=t_1$ of the negative current pulse, the energy loss of the windings having the inherent resistance r is produced by a flux change of $|\Delta\Phi_4{}^{*}|=|\Delta\Phi_2{}^{*}|=|I_2|\cdot r\cdot t_2$. After the time interval t_2 has elapsed, the core K^{II} has a magnetization indicated by point **6** and the current i_1 of the core K^{II} is turned off. The present flux $|\Delta\Phi_1|=L\cdot|I_2|$ is just sufficient to reduce the current $-I_2$ in the inductance L to zero. In other words, the core K^{II} returns directly to saturation point O and the negative current pulse obtains a steep trailing edge, as shown in FIGURE 2*c*.

In the following, the two devices shown in FIGURES 1*a* and 2*a* are being compared.

(1) In an arrangement using two cores, the core K^{I} (FIGURE 2*a*) is proportioned to merely produce a flux difference $\Delta\Phi_1+\Delta\Phi_2{}^{*}$, the latter sum exceeding the flux $\Delta\Phi_1$, desired by the inductive load only by an amount $\Delta\Phi_2{}^{*}=I_2\cdot r\cdot t_1$, due to the unaviodable energy loss in the windings. The core K^{II} is proportioned only to produce a flux $\Delta\Phi_1$. Thus, the flux to be produced by the two cores totals $2\Delta\Phi_1+\Delta\Phi_2{}^{*}$. This sum is considerably smaller than the flux $\Delta\Phi_1+\Delta\Phi_2$ to be produced by the single core of FIGURE 1*a*. In the assumed example, employing a single core, the required flux $2\Delta\Phi_1+\Delta\Phi_2{}^{*}$, where $r\cong 0$ and, therefore, $\Delta\Phi_2{}^{*}=0$, is theoretically only 50% (or 33%), practically 60% (or 40%) of the required flux

$\Delta\Phi_1+\Delta\Phi_2=4\Delta\Phi_1$ (or $6\Delta\Phi_1$) of one core in the present arrangement, if the ratio of the puse width

$$\frac{t_2}{t_1}=\frac{2}{3}\left(\text{or }\frac{4}{5}\right)$$

Consequently, if a double-core arrangement is used, the switching power to be produced by the primary driving stage and the secondary disturbance pulses of semi-excited cores are considerably smaller than they are in a single core arrangement, because the said power and the said disturbance pulses increase with the total flux change of a core.

This advantage shows off particularly where the operation takes place with a high current efficiency factor of $2I_2/i_1$ which, in turn affects the driving power requirements.

(2) During the time interval t_1, the magnetization of the core K^{I} of a double core arrangement merely shifts by the small amount of $\Delta\Phi_2{}^{*}=I_2\cdot r\cdot t_1$ on the irreversible branch of the hysteresis loop having a finite slope. Thus, the slope of the current during this interval t_1 is considerably reduced as compared with the corresponding slope when a single core arrangement is used, wherein the long portion $\Delta\Phi_2=I_2\cdot r\cdot t_1=3\Delta\Phi_1$ (or $5\Delta\Phi_1$), on the irreversible branch of the hysteresis loop is required to be covered during the time interval t_1.

(3) When a double core arrangement is used, the pulse width ratio amounts to

$$\frac{t_2}{t_1}=1$$

and the trailing edge of the negative current pulse slopes down steeply and the slope does not follow a relatively slow exponential function having a time constant of L/R. The time of one cycle totals only $t_1+t_2=2t_1$, which is given by the load requirements, to which sum merely the naturally finite slope of leading and trailing edge is added, said slopes being determined by the driving stage. There are no waiting periods between pulses which must elapse during a proper operation of the switch core matrix.

Having now fully disclosed the salient element used in the present invention, examples of complete arrangements thereof are being explained in the following with reference to FIGURES 3, 4*a* and 4*b*.

In FIGURE 3, there are illustrated m lines and n rows of a switch core matrix having pairs of cores $K_{11}{}^{I}$, $K_{11}{}^{II}$; $K_{12}{}^{I}$, $K_{12}{}^{II}$ . . ., $K_{1n}{}^{I}$, $K_{1n}{}^{II}$; $K_{21}{}^{I}$, $K_{21}{}^{II}$; $K_{22}{}^{I}$, $K_{22}{}^{II}$ . . .; $K_{2n}{}^{I}$, $K_{2n}{}^{II}$ . . .; $K_{m1}{}^{I}$, $K_{m1}{}^{II}$; $K_{m2}{}^{I}$, $K_{m2}{}^{II}$ . . .; $K_{mn}{}^{I}$, $K_{mn}{}^{II}$.

Every core is provided with a bias winding connected to an appropriate voltage source similar to the winding W_v, shown in FIGURE 1. Every core is further provided with a pickup winding corresponding to the winding W, shown in FIGURES 1*a* and 2*a*. Pickup windings of corresponding cores are connected in series, as shown with the windings W^{I} and W^{II}, as shown in FIGURE 2*a*.

FIGURE 3 shows $n\cdot m$ arrangements, are shown in FIGURE 2*a*. Furthermore, there are provided n electronic timing switches S_{z1}, S_{z2}, . . . S_{zm}, adapted to turn on and off the current in column excitation wires 31^{I}, 31^{II}; 32^{I}, 32^{II}; . . . $3_n{}^{I}$, $3_n{}^{II}$, respectively. These column wires pass through the cores, as shown, and it is to be understood that they have appropriate windings connected in series to excite the said wires. Line wire 31^{I}, 32^{I} . . . $3_n{}^{I}$ terminate at a common conductor **41** which is connected to the negative terminal **46** of a voltage source via an electronic time switch S^{I}, while column wires 31^{II}, 32^{II}, . . . $3_n{}^{II}$ terminate at a common conductor **42** which is also connected to the negative terminal **46** of the said voltage source. Every one of the wires has inserted a diode $D_{z1}{}^{I}$, $D_{z1}{}^{II}$, $D_{z2}{}^{I}$, $D_z{}^{II}$, . . . $D_{zn}{}^{I}$, $D_{zn}{}^{II}$, respectively. It will be appreciated that, for example, the wire 31^{I} is connected in series with the diode $D_{z1}{}^{I}$ and with the

switch S^I, and the wire 31^{II} is connected in series with the diode D_{z1}^{II} and with the switch S^{II}, while these two series circuits are connected in parallel and are further connected in series with the electronic switch S_z, the latter being connected to a positive terminal 47 of the voltage source via a conductor 43. The cores K_{11}^I, K_{21}^I to K_{m1}^I are passed by a common row wire 51^I, cores K_{12}^I, K_{22}^I, to K_{m2}^I are penetrated by a common row wire 52^I and, correspondingly, cores K_{1n}^I, K_{2n}^I to K_{mn}^I are penetrated by a common wire 5_n^I. Cores forming the in-between rows are correspondingly penetrated by common wires. Furthermore, cores K_{11}^{II}, K_{21}^{II} to K_{m1}^{II} are penetrated by a common row wire 51^{II} connected to wire 51^I; cores K_{12}^{II}, K_{22}^{II} to K_{m2}^{II} are penetrated by a common row wire 52^{II} which is connected to wire 52^I.

The cores of the following rows are penetrated by common row wires which are, in turn, connected to the corresponding wires penetrating the cores marked with I. Wires 51^I, 52^I to 5_n^I are connected to a common line 44 which, in turn, is connected to line 41 and to switch S^I. Correspondingly, the wires 51^{II}, 52^{II} to 5_n^{II} are connected to a common line 45 which, in turn, is connected to line 42 and switch S^{II}.

The wires 51^I, 51^{II}, 52^I, 52^{II}, to 5_n^I, 5_n^{II} are connected in series with diodes D_{s1}^I, D_{s1}^{II}, D_{s2}^I, D_{s2}^{II}, to D_{sn}^I, D_{sn}^{II}, respectively.

Thus, the wire 51^I is connected in series with the diode D_s^I, said wire 51^I being connected with the diode D_s^{II} and these two series circuits are connected in parallel and are further connected to the positive terminal of the voltage source via an electronic switch S_{s1}. Correspondingly, the wire 52^I with diode D_{s2}^I is connected in parallel to the wire 52^{II} with diode D_{s2}^{II} and both are connected in series with the switch S_{s2}^{II} which, in turn, is connected to the positive terminal of the voltage source. The other row wires are connected correspondingly and, finally, wire 5_n^I with diode D_{sn}^I is connected in parallel to the wire 5_n^{II} and the diode D_{sn}^{II}, while both are connected to the positive terminal via an electronic switch S_{sn}.

It will be appreciated that there are two matrices of cores which correspond to each other. Thus, core K_{11}^I and K_{11}^{II}, K_{12}^I and K_{12}^{II} . . . form pairs of switch cores and the entire device becomes a double-core matrix arrangement.

When, for example, the electronic column switch S_{zm} is closed, column m is selected and, furthermore, when electronic switch S_{s2} is closed, the second row is selected and the core pair K_{m2}^I and K_{m2}^{II} may be energized. This is caused by closing the switch S^I for the time of a positive current pulse and by closing the switch S^{II} for the time of a negative current pulse. Upon closing switch S^{II}, the switch S^I is opened simultaneously. The switches S^I and S^{II} thus energize those cores which were selected by any of the switches S_{z1} to S_{zm} and by any one of the switches S_{s1} to S_{sn}. The diodes avoid the excitation of the cores of group II during the positive current pulse and the excitation of the cores of group I during the negative current pulse via shunt paths. Considering, for example, the case discussed above, wherein the switch S_{s2} was closed for selecting row 2, and wherein for the time of the positive current pulse switch S^I was closed. Thus, there was flowing a current through the wire 52^I. The switch S^{II} was still open, because no current is supposed to flow through the wire 52^{II} during the time of a positive pulse. However, suppose diode D_{s1}^{II} were not there, a current would flow from the positive terminal via closed switch S_{s2}, wire 52^{II}, wire 51^{II}, wire 51^I, line 44, closed switch S^I to the negative terminal. Similar parallel currents could flow through all other wires of group II if the diodes were omitted. Thus, without diodes, there would be a strong excitation of the cores in group II during the time of a positive pulse, even if the switch S^{II} were open.

When, for example, the core pair K_{m2}^I and K_{m2}^{II} is selected by closing the switches S_{zm} and S_{s2}, the switch S^I is closed for a first time interval and switch S^{II} is closed immediately thereafter for a second time interval of a length equal to the first time interval. The cores K_{m2}^I and K_{m2}^{II} are energized thereby in a manner explained with reference to FIGURES 2*a* to 2*c* and, upon selection of any core pair, similar excitation will result.

FIGURE 4*a* illustrates a modification of the device shown in FIGURE 3. For the sake of facilitation, the matrix shown has three columns and three rows, but it is to be understood that this number is in no way a limitation of the concept of the invention and any other number of columns and rows may be used, whereby the number of rows may not necessarily be equal to the number of columns. Core pairs are shown in related position and they are penetrated by common column wires 61, 62 and 63.

There are three pairs of row wires 71^I, 71^{II}; 72^I, 72^{II}; 73^I, 73^{II}; and each wire pair penetrates each core of its associated row. However, the fluxes produced in each core by different wires oppose one another. Diodes are inserted only in the row wires because the diodes in the column wire may be omitted. It is to be understood that, in a given matrix, the designation rows and columns is arbitrary. Thus, either the row diodes or the column diodes in FIGURE 3 may be omitted. The arrangement of FIGURE 4*a* has the advantage over that in FIGURE 3, that a compensation of the noise pulses can be provided, said compensation being explained more fully with reference to FIGURE 5.

The exact circuit of the windings for every one of the core pairs is shown in FIGURE 4*b*. The cores are generally designated by K_{k1}^I and K_{k1}^{II} in general. Every core has five windings $W_{k1,1}^I$, $W_{k1,2}^I$, $W_{k1,3}^I$, $W_{k1,4}^I$, $W_{k1,5}^I$, and $W_{k1,1}^{II}$, $W_{k1,2}^{II}$, $W_{k1,3}^{II}$, $W_{k1,4}^{II}$, $W_{k1,5}^{II}$, respectively. $W_{k1,1}^I$ and $W_{k1,1}^{II}$ are connected in series and to the voltage source via a switch S_{vm} to produce a pre-magnetization, shifting the two cores into the position of negative remanence (point O in FIGURE 2*b*). The windings $W_{k1,2}^I$ and $W_{k1,2}^{II}$ are also connected in series, but they produce fluxes in the two cores of equal magnitude but opposite to the fluxes produced by windings $W_{k1,1}^I$ and $W_{k1,1}^{II}$. These windings $W_{k1,2}^I$ and $W_{k1,2}^{II}$ are inserted in the column wire which would be designated in FIGURE 4*a* with GI_{k1} controlled by switch S_{z1}, wherein k can be an integer from 1 to 3 and l can also be any integer from 1 to 3. The windings $W_{k1,3}^I$ and $W_{k1,3}^{II}$ are connected in series, but in such a manner that winding $W_{k1,3}^I$ produces a flux of the same magnitude in the same direction of the flux produced by winding $W_{k1,2}^I$, while winding $W_{k1,3}^{II}$ produces a flux of equal magnitude in the same direction as the flux produced by winding $W_{k1,1}^{II}$. Upon closure of switches S_{s1} and S^I during a positive pulse, the pre-magnetization of core W_{k1}^I by winding $W_{k1,1}^I$ is compensated to zero, while the pre-magnetization of core K_{k1}^I by winding $W_{k1,1}^{II}$ is increased towards negative saturation. If both switches S_{zk} and S_{z1} are closed upon coincidence of row and column for selecting core pair K_{k1}^I and K_{k1}^{II}, the magnetization of core K_{k1}^I is reversed and shifted into positive saturation. Thereby, a pulse is produced in an output winding W_{k1}^I and in its load L_{k1} which is an associated column or row wire of a storage matrix (not shown.) The fourth windings $W_{k1,4}^I$ and $W_{k1,4}^{II}$ are connected in parallel but in such a manner, as to oppose the fluxes produced by windings $W_{k1,3}^I$ and $W_{k1,3}^{II}$. Upon a negative current pulse, switches S_{s1} and S^{II} are closed and the core K_{k1}^I is shifted even more into negative saturation. While in the second core K_{k1}^{II}, the pre-magnetization produced by winding $W_{k1,1}^{II}$ is cancelled to zero. Switch S_{zk} is still closed, thus, core K_{k1}^I remains negatively saturated. The magnetization of core K_{k1}^{II} is shifted to positive saturation, whereby an output pulse is produced in winding $W_{k1,5}^{II}$, connected in series with winding $W_{k1,5}^I$. Due to the direct series connection of

the windings $W_{k1,2}^{I}$ and $W_{k1,2}^{II}$, the noise pulses compensate each other in the fifth windings, which are connected to produce oppositely directed pulses. The noise pulses occur, due to the slight slope of the saturation branches of the hysteresis loop of half-way excited cones.

FIGURE 5 illustrates how the noise pulses are cancelled which pulses are produced by the half-way excited cores of a switch core matrix in accordance with the invention. This figure shows the output windings of the first row of the matrix shown in FIGURE 4*a*, $W_{11,5}^{I}$, $W_{11,5}^{II}$, $W_{21,5}^{I}$, $W_{21,5}^{II}$, $W_{31,5}^{I}$, $W_{31,5}^{II}$. Winding $W_{11,5}^{I}$ is the output winding (the fifth winding according to the circuit shown in FIGURE 4*b*), of core K_{11}^{I} and is connected in series with windings $W_{11,5}^{II}$ of core K_{11}^{II}, in a manner also shown in FIGURE 4*b*. These two windings are connected with output inductance L_{11}. Accordingly windings $W_{21,5}^{I}$ and $W_{21,5}^{II}$ of cores W_{21}^{I} and W_{21}^{II} respectively of FIGURE 4*a* are connected in series with output inductance L_{21}. Thus, windings $W_{31,5}^{I}$ and $W_{31,5}^{II}$ are connected in series with output inductance L_{31}. All three series circuits are connected in parallel and they are all connected in series with an inductance L_1. The windings of the second and third row are connected correspondingly and have series inductances L_2 and L_3, respectively.

Thus, in every one of the three rows of a matrix, the series circuits of the output windings and the inductive output load of each of these circuits are connected in parallel and they are connected in series with a common inductance. L_1, L_2, L_3. The latter compensation inductances are designed in such a manner that, upon a current pulse therethrough, the voltage drop produced thereby equals the disturbance pulse produced in any one of the output windings of any row when the cores, as described above, are initially half-way excited.

The examples shown in FIGURES 4*a*, 4*b* and 5 illustrate that the switch core matrix in accordance with the present invention provides for a theoretically complete cancellation of noise pulses. Even though in practice one can reduce the noise currents to a fraction of their signal magnitude, the invention provides for a considerable improvement along the same line as the possible reduction of all the core columns, as outlined above.

I claim:

1. In a switch core matrix having intersecting column and row conductors and having a core circuit at each intersection of a column and a row, said core circuits each comprising a pair of permeable cores each having a substantially rectangular hysteresis loop, an output winding on each core of the pair and connected in series with means for producing first a positive and thereafter a negative pulse in a predominantly inductive load connected thereacross; first and second exciter windings on each core of the pair, one of the windings on each core being excited by a column conductor and the other winding on each core being excited by a row conductor; bias winding means on each core normally biasing the cores of each pair to saturation in opposition to the exciter direction of both associated exciter windings, and switch means to selectively excite one row conductor and one column conductor in the matrix.

2. In a matrix core circuit as set forth in claim 1, one core of each pair having a different saturation flux than the other core.

3. In a core matrix as set forth in claim 1, said switch means comprising selector switches selecting the row conductor and the column conductor to be excited, and exciter switch means successively energizing one core to produce in the output winding a pulse of one polarity and then energizing the other core of the pair to produce in its output winding a pulse of the opposite polarity.

4. A core circuit to be inserted at each column and row conductor intersection in a switch core matrix, comprising a first and a second core each having a substantially rectangular hysteresis loop, bias winding means to pre-magnetize said first and said second cores, first exciter winding means connected to a column conductor to selectively magnetize said first and said second cores in opposition to said pre-magnetization, second exciter winding means connected to a row conductor to selectively magnetize said first core in opposition to said pre-magnetization and said second core in opposition to the magnetization caused by said first exciter winding means, third exciter winding means actuated in positive relationship with and immediately after operation of said second exciter winding means and adapted to magnetize said first core in opposition to said magnetization caused by said first exciter winding means and to magnetize said second core in opposition to said pre-magnetization, an inductive load, first output winding means adapted to derive an output from said first core, and second output winding means connected in series with said first output winding means through sad load and adapted to derive an output from said second core, said output windings producing successive positive and negative pulses in said inductive load.

5. A switch core matrix including at each column and row intersection a core circuit as set forth in claim 4, and the output winding and load circuits of each core circuit in one conductor being connected mutually in parallel; and the parallelly connected circuits being connected in series wtih a common load inductance, the common load inductance being so proportioned that the voltage drop caused by a current pulse in one of the output circuits cancels the noise pulses from the other output circuit associated with the same selected conductor.

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