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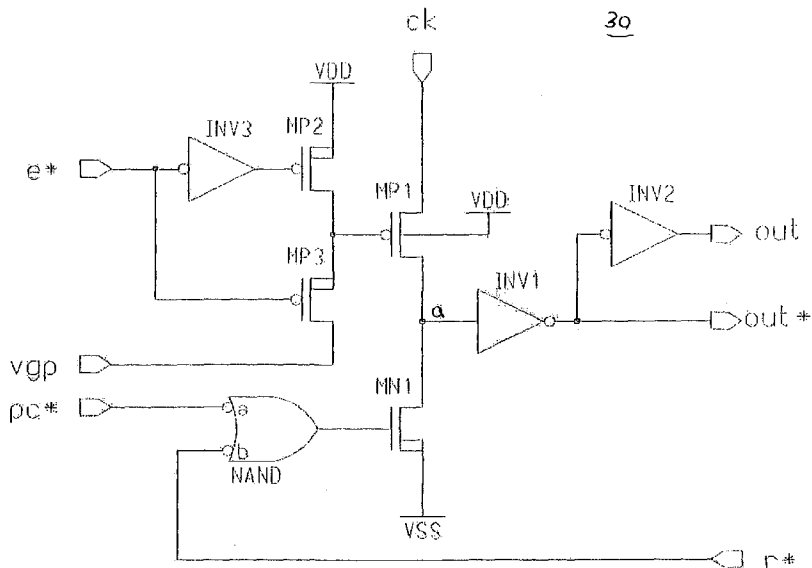
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(57) Abstract: A high voltage shift register stage which directly accepts low voltage clock signal inputs without using clock buffers. In particular, a shift register stage circuit is adapted to operate with a low voltage swing clock signal, with the stage circuit having a single state node, a, driven directly. This arrangement allows for reduced power consumption and higher operating speeds.

WO 2008/063477 A3

INTERNATIONAL SEARCH REPORT

International application No.
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<p>A. CLASSIFICATION OF SUBJECT MATTER IPC(8) - G09G 3/36 (2008.04) USPC - 345/100 According to International Patent Classification (IPC) or to both national classification and IPC</p>																				
<p>B. FIELDS SEARCHED</p> <p>Minimum documentation searched (classification system followed by classification symbols) IPC(8) - G09G 3/36 (2008.04) USPC - 345/100</p> <p>Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched</p> <p>Electronic data base consulted during the international search (name of data base and, where practicable, search terms used) PatBase.com, Google Patents</p>																				
<p>C. DOCUMENTS CONSIDERED TO BE RELEVANT</p> <table border="1"> <thead> <tr> <th>Category*</th> <th>Citation of document, with indication, where appropriate, of the relevant passages</th> <th>Relevant to claim No.</th> </tr> </thead> <tbody> <tr> <td>Y</td> <td>Applicant's Admitted Prior Art, Page 2 and 3; figure 2</td> <td>1-12</td> </tr> <tr> <td>Y</td> <td>US 6,934,210 B2 (AKIBA et al) 23 August 2005 (23.08.2005) entire document</td> <td>1-12</td> </tr> <tr> <td>Y</td> <td>US 5,869,857 A (CHEN) 09 February 1999 (09.02.1999) entire document</td> <td>1-12</td> </tr> <tr> <td>Y</td> <td>US 5,479,370 A (FURUYAMA et al) 26 December 1995 (26.12.1995) entire document</td> <td>9, 12</td> </tr> <tr> <td>Y</td> <td>US 6,232,939 B1 (SAITO et al) 15 May 2001 (15.05.2001) entire document</td> <td>10-12</td> </tr> </tbody> </table>			Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.	Y	Applicant's Admitted Prior Art, Page 2 and 3; figure 2	1-12	Y	US 6,934,210 B2 (AKIBA et al) 23 August 2005 (23.08.2005) entire document	1-12	Y	US 5,869,857 A (CHEN) 09 February 1999 (09.02.1999) entire document	1-12	Y	US 5,479,370 A (FURUYAMA et al) 26 December 1995 (26.12.1995) entire document	9, 12	Y	US 6,232,939 B1 (SAITO et al) 15 May 2001 (15.05.2001) entire document	10-12
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<p>Name and mailing address of the ISA/US Mail Stop PCT, Attn: ISA/US, Commissioner for Patents P.O. Box 1450, Alexandria, Virginia 22313-1450 Facsimile No. 571-273-3201</p>		<p>Authorized officer: Blaine R. Copenheaver PCT Helpdesk: 571-272-4300 PCT OSP: 571-272-7774</p>																		