



(51) International Patent Classification:

C23C 18/16 (2006.01) H05K 1/09 (2006.01)
C23C 18/38 (2006.01) H05K 1/11 (2006.01)
H05K 1/02 (2006.01) H05K 3/10 (2006.01)
H05K 1/03 (2006.01) H05K 3/18 (2006.01)

(21) International Application Number:

PCT/US2019/066990

(22) International Filing Date:

17 December 2019 (17.12.2019)

(25) Filing Language:

English

(26) Publication Language:

English

(30) Priority Data:

16/237,702 01 January 2019 (01.01.2019) US

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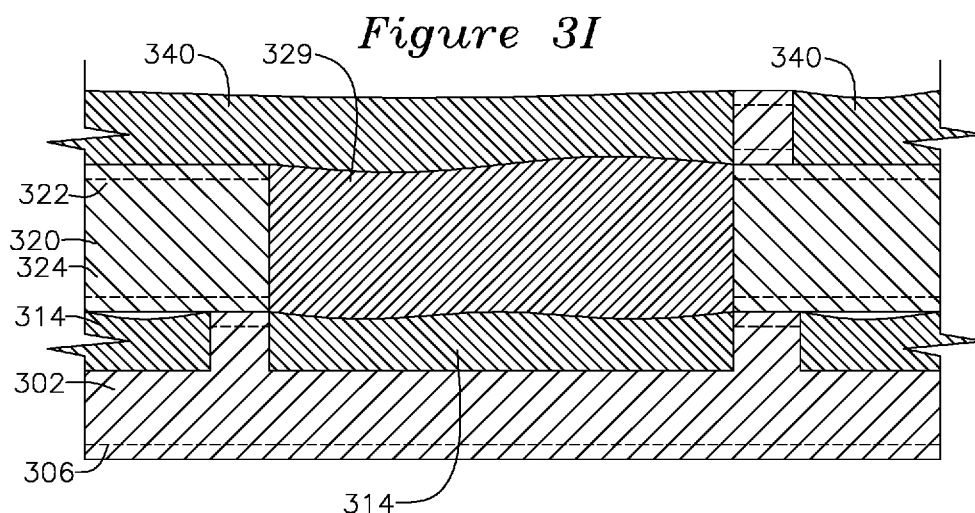
(81) Designated States (unless otherwise indicated, for every kind of national protection available): AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BN, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DJ, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IR, IS, JO, JP, KE, KG, KH, KN, KP, KR, KW, KZ, LA, LC, LK, LR, LS, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PA, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SA, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(84) Designated States (unless otherwise indicated, for every kind of regional protection available): ARIPO (BW, GH, GM, KE, LR, LS, MW, MZ, NA, RW, SD, SL, ST, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, KM, ML, MR, NE, SN, TD, TG).

Published:

— with international search report (Art. 21(3))

(54) Title: MULTI-LAYER CIRCUIT BOARD WITH TRACES THICKER THAN A CIRCUIT BOARD LAYER



(57) Abstract: A multi-layer circuit board is formed multiple layers of a catalytic layer, each catalytic layer having an exclusion depth below a surface, where the catalytic particles are of sufficient density to provide electroless deposition in channels formed in the surface. A first catalytic layer has channels formed which are plated with electroless copper. Each subsequent catalytic layer is bonded or laminated to an underlying catalytic layer, a channel is formed which extends through the catalytic layer to an underlying electroless copper trace, and electroless copper is deposited into the channel to electrically connect with the underlying electroless copper trace. In this manner, traces may be formed which have a thickness greater than the thickness of a single catalytic layer.



Multi-layer Circuit Board with Traces Thicker than a
Circuit Board Layer

[0001] Field of the Invention

[0002] The present invention relates to a multi-layer printed circuit board formed with at least two catalytic layers and having traces having a depth formed continuously across at least two catalytic layers using electroless deposition in channels formed in adjacent catalytic layers to form traces with dimensional thickness spanning more than one catalytic layer.

[0003] Background of the Invention

[0004] Prior art printed circuit boards (PCB) are formed using a subtractive process by etching a sheet of copper laminated to a substrate using patterned resist to form conductive metal interconnects (known as "traces") on the dielectric substrate, where each surface carrying conductors is known as a "layer". Each dielectric core has traces formed on one surface or on both surfaces, and by stacking several such dielectric cores having traces formed on one or more surfaces, and interspersed with bare

1 dielectric layers, a multi-layer printed circuit may be
2 formed by laminating them together under temperature and
3 pressure. The dielectric substrate comprises an epoxy
4 resin embedded in a fiber matrix such as glass fiber woven
5 into a cloth. In one prior art fabrication method, copper
6 is laminated onto the outer surfaces of a dielectric layer,
7 the copper surfaces are patterned such as with a
8 photoresist or photo sensitive film to create masked and
9 unmasked regions, and then etched to form a conductive
10 trace layer on one or both sides of the core dielectric. A
11 stack of dielectric cores with conductive traces may then
12 be laminated together to form a multi-layer circuit board,
13 and any layer to layer trace interconnects made with vias,
14 which are drilled holes plated with copper to form annular
15 rings which provide connectivity from one layer to another.

16 [0005] Printed circuit boards (PCB) are typically used
17 to provide conductive traces between various electronic
18 components mounted on the PCB. The dimension of a trace
19 which is parallel to the surface of the laminate is
20 considered a trace width, and the dimension of a trace
21 which is perpendicular to the surface of the laminate is
22 considered a trace thickness. One type of electronic
23 component is a through-hole device which is mounted on the
24 PCB by having leads positioned through one or more holes in

1 the PCB, where the PCB hole includes a conductive annular
2 ring pad on each trace connect layer, and the component
3 lead is soldered to the annular ring pad of the PCB hole.
4 Through hole components have leads which tend to be
5 difficult to align with the associated PCB mounting hole,
6 but surface mount technology (SMT) provides a preferable
7 mounting system, where component leads are simply placed on
8 the surface of a PCB pad or land and soldered, which is
9 preferred for PCB assembly because of the smaller size and
10 higher density of SMT components and ease of mechanized
11 assembly compared to through-hole components. Surface
12 mount components require only surface mount pads which
13 provide a surface soldering terminal on an outside finished
14 PCB layer. Within a two layer or multi-layer PCB,
15 interconnects of conductive traces from one layer to
16 another are accomplished using through-hole vias, where a
17 conductive trace on one trace layer leads to a hole which
18 is typically drilled through one or more dielectric layers
19 of the PCB and plated with copper or other conductive metal
20 to complete the trace layer connection. A hole drilled
21 through all dielectric layers is known as a thru-via, a
22 hole drilled through an outer layer only (typically as part
23 of the fabrication of the individual layer) is known as a
24 micro-via, and a hole drilled through one or more inner

1 layers is known as a blind via. For any of these via
2 types, the via is patterned to include an annular ring
3 conductor region on opposite trace layers of the PCB, with
4 the drilled hole lined with conductive material which
5 connects the annular ring conductors on either side of the
6 laminate or PCB.

7 [0006] The thickness of pre-patterned or post-
8 patterned copper on a printed circuit board laminate may be
9 increased using electroplating, where the PCB or dielectric
10 layer with traces is placed in an electrolytic bath, and a
11 DC source is connected between a sacrificial anodic
12 conductor electrode (such as a copper rod) to an electrode
13 clamped or attached to an existing conductive layer of a
14 PCB which forms the two electrodes across which a DC
15 current may be applied. Where a pre-existing conductive
16 copper layer is not present on a PCB to facilitate
17 electroplating, such as the case of bare dielectric
18 material or drilled via holes, a seed layer of copper must
19 first be deposited. This is done using an electroless
20 process with the assistance of a "seed" catalytic material
21 (which enhances the deposition of a particular conductive
22 material) which is deposited on the surface of the
23 dielectric, and the board is then placed in an electroless
24 bath. For a catalyst such as palladium and an electroless

1 bath of copper, the copper ions in solution deposit over
2 the palladium until the surface is covered sufficiently to
3 provide uniform electrical conductivity, after which the
4 copper deposited using the electroless process provides a
5 conductive scaffold for the subsequent addition of material
6 using the electroplating process. Electroplating is
7 preferred for finishing the plating operation, as it has a
8 faster deposition rate than the electroless plating
9 process.

10 [0007] As electronic assemblies increase in
11 complexity, it is desired to increase component densities
12 on PCB assemblies, such as by using smaller trace widths
13 (known as fine pitch traces) in conjunction with
14 increasingly dense integrated circuit (IC) lead patterns.
15 One problem of prior art surface mount PCB fabrication and
16 assembly methods is that because the traces are formed on
17 the surface of the dielectric, the adhesion between copper
18 trace and underlying laminate for narrower conductor line
19 widths (known as fine pitch traces) is reduced, causing the
20 fine pitch traces and component pads to separate (lift)
21 during a component replacement operation, ruining the
22 entire circuit board assembly and expensive components on
23 it. Another problem of fine pitch surface traces is that
24 when fabricating a multi-layer circuit board, the

1 individual trace layers are laminated together under
2 pressure in an elevated temperature environment. During
3 lamination, fine pitch traces tend to migrate laterally
4 across the surface of the dielectric. In high speed
5 circuit board layout and design, it is desired to maintain
6 a fixed impedance between traces, particularly for
7 differential pair (edge coupled) transmission lines. This
8 lateral migration of traces during lamination causes the
9 transmission line impedance of the finished PCB
10 differential pair to vary over the length of the trace,
11 which causes reflections and losses in the transmission
12 line compared to one with fixed impedance characteristics
13 resulting from constant spacing.

14 [0008] Where traces are formed using subtractive
15 processes such as etching a copper foil surface layer to
16 form traces, lower resistance traces can be formed using
17 electroplating to build up the thickness of the traces on
18 the outer surface to reduce the trace resistance, or by
19 widening the traces on the top surface to reduce the
20 current density in the trace. However, it becomes
21 difficult to electroplate more than 3oz of copper because
22 of bleeding of the copper to surrounding areas, and width
23 increase of the traces, limiting the thickness of the
24 copper which can be electroplated. Typically, the trace is

1 made wider during the design of the circuit board, which
2 consumes available real estate on the board, or the trace
3 is replicated onto lower trace layers to form parallel
4 traces on separate inner trace layers separated by
5 dielectric, where the inner layers are typically formed
6 from thinner base copper such as 1/2 oz copper (~0.5 mil
7 thick). Alternatively, traces may be formed in channels
8 using the applicant's additive process as described in U.S.
9 Patents 9,706,650, 9,380,700, 9,674,967, and 9,631,279. It
10 is similarly possible to extend the width of these additive
11 process traces formed in a channel to reduce trace
12 resistance, subject to the same limitation of increasing
13 the width of the trace to support greater current density.
14 It is desired to provide traces with lower resistance than
15 is provided by the prior art processes, and without
16 increasing the width of the trace.

17
18 [0009] Objects of the Invention

19 [0010] A first object of the invention is a circuit
20 board having a first catalytic layer formed from either a
21 catalytic laminate or catalytic adhesive, with a trace
22 having a width and depth, the trace formed in a channel
23 which is filled with a conductive metal using electroless

1 deposition, the first catalytic layer laminated to a second
2 catalytic layer formed from either a catalytic laminate or
3 catalytic adhesive, the second catalytic layer having a
4 channel formed through the thickness of the second
5 catalytic layer to the trace of the first catalytic layer,
6 the channel filled with a conductive metal such as from
7 electroless deposition to form a circuit board with an
8 elongated trace which has greater depth than the thickness
9 of a single layer of a circuit board and having an
10 elongated trace span, and with the electroless deposition
11 of the first catalytic layer in electrical contact with the
12 electroless deposition of the second catalytic layer.

13 [0011] A second object of the invention is a process
14 for forming a circuit board, the process comprising:

15 [0012] forming a channel having a width and a depth
16 into a first catalytic layer formed from either a catalytic
17 laminate or a catalytic adhesive;

18 [0013] electroless plating a conductive trace into the
19 first catalytic layer;

20 [0014] laminating a second catalytic layer formed from
21 either a catalytic laminate or a catalytic adhesive to the
22 first catalytic layer;

[0015] forming a channel having a width and a depth into the second catalytic layer, the channel depth reaching the conductive trace of the first catalytic layer;

[0016] electroless plating a conductive trace into the second catalytic layer which is in electrical contact with the conductive trace of the first catalytic layer.

[0017] A third object of the invention is a multi-layer circuit board having at least one trace formed in a first catalytic layer formed from either a catalytic laminate or catalytic adhesive, the first catalytic layer having a channel which is filled with an electroless deposition of a conductive metal, the first catalytic layer adjacent to subsequent adjacent catalytic layers, each adjacent catalytic layer formed from a catalytic adhesive or catalytic laminate and bonded or laminated to a previous catalytic layer and having a channel formed and deposited with electroless metal into the channel, the metal deposition extending into the electroless metal deposition of the previous adjacent layer, thereby forming a homogeneous trace with a trace depth which spans at least two catalytic layers.

[0018] Summary of the Invention

1 [0019] In a first embodiment of the invention, a first
2 catalytic layer formed from either a catalytic laminate or
3 a catalytic adhesive has catalytic particles an exclusion
4 depth below at least one surface of the catalytic layer,
5 the catalytic layer having channels formed into at least
6 one surface of the catalytic layer which have a depth of at
7 least the exclusion depth, the channels thereby exposing
8 catalytic particles. The channels of the first catalytic
9 layer are exposed to electroless plating of a conductive
10 metal such as copper for a duration of time sufficient for
11 a deposition of metal with a thickness from the bottom of
12 the channel to a depth near the surface of the first
13 catalytic layer. The first catalytic layer is bonded or
14 laminated to a second catalytic layer and at least one
15 channel is formed into the second catalytic layer which
16 extends through the thickness of the second catalytic layer
17 and to the deposition of metal on the first catalytic
18 layer, after which the second catalytic layer channel is
19 electroless plated over a depth from the metal deposition
20 of the first catalytic layer to the surface of the second
21 catalytic layer, thereby forming a trace which has greater
22 depth than a single catalytic layer. Additional catalytic
23 layers may be bonded or laminated to previous catalytic
24 layers, the additional catalytic layers each having full

1 depth channels formed to the underlying metal deposition of
2 an adjacent catalytic layer, with the electroless
3 deposition plated to form traces having a trace depth which
4 spans each additional catalytic layer to form traces with a
5 depth which spans the several catalytic layers, each
6 catalytic layer providing a full depth channel.

7 [0020] In a second embodiment of the invention,
8 catalytic layers are formed as either catalytic laminates
9 or catalytic adhesives. Catalytic laminates are formed by
10 curing a mixture of a resin, catalytic particles, and a
11 fiber mesh, the catalytic particles an exclusion depth
12 below the surface of the catalytic laminate. Catalytic
13 adhesives are formed as a mixture of resin and catalytic
14 particles which are cured onto an underlying surface, the
15 surface of the cured catalytic adhesive having catalytic
16 particles an exclusion depth below the surface of the cured
17 catalytic adhesive. In this embodiment, traces are formed
18 having a depth of a plurality of catalytic layers, where a
19 first catalytic layer has a channel formed, and the channel
20 deposited with a metal using electroless plating to
21 substantially fill the channel to a surface layer. The
22 first catalytic layer is then bonded or laminated to one or
23 more subsequent catalytic layers, each subsequent catalytic
24 layer having a channel formed through the catalytic layer

1 to the level of the first catalytic layer electroless
2 plated metal, after which electroless copper is deposited
3 in the channel to the surface of each subsequent layer,
4 thereby providing traces continuous in depth over multiple
5 catalytic layers, the resulting trace having a thickness
6 greater than the thickness of a single catalytic layer, and
7 spanning the depth of the multiple catalytic layers which
8 form the trace. The lamination of a subsequent catalytic
9 laminate to an underlying catalytic laminate layer with a
10 formed channel may be performed with an electroless
11 deposition after each lamination and channel forming step,
12 or the channel may be formed through multiple catalytic
13 laminate layers and electroless plated in a single step.
14 In one example of the invention, the step of performing a
15 sequential lamination of a catalytic laminate, forming a
16 channel in the catalytic laminate after each lamination,
17 and electroless plating each channel, are done in a
18 repeating sequence until the desired trace depth is formed.

19 [0021] In a third embodiment of the invention, a
20 process for forming traces in a catalytic layer formed from
21 either catalytic laminate or a catalytic adhesive has at
22 least one trace sequentially formed in a channel, the
23 resultant trace having a thickness greater than the depth
24 of a single catalytic layer, where the process comprises:

1 [0022] forming channels in one or more surfaces of a
2 first catalytic layer to below the exclusion depth, thereby
3 revealing catalytic particles;

4 [0023] electroless plating the channels with an
5 electrically conductive metal to approximately the depth of
6 the channel;

7 [0024] laminating or bonding one or more additional
8 catalytic layers to the first catalytic layer;

9 [0025] forming a channel having a width and depth
10 which extends through the thickness of the additional
11 catalytic layer to the electroless metal deposition of the
12 previous catalytic layer;

13 [0026] performing electroless deposition of conductive
14 metal in the channel of each additional catalytic layer
15 which is in electrical contact with the previously
16 deposited electroless plating of an adjacent catalytic
17 layer.

18
19 [0027] Brief Description of the Drawings

20 [0028] Figure 1 shows a cross section and
21 corresponding plot of catalytic particle distribution in a
22 catalytic layer with respect to the section view of the
23 catalytic layer.

1 [0029] Figure 2A shows a schematic diagram of a
2 switching power supply circuit with pulsatile current flow
3 in certain components.

4 [0030] Figure 2B shows waveform plots for the
5 switching power supply circuit of figure 2A.

6 [0031] Figure 2C shows a plan view of a printed
7 circuit board layout for a section of the power supply
8 circuit of figure 2A.

9 [0032] Figure 3A shows a section view of a catalytic
10 pre-preg laminate layer.

11 [0033] Figure 3B shows figure 3A after formation of
12 channels in a surface layer.

13 [0034] Figure 3C shows figure 3B after deposition of
14 metal traces such as by electroless deposition.

15 [0035] Figure 3D shows figure 3C after bonding or
16 lamination of a second catalytic pre-preg layer to a
17 previous catalytic pre-preg layer.

18 [0036] Figure 3E shows figure 3D after forming a
19 channel with a depth through the thickness of pre-preg
20 which reaches the electroless deposition of the first layer
21 applied in figure 3C.

1 [0037] Figure 3F shows figure 3E after electroless
2 deposition of a metal which is in contact with the
3 electroless deposited trace of figure 3C.

4 [0038] Figure 3G shows an optional additional step of
5 adding a catalytic layer to the laminate of figure 3F.

6 [0039] Figure 3H shows figure 3G after forming a
7 channel to the catalytic layer added in figure 3G.

8 [0040] Figure 3I shows figure 3G after electroless
9 deposition of a metal which is in contact with the
10 electroless deposited trace of figures 3C and 3H.

11 [0041] Figure 4 shows the processing steps for forming
12 variable thickness trace layers using catalytic layers.

13
14 [0042] Detailed Description of the Invention

15 [0043] Figure 1 shows an example catalytic pre-preg
16 for use in one aspect of the current invention. The
17 catalytic pre-preg consists of a matrix of pre-impregnated
18 fibers bound in a resin containing catalytic particles.
19 Many different materials may be used for the fibers of pre-
20 preg, including woven glass-fiber cloth, carbon-fiber, or
21 other fibers, and a variety of different materials may be
22 used for the resin, including epoxy resin, polyimide resin,

1 cyanate ester resin, PTFE (Teflon) blend resin, or other
2 resins. One aspect of the invention is a printed circuit
3 board laminate capable of supporting fine pitch conductive
4 traces on the order of 1 mil (25u), and while the
5 description is drawn to the formation of copper traces
6 using catalysts for electroless copper formation, it is
7 understood that the scope of the invention may be extended
8 to other metals suitable for electroless plating and
9 electro-plating. For electroless deposition of copper (Cu)
10 channels, elemental palladium (Pd) is preferred as the
11 catalyst, although selected periodic table transition metal
12 elements, such as group 9 to 11 platinum (Pt), rhodium
13 (Rh), iridium (Ir), nickel (Ni), gold (Au), silver (Ag),
14 cobalt (Co), or copper (Cu), or other compounds of these,
15 including other metals such as iron (Fe), manganese (Mn),
16 chromium (Cr), molybdenum (Mo), tungsten (W), titanium
17 (Ti), tin (Sn), or mixtures or salts of the above, any of
18 which may be used as catalytic particles. The present
19 candidate list is intended to be exemplar rather than
20 comprehensive, it is known in the art that other catalysts
21 for attracting copper ions may also be used. In one
22 example of the invention, the catalytic particles are
23 homogeneous catalytic particles. In another example of the
24 invention, the catalytic particles are inorganic particles

1 or high temperature resistant plastic particles which are
2 coated with a few angstrom thickness of catalytic metal,
3 thereby forming heterogeneous catalytic particles having a
4 thin catalytic outer surface encapsulating a non-catalytic
5 inner particle. This formulation may be desirable for
6 larger catalytic particles, such as those on the order of
7 25u in longest dimension. The heterogeneous catalytic
8 particle of this formulation can comprise an inorganic,
9 organic, or inert filler such as silicon dioxide (SiO₂), an
10 inorganic clay such as Kaolin, or a high temperature
11 plastic filler coated on the surface with a catalyst such
12 as palladium adsorbed onto the surface of the filler, such
13 as by vapor deposition or chemical deposition. Only a few
14 atomic layers of catalyst are required for the catalytic
15 particle to have desirable properties conducive to
16 electroless plating.

17 [0044] In another example of a catalytic layer formed
18 using a catalytic adhesive, the catalytic adhesive
19 formulation is the same as for the catalytic laminate
20 except that no fiber is introduced into the resin and
21 catalytic particle mixture and the resin and catalytic
22 particle mixture is applied to an underlying surface and
23 cured such that catalytic particles are an exclusion depth
24 below the surface of the cured catalytic adhesive, as was

1 the case with the catalytic particle distribution of the
2 catalytic laminate layer, thereby enabling electroless
3 plating only in channels which are formed which extend
4 below the exclusion depth for catalytic particles.

5 [0045] In one example of forming heterogeneous
6 catalytic particles, a bath of fillers (organic or
7 inorganic) is sorted by size to include particles less than
8 25u in size, these sorted inorganic particles are mixed
9 into an aqueous bath in a tank, agitated, and then a
10 palladium salt such as PdCl (or any other catalyst such as
11 a salt of silver or other catalyst) is introduced with an
12 acid such as HCl, and with a reducing agent such as
13 hydrazine hydrate, the mixture thereby reducing metallic Pd
14 which coats the inorganic particles provide a few angstroms
15 of thickness of Pd coated on the filler, thereby creating a
16 heterogeneous catalytic particle which has the catalytic
17 property of a homogeneous Pd particle with a greatly
18 reduced volume requirement of Pd compared to using
19 homogeneous Pd metallic particles. For extremely small
20 catalytic particles on the order of a few nm, however,
21 homogeneous catalytic particles (such as pure Pd) may be
22 preferred.

[0046] Example inorganic fillers include clay minerals such as hydrous aluminum phyllosilicates, which may contain variable amounts of iron, magnesium, alkali metals, alkaline earths, and other cations. This family of example inorganic fillers includes silicon dioxide, aluminum silicate, kaolinite ($\text{Al}_2\text{Si}_2\text{O}_5(\text{OH})_4$), polysilicate, or other clay minerals which belong to the kaolin or china clay family. Example organic fillers include PTFE (Teflon) and other polymers with high temperature resistance.

[0047] Examples of palladium salts are: BrPd , Cl_2Pd , $\text{Pd}(\text{CN})_2$, I_2Pd , $\text{Pd}(\text{NO}_3)_2 \cdot 2\text{H}_2\text{O}$, $\text{Pd}(\text{NO}_3)_2$, PdSO_4 , $\text{Pd}(\text{NH}_3)_4\text{Br}_2$, $\text{Pd}(\text{NH}_3)_4\text{Cl}_2\text{H}_2\text{O}$. The catalytic powder of the present invention may also contain a mixture of heterogeneous catalytic particles (for example, catalytic materials coated over inorganic filler particles), homogeneous catalytic particles (such as elemental palladium), as well as non-catalytic particles (selected from the family of inorganic fillers).

[0048] Among the catalysts, palladium is a preferred catalyst because of comparative economy, availability, and mechanical properties, but other catalysts may be used.

[0049] In one method of forming catalytic laminates, a woven glass fiber is fed through a set of rollers infused

1 the fabric with epoxy resin blended with catalytic
2 particles and mixed with a volatile liquid to reduce the
3 viscosity, thereby forming an A-stage (liquid) pre-preg.

4 [0050] The resin may be a polyimide resin, a blend of
5 epoxy and cyanide ester (which provides curing at elevated
6 temperatures), or any other suitable resin formulation with
7 selectable viscosity during coating and thermosetting
8 properties after cooling. Fire retardants may be added,
9 for example to comply with a flammability standard, or to
10 be compatible with one of the standard FR series of pre-
11 preg such as FR-4 or FR-10. An additional requirement for
12 high speed electrical circuits is dielectric constant ϵ
13 (permittivity), which is often approximately 4 and governs
14 the characteristic impedance of a transmission line formed
15 on the dielectric, and loss tangent δ , which is measure of
16 frequency-dependent energy absorption over a distance,
17 whereby the loss tangent is a measure of how the dielectric
18 interacts with high frequency electric fields to
19 undesirably reduce signal amplitude by a calculable amount
20 of dB per cm of transmission line length. The resin is
21 blended with catalytic particles which have been sorted for
22 size. In one example formulation, the catalytic particles
23 include at least one of: homogeneous catalytic particles

1 (metallic palladium), or heterogeneous catalytic particles
2 (palladium coated over an inorganic particle or high
3 temperature plastic), and for either formulation, the
4 catalytic particles preferably having a maximum extent of
5 less than 25u and with 50% of the particles by count sized
6 between 12u and 25u, or the range 1-25u, or smaller. These
7 are example catalytic particle size embodiments not
8 intended to limit the scope of the invention. In one
9 example embodiment, the catalytic particles (either
10 homogeneous or heterogeneous) are in the size range 1u-25u.
11 In another example of the invention, homogeneous catalytic
12 particles are formed by grinding metallic palladium into
13 particles and passing the resultant particles through a
14 sieve with a mesh having 25u rectangular openings. In
15 another example, the catalytic resin mixture is formed by
16 blending homogeneous or heterogeneous catalytic particles
17 into the pre-preg resin by a ratio of weights, such as the
18 ratio of substantially 12% catalytic particles by weight to
19 the weight of resin. The ratio by weight of catalytic
20 particles in the resin mixture may alternatively be in the
21 range of 8-16% of catalytic particle weight to the total
22 weight of resin. It is understood that other blending
23 ratios may also be used, and it may be preferable to use
24 smaller particles. In one example of the invention, the

1 catalytic particle density is chosen to provide a mean
2 distance between catalytic particles on the order of 3u-5u.

3 [0051] In one example of the invention, to create the
4 resin rich surface which excludes catalytic particles, the
5 pre-preg sheets positioned near the outer surfaces (which
6 will later have the surface removed to expose the
7 underlying catalytic particles) are selected to have
8 greater than 65% resin, such as Glass 106 (71% resin),
9 Glass 1067, or Glass 1035 (65% resin), and the inner pre-
10 preg sheets (which are not subject to surface removal) are
11 selected to have less than 65% resin. Additionally, to
12 reduce the likelihood of fiberglass being present near the
13 surface of the catalytic pre-preg, a woven fiberglass may
14 be used with the inner pre-preg layers and a flat unwoven
15 fiberglass may be used in the outer resin rich pre-preg
16 layers. The combination of resin-rich pre-preg and flat
17 unwoven fiberglass on the outer surface layer results in an
18 exclusion zone of .7 mil (17u) to .9 mil (23u) between an
19 outer surface and the encapsulated fiberglass. Glass
20 styles 106, 1035, and 1067 are preferred for use on the
21 outer resin rich surface since the glass fiber thicknesses
22 are smaller (1.3-1.4 mil / 33-35u) than the glass fiber
23 thickness found in typical pre-preg sheets with greater
24 than 65% resin used in the central regions of the laminate,

1 such as glass style 2116, which has 3.7 mil (94u) fibers.
2 These values are given as examples, the smallest glass
3 fibers which are commercially available are expected to
4 continue to reduce in diameter. During processing of the
5 catalytic laminate for use with the present invention, a
6 temperature vs. time sequence is applied to cause the
7 catalytic particles and fiberglass to migrate away from the
8 outer surface of the laminate, repelled by the surface
9 tension of the epoxy during a liquid state of the gel point
10 temperature. After the cooling cycle, the cured C-stage
11 pre-preg sheets are offloaded. The process which forms the
12 cured C-stage pre-preg sheets may use single or multiple
13 sheets of fiber fabric to vary the finished thickness,
14 which may vary from 2 mil (51u) to 60 mil (1.5mm). A
15 complete description of the process for forming catalytic
16 laminates, catalytic adhesives, and resins may be found in
17 U.S. Patent 9,706,650 by the present inventors and commonly
18 assigned, which is incorporated by reference.

19 [0052] Figure 1 shows the resultant catalytic pre-preg
20 102 formed by the pre-preg process, where the catalytic
21 particles 114 are distributed uniformly within the central
22 region of pre-preg 102, but are not present below a
23 boundary region 108 below first surface 104, or below
24 boundary region 110 below second surface 106. This boundary

1 region 110 is a fundamental characteristic of the catalytic
2 particle exclusion zone common to both catalytic laminate
3 and catalytic adhesive catalytic layers. For the example
4 particle distribution of particles smaller than 25μ , the
5 catalytic particle boundary is typically $10-12\mu$ below the
6 surface (on the order of half of the length of a catalytic
7 particle), accordingly this depth or greater of surface
8 material must be removed for the embedded catalytic
9 particles to be available for electroless plating. The
10 region from surface 106 to catalytic particles at region
11 110 and from surface 104 to catalytic particles at region
12 108 are referred to as catalytic particle exclusion zones
13 in the present application. In one example of the
14 invention, the catalytic particle exclusion zone contains
15 an insufficient density of catalytic particles to enable
16 electroless plating without forming a channel below the
17 catalytic particle exclusion depth. In another example of
18 the invention, the density of catalytic particles in the
19 exclusion zone is less than $1/100$ of the catalytic particle
20 density in non-exclusion zone regions of the catalytic
21 laminate. In another example of the invention, the
22 exclusion zone regions are unable to form continuous
23 conductors through electroless plating in a given duration
24 of time, whereas the regions below the exclusion zone are

1 able to form continuous conductors in the same interval of
2 time.

3 [0053] Prior art catalytic laminates have activated
4 surfaces that must be masked to prevent unwanted
5 electroless plating on the activated surface of the
6 catalytic laminate. By contrast, the catalytic laminate
7 and catalytic adhesives of the present invention exclude
8 catalytic particles over the thickness extent from first
9 surface 104 to first boundary 108, and from second surface
10 106 to second boundary 110, providing the benefit that a
11 separate mask layer preventing contact with the catalytic
12 particles is not required for electroless plating as it is
13 in the prior art. Accordingly, removal of surface material
14 from either first surface 104 to the depth of boundary
15 layer 108 or deeper, or removal of surface material from
16 second surface 106 to second boundary 110, results in the
17 exposure of catalytic material which may be used for
18 electroless plating. It is also desirable for the process
19 which provides the resin rich surface to also exclude not
20 only catalyst, but the fiber fabric, as removal of the
21 surface layer in subsequent steps which results in the
22 exposure of fibers requires additional cleaning steps,
23 accordingly it is preferred that the surface removal be of
24 resin only, so as to expose only the underlying catalytic

1 particles. This is accomplished by using a combination of
2 resin-rich outer pre-preg layers and flat unwoven
3 fiberglass layers having smaller diameter fibers on the
4 outside layers. An additional advantage of forming traces
5 in channels using electroless plating is that the traces
6 are mechanically supported on three sides, which provides
7 greatly improved trace adhesion to the dielectric laminate.

8 [0054] Figure 2A shows a prior art buck regulator
9 circuit. When the switch 202 is closed, inductor charging
10 current flows from the power source 204 through energy
11 storage inductor 208 and to smoothing capacitor 218,
12 increasing the voltage in smoothing capacitor 218. When
13 switch 202 is open, inductor discharge current continues to
14 flow through inductor 208, through the path of diode 212
15 and capacitor 218. Steady state currents I3 and I4 drawn
16 by load 214 and 216, respectively, are significantly lower
17 than the peak pulsatile current I1 206 through switch 202
18 or peak pulsatile current I2 210 through inductor 208.

19 [0055] Figure 2B shows the current waveform plots 230
20 for I1 showing the switch opening and closing, Inductor
21 current I2 232, and steady state currents I3 234 and I4
22 236.

1 [0056] Figure 2C illustrates an example of the effect
2 on a prior art printed circuit board which is designed for
3 pulsatile vs steady state current flows. Inductor 208A
4 corresponds to 208 of figure 2A and capacitor 218A of
5 figure 2C corresponds to 218 of figure 2A. The trace 237A
6 (corresponding to thick line 237 of schematic of figure 2A)
7 carries peak pulsatile currents and so must be
8 comparatively wide to reduce I^2R losses associated with I_2 ,
9 whereas the width of the traces 214A and 216A carrying
10 steady state currents I_3 and I_4 (associated with
11 corresponding lines 214 and 216 of figure 2A) may be
12 significantly narrower. Further, it is typically the case
13 that small signal traces are excluded from power supply
14 areas during printed circuit design, to prevent coupling of
15 unwanted transient signals from the pulsatile current flows
16 into the small signal traces by magnetic induction or
17 electrostatic displacement currents through cross-coupling
18 of the traces.

19 [0057] For this reason, it is desired to provide
20 traces which can grow in thickness rather than width, and
21 which can utilize the thickness of two or more layers of a
22 multi-layer circuit board to form the conductive traces.

1 [0058] The sequence of figures 3A to 3I shows example
2 process steps for understanding the invention. Figure 3A
3 shows a cross section view of a catalytic laminate (or
4 catalytic adhesive) 302 with the catalytic particle
5 distribution plot of figure 1, where the catalytic
6 particles are distributed throughout the inner regions of
7 the catalytic layer (either a catalytic laminate or
8 catalytic adhesive), and the catalytic particles are below
9 the surface exclusion depth 306 and 304 of the associated
10 outer surfaces, thereby providing a density of catalytic
11 particles from 304 to 306 which is sufficient to provide
12 electroless deposition of conductive metal such as copper
13 in regions which extend below the surface catalytic
14 particle exclusion zone, and to exclude electroless
15 deposition at native surfaces 303 or 307.

16 [0059] Catalytic particles (not shown) in the region
17 between 304 and 306 may be in the size range of 25u and
18 smaller, in the present example they may be in the range
19 12u to 25u. The catalytic particles may include
20 heterogeneous catalytic particles (organic or inorganic
21 particles having a catalytic surface coating) or
22 homogeneous particles (catalytic metal particles), as
23 described previously. The exclusion boundary 304 is
24 approximately 25u below the first surface 303. The second

1 surface 307 and second surface exclusion boundary 306 on
2 the opposite surface are shown for reference, but it is
3 understood that the process may be used on one or both
4 sides of a candidate catalytic laminate or catalytic
5 adhesive.

6 [0060] Figure 3B shows the laminate of figure 3A with
7 a channel 310 formed by removal of the surface layer 303
8 below exclusion zone 304 in a region where a trace is
9 desired. The removal of surface material to form channels
10 in the catalytic laminate or catalytic adhesive 302 may be
11 by laser ablation, where the temperature of the catalytic
12 pre-preg is instantly elevated until the catalytic pre-preg
13 is vaporized, while leaving the surrounding catalytic pre-
14 preg structurally unchanged, leaving the catalytic
15 particles exposed. It may be preferable to use a laser
16 with a wavelength with a low reflectivity and high
17 absorption of this optical wavelength for the pre-preg
18 material being ablated, such as ultraviolet (UV)
19 wavelengths. Examples of such UV lasers are the UV excimer
20 laser or yttrium-aluminum-garnet (YAG) laser, which are
21 also good choices because of the narrow beam extent and
22 high available power which for forming channels of precise
23 mechanical depth and with well-defined sidewalls. An
24 example laser may remove material in a 0.9-1.1 mil (23u to

1 28u) diameter width with a depth governed by laser power
2 and speed of movement across the surface. Another surface
3 removal technique for forming channel 210 is plasma
4 etching, which may be done locally or by preparing the
5 surface with a patterned mask which excludes the plasma
6 from the surface layers 206 or 205, such as a dry film
7 photoresist or other mask material which has a low plasma
8 etch rate compared to the plasma etch rate of catalytic
9 pre-preg. The photoresist thickness is typically chosen
10 based on epoxy/photoresist etch selectivity (such that
11 plasma etch to the desired depth of removal of the cured
12 epoxy leaves sufficient photoresist at the end of the
13 etch), or in the case of photoresist which is used as an
14 electroplate mask, the thickness is chosen according to
15 desired deposition thickness. Typical dry film thickness
16 is in the range of 0.8-2.5 mil (20-64u). Plasmas suitable
17 for etching the resin rich surface include mixtures of
18 oxygen (O) and CF₄ plasmas, mixed with inert gasses such as
19 nitrogen (N), or argon (Ar) may be added as carrier gasses
20 for the reactive gases. A mask pattern may also be formed
21 with a dry film mask, metal mask, or any other type of mask
22 having apertures. Where a mechanical mask is used, the
23 etch resist may be applied using any of photolithography,
24 screen printing, stenciling, squeegee, or any method of

1 application of etch resist. Another method for removal of
2 the surface layer of catalytic pre-preg is mechanical
3 grinding, such as a linear or rotational cutting tool. In
4 this example, the catalytic pre-preg may be secured in a
5 vacuum plate chuck, and a rotating cutter (or fixed cutter
6 with movable vacuum plate) may travel a pattern defining
7 the traces such as defined by x,y coordinate pairs of a
8 Gerber format photofile. In another example of removing
9 surface material, a water cutting tool may be used, where a
10 water jet with abrasive particles entrained in the stream
11 may impinge on the surface, thereby removing material below
12 the first boundary 304. Any of these methods may be used
13 separately or in combination to remove surface material and
14 form channel 310 from catalytic pre-preg 302, preferably
15 with the channel extending below the first boundary 304.
16 Accordingly, the minimum channel depth is the depth
17 required to expose the underlying catalytic particles,
18 which is a characteristic of the cured pre-preg. As the
19 catalytic material is dispersed uniformly through the cured
20 pre-preg below the exclusion boundary 304, the maximum
21 channel depth may be limited by the depth of the woven
22 fiber (such as fiberglass) fabric, which tends to
23 complicate channel cleaning, as the fibers may break off
24 and re-deposit in channels intended for electroless

1 plating, or otherwise interfere with subsequent process
2 steps. Typical channel depths are 1 mil (25u) to 2 mil
3 (70u), but may extend deeper into the prepreg for reduced
4 electrical resistance after electroless deposition. The
5 final step after removing the surface material to form the
6 channel 310 is to clean away any particles of material
7 which were removed, which may be accomplished using
8 ultrasound cleaning, jets of water mixed with surfactant,
9 or any other cleaning means which does not result in
10 surface 304 material surrounding the channel from being
11 removed. Alternatively, the use of a catalytic adhesive,
12 which may be applied to the underlying catalytic layer and
13 cured, and contains no fabric, may be preferable for deep
14 channels extending through a single layer, as there are no
15 remaining fibers after ablation or channel formation to
16 interfere with subsequent deposition steps.

17 [0061] Figure 3C shows an electroless deposition 314
18 step, which is allowed to progress until the deposition
19 approximately reaches the upper surface 303, which allows
20 for application of a subsequent layer of catalytic layer
21 (which may be a catalytic laminate or catalytic adhesive)
22 320 shown in figure 3D. Catalytic layer 320 also has
23 associated surface catalytic particle exclusions depth 322
24 and 324, as did the catalytic layer 302 previously

1 described. The use of catalytic adhesive for catalytic
2 layer 320 is preferred to avoid interference between
3 unablated or remaining fibers in the channel after the
4 channels 326 are formed of figure 3E, which may interfere
5 with the subsequent electroless copper deposition 329 of
6 figure 3F. The subsequent layer of catalytic layer 320 may
7 be bonded or laminated to the adjacent catalytic layer 302
8 and electroless deposition 314 of figure 3D using vacuum
9 lamination or other process for layer bonding or lamination
10 known in PCB fabrication prior art.

11 [0062] Figure 3E shows the removal of catalytic layer
12 326 through the depth of catalytic layer 320 using the
13 previously described method from the surface 321 of
14 catalytic layer 320 through to the underlying electroless
15 deposition 314 of the first layer 302. The formation of the
16 channel 326 may be done using any known method for removing
17 laminate, although laser ablation is preferred.

18 [0063] Figure 3F shows electroless plating 329 of the
19 channel 326 from the deposition 314 below to the top level
20 321 of the catalytic layer 320. The resulting circuit
21 board now has a homogeneous trace with a trace thickness
22 which is greater than the thickness of a single catalytic
23 layer 320 or 302. The circuit board may be used in a

1 finished form of figure 3F in this manner after the
2 addition of components. High current trace segments, such
3 as trace segment 320 of figure 2C, may have its resistance
4 reduced using the current method, and additional layers may
5 be bonded or laminated to continue the process and increase
6 the depth of the trace segment, as shown in figure 3G where
7 catalytic layer 332 (where first exclusion surface 330 and
8 second exclusion surface 334 may be present, as before).

9 [0064] Figure 3H shows the subsequent step of forming
10 channel 336 in catalytic layer 332 of figure 3G. Figure 3I
11 shows a final step, where electroless deposition of metal
12 340 is in electrical contact with previous electroless
13 depositions 329 and 314, thereby providing a method for
14 forming a low resistance elongate conductor of selectable
15 thickness, which can be narrower than allowed by the prior
16 art for a given deposition metal resistivity (which
17 translates to resistance per inch for a given trace
18 thickness and width) of trace having a greater depth than
19 provided in the prior art. Although boundaries are shown
20 between trace deposition layers 314, 329, and 340 for
21 clarity in understanding the steps of the process and
22 resulting circuit, the electroless metal deposition is
23 homogeneous across layers, providing a low resistance trace

1 which spans the several dielectric layers and without the
2 boundaries shown in the figures.

3 [0065] Electroless plating for 329 of figure 3F and
4 314 of figure 3C may be performed several different ways.

5 One example electroless copper bath formulation uses a
6 mixture of Rochelle salt as the complexing agent, copper
7 sulfate as the copper metal source, formaldehyde as the
8 reducing agent, and sodium hydroxide as a reactant. In
9 this example, the tartrate (Rochelle salt) bath is
10 preferred for ease of waste treatment; the Rochelle salt
11 does not chelate as strongly as alternatives such as EDTA
12 or quadrol. In this example, the tartrate (Rochelle salt)
13 is the completing agent, copper sulfate is the metal
14 source, formaldehyde is the reducing agent, and sodium
15 hydroxide is a reactant. Other electroless plating
16 formulations are possible, this example is given for
17 reference. The electroless plating initially forms over
18 the surfaces of the exposed catalytic particles and
19 progresses until the deposition is below the native outer
20 surfaces of the catalytic layer.

21 [0066] A key advantage of electroless plating of
22 channels etched in catalytic material is that the
23 electroless plating progresses on all three sides at once,

1 compared to electroplating which only progresses from a
2 bottom (initially plated) layer.

3 [0067] Figure 4 shows a series of process steps for
4 using catalytic layers (catalytic adhesive or catalytic
5 laminate) to form circuit boards with trace layers having a
6 thickness greater than a single laminate layer thickness.
7 Apertures (if needed) are formed in step 402 such as for
8 interlayer vias (not shown but well known in the prior
9 art), followed by channels in step 404 such as channel 310
10 of figure 3B. Electroless plating is performed in step 406
11 corresponding to 314 of figure 3C, and a series of steps
12 408, 410, and 412 are iteratively performed as needed for
13 each layer of laminate/channel/electroless plate to extend
14 the thickness of the electroless deposition of step 406.
15 Step 408 corresponds to the bonded or laminated subsequent
16 layers 320 of step 3D and layer 332 to 302 of step 3G.
17 Step 410 corresponds to the formation of channels 326 of
18 figure 3E or 336 of figure 3H. Step 412 corresponds to the
19 electroless plating 329 of figure 3F or 340 of figure 3I.
20 The process of adding additional layers to further extend
21 the thickness of the traces may be performed by the path
22 414 following step 412 for each iteration.

1 [0068] The preceding description is only to provide
2 examples of the invention for understanding the underlying
3 mechanisms and structures used, and is not intended to
4 limit the scope of the invention to only the particular
5 methods or structures shown. For example, the sequences of
6 figures 3A to 3I show a single sided construction with the
7 trace channels formed over a plurality of catalytic layers
8 built above a first layer 302, whereas the first catalytic
9 layer 302 may have surface 307 subsequently ablated to the
10 level of electroless deposition 314 and additional layers
11 added to surface 307 in the opposite direction using
12 convention methods of multi-layer boards, or the method for
13 extending the trace thickness described above.

14 [0069] The trace structures of figures 3A to 3I are
15 shown in combination as they would normally occur on a PCB,
16 these examples are only for illustration, and are not
17 intended to limit the invention to these constructions. The
18 result of using the present invention for the example given
19 in figure 2A and 2C is that if trace 237A is .25" wide and
20 3 mil thick for a conventional subtractive circuit board
21 process, and the top and underlying catalytic layers 15 mil
22 thick (30 mil total) were used to form the trace described
23 in figures 3A to 3I, then trace 237 could be reduced from
24 250 mil to 25 mil width.

1 [0070] In the present specification, "approximately"
2 is understood to mean less than a factor of 4 greater or
3 smaller than a given nominal value, "substantially" is
4 understood to mean less than a factor of 2 greater or
5 smaller than a given nominal value. "Order of magnitude"
6 of a value includes the range from 0.1 times the nominal
7 value to 10 times the nominal value.

8 [0071] Certain post-processing operations are not
9 shown which are generic to printed circuit board
10 manufacturing and may be performed using prior art methods
11 on boards produced according to the novel process. Such
12 operations include tin plating for improved solder flow,
13 gold flash for improved conductivity and reduced corrosion,
14 soldermask operations, silkscreening information on the
15 board (part number, reference designators, etc.), scoring
16 the finished board or providing breakaway tabs, etc. The
17 circuit board formed using the current process has a planar
18 surface compared to the prior art of subtractive copper
19 etching which leaves an elevated trace on top of a lower
20 underlying substrate. Certain of these operations may
21 produce improved results when performed on the co-planar
22 trace and substrate surfaces of the present invention. For
23 example, silkscreened lettering over traces or vias
24 traditionally breaks up because of trace and via thickness

1 over the board surface, whereas these operations would
2 provide superior results on a planarized surface.

3

1 We claim:

2 1) A multi-layer circuit board comprising:

3 a first layer formed of catalytic layer having a
4 conductive trace formed by electroless deposition in a
5 channel in the first layer;

6 a second catalytic layer applied, bonded, or laminated
7 to the first layer, the second catalytic layer having a
8 channel formed through the thickness of the second
9 catalytic layer and extending in depth to the conductive
10 trace of the first catalytic layer;

11 the channel of the second catalytic layer filled with
12 a conductive metal by electroless deposition and in contact
13 with the electroless deposition of the first catalytic
14 layer.

15

16 2) The multi-layer circuit board of claim 1 where the
17 catalytic layer of the first or second layer is formed
18 using heterogeneous catalytic particles.

19

20 3) The multi-layer circuit board of claim 2 where the
21 heterogeneous catalytic particles are an inorganic material
22 coated with a catalyst.

23

1 4) The multi-layer circuit board of claim 1 where the
2 catalytic layer contains at least one of: (Pt), rhodium
3 (Rh), iridium (Ir), nickel (Ni), gold (Au), silver (Ag),
4 cobalt (Co), or copper (Cu), or compounds therein which may
5 include other metals such as iron (Fe), manganese (Mn),
6 chromium (Cr), molybdenum (Mo), tungsten (W), titanium
7 (Ti), tin (Sn), or mixtures or salts therein.

8
9 5) The multi-layer circuit board of claim 1 where the
10 catalytic layer contains palladium salts including at least
11 one of: BrPd, Cl_2Pd , $\text{Pd}(\text{CN})_2$, I_2Pd , $\text{Pd}(\text{NO}_3)_2 \cdot 2\text{H}_2\text{O}$, $\text{Pd}(\text{NO}_3)_2$,
12 PdSO_4 , $\text{Pd}(\text{NH}_3)_4\text{Br}_2$, $\text{Pd}(\text{NH}_3)_4\text{Cl}_2\text{H}_2\text{O}$.

13
14 6) The multi-layer circuit board of claim 1 where the
15 catalytic layer includes a resin containing at least one
16 of: polyimide resin, or blend of epoxy and cyanide ester.

17
18 7) The multi-layer circuit board of claim 1 where at
19 least one of the first catalytic layer or the second
20 catalytic layer is a catalytic adhesive or a catalytic
21 laminate.

1 8) A process for forming a circuit board, the process
2 comprising:

3 forming a channel having a width and a depth into a
4 first catalytic layer;

5 electroless plating a conductive trace into the first
6 catalytic layer to approximately the depth of the channel
7 of the first catalytic layer;

8 for at least one subsequent layer:

9 laminating a subsequent catalytic layer to a
10 previously applied layer;

11 forming a channel into the subsequent catalytic
12 layer to a depth which reaches the conductive trace of a
13 previous laminate layer;

14 electroless plating a conductive trace into the
15 subsequent catalytic layer, the electroless plating in
16 electrical contact with the conductive trace of a previous
17 catalytic layer.

18
19 9) The process of claim 8 where at least one catalytic
20 layer is formed using heterogeneous catalytic particles.

21
22 10) The process of claim 9 where the heterogeneous
23 catalytic particles are an inorganic material coated with a
24 catalyst.

1

2 11) The process of claim 8 where the electroless
3 deposition is copper.

4

5 12) The process of claim 8 where the heterogeneous
6 catalytic particles are an inorganic material coated with a
7 catalyst.

8

9 13) The process of claim 8 where the catalytic
10 particles are palladium with the majority of the particles
11 having a maximum dimension less than 25u

12

13 14) The process of claim 8 where at least one of the
14 first catalytic layer or a subsequent catalytic layer is a
15 catalytic adhesive or a catalytic laminate.

16

17 15) A multi-layer circuit board having at least one
18 trace formed in a channel which spans the thickness of more
19 than one layer and is contiguous with at least one other
20 trace formed into a channel on an adjacent layer.

21

22 16) The multi-layer circuit board of claim 15 where
23 the catalytic layer is formed using heterogeneous catalytic

1 particles, the majority of the particles smaller than
2 approximately 25u.

3
4 17) The multi-layer circuit board of claim 15 where
5 the catalytic layer contains at least one of: (Pt), rhodium
6 (Rh), iridium (Ir), nickel (Ni), gold (Au), silver (Ag),
7 cobalt (Co), or copper (Cu), or compounds therein which may
8 include other metals such as iron (Fe), manganese (Mn),
9 chromium (Cr), molybdenum (Mo), tungsten (W), titanium
10 (Ti), tin (Sn), or mixtures or salts therein.

11
12 18) The multi-layer circuit board of claim 15 where
13 the catalytic material contains heterogeneous catalytic
14 particles comprising an inorganic material coated with a
15 catalyst.

Figure 1

Catalytic Particle Distribution through Catalytic Layer

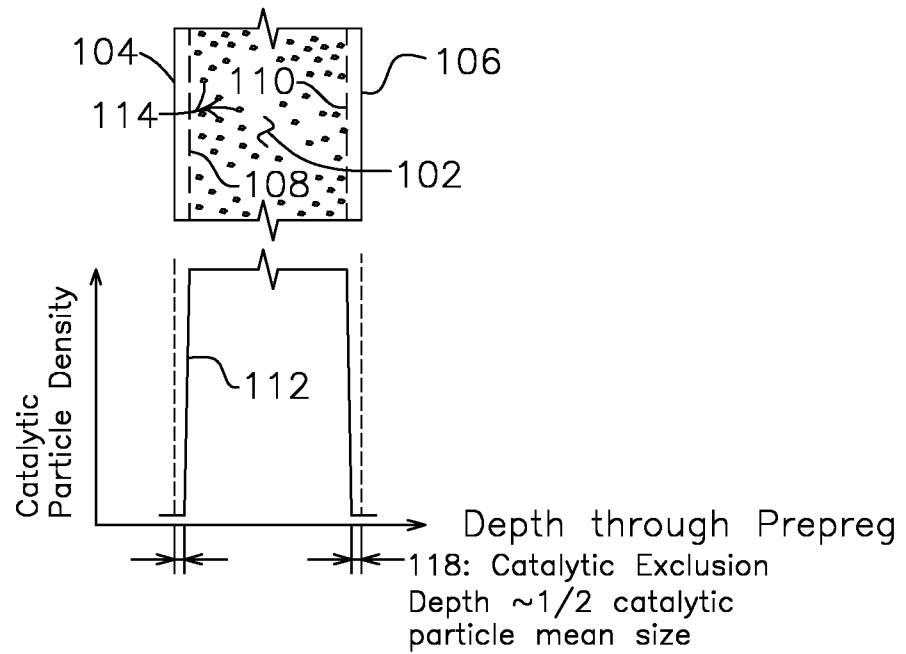


Figure 2A

Prior Art

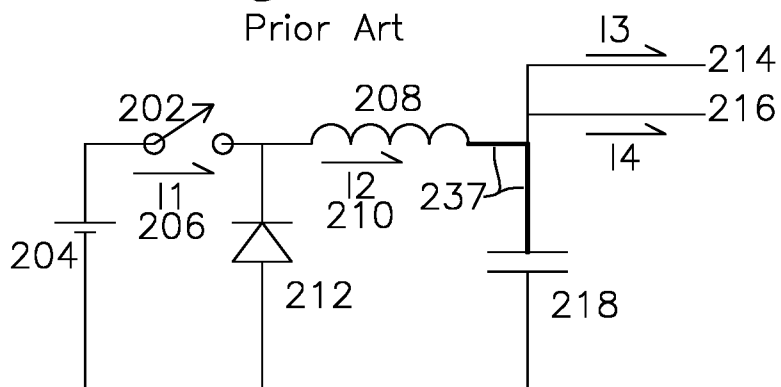


Figure 2B

Prior Art

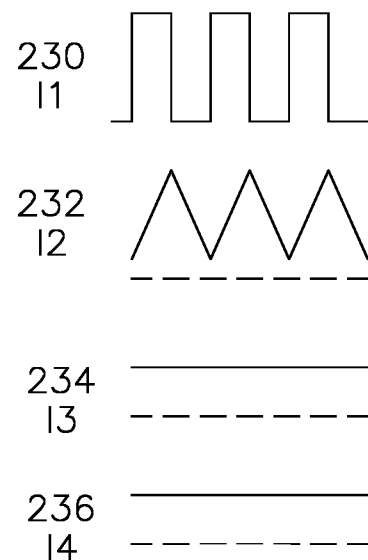


Figure 2C

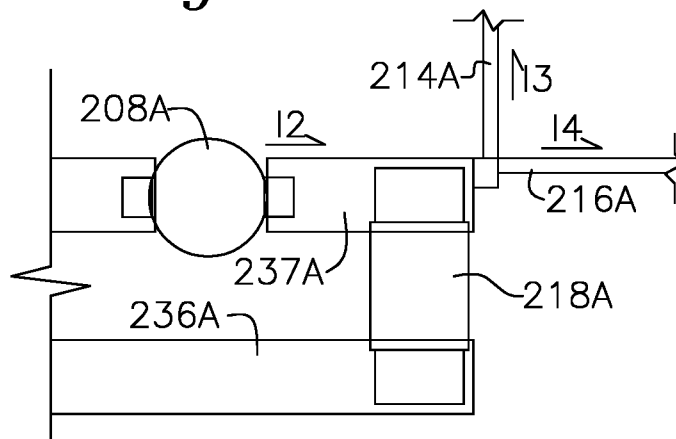


Figure 3A

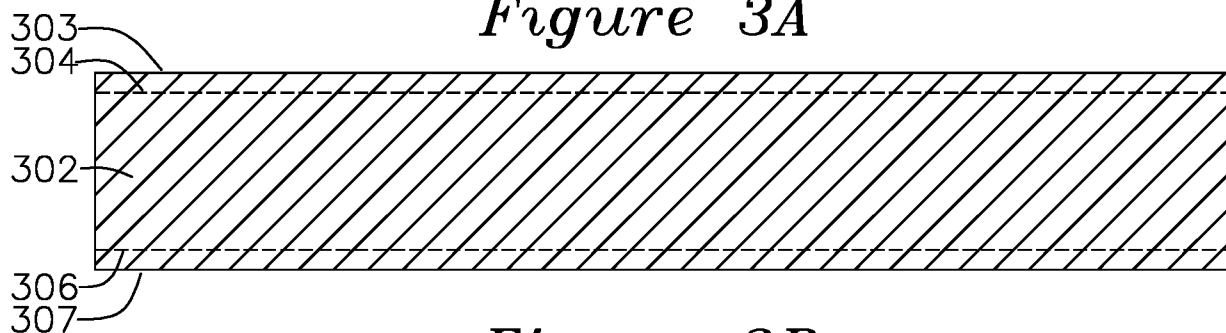


Figure 3B

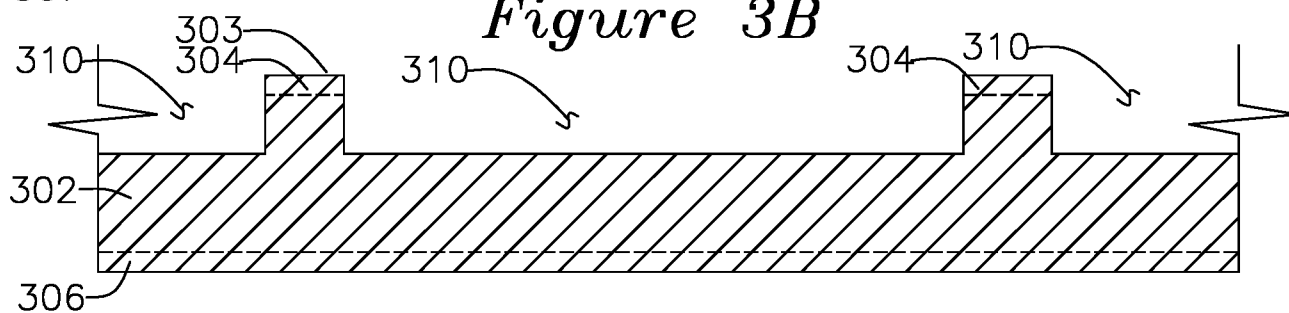


Figure 3C

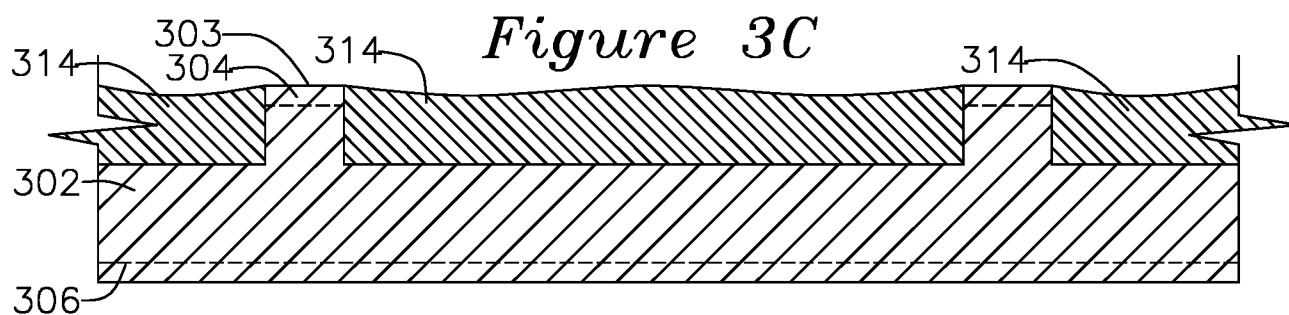


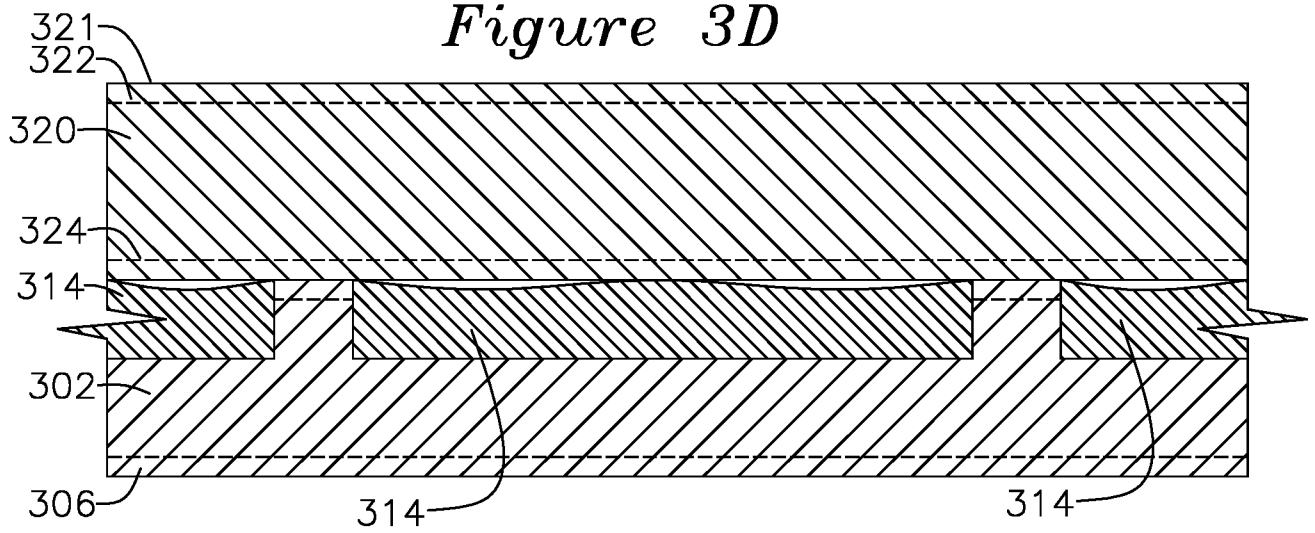
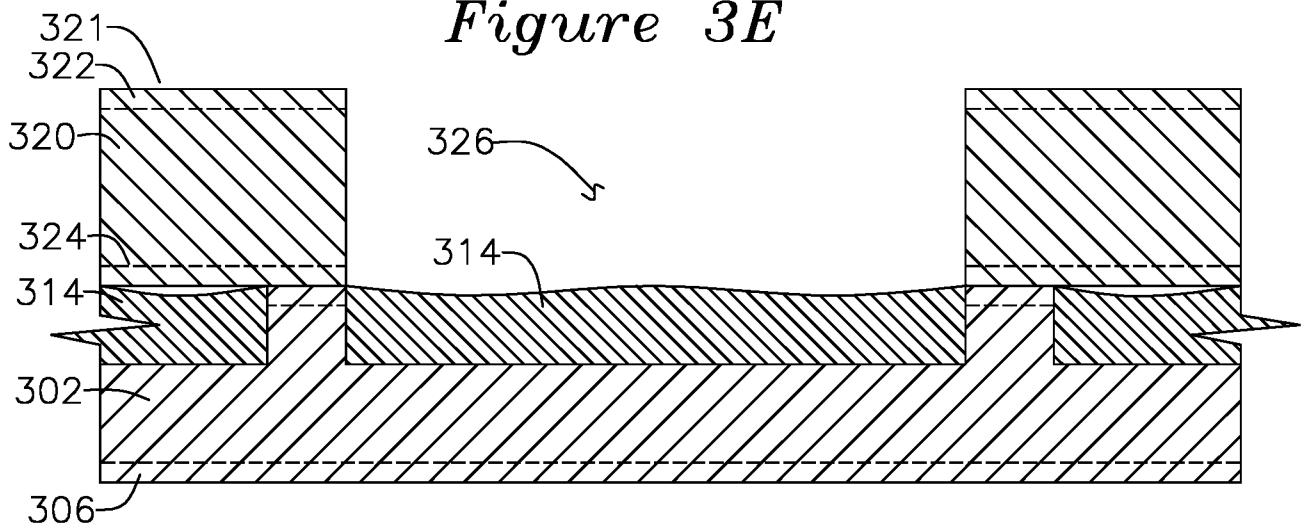
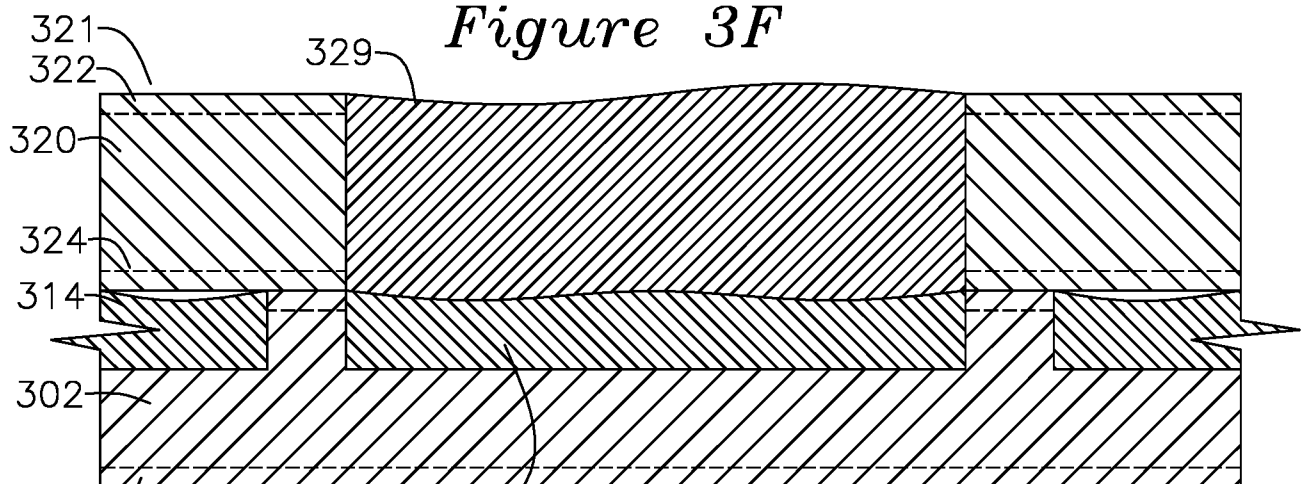
Figure 3D*Figure 3E**Figure 3F*

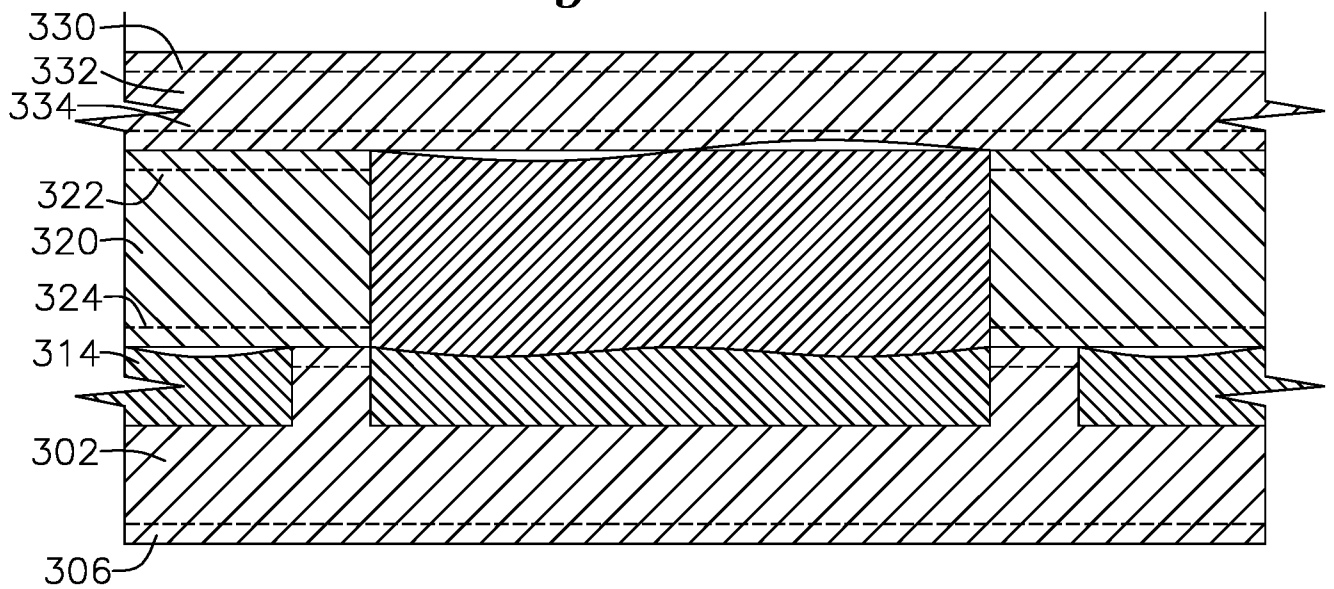
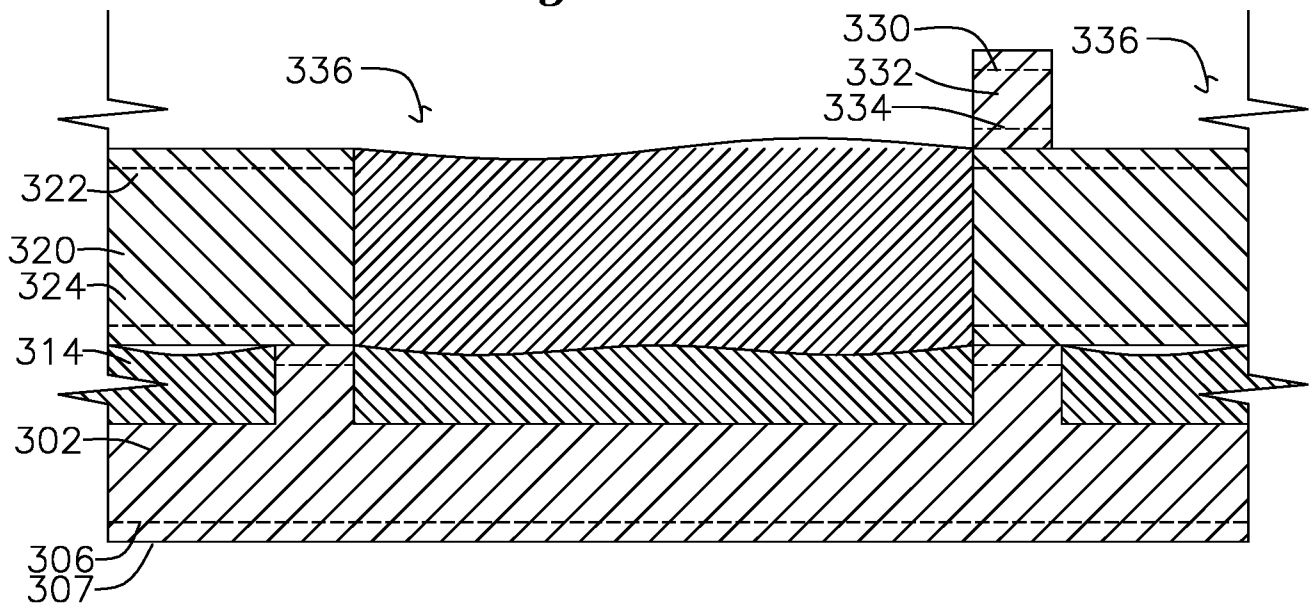
Figure 3G*Figure 3H*

Figure 3I

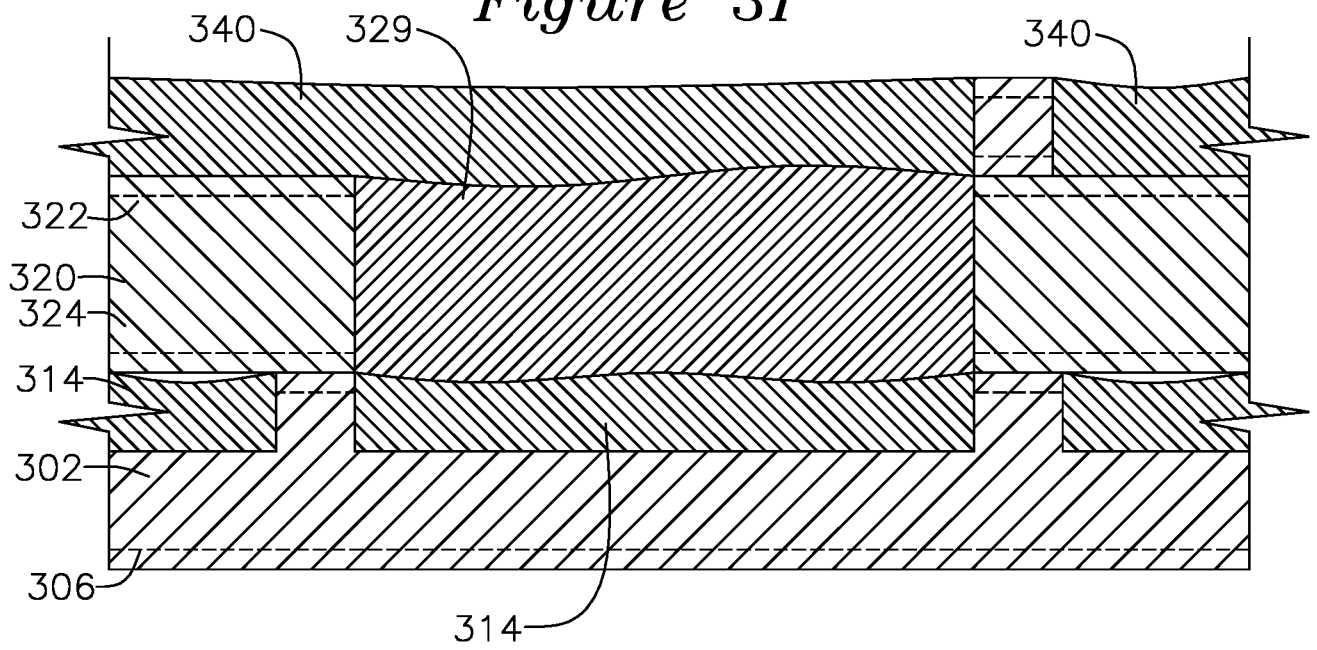
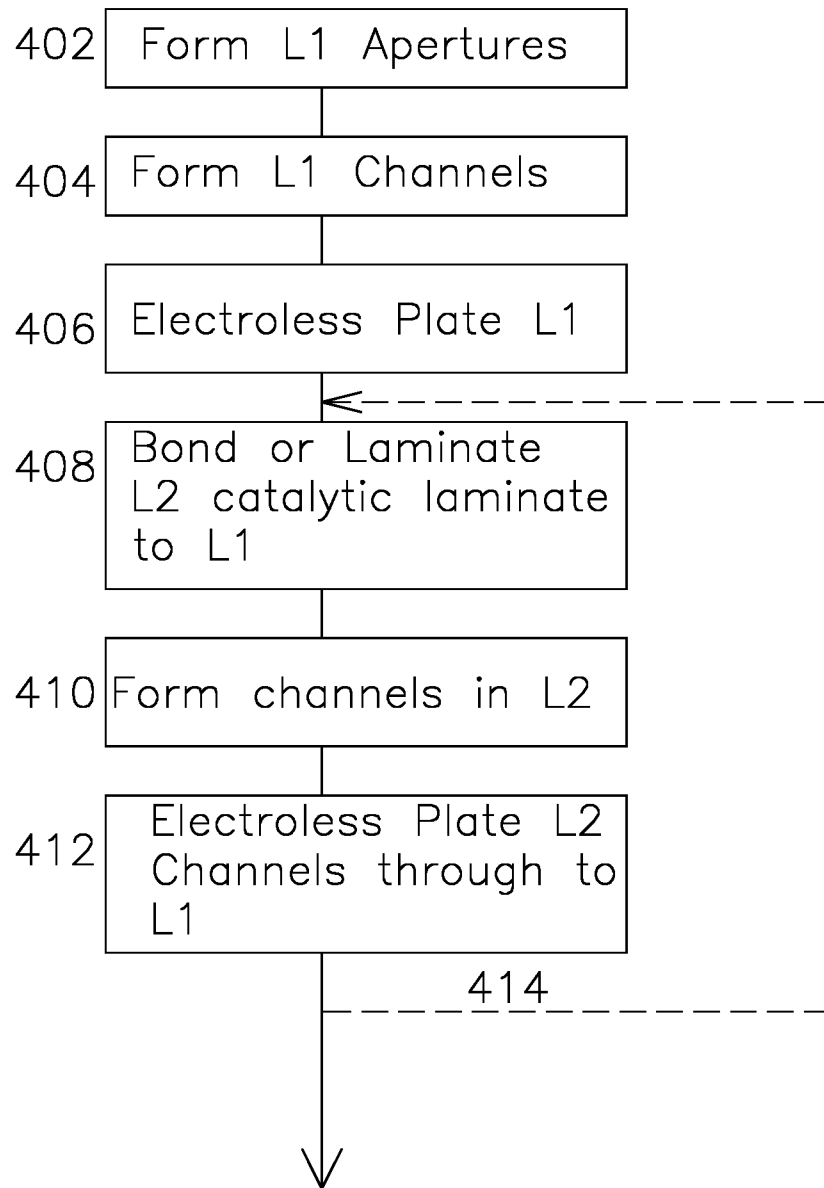


Figure 4
Multi-Layer Elongate Trace Formation



INTERNATIONAL SEARCH REPORT

International application No.

PCT/US19/66990

A. CLASSIFICATION OF SUBJECT MATTER

IPC - C23C 18/16, 18/38; H05K 1/02, 1/03, 1/09, 1/11, 3/10, 3/18 (2020.01)

CPC - C23C 18/16, 18/38; H05K 1/02, 1/03, 1/09, 1/11, 1/115, 3/10, 3/107, 3/18, 3/181, 3/187, 3/4038, 3/465, 3/4661

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

See Search History document

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

See Search History document

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

See Search History document

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X --- Y	US 9,706,650 B1 (SIERRA CIRCUITS, INC) 11 July 2017; figures 1C-5F; column 6, line 33 to column 7, line 26; column 9, line 28 to column 12, line 26	1-7, 15-18 --- 9-10, 12-13
X --- Y	US 2016/0278206 A1 (SIERRA CIRCUITS, INC) 22 September 2016; figures 2, 4-9; paragraphs [0003], [0014], [0020]-[0025]	8, 11, 14 --- 9-10, 12-13
A	US 2009/0272562 A1 (YOSHIOKA, S ET AL) 05 November 2009; see entire document	1-18
A	US 2005/0100720 A1 (SHIRAI, S ET AL) 12 May 2005; see entire document	1-18
A	US 6,534,723 B1 (ASAI, M ET AL) 18 March 2003; see entire document	1-18
A	US 2018/005489 A1 (DABROWSKI, S) 04 January 2018; see entire document	1-18
P, X	US 2019/0014667 A1 (SIERRA CIRCUITS, INC) 10 January 2019; see entire document	1-18

☐ Further documents are listed in the continuation of Box C.☐ See patent family annex.

* Special categories of cited documents:

"A" document defining the general state of the art which is not considered to be of particular relevance

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Date of the actual completion of the international search

18 February 2020 (18.02.2020)

Date of mailing of the international search report

03 MAR 2020

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