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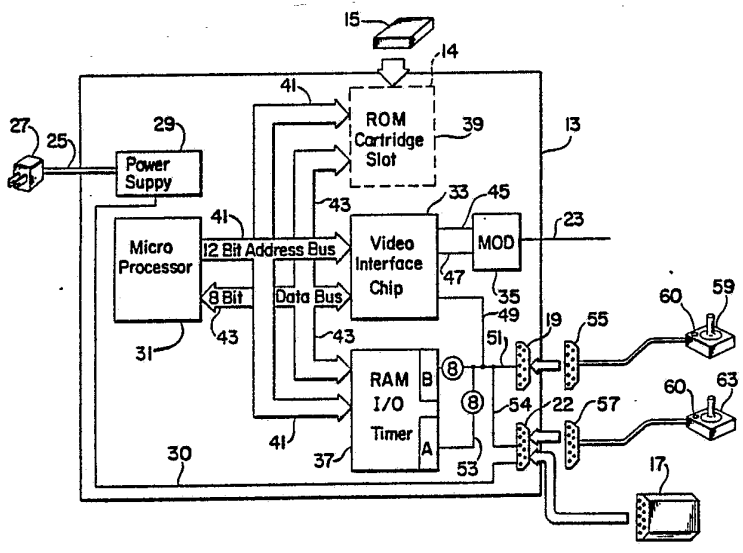

(57) Abstract

In a home video game computer (13) such as the Atari VCS, VIC-20, or Atari 5200, for example, which use pluggable game cartridges (15) to determine what game can be played, information generated as the result of a game playing session can not be carried forward to a next game playing session. According to the present invention a small solid state memory module or key (17) can be plugged into the home video game computer (13) in place of a control paddle or joystick (59, 63) for storing a variety of information. The key (17) includes a nonvolatile, electrically erasable programmable memory chip (71). The game cartridge (15) determines the particular game that can be played and the type of information that can be stored in the transportable key (17). One example of the type of information that can be stored in the key (17) is high score information. The key (17) would contain a record of the highest score achieved by a particular player for a particular game.

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TRANSPORTABLE READ/WRITE STORAGE SYSTEM FOR HOME VIDEO GAME COMPUTER

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates generally to improvements in computer systems, and more particularly pertains to new and improved television connectable video game computers wherein a cartridge insert determines the game to be played.

2. Description of the Prior Art

Present television connectable video game computers such as the Atari 2600, the VIC-20 or the Atari 5200 are designed so that when the unit is turned off, all memory contents are destroyed. Each game must be played from the very beginning at every session. These video game computers do not utilize a memory which can provide for permanent storage of information. Higher priced computers which have mass storage capability such as, for example, cassette tape or floppy disk, are able to store information on the tape or disk and carry it forward to the next game playing session.

None of these systems, however, utilize or even contemplate the utilization of a solid state, external, modular plug attached memory which requires no costly drive or transport mechanism.

SUMMARY OF THE INVENTION

A plug-connectable module for a television connectable video game computer containing a nonvolatile read/write memory is used to store and, if desired, transport certain information from one game to the next. The game cartridge determines what information can be stored in the module which may be connected to a control input socket of the video game computer. The game cartridge program determines whether the key is connected to the video game computer. If it is, then that part of the game cartridge program which is designed to take advantage of the read/write memory in the module is enabled. One example of such a program is the determination of whether the previous high score for the particular game cartridge stored in the module has been bested, and the storage of the new high score in the module memory.

BRIEF DESCRIPTION OF THE DRAWINGS

The objects and many of the attendant advantages of this invention will be readily appreciated as the same becomes better understood by reference to the following detailed description when considered in conjunction with the accompanying drawings in which like reference numerals designate like parts throughout the figures thereof, and wherein:

Figure 1 is a perspective view showing the video game computer system with the external memory module attached.

Figure 2 is a block diagram illustration of the video game computer system and its interface with the game cartridge, the external manually manipulatable controls and the external memory module.

Figure 3 is a block diagram showing the structural interrelationship between the external memory module and the game cartridge.

Figure 4 is a block diagram of the I.C. memory structure utilized in the memory module.

Figure 5 is a block diagram of the I.C. input/output structure utilized in the video game computer.

Figure 6 is a flow chart illustrating an example of how the memory module could be utilized to store information transportable from one game to the next.

Figure 7 is a flow chart showing how the external memory module is read pursuant to program codes stored in the game cartridge.

Figure 8 is a flow chart illustrating how the external memory module is erased under command of program code stored in the game cartridge.

Figure 9 is a flow chart showing how the external memory module is written into under program code stored in the game cartridge.

DESCRIPTION OF THE PREFERRED EMBODIMENT

Figure 1, which illustrates the preferred embodiment 11 for a transportable read/write storage system for video game computers, shows a game computer 13 such as an Atari 2600, a VIC-20 or Atari 5200, for example. This computer typically has a slot 14 for receiving a game cartridge 15 as well as at least a pair of connectors 19 and 22 for receiving input data from controls such as a joystick, paddle control (rotary knob) or primitive keyboard. The computer is powered by way of a transformer device (not shown) over lines 25, and provides signals to a CRT for display on the screen over lines 23. The transportable read/write memory

module 17 is preferably adapted to have a connector that physically mates with a connector 22 of the video game computer 13.

The module 17 may be constructed so that an input controller, such as a joystick, connects to the other end of the module 17 (not shown). Such a structure for the module 17 permits the module to act as a conduit for the controller device connected to it, besides acting as a transportable external memory unit.

The function of the connectors 19 and 22 as I/O ports is determined by the program code stored in the game cartridge 15. How this is accomplished will be seen more clearly hereinafter.

Referring now to Figure 2, a detailed block diagram is presented to facilitate a better understanding of the relationship and control functions between the game cartridge 15, the external memory module 17 and the computer 13. The computer 13 is basically an 8-bit data bus structure utilizing a 6507 microprocessor chip. A power supply 29 is supplied with an appropriate power source by way of transformer 27 which is plugged into a standard 110 volt AC outlet.

Besides the two input ports 19 and 22, the computer 13 has a cartridge slot 14 with an interface connector 39 which receives the game cartridge 15. The game cartridge contains the programming which determines the game that can be played and the images that are displayed on the CRT video screen (not shown). The CRT unit, which is typically a home television unit, is fed over cable 23 by way of modulator 35. The modulator is in turn fed with video and sound signals from the video interface circuit 33 over video line 45 and sound line 47. A 6507 microprocessor 31 communicates with the game cartridge memory and the video interface circuit 33 by way of a 12-bit address bus 41 and an 8-bit data bus 43.

In normal operation, the manually-manipulatable input devices such as joystick 59 and 63, for example, are connected by way of connectors 55 and 57, to connectors 19 and 22, respectively. With both joysticks connected, two players can input data to the computer simultaneously. Joystick devices are well known to provide movement data for the object being displayed on the screen, as well as firing, or other, commands by way of a button 60 mounted on the unit.

The data supplied at either input connector 19 or 22 is provided both to the video interface circuit over lines 49 and to port A of the 6532 input/output circuit 37. The 6532 I/O circuit 37 is manufactured by Synertek Corporation and others. This circuit module is displayed in the Synertek catalog as No. SY6532 and is described on pages 3-129 to 3-136 thereof. The explanatory material and diagrams set forth in these pages are incorporated herein by reference as if fully set forth herein. The reader is referred to the catalog and its descriptive material about the Synertek RAM, I/O Timer Array SY6532 for a complete understanding of its function.

In normal operation, port A and port B of the 6532 I/O circuit 37 are input ports that simply receive data from controller devices 59 and 63 and others, and provide them to the video interface circuit 33 or the 6507 microprocessor 31 over data bus 43.

According to a preferred embodiment of the present invention, the modular external memory 17 utilizes a nine-pin connector which mates with the connector 22 of the video game computer 13. Besides simply providing for a physical connection between the memory module 17 and the computer 13, the connector 22 must be configured to an I/O port which is able to handle the transmission of data in both directions, out, as well as

into the computer 13. This is accomplished according to the present invention by the instruction code stored in the game cartridge 15, as will be explained hereinafter.

As is more fully explained in the publication regarding the Synertek 6532 circuit 37, port A and port B comprise an eight-line input/output port. Connector sockets 19 and 22 are nine-pin sockets. Two of the pins are reserved and used as a power output channel for the memory module 17, a ground line and a power line. The memory module 17 is connected to the power supply 29 by way of line 30. The eight lines 53 of port A are split between the connectors 19 and 22. Four lines 51 go to connector 19. Four lines 54 go to connector 22.

Figure 3 illustrates in block diagram form the basic functional interrelationship between the game cartridge 15 and the modular external memory 17. As is well known, the game cartridge 15 basically comprises a read-only memory (ROM) 69 that is connected to the home video game computer 13 by an interface connector and interface lines 65 that tie into the 12-bit address bus 41 and the 8-bit data bus 43 (Figure 2) of the home video game computer 13.

The modular external memory 17 preferably comprises a nonvolatile sequential access electrically-erasable programmable memory 71. A form of such memory is manufactured by National Semiconductor and is known as the NMC 9306, 256-bit Serial Electrically Erasable Programmable Memory. A description of such memory is published in a preliminary specification sheet dated August 1982. The reader is referred to that preliminary specification for a complete understanding of the function of the external memory. The information contained therein is hereby incorporated by reference as if fully set forth herein.

Essentially, the NMC 9306 programmable memory chip connects to the home video game computer 13 by way of an input/output port on the 6532 I/O circuit 37 (Figure 2) through appropriate pin connectors or an equivalent physical connection means 67.

The program code stored in the ROM 69 of the game cartridge 15 determines if the modular memory 17 is connected, and proceeds to read, write or erase the information contained in modular memory 17 in a manner which relates to the game program stored in ROM 69.

A block diagram of the NMC 9306 memory 71 is set forth in Figure 4. The circuit is essentially a peripheral memory for data storage which is accessed by a simple serial interface. DO terminal 81 is the data output line. DI terminal 75 is the data input line. The NMC 9306 contains a 256-bit E^2 PROM which is divided into 16 registers of 16 bits each. Each 16-bit word is read or written serially. The written information is stored in a floating gate cell with at least ten years data retention. The stored data can be updated by an erase/write cycle. The input and output pins are controlled by separate serial formats. Six 9-bit instructions can be executed. The instruction format has a logical 1 as a start bit, 4 bits as an OP code and 4 bits of address. The on chip programming voltage generator allows the user to use a single power supply (VCC). The DO serial output pin 81 is valid only during the read mode.

A read instruction to the NMC 9306 circuit 71 is the only instruction which outputs the serial data on the output pin 81. After a read instruction is received, the instruction and address are decoded, and data is transferred from the memory register into a 16-bit serial out register (data register). A dummy bit

(logic 0) precedes the 16-bit data output string. The output data changes during the high states of the system clock CLK.

Before the contents of the E^2 PROM memory of the external memory circuit 71 can be changed, its contents must first be erased. Before an erase function or a write function can be performed, an erase/write enable instruction (EWEN) must be transmitted. After the appropriate changes in memory have been made, an erase/write disable instruction (EWDS) must be sent. These instructions, especially the erase/write disable instruction, are provided to protect against accidental disturbance of the data in the E^2 PROM of circuit 71. When executing a read instruction, no EWEN or EWDS instruction need be used.

If a certain 16-bit register in the E^2 PROM is to be reprogrammed by changing its contents, the register must first be erased by setting all the bits to binary 1's. Subsequent programming, of course, is then accomplished by setting certain of these 1 bits to 0's. After an erase instruction is supplied, the CS input chip select line 77 determines the start of the programming. The register in the E^2 PROM specified by the address in the instruction received is then set entirely to binary 1's. When the erase/write program main time constraint has been satisfied, the CS chip select input 77 is brought up for at least one clock period on SK clock line 79. A new instruction may then be supplied.

The entire contents of the E^2 PROM may be erased by setting all the register in the memory array to a 1 by providing an erase all registers instruction (ERAL).

After the appropriate register or the entire E^2 PROM has been erased, new data may be written into memory by a write instruction which is followed by 16 bits of data written into the register specified by the address code. The data is inputted serially at DI line 75. The erase/write time is determined by the low state of the signal on CS line 77 following the instruction. Timing should be arranged accordingly so that the programming modes should all end with the signal on the CS line 77 high for one SK clock period on line 79, or followed by another instruction.

The I/O circuit 37 of the home video game computer 13 is a general purpose I/O circuit which permits its PA0 - PA7 interface lines 53 and interface line 51 to act as either inputs or outputs. Under normal use of the home video game computer, these lines function only as inputs for the controllers which are attached to them. However, when the external modular memory 17 is connected to either one of the connectors 19, 22, some of the interface lines are reconfigured to function as output lines as well as input lines.

Generally, the memory 71 requires +5 volts power (VCC) and ground (GND) available at the socket. In addition, three output and one input pin are needed to interface the external modular memory circuit 71 with the computer 13. Referring now to Figure 5, a block diagram of the input/output circuit 37 is illustrated showing the two I/O ports 53 and 51. This I/O circuit is divided into four basic sections, a random access memory (RAM), an I/O section, a timer section and an interrupt control section. The RAM interfaces directly with the microprocessor through the system data bus 43 and address lines 41. The I/O section consists of two 8-bit halves, half A, and half B. Each half contains a

Data Direction Register and an Output Register. The RAM is a 128 x 8 Static RAM which is addressed by signals on lines A0 to A6 at port 53, a signal at $\overline{RS}$, a signal at CS1 and a signal at $\overline{CS2}$.

There are four 8-bit internal registers in the I/O circuit 37, a Data Direction Register A, a Data Direction Register B, an Output Register A, and an Output Register B. The two Data Direction Registers, A and B, control the direction of data into and out of the peripheral unit that may be connected to ports 53 and 51. A logic 0 in the bit position of the Data Direction Register for a certain line causes the corresponding line of the I/O port to act as an input line. A logic 1, on the other hand, causes the corresponding line to act as an output line. The voltage on any line programmed as an output is determined by the corresponding bit in the output register. Data is read directly from the PA0 to PA7 lines during a peripheral read operation.

To address the I/O circuit 37, seven address inputs are utilized, A0 to A6, as well as $\overline{RS}$ and the two chip select inputs CS1 and $\overline{CS2}$. To address the random access memory, for example, CS1 must be high with $\overline{CS2}$ and $\overline{RS}$ low. To address the I/O and interval timer, CS1 and $\overline{RS}$ must be high with $\overline{CS2}$ low. Thus, to access the circuit, CS1 must be high and $\overline{CS2}$ must be low. In order to distinguish between the RAM and the I/O and timer section, the $\overline{RS}$ input is used. When this input is low, the random access memory is accessed. When this input is high, the I/O and interval timer section is addressed. To distinguish between the timer and the I/O section, address line A2 is utilized. When A2 is high the interval timer is accessed. When A2 is low the I/O section is addressed. The data is transmitted to and from the microprocessor 31 by way of D0 to D7 data lines 43 and address lines 41.

An example of the use that may be made of the external storage module in connection with a game cartridge is shown by the flow chart of Figure 6 which sets forth the steps of the program utilized to store and retain in the external memory module, a new high game score. Programming code for this program is stored in the game cartridge along with the game itself.

When the video game computer is turned on 83 it comes out of the inactive mode 81 and the particular game of that cartridge is activated. The game is played 85 until completion. The program then provides a "game over" indication 87. This indication initiates a determination 89 of whether the external modular memory or key is connected to the computer.

This is accomplished by sending a read instruction to A input port 53 to interrogate first connector 19 and then connector 22. If the key or external modular memory is not connected to either connector, then no data is received and the key is assumed not to be connected. Upon making the determination that the key is not connected, the program goes back 107 to its inactive mode 81.

If data is received from either connector, then the key is assumed to be connected 91, and the program goes into its next function 93 of determining whether the data received is representative of a game score. If it is 95, then the program goes to its next function. If it is not 97, for example, the output may be all 1's, which indicates that the external memory module has been erased, then the program goes into a separate branch routine.

Assuming for the present that the data received is a score, the program will then determine 99 whether the score stored in the external memory module has been exceeded by the score generated by the present

game play. If the score generated by the game play is higher 101, then the program goes into one routine. If it is not higher 107, then the program goes into its inactive mode 81, thereby leaving the score stored in the external memory module intact.

In the instance where it was determined that, either the external memory module did not contain any score, or that the score contained in the external memory module was bested by the latest game play, the new high score information generated by the most recent game play is stored in the external memory module or key by writing 105 that high score information into memory. Then the routine goes 107 into its inactive mode 81.

Figure 7 is a flow chart illustration of the program steps required to read the contents of one register or all the registers of the external memory module 17. Assume, for the sake of example, that the four input/output lines D1 line 75, CS line 77, SK line 79 and DO line 81 of the memory module 71 are connected to lines PA0, PA1, PA2 and PA3, respectively, of the I/O circuit 37 in the home video game computer 13. The read instruction would be as follows.

Three of the I/O lines must be set to output status. This is accomplished by setting a binary 1 in their respective positions in the A Data Direction Register. It should be remembered that this example is for I/O port A which has PA0 to PA7 lines 53. Assume that D1 input data 75 is connected to PA0, the CS chip select input line 77 is connected to PA1, the SK clock input line 79 is connected to PA2, and the DO data output line 81 is connected to PA3. Then PA0, PA1 and PA2 are configured as output lines, in order to supply data, chip select, and clocking signals to the external

memory module. Line PA3 would remain as an input line to receive the data out (DO) from the external memory module 17.

After this reconfiguration step 127, the program goes 129 into its read command function 131 as follows. A binary high signal is supplied to chip select input CS. A read command comprising the following format 11000A3A2A1A0 is sent over the PA0 pin to the D1 data input line 75. The last four digits, A3, A2, A1, A0 are the 4-bit address for the 16-bit register that is to be read out. The data is clocked out by clocking signals supplied over the PA2 pin to the SK input 79. Accordingly, 16 bits of data are clocked out over the DO output terminal to input pin PA3. The 16 bits of data are stored as two 8-bit bytes in the static RAM of the I/O chip 37 (Figure 5). This process is repeated 16 times, varying the address bits A3, A2, A1, A0 from 0000 to 1111 for each time, so as to address each register in the E^2 PROM of the external memory module 71. When all the data has been read out, the chip select CS input provided by pin PA1 is dropped low. This brings up the last step 133. The three pins that were configured as output lines, PA0, PA1 and PA2, are reconfigured 135 to be input lines again. This is accomplished by replacing the binary 1's in the respective positions of the Data Direction Register A with binary 0's. The A port then again becomes an input port for receiving data on all five input lines. A manually-manipulative controller such as a joystick may then be utilized by this port.

Prior to any programming function whereby new data is written into the external memory module 17, an erase function must be performed to set all the bit positions in the 16-bit registers of the external memory module to a binary "1". This operation is accomplished

in the manner illustrated by the flow chart of Figure 8. Assume again that the external memory module 17 is connected to pins PA0, PA1, PA2 and PA3 of port A. Before an erase function can be performed, three of these pins, PA0, PA1 and PA2 must be configured as output pins. This is step 109. It is performed in the manner discussed above.

As soon as the external memory module is configured to receive clocking, data, and chip select, an erase/write enable (EWEN) command must be sent 113. This command is sent as follows. The CS chip select input is set high. A data signal in the form 10011000 is sent over PA0 pin to the data input pin D1. This data is clocked in at SK by the clocking signal at pin PA2. When this step is completed, the CS chip select is dropped to a low. This completes the sending of the EWEN 115.

The next step 117 is an erase all registers command (ERAL), which is accomplished as follows. The CS chip select input is raised. A data signal in the form 100100000 is sent over pin PA0 to the DI input of the external memory module. This data is clocked over the clocking input SK from pin PA2. When this data is all clocked in, the CS chip select signal is again lowered. That completes this function 119.

The next function 121 to be performed is an erase/write disable command (EWDS). The erase/write disable command is accomplished in the following manner. The CS chip select signal is raised to a high at pin PA1. A data signal 100000000 is transmitted to the external memory module at its data input line DI by way of pin PA0. This data is clocked in by the clocking signal supplied to the SK input at pin PA2. When this data is clocked in, the chip select signal is again lowered. This completes 123 the erase/write disable

function. The entire contents of memory in the external memory module is now in a binary 1 condition. At this point all the pins are again reconfigured 125 in the manner described in connection with Figure 7. The pins that were configured as output pins are again input pins. In this erased condition, the external memory module is ready to receive new data.

The procedure for supplying new data to the external memory module 17 is set forth in the flow chart of Figure 9. Assuming that the external memory module 17 is still connected to the same pins of the A port, the first step 137 is to set three of the pins PA0, PA1 and PA2 to be output lines so that data may be supplied to the D1, CS and SK inputs of the external memory module. Upon this operation being completed 139, an erase/write enable command (EWEN) is sent 141 in the manner described with respect to step 113 of Figure 8. Upon reception 143 of this programming enable command, a write command 145 is sent sixteen times in the following 9-bit format: 10100A3A2A1A0. The last four bits A3A2A1A0 are the address of the register to be written into. These four bits change from 0000 to 1111 as each register is addressed. This operation transmits 32, 8-bit bytes of data from the static RAM in the I/O circuit 37 to pin PA0 to be inputted into the external memory module at input line D1. Upon completing 147 the writing of all the registers in the external memory module, an erase/write disable instruction 149 is performed in the manner of step 121 of Figure 8. Completion 151 of the EWDS instruction activates the procedure for reconfiguring the three pins that were configured as output pins into input pins. This is accomplished in the manner described above in connection with Figure 7.

Obviously, many different programs may be stored in the external program memory module 17 by use of the routines described above to supplement and enhance the particular game program stored in the game cartridge. It is therefore to be understood that within the scope of the appended claims, the invention may be practiced otherwise than as specifically described.

WHAT IS CLAIMED IS:

1. In combination with a computer connectable to a television unit and utilizing game cartridges for determining the particular game to be played, said video game computer also having connector sockets for receiving multi-pin plugs from manually-manipulatable control devices, the improvement which comprises:

a nonvolatile memory means for connection to the computer by plug connecting means;

means for recognizing the nonvolatile memory means is connected to the computer; and

means for storing information related to the game defined by the game cartridge in said nonvolatile memory means.

2. In the improved computer of Claim 1 further comprising a housing means for housing said nonvolatile memory means and said plug connecting means, said plug connecting means being adapted to mate with a connector of the computer.

3. In the improved computer of Claim 2 wherein said means for recognizing that the nonvolatile memory means is connected to the computer is activated after the game determined by the game cartridge is over.

4. In the improved computer of Claim 1, further comprising:

means to determine if a high score is stored in the nonvolatile memory means;

means to determine if the present score is higher; and

means to store the present score in the nonvolatile memory means if it is higher than the stored score.

5. In the improved computer of Claim 1 wherein said storing means comprises:

means for erasing the contents of said nonvolatile memory means; and

means for writing data bits into said nonvolatile memory means after said memory means has been erased.

6. In the improved computer of Claim 1 wherein said storing means comprises:

means for configuring at least one pin connector in one multi-pin socket of the computer as an output before beginning any data transfer operation; and

means for reconfiguring the pin connector serving as an output during data transfer back to an input after the data transfer operation is complete.

7. In combination with a computer connectable to a CRT unit and utilizing a separate insertable medium for determining the function to be performed by said computer, the computer also being adapted to physically connect to an input/output device by way of pin connectors, the improvement which comprises:

an external memory means adapted for physical connection to the computer;

means for recognizing the memory means is physically connected; and

means for storing information related to the function defined by said insertable medium in said external memory means.

8. The improved computer of Claim 7 wherein said external memory means comprises a housing for the memory which includes a plug connector for connecting the memory to the computer.

9. The improved computer of Claim 7 wherein said storing means comprises:

means for configuring at least one pin conector of the computer as an output before starting any data transfer operation between the computer and the external memory; and

means for reconfiguring the pin connector serving as an output during data transfer back to an input after the data transfer operation is completed.

10. The improved computer of Claim 7 wherein said storing means comprises:

means for erasing the contents of said external memory means; and

means for writing data into said external memory means after said memory means has been erased.

11. In combination with a computer connectable to a CRT unit and utilizing a separate insertable medium for determining the function to be performed by said computer, the computer being adapted to physically connect to an input/output device by way of connectors, the improvement which comprises:

an external memory means adapted for physical connection to the computer;

means for recognizing the memory means is physically connected;

means for configuring at least one line of the connector of the computer as an output before starting a data transfer operation between the computer and the external memory; and

means for reconfiguring the pin connector serving as an output during data transfer back to an input after the data transfer operation is completed.

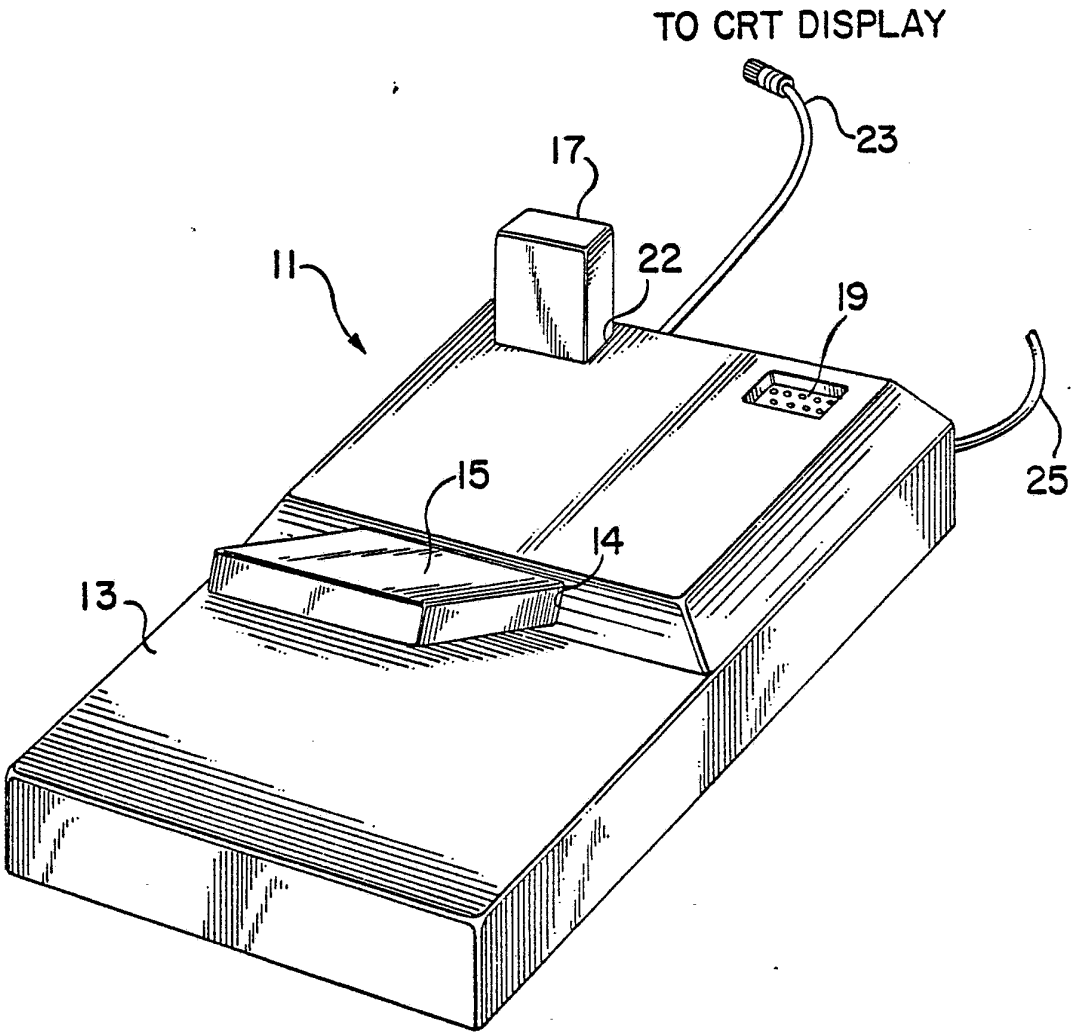

FIG. 1

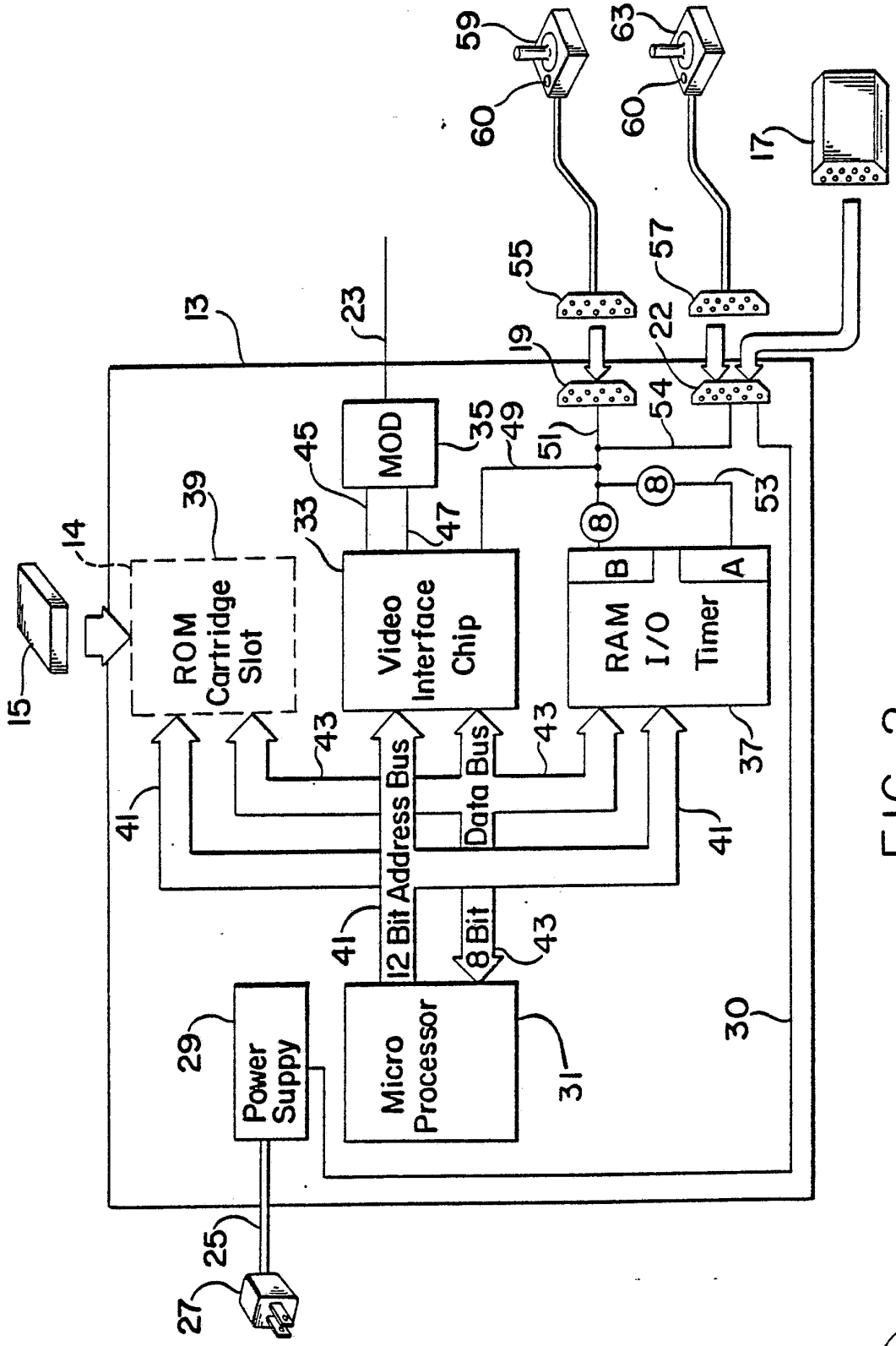

FIG. 2

SUBSTITUTE SHEET

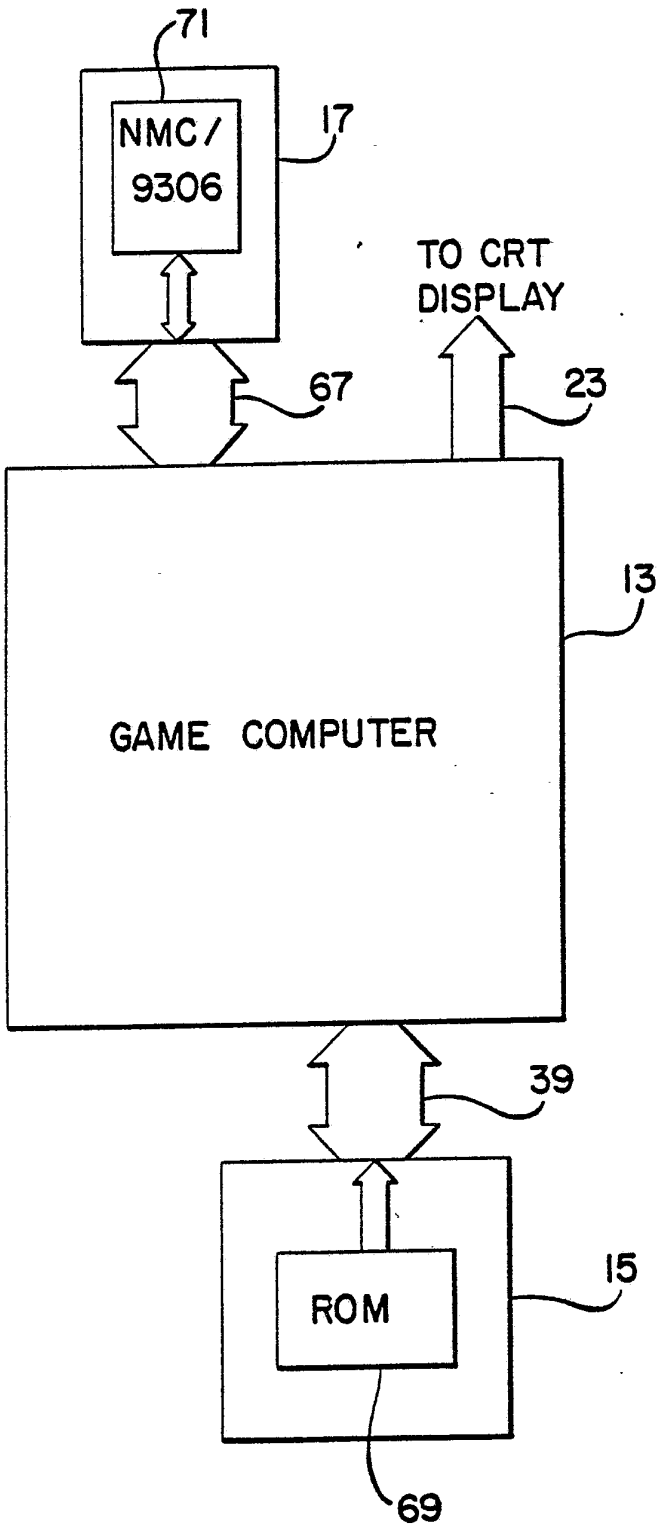

FIG. 3

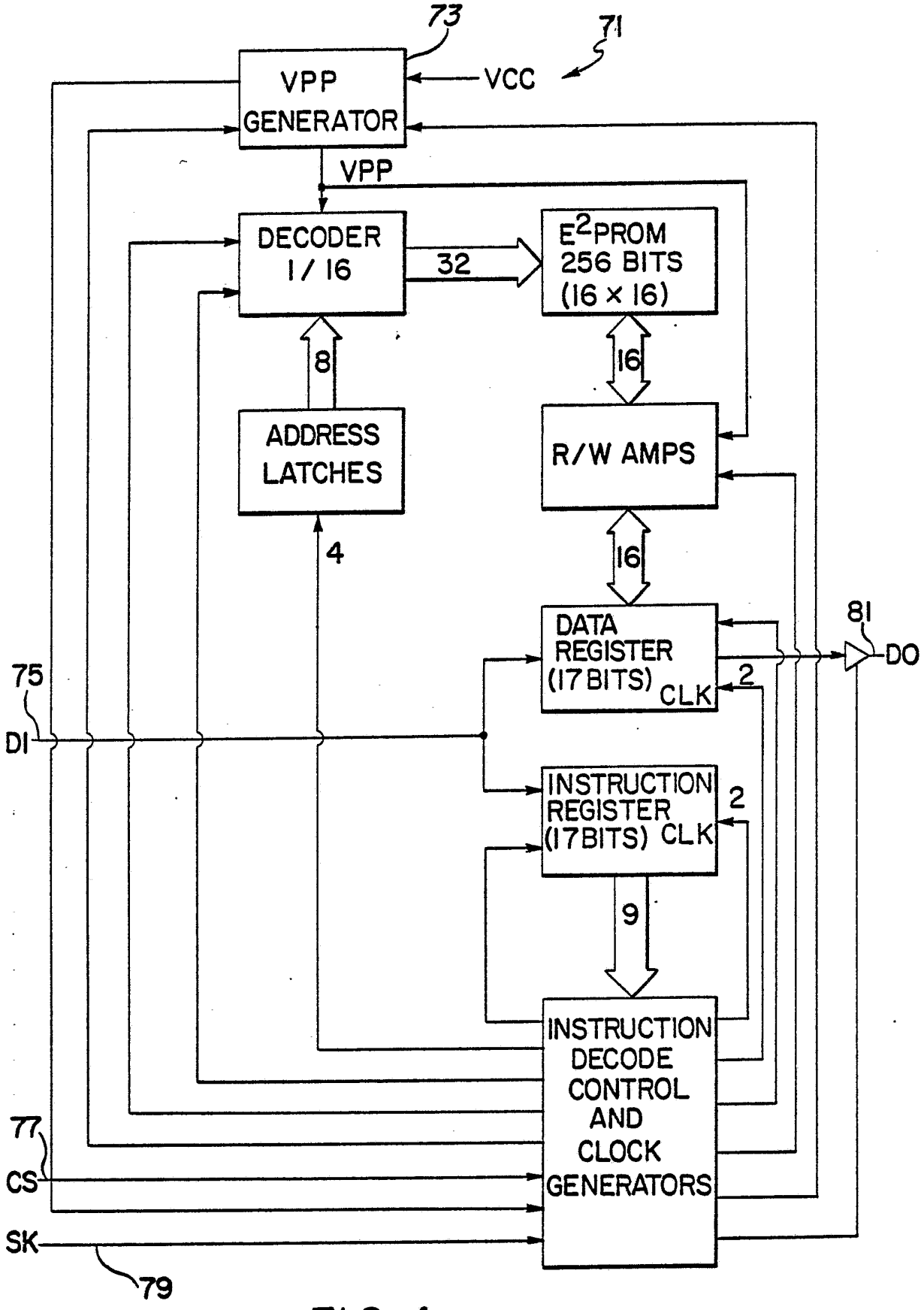

FIG. 4

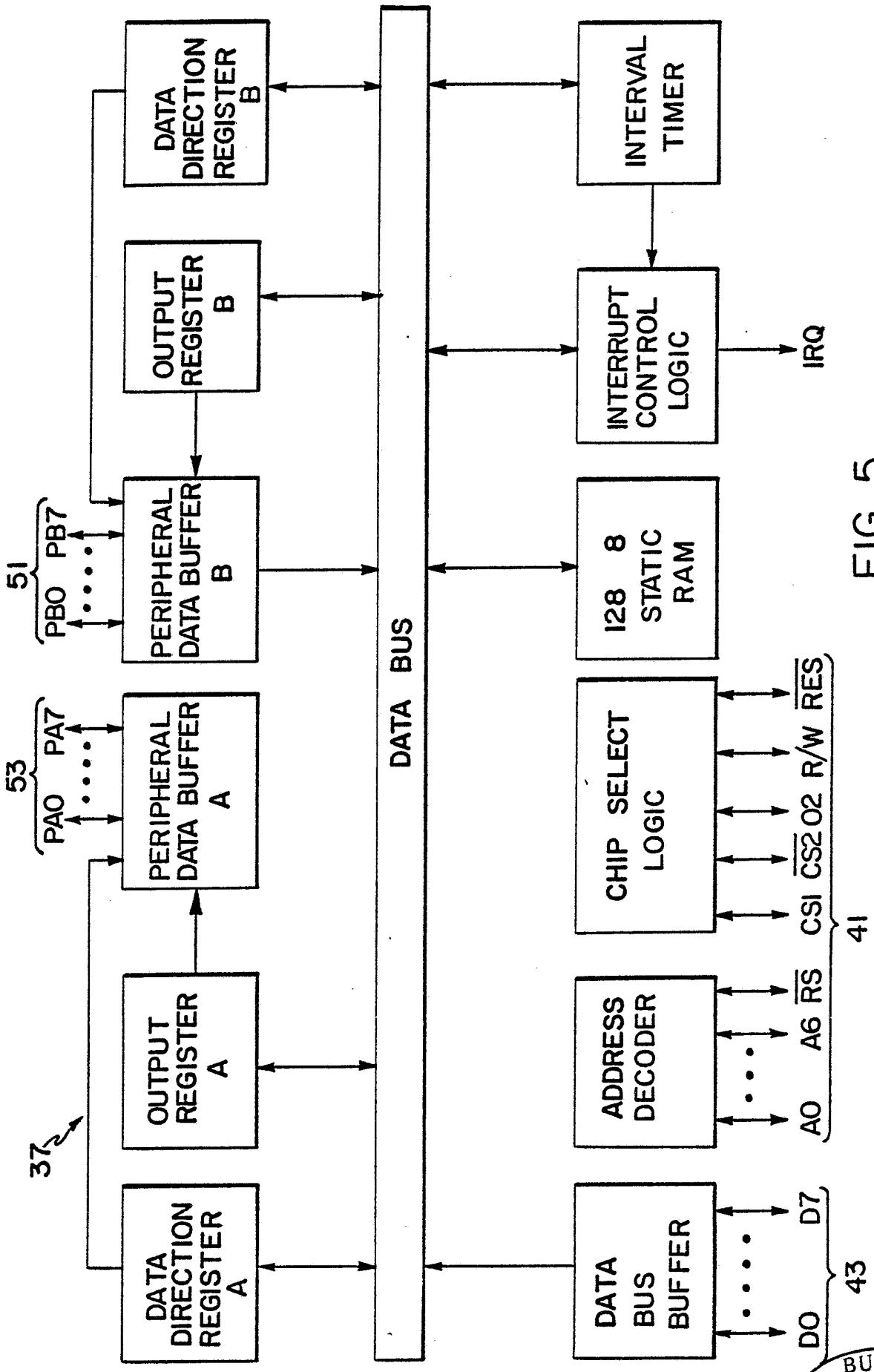

FIG. 5

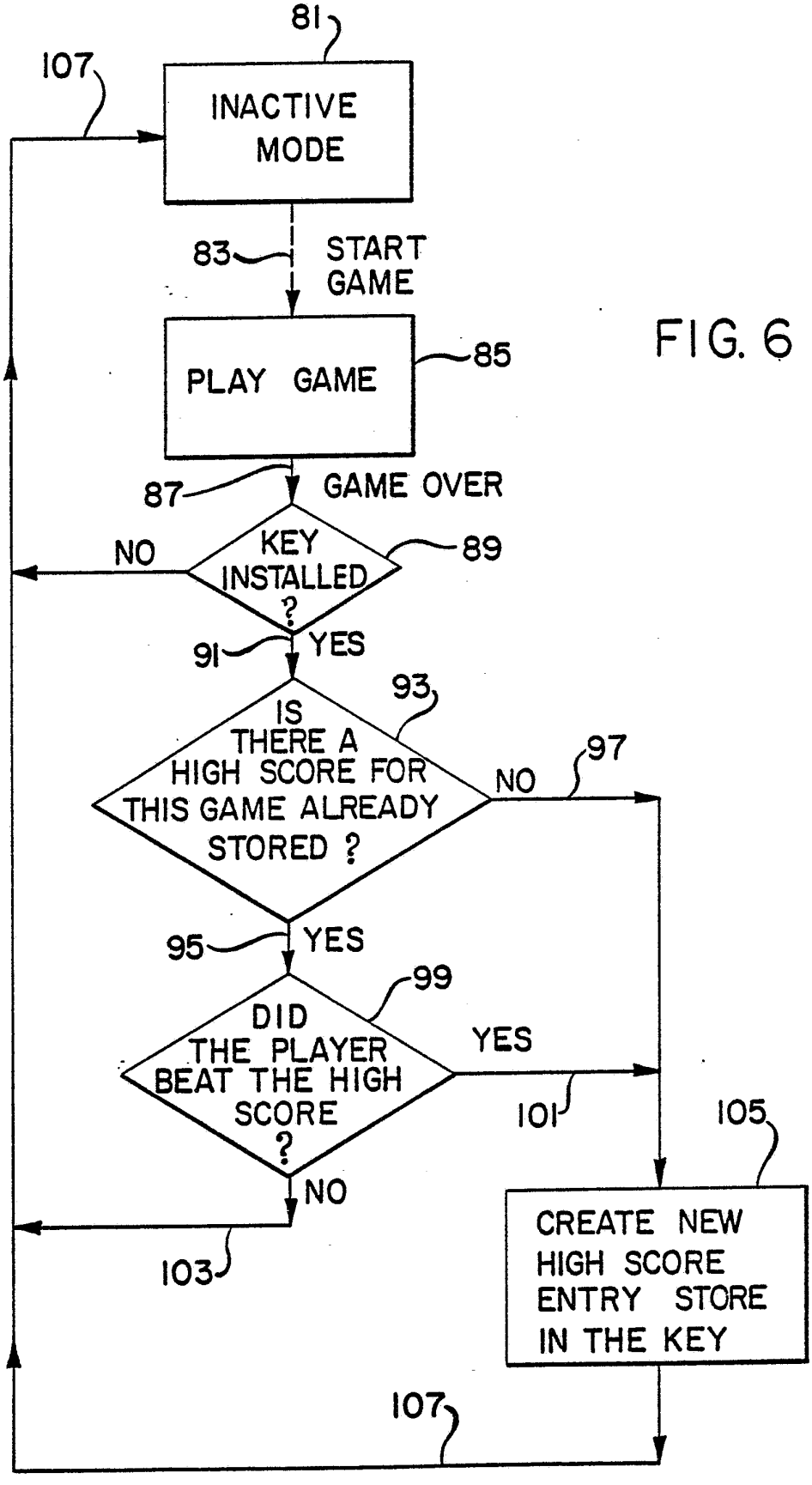

FIG. 6

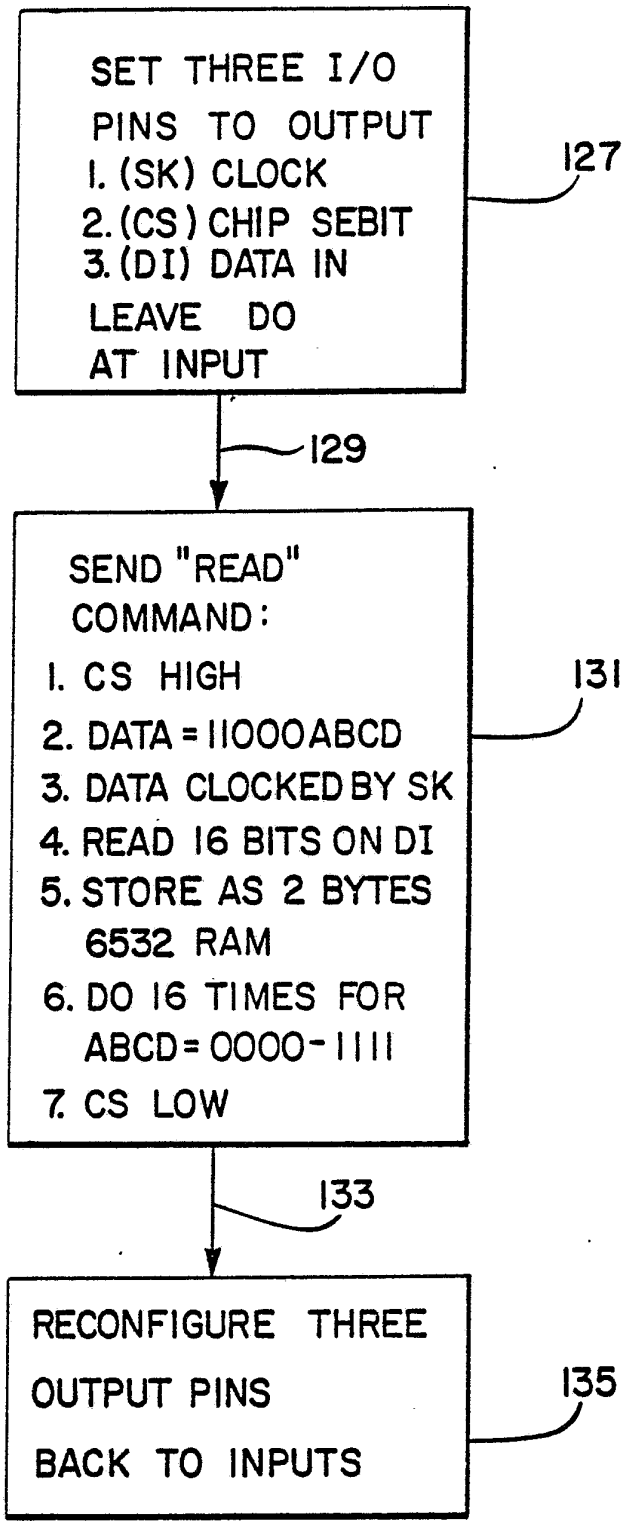

FIG. 7

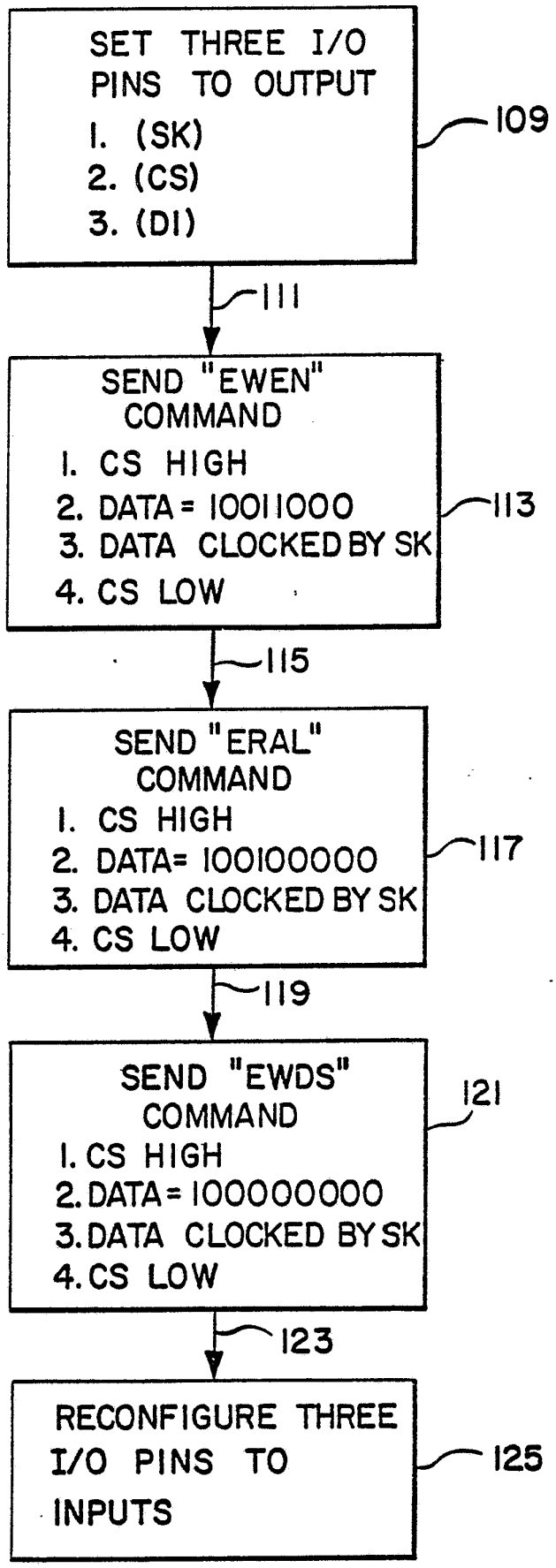

FIG. 8

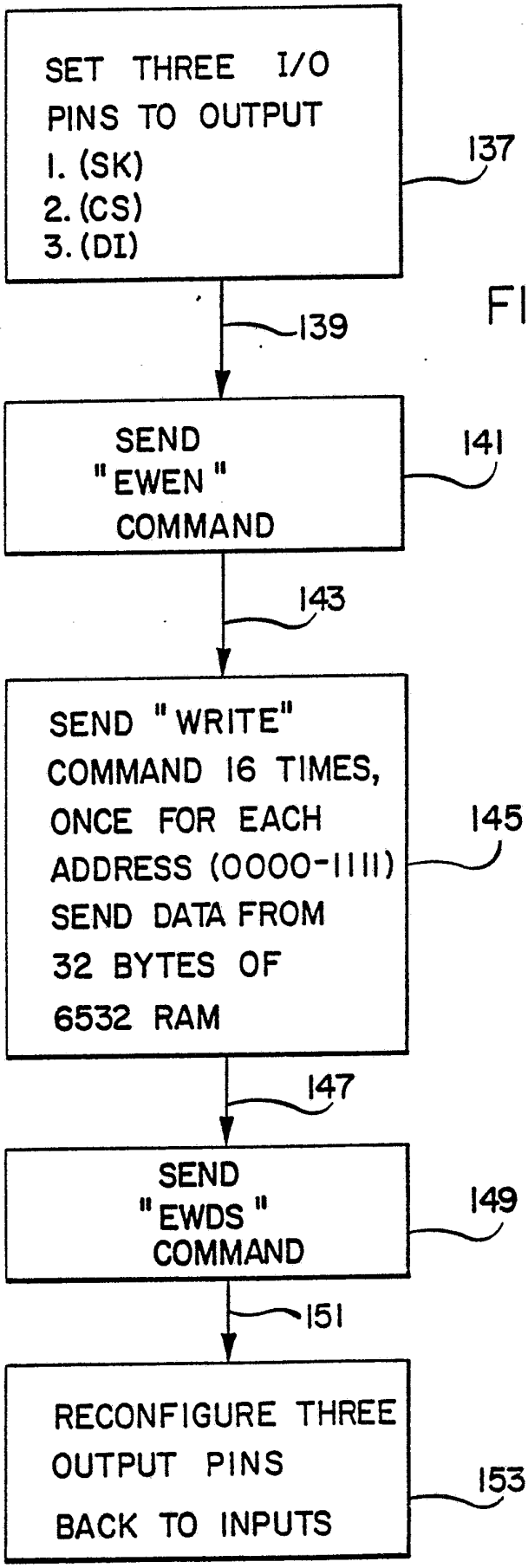

FIG. 9

INTERNATIONAL SEARCH REPORT

International Application No PCT/US84/00765

I. CLASSIFICATION OF SUBJECT MATTER (if several classification symbols apply, indicate all) [3]

According to International Patent Classification (IPC) or to both National Classification and IPC

INT. CL.[3] G06F 15/44; A63F 9/22
U.S. CL. 364/410; 273/85G

II. FIELDS SEARCHED

Minimum Documentation Searched [4]

Classification System	Classification Symbols
U.S.	273/85G, DIG 26, DIG 28 364/410

Documentation Searched other than Minimum Documentation to the Extent that such Documents are Included in the Fields Searched [5]

III. DOCUMENTS CONSIDERED TO BE RELEVANT [14]

Category *	Citation of Document, [16] with indication, where appropriate, of the relevant passages [17]	Relevant to Claim No. [18]
Y	US,A, 4,156,928 (Inose et al) 29 May 1979	1,2,6-9 and 11
A	US,A, 4,259,668 (Nishimura et al) 31 March 1981	
Y	US,A, 4,300,207 (Eivers et al) 10 November 1981	6, 9 and 11
A,P	US,A, 4,386,773 (Bronstein) 07 June 1983	
A,P	US,A, 4,432,067 (Nielsen) 14 February 1984	
Y	GB,A, 2,070,810 (Yokoi et al) 9 September 1981	1-11

* Special categories of cited documents: [15]

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

IV. CERTIFICATION

Date of the Actual Completion of the International Search [2]	Date of Mailing of this International Search Report [2]
20 JUNE 1984	03 JUL 1984
International Searching Authority [1]	**Signature of Authorized Officer [20]**
ISA/US	Jerry Smith

FURTHER INFORMATION CONTINUED FROM THE SECOND SHEET

A,T	Buchsbaum, W.H. and Mauro, R. 'Microprocessor-based electronic games', 1983, Mc Graw-Hill Inc., New York, pages 253-266.	
Y	MARS™ and JUMPBUG™ advertisement. Play Meter, Vol. 8, No. 5, March 1, 1982, pages 60, 61, 91 and 92.	1-11

V. ☐ OBSERVATIONS WHERE CERTAIN CLAIMS WERE FOUND UNSEARCHABLE [10]

This international search report has not been established in respect of certain claims under Article 17(2) (a) for the following reasons:

1. ☐ Claim numbers ....., because they relate to subject matter [12] not required to be searched by this Authority, namely:

2. ☐ Claim numbers ....., because they relate to parts of the international application that do not comply with the prescribed requirements to such an extent that no meaningful international search can be carried out [13], specifically:

VI. ☐ OBSERVATIONS WHERE UNITY OF INVENTION IS LACKING [11]

This International Searching Authority found multiple inventions in this international application as follows:

1. ☐ As all required additional search fees were timely paid by the applicant, this international search report covers all searchable claims of the international application.

2. ☐ As only some of the required additional search fees were timely paid by the applicant, this international search report covers only those claims of the international application for which fees were paid, specifically claims:

3. ☐ No required additional search fees were timely paid by the applicant. Consequently, this international search report is restricted to the invention first mentioned in the claims; it is covered by claim numbers:

4. ☐ As all searchable claims could be searched without effort justifying an additional fee, the International Searching Authority did not invite payment of any additional fee.

Remark on Protest

☐ The additional search fees were accompanied by applicant's protest.

☐ No protest accompanied the payment of additional search fees.