



(43) International Publication Date
22 September 2016 (22.09.2016)

WIPO | PCT

- | | |
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| <p>(51) International Patent Classification:
 <i>H03B 5/12</i> (2006.01)</p> <p>(21) International Application Number:
 PCT/CN2016/076499</p> <p>(22) International Filing Date:
 16 March 2016 (16.03.2016)</p> <p>(25) Filing Language:
 English</p> <p>(26) Publication Language:
 English</p> <p>(30) Priority Data:
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 kind of national protection available</i>): AE, AG, AL, AM,
 AO, AT, AU, AZ, BA, BB, BG, BH, BN, BR, BW, BY,
 BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DK, DM,
 DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT,
 HN, HR, HU, ID, IL, IN, IR, IS, JP, KE, KG, KN, KP, KR,
 KZ, LA, LC, LK, LR, LS, LU, LY, MA, MD, ME, MG,
 MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM,
 PA, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SA, SC,
 SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN,
 TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.</p> <p>(84) Designated States (<i>unless otherwise indicated, for every
 kind of regional protection available</i>): ARIPO (BW, GH,
 GM, KE, LR, LS, MW, MZ, NA, RW, SD, SL, ST, SZ,
 TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, RU,
 TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE,
 DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU,
 LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK,
 SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ,
 GW, KM, ML, MR, NE, SN, TD, TG).</p> |
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[Continued on next page]

- (54) Title:** TAPPED INDUCTOR VOLTAGE CONTROLLED OSCILLATOR

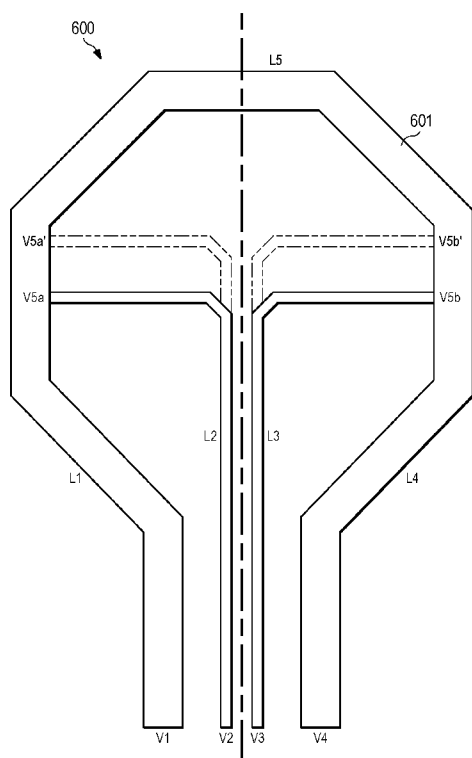


FIG. 6

- (57) Abstract:** A voltage controlled oscillator includes a resonator and an amplifier. The resonator includes a capacitive element and an inductive element. The inductive element has a plurality of conductive segments forming a physical loop. The inductive element has electrical connections on the physical loop to the plurality of conductive segments forming at least one electrical loop disposed within an interior space formed by the physical loop. The amplifier has an input and an output, the input coupled to a first conductive segment forming a first impedance and the output coupled to a second conductive segment forming a second impedance.

**Declarations under Rule 4.17:**

- *as to applicant's entitlement to apply for and be granted a patent (Rule 4.17(ii))*
- *as to the applicant's entitlement to claim the priority of the earlier application (Rule 4.17(iii))*

Published:

- *with international search report (Art. 21(3))*

TAPPED INDUCTOR VOLTAGE CONTROLLED OSCILLATOR

CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] This application claims priority to U.S. non-provisional patent application Serial No. 14/659,244, filed on March 16, 2015 and entitled “Tapped Inductor Voltage Controlled Oscillator”, which is incorporated herein by reference as if reproduced in its entirety.

TECHNICAL FIELD

[0002] This disclosure is generally directed to voltage controlled oscillators (VCOs) and more particularly to a VCO employing an integrated tapped inductor with a novel topology and layout to improve noise performance and reduce power consumption.

BACKGROUND

[0003] With the growth of wireless communication systems such as cellular, wireless local area networks (WLAN), satellite communications, the global positioning system (GPS), and the like, demands for smaller size, lower cost, and higher frequency products have continuously increased. In this regard, voltage controlled oscillators (VCOs) play a critical role in communication systems, providing periodic signals required for timing in digital circuits and frequency translation in radio frequency (RF) circuits. A VCO may be embodied as a stand-alone module separate from other circuits or integrated into an application specific integrated circuit (ASIC), for use in devices such as, but not limited to, handsets, base stations, and virtually every communication device. As RF frequencies increase and supply voltages decrease, it has become increasingly more difficult to design VCOs that meet system noise and power requirements while meeting the demands for smaller size, lower cost, and higher frequency products.

[0004] The noise performance of a LC resonant VCO is directly related to its signal power, which is proportional to the energy stored in the resonant inductor-capacitor (LC) tank circuit. In traditional VCO designs, the energy stored in the LC circuit is proportional to the size of the inductor and the square of the supply voltage for the amplifier in the VCO.

[0005] As semiconductor device geometries shrink, the supply voltage for the amplifier is required to decrease to avoid hot carrier injection (HCI). HCI is a phenomenon wherein charge carriers become trapped in the gate dielectric of a MOS transistor and permanently change its switching characteristics.

[0006] To compensate for the decrease in voltage, the inductor used in the LC tank circuit must also decrease in size so that the resulting noise performance of the VCO remains the same. Increases in required frequency also require the inductor size to be decreased. The decrease in inductor size presents a challenge since as an inductor gets smaller in size, its quality factor (Q) decreases as well, further increasing the thermal noise of the VCO.

[0007] A so-called Hartley VCO is an active circuit comprising an amplifier, capacitor(s), and inductors. A characteristic of the Hartley VCO is a tuned circuit comprising capacitor(s) in parallel with two or more inductors in series, and a feedback signal for oscillation taken from a connection in between the inductors.

[0008] Referring now to FIGURE 1, a schematic is illustrated of a prior art differential Harley VCO 100 employing a conventional LC tank circuit resonator. Transistors M1-M4 form an amplifier. PMOS transistors M3 and M4 have their sources coupled to the positive supply rail (e.g. VDD), and their respective gates cross coupled to the drains of the opposing PMOS transistor and to the sources of PMOS transistors M1 and M2, respectively. PMOS transistors M1 and M2 have their drains coupled to the negative supply rail (e.g. ground), and their respective gates coupled to the conventional LC tank resonator formed with inductors L1 and L2 and capacitors C_v.

[0009] FIGURE 2 illustrates a prior art layout for tapped inductors L1 and L2 schematically depicted in FIGURE 1. In FIGURE 2, the inductors L1 and L2 are shown as nested loops 201-202. The nesting provides the mutual couplings k_1 and k_2 shown in FIGURE 1.

[0010] FIGURE 3A illustrates a schematic diagram of a prior art simplified differential Harley VCO circuit employing a conventional LC tank circuit resonator. FIGURE 3B illustrates a simplified schematic diagram of the small signal half circuit resonator of the circuit in FIGURE 3A.

[0011] FIGURE 4 illustrates an integrated circuit die for the circuit depicted in FIGURES 3A and 3B including the prior art layout for the tapped inductors. In FIGURE 4, the inductor elements L1 and L2 are shown as nested loops 401-402. The nesting provides the mutual coupling K shown in FIGURE 3A. Inductive elements L3 and L4 in FIGURE 3A are shown as separate loops 403-404 in FIGURE 4.

[0012] In the prior art layouts depicted in FIGURES 2 or 4, separate loops (e.g., loops 201-202 and loops 401-402) are utilized for inductances L1 and L2. These separate loops put physical limits on how small an inductor element can be used in a Hartley VCO design. For example, because of the inductor topology, the minimum to maximum frequency range of the VCO circuits depicted in FIGURES 1 and 3 is on the order of ten to fifteen percent due to the parasitic capacitance associated with the large physical inductances.

SUMMARY

[0013] According to an embodiment of the present disclosure, a voltage controlled oscillator (VCO) includes a resonator and an amplifier. The resonator includes a capacitive element and an inductive element, the inductive element having a plurality of conductive segments forming a physical loop. The inductive element has electrical connections on the physical loop to the plurality of conductive segments forming at least one electrical loop disposed within an interior space formed

by the physical loop. The amplifier has an input and an output, the input coupled to a first conductive segment forming a first impedance and the output coupled to a second conductive segment forming a second impedance.

[0014] According to another embodiment of the present disclosure, a non-transitory computer-readable medium is disclosed for use with a computer having software for creating integrated circuits. The computer-readable medium has stored thereon one or more computer-readable data structures having photomask data for making a voltage controlled oscillator. The voltage controlled oscillator includes a resonator and an amplifier. The resonator includes a capacitive element and an inductive element, the inductive element having a plurality of conductive segments forming a physical loop. The inductive element has electrical connections on the physical loop to the plurality of conductive segments forming at least one electrical loop disposed within an interior space formed by the physical loop. The amplifier has an input and an output, the input coupled to a first conductive segment forming a first impedance and the output coupled to a second conductive segment forming a second impedance.

[0015] The present disclosure provides a VCO with reduced current, lower noise, higher Q at higher frequencies, and better linearity.

BRIEF DESCRIPTION OF THE FIGURES

[0016] FIGURE 1 illustrates a schematic of a prior art differential Harley VCO circuit employing a conventional LC tank circuit resonator;

[0017] FIGURE 2 illustrates an integrated circuit die for the circuit depicted in FIGURE 1 including the prior art layout for the tapped inductors;

[0018] FIGURE 3A illustrates a schematic of a prior art simplified differential Harley VCO circuit employing a conventional LC tank circuit resonator and FIGURE 3B illustrates the small signal half circuit resonator of the circuit in FIGURE 3A;

[0019] FIGURE 4 illustrates an integrated circuit die for the circuit depicted in FIGURES 3A and 3B including the prior art layout for the tapped inductors;

[0020] FIGURE 5 illustrates a schematic of a differential LC resonant circuit including parasitic resistance for use in a differential VCO;

[0021] FIGURE 6 illustrates an example layout for a differential tapped inductor for use in an LC tank circuit and for integration onto an integrated circuit in accordance with principles of the present invention;

[0022] FIGURE 7 illustrates a differential LC tank circuit resonator including a schematic representation of the equivalent inductances of the tapped inductor of FIGURE 6 coupled in parallel with a capacitor, in accordance with principles of the present disclosure;

[0023] FIGURE 8 illustrates a block diagram of a differential VCO practiced in accordance with principles of the present disclosure;

[0024] FIGURE 9 illustrates a schematic of an example differential VCO employing an amplifier having a CMOS topology and a resonator practiced in accordance with the principles of the present disclosure;

[0025] FIGURE 10 illustrates an example layout for a single ended tapped inductor for use in an LC tank circuit and for integration onto an integrated circuit in accordance with principles of the present invention;

[0026] FIGURE 11 illustrates a single ended LC tank circuit resonator including a schematic representation of the equivalent inductances of the tapped inductor in FIGURE 10 coupled in parallel with a capacitor.

[0027] FIGURE 12 illustrates a schematic of a single ended LC resonant circuit including parasitic resistance for use in a single ended VCO;

[0028] FIGURE 13 illustrates a schematic of an example single ended VCO employing an amplifier having a CMOS topology and a resonator practiced in accordance with the principles of the present disclosure;

[0029] FIGURE 14 illustrates a simplified ASIC design flow employing EDA tools for producing ASICs having embodiments of the present disclosure; and

[0030] FIGURE 15 illustrates an illustrative example of a computing device for practicing the design flow of FIGURE 14.

DETAILED DESCRIPTION

[0031] The construction and practice of various embodiments are discussed in detail below. It should be appreciated, however, that the present disclosure provides many applicable inventive concepts that can be embodied in a wide variety of specific contexts. Though specific embodiments discussed herein are merely illustrative of specific ways to make and practice the teachings and technology herein, they do not limit the scope of this disclosure.

[0032] Unless defined otherwise, all technical and scientific terms used herein have the same meaning as commonly understood by those of skill in the art to which this disclosure pertains.

[0033] Various circuits or other components may be described or claimed as "configured to" perform a task or tasks. In such contexts, "configured to" is used to connote structure by indicating that the circuits/components include structure (e.g., circuitry) that performs the task or tasks during

operation. As such, the circuit/component can be said to be configured to perform the task even when the specified circuit/component is not currently operational (e.g., is not on). The circuits/components used with the "configured to" language include hardware - for example, circuits to implement the operation, etc. Reciting that a circuit/component is "configured to" perform one or more tasks is expressly intended not to invoke 35 U.S.C. 112 (f).

[0034] Reference throughout this specification to "one embodiment", "an embodiment", "a specific embodiment", or "particular embodiment" means that a particular feature, structure, or characteristic described in connection with the particular embodiment is included in at least one embodiment and not necessarily in all particular embodiments. Thus, respective appearances of the phrases "in a particular embodiment", "in an embodiment", or "in a specific embodiment" in various places throughout this specification are not necessarily referring to the same embodiment. Furthermore, the particular features, structures, or characteristics of any specific embodiment may be combined in any suitable manner with one or more other particular embodiments. It is to be understood that other variations and modifications of the particular embodiments described and illustrated herein are possible in light of the teachings herein and are to be considered as part of the spirit and scope.

[0035] Turning now to FIGURE 5, a schematic of an LC resonant circuit 500 including parasitic resistances R_c and R_l is illustrated for use in a differential VCO. The VCO amplifier supplies a current to the input impedance of the LC circuit 500 that produces a voltage across the LC circuit equal to the voltage at the input of the amplifier. In a traditional single inductor VCO (e.g., a Pierce configuration), the amplifier drives the impedance $Z_2(\omega_o)$ and the voltage at the input of the amplifier is that indicated as being across $Z_2(\omega_o)$.

[0036] In the present disclosure, a single inductor is tapped (e.g., divided into at least two parts) in a manner described by a coefficient K . The amplifier drives the inductor tap defined by impedance $Z_1(\omega_o)$ while the voltage at the input of the amplifier is from a signal across the inductor tap defined by impedance $Z_2(\omega_o)$. Theoretically, inductor segments KL and $(1-K)/2 * L$ can be viewed as separate inductors for small inductances and very high frequencies. However, separate inductors are impractical due to the physical size requirements and mutual coupling.

[0037] Since the input and the output of the amplifier are at different points in the LC circuit (i.e. Z_2 and Z_1), the input voltage to the amplifier in the VCO can be much larger than its output voltage as determined by the voltage divider action of the tapped inductor. There are a number of advantages to this arrangement.

[0038] The HCI voltage limitations of the amplifier are constrained to the output. This allows the input signal to exceed the supply voltage restrictions of the amplifier. Since the input voltage is representative of the energy stored in the LC circuit, the VCO noise is lower for the same total inductance than a VCO with a traditional resonator because the LC circuit voltage is higher. Moreover, the inductor does not have to decrease in size to meet noise requirements allowing for a higher inductor Q when integrated onto an integrated circuit, such as, for example, as part of an ASIC.

[0039] Since the input voltage to the amplifier exceeds the power supply rails, the gain of the amplifier is higher for a given power consumption. The output current of the amplifier is the product of the input voltage across Z_2 and its transconductance g_m . Since the input voltage is increased, the amplifier has more gain for the same current. This reduces the power requirements for the system.

[0040] As can be seen from FIGURE 5 and equations (1) – (5) below, the impedance of the LC circuit at $Z_1(\omega_o)$ is lower than the impedance $Z_2(\omega_o)$ by a factor of K^2 . The linearity of the amplifier under large signal conditions is dominated by the linearity at its output rather than its input. Having a lower impedance at the output of the VCO reduces the non-linear mixing of flicker noise to the VCO frequency thus improving its close-in sideband noise spectrum. Those skilled in the art will recognize that flicker noise at baseband frequencies is a type of electronic noise with a $1/\omega$ density spectrum but once mixed by nonlinear elements, produces a $1/\omega^3$ portion of the VCO single side band phase noise.

$$\text{At resonance } \omega_o^2 = \frac{1}{LC} \text{ and } \omega_o L = X_o \quad (1)$$

$$\text{Re}\{Z_1(\omega_o)\} = \frac{KR_l[(1-K)R_l + R_c]}{R_l + R_c} + \frac{(K\omega_o L)^2}{R_l + R_c} \quad (2)$$

$$\text{Re}\{Z_1(\omega_o)\} \approx K^2 \left[\frac{X_o^2}{R_l + R_c} \right] \quad (3)$$

$$\text{Re}\{Z_2(\omega_o)\} = \frac{R_l R_c}{R_l + R_c} + \frac{(\omega_o L)^2}{R_l + R_c} \quad (4)$$

$$\text{Re}\{Z_2(\omega_o)\} \approx \left[\frac{X_o^2}{R_l + R_c} \right] \quad (5)$$

Where: ω_o is the oscillation frequency (rad/s),

L is the inductance,

C is the capacitance,

R_l is the parasitic resistance of the inductor,

R_c is the parasitic resistance of the capacitor,

K is a constant relating Z_1 to Z_2 ,

X_o is the reactance of inductor L at the resonant frequency ω_o .

[0041] Reference is now made to FIGURE 6 that illustrates an example layout for a differential tapped inductor 600 for use in an LC tank circuit (such as that shown in FIGURE 5) and for integration onto an integrated circuit in accordance with principles of the present invention. FIGURE 7 illustrates an ideal schematic of a differential LC tank circuit resonator 702 including representation of the equivalent inductances 600' of the tapped inductor 600 in FIGURE 6 coupled in parallel with a capacitor C. Note that the segments V1-V5a, V2-V5a, V3-V5b, V4-V5b, and V5a-V5b in FIGURE 6 correspond to inductors L1, L2, L3, L4, and L5 in the schematic of FIGURE 7, respectively.

[0042] The differential tapped inductor 600 comprises one or more conductive segments (e.g. V1-V5a, V4-V5b, and V5a-V5b) forming a physical loop 601. As used herein, the term “physical loop” refers to a closed or nearly closed geometric shape having beginning and ending points that are co-located or in close proximity to each other, and that includes at least one substantially convex portion that defines an interior space within the convex portion (e.g., a cyclic polygon or cyclic polygon segment). Thus, a physical loop is to be distinguished from an “electrical loop” which typically represents a closed path of any shape through which electrical current may flow.

[0043] The physical loop 601 is preferably symmetrical and, in the case of the inductor 600, is depicted as a generally octagonal shape. Those skilled in the art will recognize that the physical loop 601 may include other symmetrical and non-symmetrical shapes without departing from the scope of the present disclosure (e.g., a rectangle, square, hexagon, etc.). The inductor 600 is tapped with electrical connections at V5a and V5b with segments V2-V5a and V3-V5b forming electrical

loops (L2 and L3) disposed within the interior space formed by the physical loop 601 (including L1, L5, and L4).

[0044] The capacitive element C of resonator 702 may be embodied as a PMOS varactor, an NMOS varactor, a metal-insulator-metal (MIM) device, or any other suitable capacitance element. In a silicon process, two types of varactors may be employed namely, a reversed-bias pn junction diode or a MOS capacitor varactor. The MOS capacitor varactor may be formed with a MOS transistor having its drain, source, and bulk connections coupled together and adjusting the capacitance based on the voltage applied between the bulk and the gate connections. Those skilled in the art will recognize other alternatives for the capacitive element C of the resonator 702 without departing from the scope of the present disclosure.

[0045] The quality factor (Q) for the resonant LC tank circuit 702 is dependent on the inductor 600 having low resistance. The resistance of the inductor 600 is minimized by using a thick/wide metallization process such as, but not limited to, aluminum, copper, gold, or other appropriate material to reduce the series resistance. The inductor 600 is preferably formed over a high dielectric substrate material such as silicon, gallium arsenide, or other appropriate material. Surface micro-machining technologies may be employed to create an air gap between the inductor and the substrate to further increase the dielectric property.

[0046] The inductor tap segments V2-V5a and V3-V5b (L2 and L3) which are coupled to the amplifier output and are not part of the LC resonant circuit. Accordingly, their parasitic resistances are not as critical as the parasitic resistances of inductor segments of L1, L4, and L5. Thus, L2 and L3 segments may be constructed with a thinner metal material as depicted in FIGURE 6.

[0047] A practical problem associated with using multiple inductors (e.g. L1-L5) is the mutual inductance in any connection from the amplifier output to the tap points V5a and V5b. The

inductor current in the resonant LC circuit is typically much higher than the current supplied from the amplifier by a factor of the circuit Q . When the mutual inductance is high, the induced current from the resonant LC circuit becomes high enough in the leads from the amplifier output to the tap point that the input impedance to the tap becomes so high that the amplifier cannot supply any current. To overcome this issue, tap segments V2-V5a (L2) and V3-V5b (L3) are routed up the middle of the inductor 600 (as depicted in FIGURE 6) so that the induced currents from the symmetric halves of the inductor 600 cancel.

[0048] Tap locations V5a and V5b can be adjusted in metal to vary the power consumption, VCO output swing, and phase noise performance. This can be used to fine tune a design held at metal such as depicted by V5a' and V5b'. To minimize the parasitic effects of the substrate, the substrate may be doped to have a high resistivity and/or the distance between the metal layer and the substrate may be increased through etching or micro-machining.

[0049] FIGURE 8 illustrates a block diagram of a differential VCO 800 practiced in accordance with principles of the present disclosure. The tapped LC tank circuit 702 (illustrated in detail in FIGURE 7) has terminals V1, V2, V3, and V4. Terminals V1 and V4 are coupled to the input of amplifier 804 and terminals V2 and V3 are coupled to the output of amplifier 804. Amplifier 804 preferably has a CMOS topology however those skilled in the art will recognize other suitable amplifier topologies such as PMOS, NMOS and bipolar, without departing from the scope of the present disclosure.

[0050] Referring to FIGURE 9, a schematic is illustrated of an example differential CMOS VCO 900 employing a LC tank resonator circuit 702 practiced in accordance with the principles of the present disclosure. A CMOS amplifier is formed with PMOS transistors 904 and 906 and NMOS transistors 908 and 910. The PMOS transistors 904 and 906 have their sources coupled to the positive supply rail (VDD) and their gates coupled to the gates of NMOS transistors 908 and

910, respectively. The gates of PMOS transistor 904 and NMOS transistor 908 are coupled to the V1 tap of differential tapped LC tank circuit 702. The gates of PMOS transistor 906 and NMOS transistor 910 are coupled to the V4 tap of differential tapped LC tank circuit 702. The NMOS transistors 908 and 910 have their sources coupled to the negative supply rail (ground) and their respective drains coupled to the drains of PMOS transistors 904 and 906, respectively.

[0051] The V3 and V4 taps of the LC tank resonator circuit 702 are coupled to the commonly coupled drains of PMOS transistor 904 and NMOS transistor 908 and commonly coupled drains of PMOS transistor 906 and NMOS transistor 910, respectively.

[0052] Referring now to FIGURE 10, an example layout is illustrated for a single ended tapped inductor 1000 for use in an LC tank circuit and for integration onto an integrated circuit in accordance with principles of the present invention. The single ended tapped inductor 1000 comprises one or more conductive segments (e.g. V1-1002 and 1002-V3) forming a physical loop 1001. The physical loop 1001 is preferably symmetrical and is depicted in a generally octagonal shape. Those skilled in the art will recognize other symmetrical and non-symmetrical shapes for the physical loop 1001 without departing from the scope of the present disclosure. The inductor 1000 is tapped with at least one electrical connection (e.g., 1002) with a segment 1002-V2 disposed within the interior of the physical loop 1001. FIGURE 11 illustrates a schematic of an ideal single ended LC tank circuit resonator 1102 including a representation of the equivalent inductances of the tapped inductor 1000 in FIGURE 10 coupled in parallel with a capacitor C.

[0053] The capacitive element C of resonator 1102 may be embodied as a PMOS varactor, an NMOS varactor, a metal-insulator-metal (MIM) device, or any other suitable capacitance element. In a silicon process, two types of varactors may be employed namely, a reversed-bias pn junction diode or a MOS capacitor varactor. The MOS capacitor varactor may be formed with a MOS transistor having its drain, source, and bulk connections coupled together and adjusting the

capacitance based on the voltage applied between the bulk and the gate connections. Those skilled in the art will recognize other alternatives for the capacitive element C of the resonator 1102 without departing from the scope of the present disclosure.

[0054] The quality factor (Q) for the resonant LC tank circuit 1102 is dependent on the inductor 1000 having low resistance. The resistance of the inductor is minimized by using a thick/wide metallization process such as, but not limited to, aluminum, copper, or other appropriate material to reduce the series resistance. The inductor 1000 is preferably formed over a high dielectric substrate material such as silicon, gallium arsenide, or other appropriate material. Surface micro-machining technologies may be employed to create an air gap between the inductor and the substrate to further increase the dielectric property.

[0055] The inductor tap segment L2 which is coupled to the amplifier output is not part of the LC resonant circuit. Accordingly, its parasitic resistance is not as critical as the parasitic resistances of inductor segments of L1 and L3. Thus, the L2 segment may be constructed with a thinner metal material as depicted in FIGURE 10.

[0056] Turning now FIGURE 12, a schematic is illustrated of a single ended LC resonant circuit 1200 including parasitic resistances R_c and R_l for use in a single ended VCO. A single ended VCO amplifier supplies a current to the input impedance of the LC circuit 1200 which produces a voltage across the LC circuit equal to the voltage at the input of the amplifier. In a traditional single ended VCO, the amplifier drives the impedance $Z_2(\omega_o)$ and the voltage at the input of the amplifier is that indicated as being across $Z_2(\omega_o)$.

[0057] In the present disclosure, the inductor is tapped (e.g. divided into at least two parts) described by a coefficient K. The amplifier drives the inductor tap defined by impedance $Z_1(\omega_o)$ while the voltage at the input of the amplifier is from a signal across the inductor tap defined by

impedance $Z_2(\omega_o)$. Theoretically, inductor segments KL and $(1-K)L$ can be viewed as separate inductors for small inductances and very high frequencies. However, separate inductors are impractical due to the physical size requirements and mutual coupling.

[0058] Since the input and the output of the amplifier are at different points in the LC circuit (i.e. Z_2 and Z_1), the input voltage to the amplifier in the VCO can be much larger than its output voltage as determined by the voltage divider action of the tapped inductor.

[0059] Turning now to FIGURE 13, a schematic is illustrated of an example single ended VCO 1300 employing an amplifier having a CMOS topology and a resonator 1102 practiced in accordance with the principles of the present disclosure. A CMOS amplifier is formed with PMOS transistor 1302 and NMOS transistor 1304. PMOS transistor 1302 has its source coupled to the positive supply rail (VDD) and its gate coupled to the gate of NMOS transistor 1304 and to the V1 tap of single ended tapped LC tank circuit 1102. The NMOS transistor 1304 has its source coupled to the negative supply rail (ground) and its drain coupled to the drain of PMOS transistor 1304 and to the V2 tap of single ended tapped LC tank circuit 1102. The V3 tap of the single ended tapped LC tank circuit 1102 is coupled to the negative supply rail (ground).

[0060] While the circuit in FIGURE 13 preferably has a CMOS topology, those skilled in the art will recognize other suitable amplifier topologies such as PMOS, NMOS and bipolar, without departing from the scope of the present disclosure.

[0061] Modern integrated circuit design and manufacturing are commonly automated with Electronic Design Automation (EDA) tools. Example tools may be found from companies such as, but not limited to, Synopsys, Cadence, and Mentor Graphics. The details of these EDA tools are not required for the present disclosure.

[0062] Reference is now made to FIGURE 14 illustrating a simplified general ASIC design flow employing (EDA) tools for producing ASICs having embodiments of the present disclosure. At step 1400, the functional design of an ASIC which may include a VCO having a tapped inductor 600 in accordance with principles of the present disclosure is created.

[0063] For those portions of the ASIC digital in nature, the functional design is typically manifested by writing Register Transfer Level (RTL) code in a Hardware Descriptive Language (HDL) such as but not limited to, VHDL or Verilog. A functional verification (behavioral simulation) is then preferably performed on the HDL data structures to ensure the RTL design is in accordance with the logic specifications. Alternatively, a schematic of the digital logic can be captured with a schematic capture program.

[0064] For portions of the ASIC that are analog in nature (such as the VCO with a tapped inductor of the present disclosure), the analog functional design is typically manifested by capturing a schematic with a schematic capture program. The output of the schematic capture program is then converted (synthesized) into gate/transistor level netlist data structures.

[0065] At step 1402, the data structures are simulated with a simulation program with integrated circuits emphasis (SPICE). At step 1404, the data structures from step 1402 are instantiated with their geometric representations and the physical layout of the ASIC is performed.

[0066] The first step in physical layout is typically so-called “floor-planning” wherein gross regions on the integrated circuit chip are assigned and input/output (I/O) pins are defined. Hard cores (e.g. arrays, analog blocks, inductors, etc.) are placed within the gross regions based on the design constraints (e.g. trace lengths, timing etc.). Clock wiring (commonly referred to as clock trees) are placed and connections between gates/analog blocks are routed. When all the elements are placed, a global and detailed routing is running to connect all the elements together. Postwiring optimization is preferably performed to improve performance (timing closure), noise (signal

integrity), and yield. The layout is modified, where possible, while maintaining compliance with the design rules set by the captive or external semiconductor manufacturing foundry of choice, to make it more efficient to produce. Such modifications may include adding extra vias or dummy metal/diffusion/poly layers.

[0067] At step 1406, the physical designed is verified. Design rule checking (DRC) is performed to determine whether the physical layout of the ASIC satisfies a series of recommended parameters i.e. design rules of the foundry. The design rules are a series of parameters provided by the foundry that are specific to a particular semiconductor manufacturing process. The design rules specify certain geometric and connectivity restrictions to ensure sufficient margins to account for variability in semiconductor manufacturing processes, to ensure that the ASICs work correctly. A layout versus schematic (LVS) check is preferably performed to verify the physical layout corresponds to the original schematic or circuit diagram of the design. A complete simulation is then preferably performed to ensure the layout phase is properly done.

[0068] After the layout is verified in step 1406, mask generation design data typically in the form of GDSII data structures is said to “tapeout” for preparation of photomasks at step 1408. The GDSII data structures are transferred through a communications medium (e.g. storage or over a network) from the circuit designer to either a photomask supplier/maker or directly to the semiconductor foundry.

[0069] At step 1410, the photomasks are created and used to manufacture ASICs in accordance with principles of the present disclosure.

[0070] Some of the techniques described herein can be implemented by software stored on one or more computer readable storage medium and executed on a computer. The selected techniques could be executed on a single computer or a computer networked with another computer

or computers. For clarity, only those aspects of the tools or computer germane to the disclosed techniques are described. Product details well known in the art may be omitted.

[0071] FIGURE 15 shows an illustrative example of a computing device 1501 for practicing the design flow of FIGURE 15. As seen in FIGURE 15, the computing device 1501 includes a computing unit 1503 with a processing unit 1505 and a system memory 1507. The processing unit 1505 may be any type of programmable electronic device for executing software instructions, but will conventionally be a microprocessor. The system memory 1507 may include both a read-only memory (ROM) 1509 and a random access memory (RAM) 1511. As will be appreciated by those of ordinary skill in the art, both the read-only memory 1509 and the random access memory 1511 may store software instructions for execution by the processing unit 1505.

[0072] The processing unit 1505 and the system memory 1507 are connected, either directly or indirectly, through a bus 1513 or alternate communication structure, to one or more peripheral devices. For example, the processing unit 1505 or the system memory 1507 may be directly or indirectly connected to one or more additional memory storage devices 1515. The memory storage devices 1515 may include, for example, a “hard” magnetic disk drive, a solid state disk drive, an optical disk drive, and a removable disk drive. The processing unit 1505 and the system memory 1507 also may be directly or indirectly connected to one or more input devices 1517 and one or more output devices 1519. The input devices 1517 may include, for example, a keyboard, a pointing device (such as a mouse, touchpad, stylus, trackball, or joystick), a scanner, a camera, and a microphone. The output devices 1519 may include, for example, a display device, a printer and speakers. With various examples of the computing device 1501, one or more of the peripheral devices 1515-1519 may be internally housed with the computing unit 1503. Alternately, one or more of the peripheral devices 1515-1519 may be external to the housing for the computing unit

1503 and connected to the bus 1513 through, for example, a Universal Serial Bus (USB) connection or a digital visual interface (DVI) connection.

[0073] With some implementations, the computing unit 1503 may also be directly or indirectly connected to one or more network interfaces cards (NIC) 1521, for communicating with other devices making up a network. The network interface cards 1521 translate data and control signals from the computing unit 1503 into network messages according to one or more communication protocols, such as the transmission control protocol (TCP) and the Internet protocol (IP). Also, the network interface cards 1521 may employ any suitable connection agent (or combination of agents) for connecting to a network, including, for example, a wireless transceiver, a modem, or an Ethernet connection.

[0074] It should be appreciated that the computing device 1501 is illustrated as an example only, and it not intended to be limiting. Various embodiments of the invention may be implemented using one or more computing devices that include the components of the computing device 1501 illustrated in FIGURE 15, or which include an alternate combination of components, including components that are not shown in FIGURE 15. For example, various embodiments of the invention may be implemented using a multi-processor computer, a plurality of single and/or multiprocessor computers arranged into a network, or some combination of both.

[0075] In one embodiment, a resonator means having inductive and capacitive means includes at least two conductive segments that form a conductive loop and an amplification means coupled to at least one conductive segment of the resonator means forming impedance means. In one embodiment, the impedance means includes first and second impedance means. In one embodiment, the at least two conductive segments form two electrical loops symmetrically disposed within the interior space formed by the resonator means.

[0076] In another embodiment, a computer means includes storage means for storing computer instructions having photomask data means for making an oscillator comprising resonator means. The resonator means having inductive and capacitive means that includes at least two conductive segments that form a conductive loop. In one embodiment, the resonator means includes an amplification means coupled to at least one conductive segment of the resonator means forming impedance means. In one embodiment, the impedance means includes first and second impedance means. In one embodiment, the at least two conductive segments form two electrical loops symmetrically disposed within the interior space formed by the resonator means.

[0077] In yet another embodiment, a floor planning means includes logic for defining or assigning gross regions on the integrated circuit and for defining input/output (I/O) pins. The floor planning means includes hard core (e.g. arrays, analog blocks, inductors, etc) placing means for placing within the gross regions based on the design constraints (e.g. trace lengths, timing etc.). Clock wiring placing means (commonly referred to as clock trees) are configured for placing clock trees and for routing connections between gates/analog blocks. A global and detailed routing means is configured to design connections to connect all the elements together.

[0078] Physical design verification means that includes design rule checking means is used to verify the physical design of the circuit (e.g., an ASIC) satisfies one or more design rules. The design rules specify certain geometric and connectivity restrictions to ensure sufficient margins to account for variability in semiconductor manufacturing processes, to ensure that the ASICs work correctly. A layout versus schematic (LVS) means is configured to verify the physical layout corresponds to the original schematic or circuit diagram of the design. A simulation means is configured to perform a complete simulation to ensure the layout phase is properly done.

[0079] Tapeout means is configured to generate mask generation design data typically in the form of GDSII data structures for preparation of photomasks. The GDSII data structures are

transferred through a communications medium (e.g. storage or over a network) from the circuit designer to either a photomask supplier/maker or directly to the semiconductor foundry. Photomask creation means create photomasks that are used to manufacture ASICs in accordance with principles of the present disclosure. Among other features, it should be understood that the above described means are configured as appropriate to generate resonator and amplification means as described and claimed herein.

[0080] Some of the techniques described herein can be implemented by software stored on one or more computer readable storage medium and executed on a computer. The selected techniques could be executed on a single computer or a computer networked with another computer or computers. For clarity, only those aspects of the tools or computer germane to the disclosed techniques are described. Product details well known in the art may be omitted.

[0081] Although features and elements are described above in particular combinations, each feature or element can be used alone without the other features and elements or in various combinations with or without other features and elements. Examples of computer-readable storage mediums include a read only memory (ROM), a random access memory (RAM), a register, cache memory, semiconductor memory devices, magnetic media such as internal hard disks and removable disks, magneto-optical media, and optical media such as CD-ROM disks, and digital versatile disks (DVDs).

[0082] While this disclosure has described certain embodiments and generally associated methods, alterations and permutations of these embodiments and methods will be apparent to those skilled in the art. In particular, it should be noted that while the present disclosure has been described in the context of CMOS amplifiers, those skilled in the art will recognize application to PMOS and NMOS amplifiers, bipolar amplifiers, and other suitable topologies without departing from the scope of the present disclosure. The present disclosure has application to virtually all

communications systems. For example, it may be used in cellular transceivers, 2-way radio communications, Wi-Fi applications, satellite receivers, and any application that uses a voltage controlled oscillator. Accordingly, the above description of example embodiments does not define or constrain this disclosure. Other changes, substitutions, and alterations are also possible without departing from the spirit and scope of this disclosure, as defined by the following claims.

What Is Claimed Is:

1. A voltage controlled oscillator comprising:
a resonator having a capacitive element and an inductive element, the inductive element having a plurality of conductive segments forming a physical loop, the inductive element having electrical connections on the physical loop to the plurality of conductive segments forming at least one electrical loop disposed within an interior space formed by the physical loop; and
an amplifier having an input and an output, the input coupled to a first conductive segment forming a first impedance and the output coupled to a second conductive segment forming a second impedance.
2. The voltage controlled oscillator of claim 1, wherein the plurality of conductive segments form two electrical loops symmetrically disposed within the interior space formed by the physical loop.
3. The voltage controlled oscillator of any one of claims 1-2, wherein the amplifier has an input voltage larger than an output voltage determined by a voltage divider formed by the first and second impedances.
4. The voltage controlled oscillator of any one of claims 1-3, wherein the input voltage exceeds a supply voltage of the amplifier.
5. The voltage controlled oscillator of any one of claims 1-4, wherein the at least one electrical loop is thinner than the physical loop.

6. The voltage controlled oscillator of any one of claims 1-5, wherein the first impedance is proportional to the second impedance.

7. The voltage controlled oscillator of any one of claims 1-6, wherein the amplifier has a CMOS topology.

8. The voltage controlled oscillator of any one of claims 1-7, wherein the amplifier has a differential output.

9. The voltage controlled oscillator of any one of claims 1-8, wherein the amplifier has a single ended output.

10. The voltage controlled oscillator of any one of claims 1-9, wherein the physical loop is symmetrically shaped.

11. The voltage controlled oscillator of any one of claims 1-10, wherein the physical loop has a substantially octagonal shape.

12. A non-transitory computer-readable medium for use with a computer having software for creating integrated circuits, the computer-readable medium having stored thereon one or more computer-readable data structures having photomask data for making a voltage controlled oscillator, the voltage controlled oscillator comprising:

a resonator having a capacitive element and an inductive element, the inductive element having a plurality of conductive segments forming a physical loop, the inductive element having electrical connections on the physical loop to the plurality of conductive segments forming at least one electrical loop disposed within an interior space formed by the physical loop; and

an amplifier having an input and an output, the input coupled to a first conductive segment forming a first impedance and the output coupled to a second conductive segment forming a second impedance.

13. The non-transitory computer-readable medium of claim 12, wherein the plurality of conductive segments form two electrical loops symmetrically disposed within the interior space formed by the physical loop.

14. The non-transitory computer-readable medium of any one of claims 12-13, wherein the amplifier has an input voltage larger than an output voltage determined by a voltage divider formed by the first and second impedances.

15. The non-transitory computer-readable medium of any one of claims 12-14, wherein the input voltage exceeds a supply voltage of the amplifier.

16. The non-transitory computer-readable medium of any one of claims 12-15, wherein the at least one electrical loop is thinner than the physical loop.

17. The non-transitory computer-readable medium of any one of claims 12-16, wherein the first impedance is proportional to the second impedance.

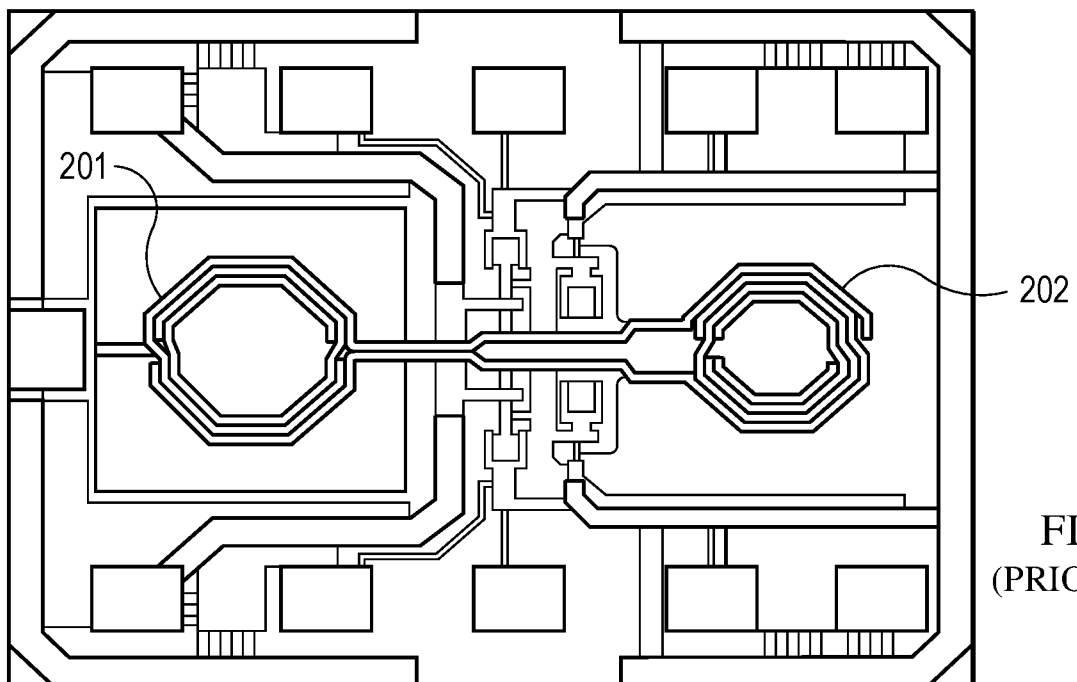
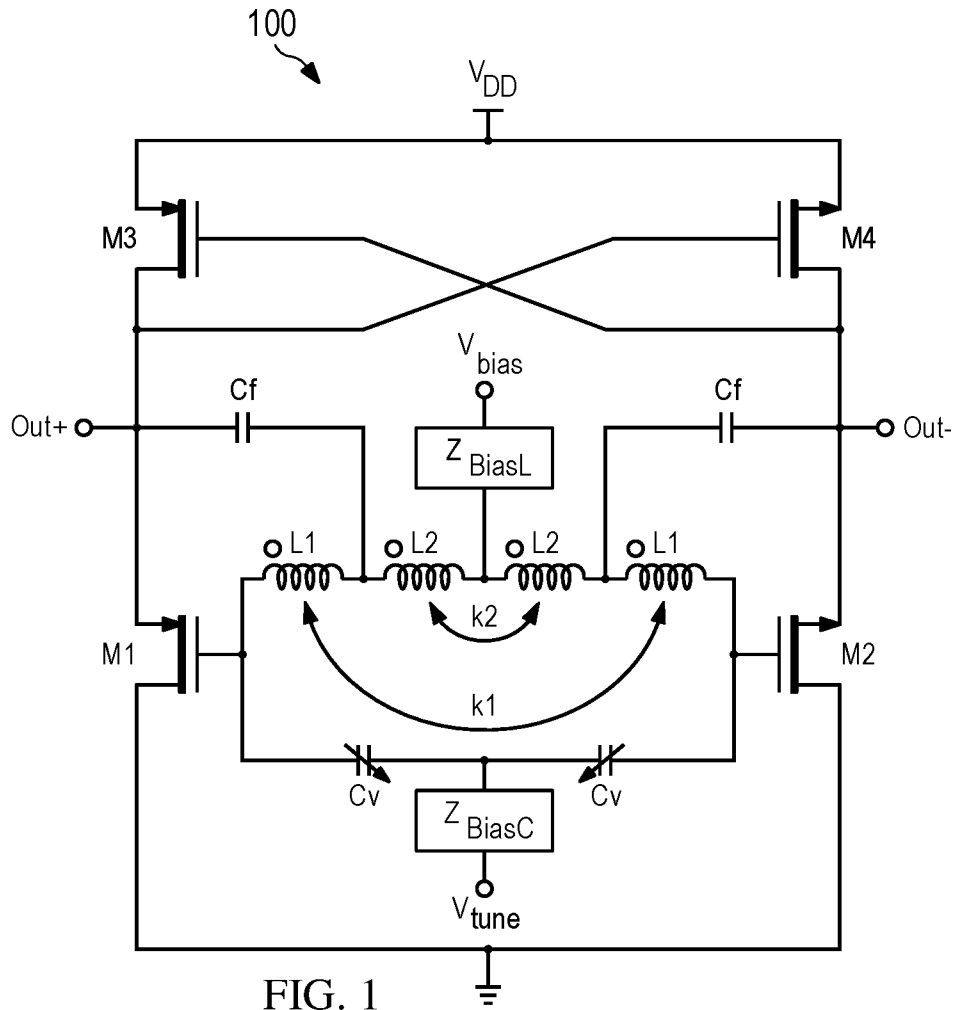
18. The non-transitory computer-readable medium of any one of claims 12-17, wherein the amplifier has a CMOS topology.

19. The non-transitory computer-readable medium of any one of claims 12-18, wherein the amplifier has a differential output.

20. The non-transitory computer-readable medium of any one of claims 12-19, wherein the amplifier has a single ended output.

21. The non-transitory computer-readable medium of any one of claims 12-20, wherein the physical loop is symmetrically shaped.

22. The non-transitory computer-readable medium of any one of claims 12-21, wherein the physical loop has a substantially octagonal shape.



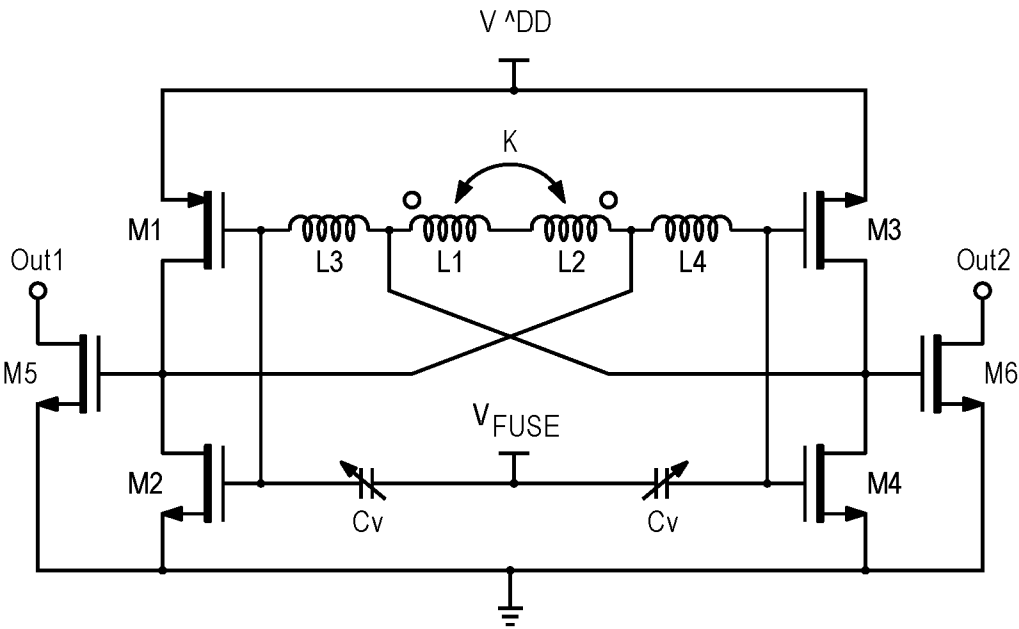


FIG. 3A
(PRIOR ART)

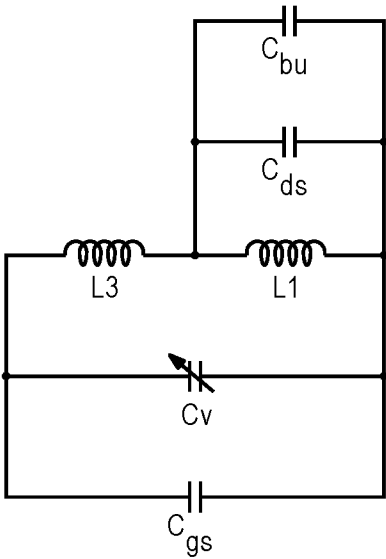


FIG. 3B
(PRIOR ART)

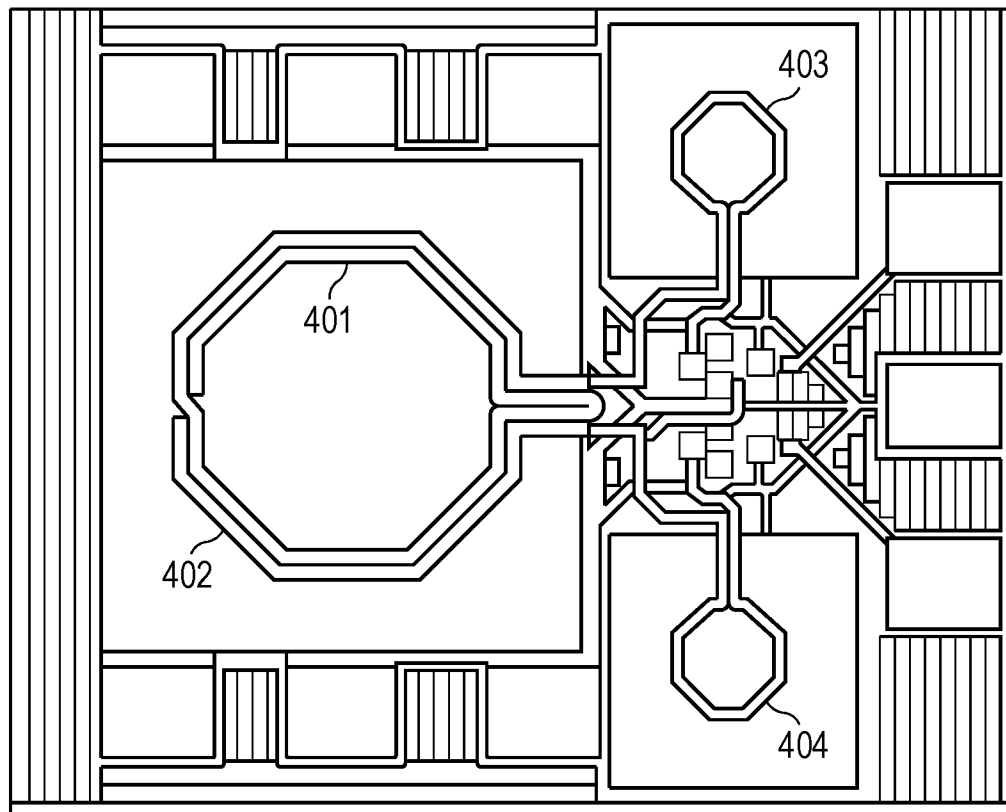


FIG. 4
(PRIOR ART)

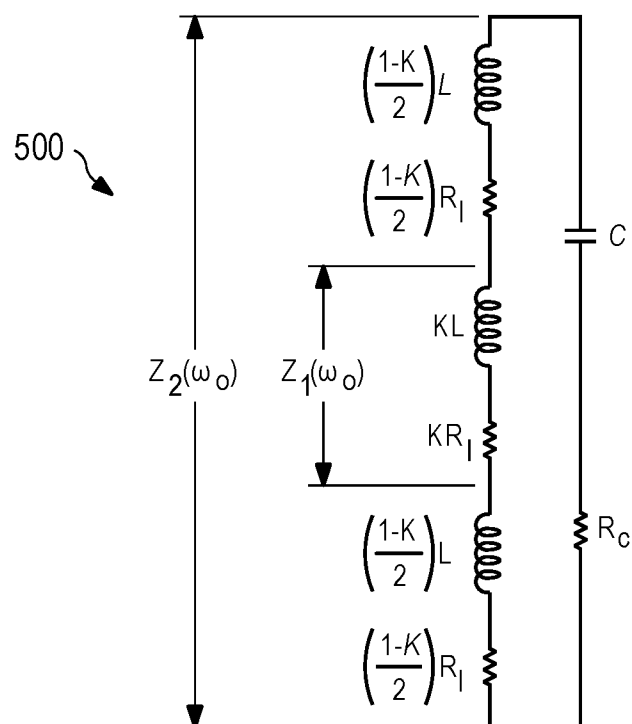


FIG. 5

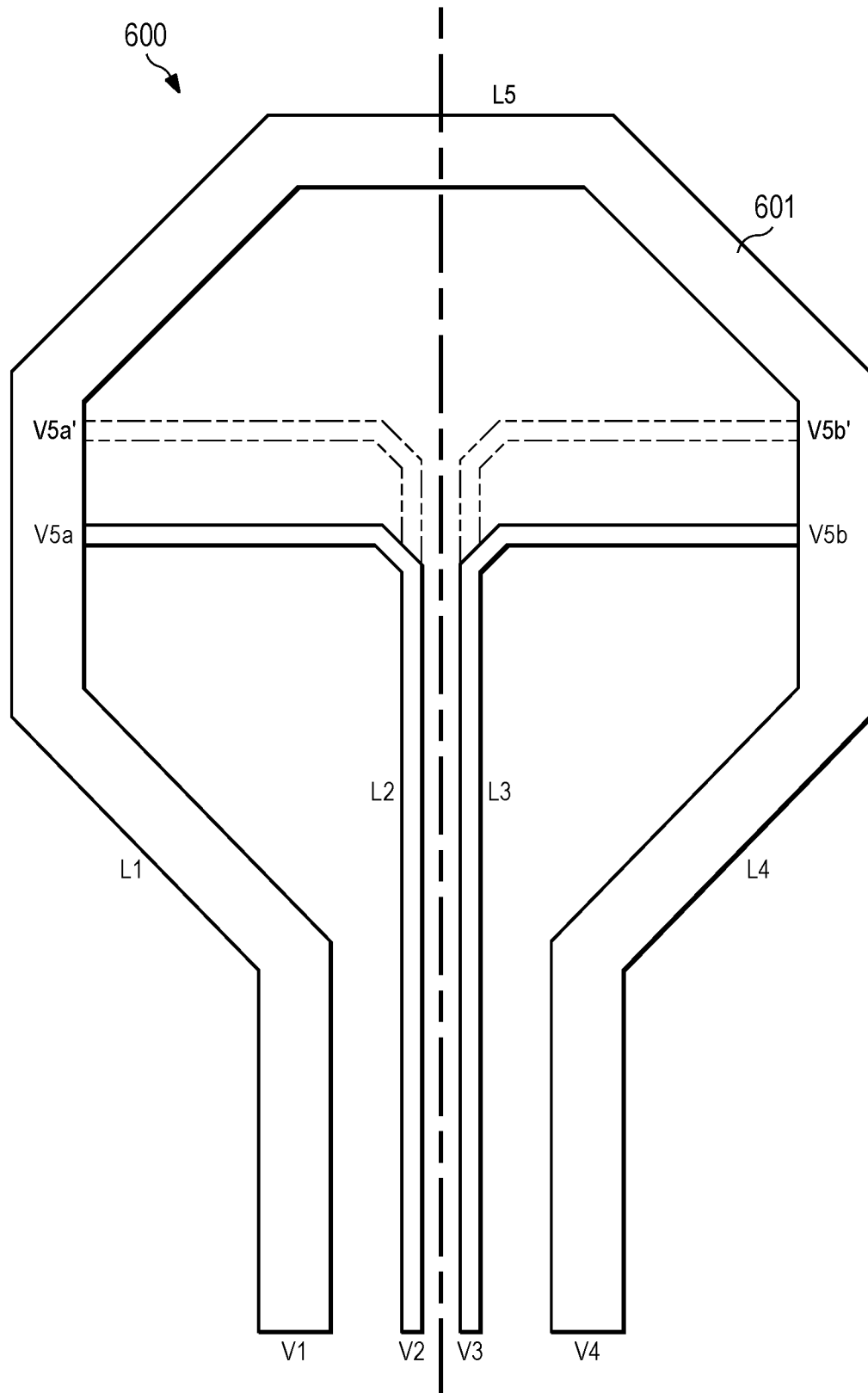


FIG. 6

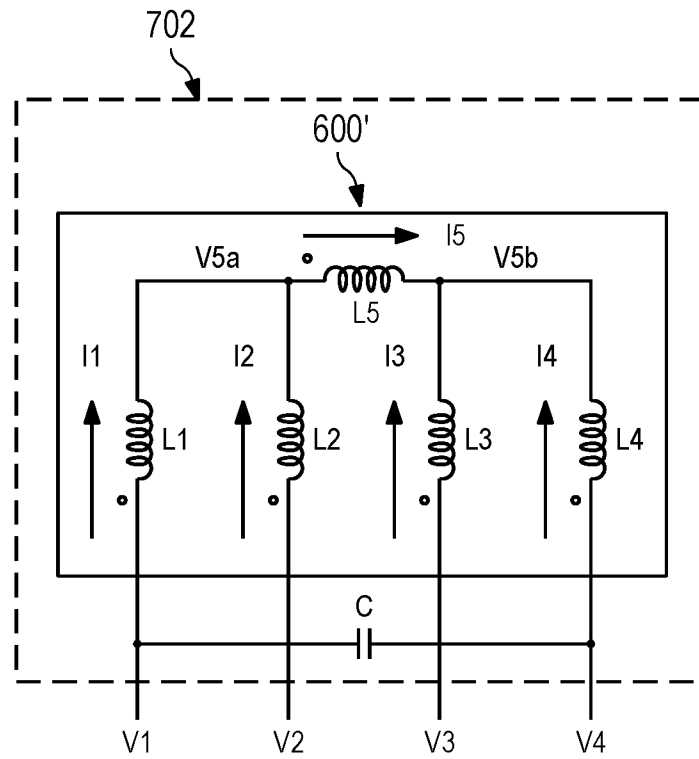


FIG. 7

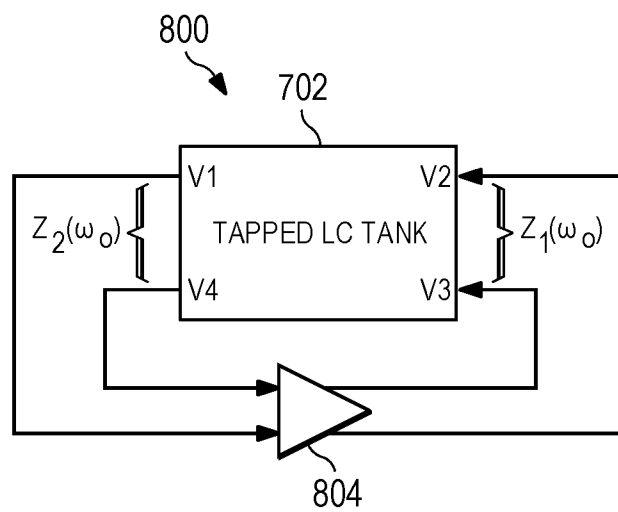


FIG. 8

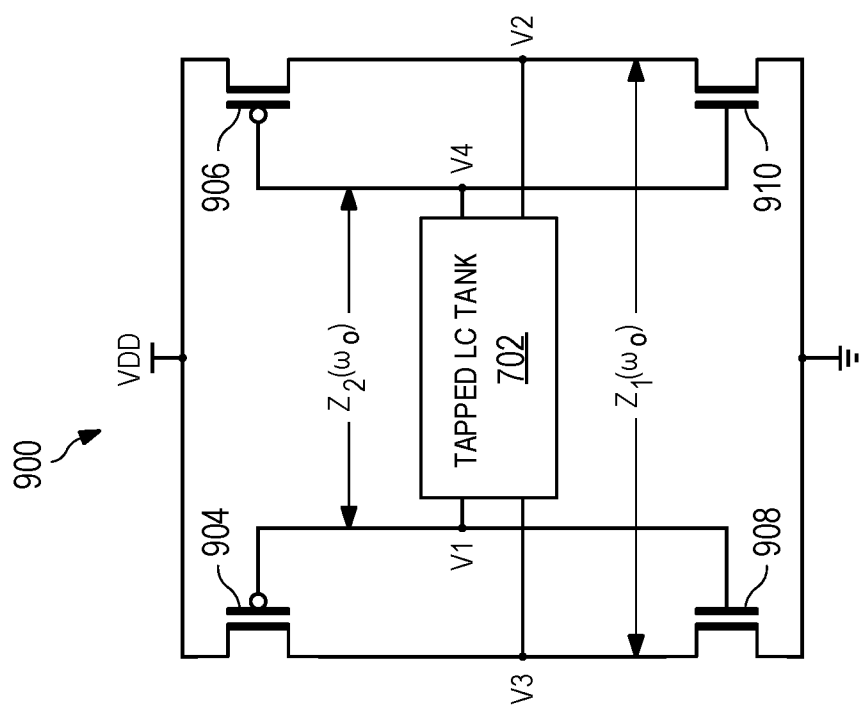


FIG. 9

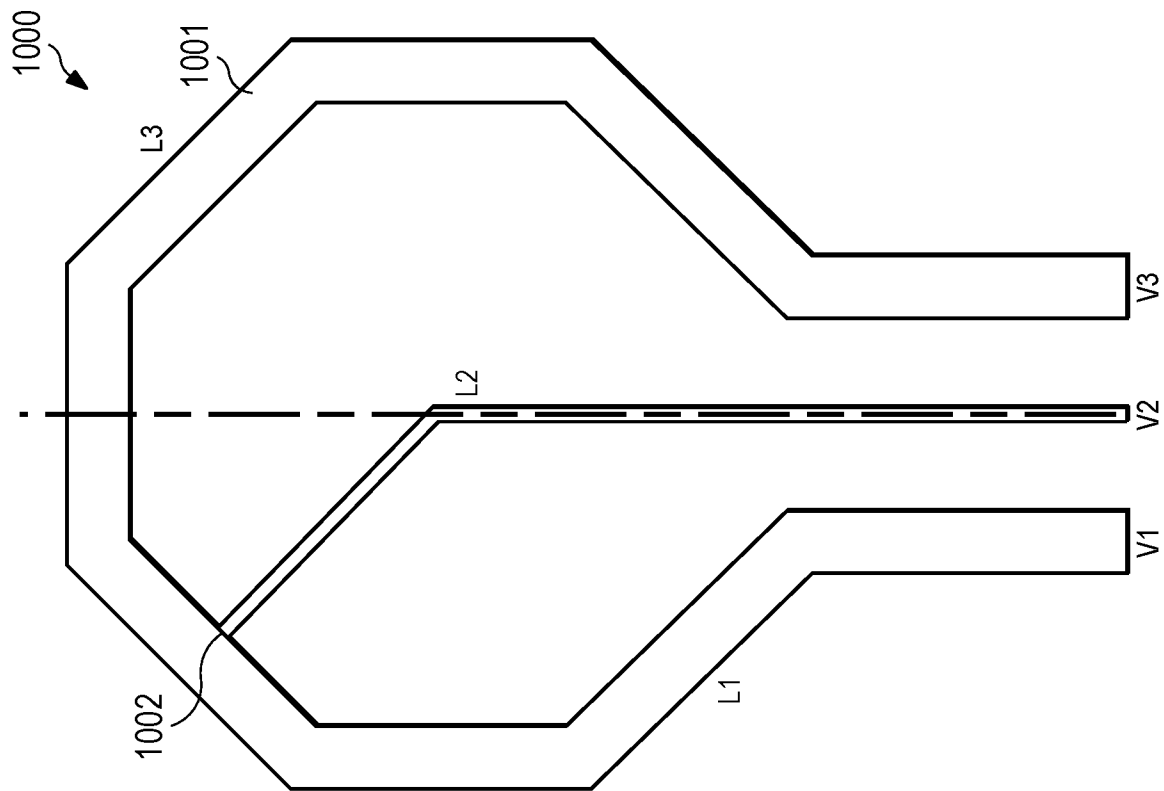


FIG. 10

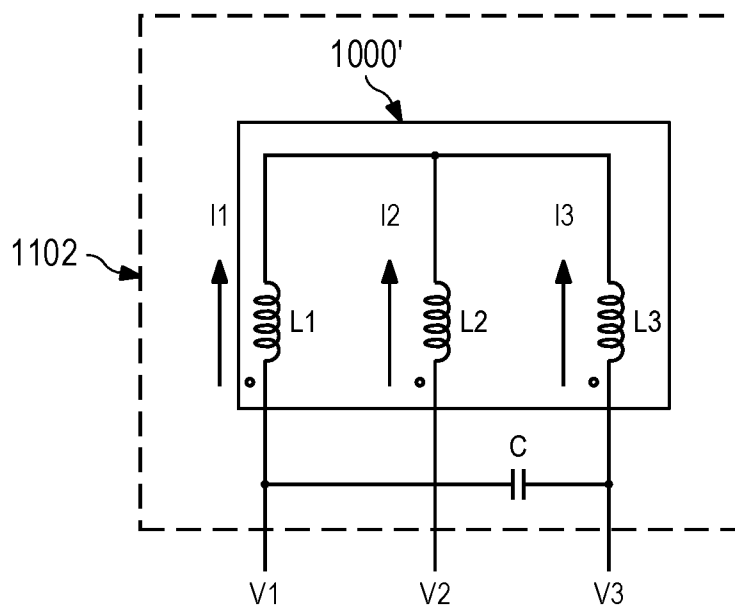


FIG. 11

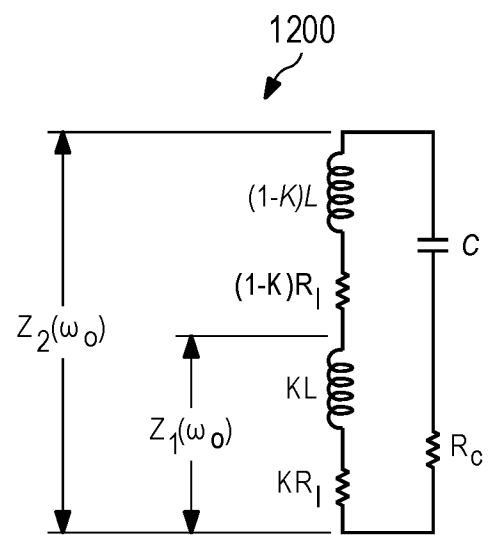


FIG. 12

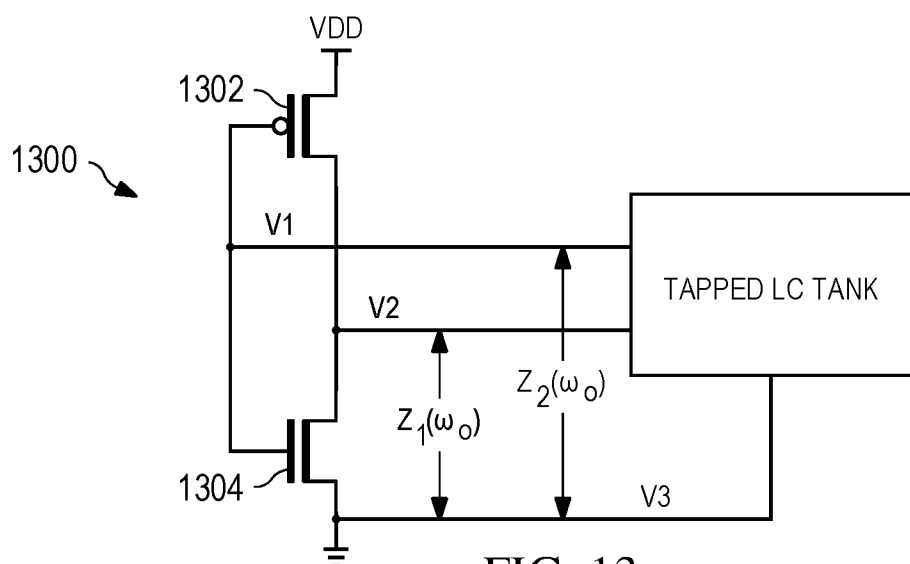


FIG. 13

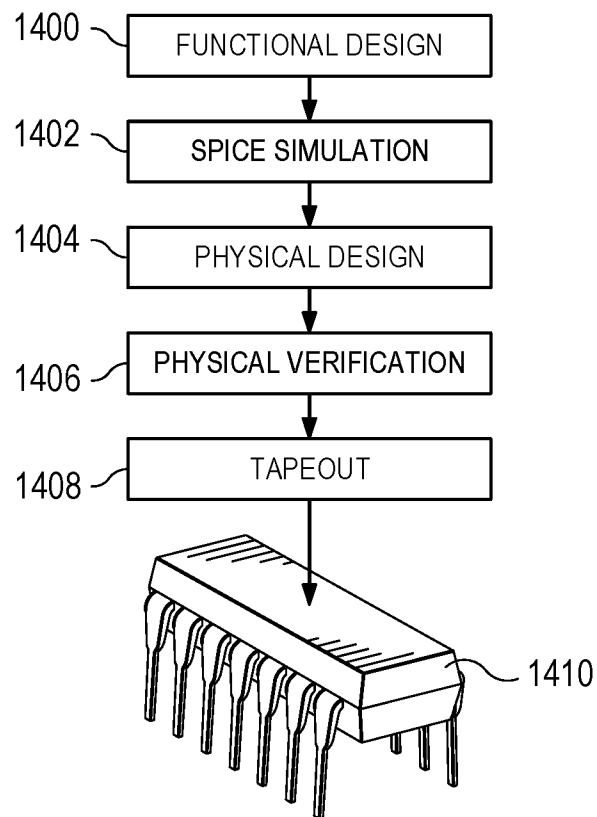


FIG. 14

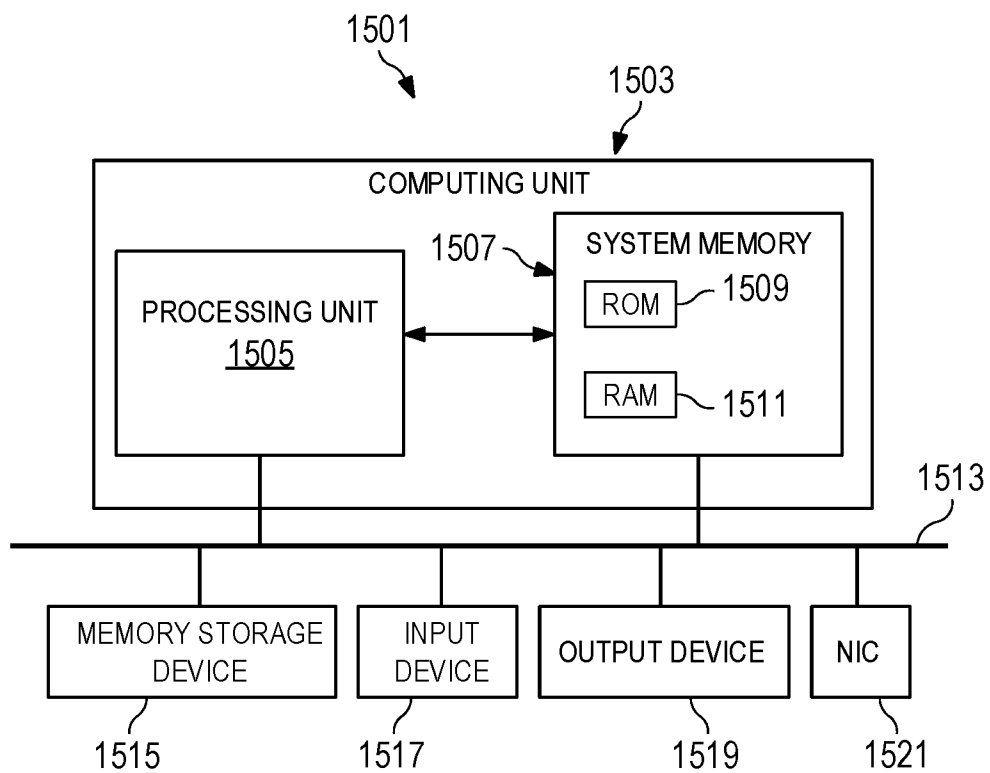


FIG. 15

INTERNATIONAL SEARCH REPORT

International application No.

PCT/CN2016/076499

A. CLASSIFICATION OF SUBJECT MATTER

H03B 5/12(2006.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

H03B

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

WPI, EPODOC, CNPAT, CNKI: oscillator, VCO, loop, amplifier, induct+, resonator, capacit+, segment?, impedance

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 2006033587 A1 (CABANILLAS, JOSE) 16 February 2006 (2006-02-16) description, paragraphs [0063]-[0070] and figures 8-9	1-22
A	CN 1889365 A (UNIV. EAST CHINA NORMAL) 03 January 2007 (2007-01-03) the whole document	1-22
A	CN 101409530 A (RUIYU SEMICONDUCTOR CO., LTD.) 15 April 2009 (2009-04-15) the whole document	1-22
A	CN 101867345 A (CHINESE ACAD SCI. INST. SEMICONDUCTORS) 20 October 2010 (2010-10-20) the whole document	1-22
A	US 2014159825 A1 (TEXAS INSTRUMENTS INC.) 12 June 2014 (2014-06-12) the whole document	1-22

☐ Further documents are listed in the continuation of Box C.☒ See patent family annex.

* Special categories of cited documents:

“A” document defining the general state of the art which is not considered to be of particular relevance

“E” earlier application or patent but published on or after the international filing date

“L” document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

“O” document referring to an oral disclosure, use, exhibition or other means

“P” document published prior to the international filing date but later than the priority date claimed

“T” later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

“X” document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

“Y” document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

“&” document member of the same patent family

Date of the actual completion of the international search

17 May 2016

Date of mailing of the international search report

01 June 2016

Name and mailing address of the ISA/CN

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Telephone No. (86-10)010-62413087

INTERNATIONAL SEARCH REPORT
Information on patent family members

International application No.

PCT/CN2016/076499

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US	2006033587	A1	16 February 2006	US	7154349	B2	26 December 2006
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				TW	I362175	B	11 April 2012
				IL	181231	D0	04 July 2007
				BR	PI0514232	A	03 June 2008
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				WO	2006020873	A1	23 February 2006
				KR	101003210	B1	21 December 2010
				TW	200703877	A	16 January 2007
				SG	129807	A1	20 March 2007
				SG	129807	B	31 August 2009
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CN	101409530	A	15 April 2009	CN	101409530	B	21 March 2012
CN	101867345	A	20 October 2010	None			
US	2014159825	A1	12 June 2014	None			