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(54) Curve approximating circuits

(57) A curve approximating circuit or log video amplifier includes a summing amplifier 45 and plural switches, D1, D2, D3, for coupling weighted inputs of the summing amplifier 45 either to a supplied input signal e_{in} or to corresponding ones of a plurality of constant voltages V_{c1}, V_{c2}, V_{c3}. The switches D1, D2, D3 are preferably formed of Schottky diodes and the constant voltages V_{c1}, V_{c2}, V_{c3} are preferably developed by plural voltage divider networks.

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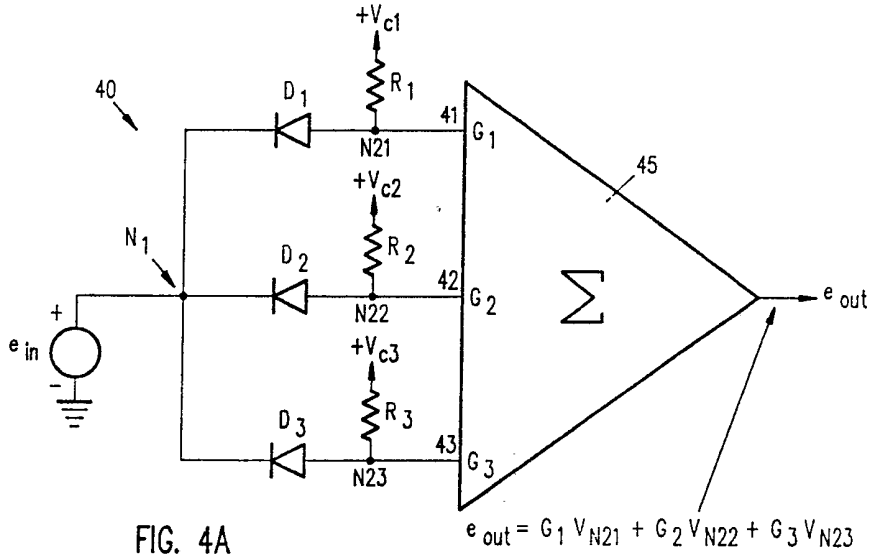

FIG. 4A

$e_{out} = G_1 V_{N21} + G_2 V_{N22} + G_3 V_{N23}$

At least one drawing originally filed was informal and the print reproduced here is taken from a later filed formal copy.

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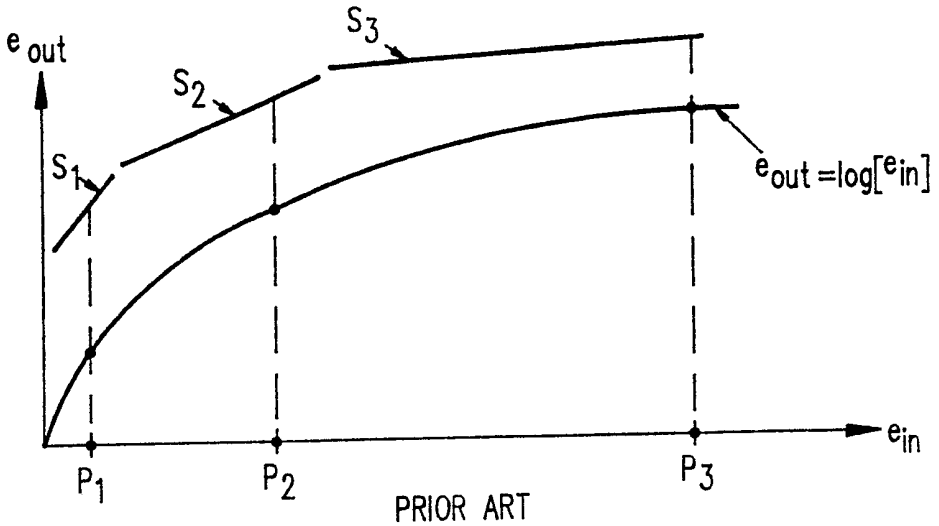
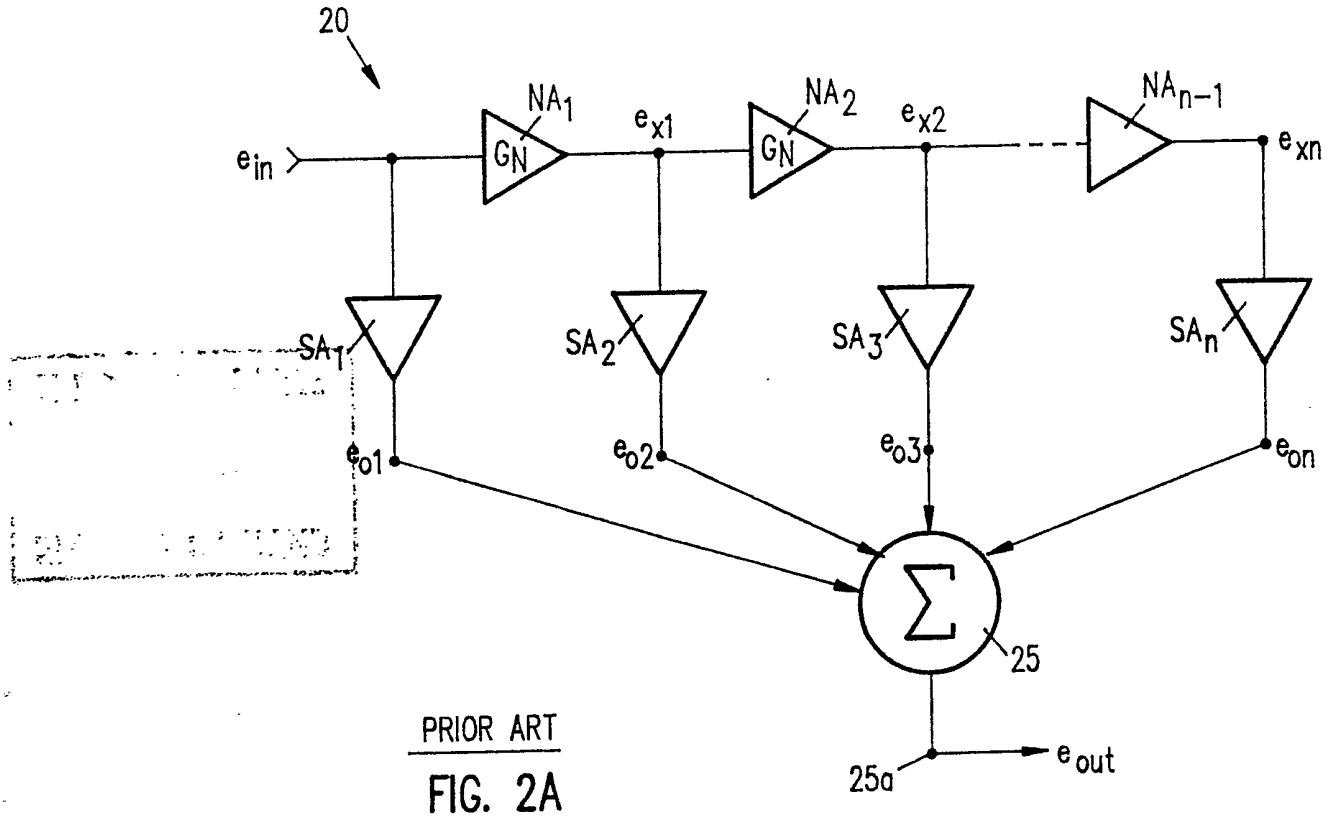


PRIOR ART

FIG. 1



PRIOR ART

FIG. 2A

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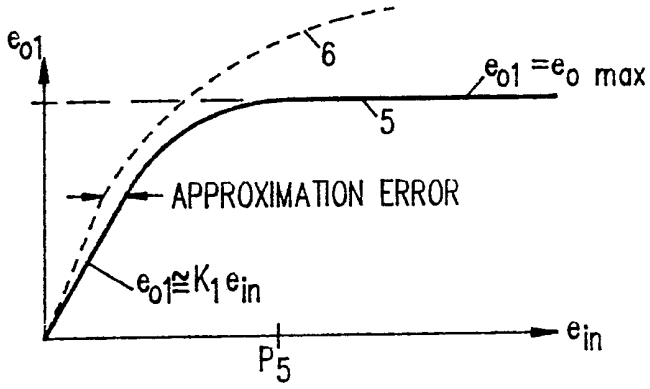
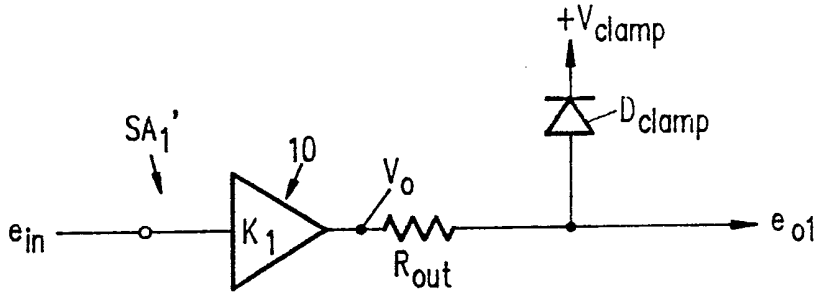


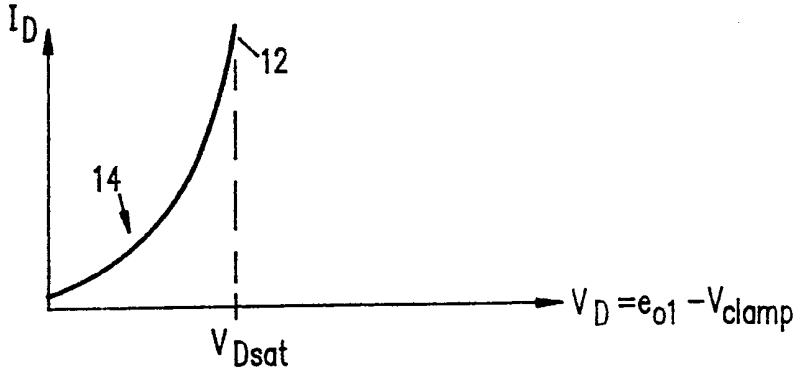
PRIOR ART

FIG. 2B



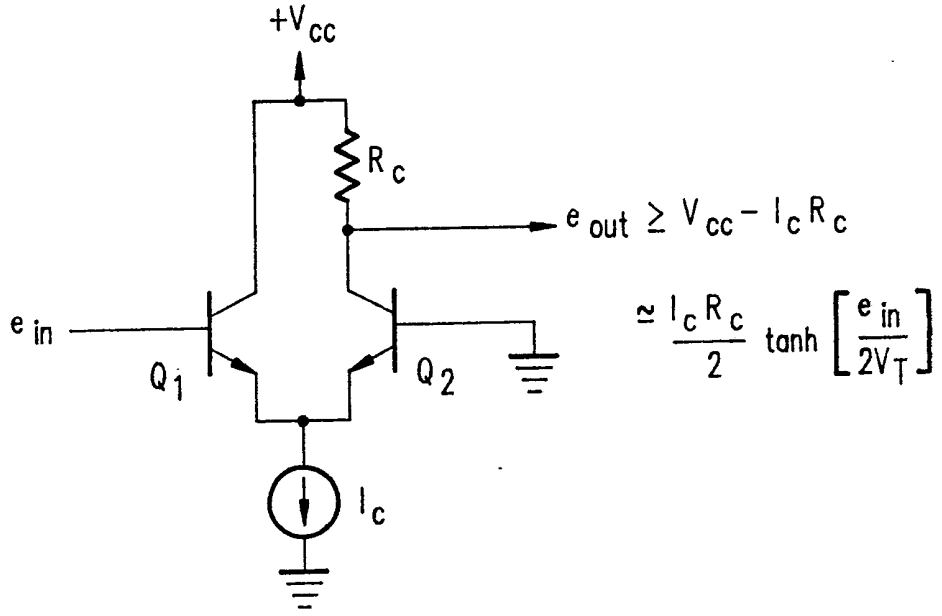
PRIOR ART

FIG. 2C



PRIOR ART

FIG. 2D



PRIOR ART

FIG. 2E

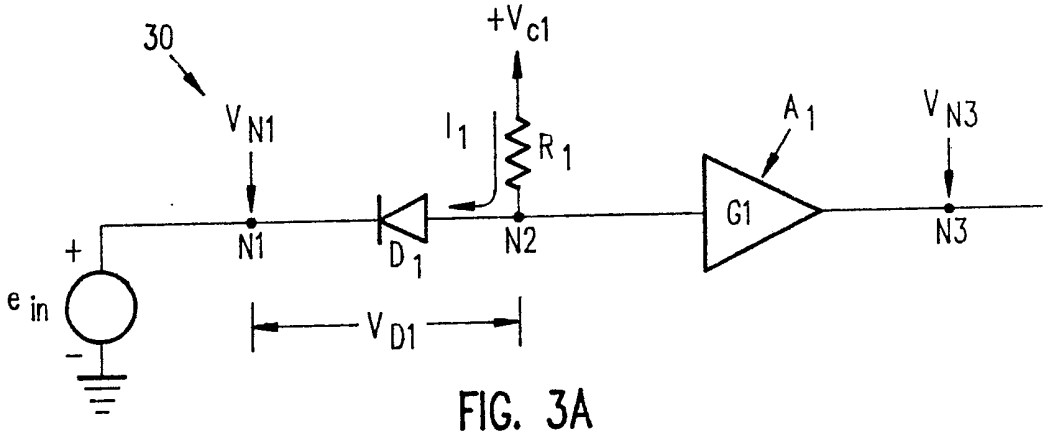


FIG. 3A

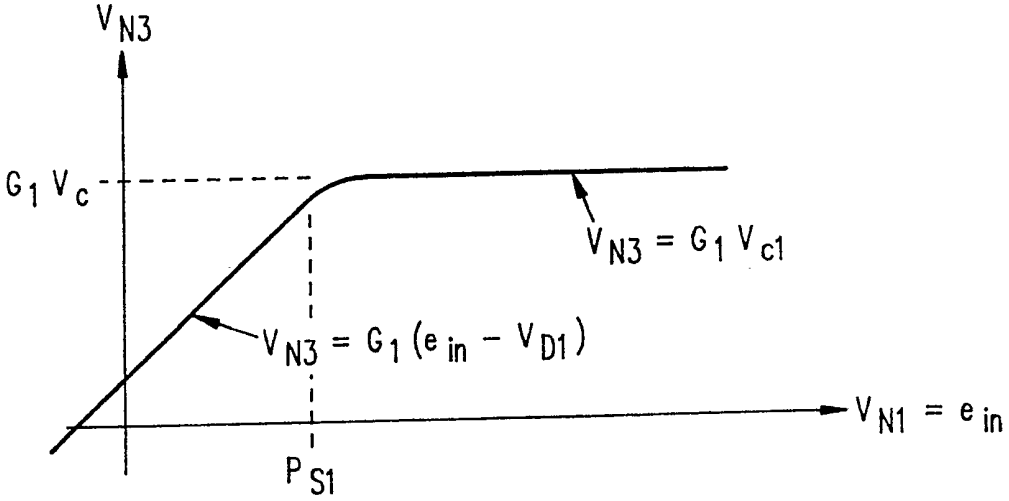


FIG. 3B

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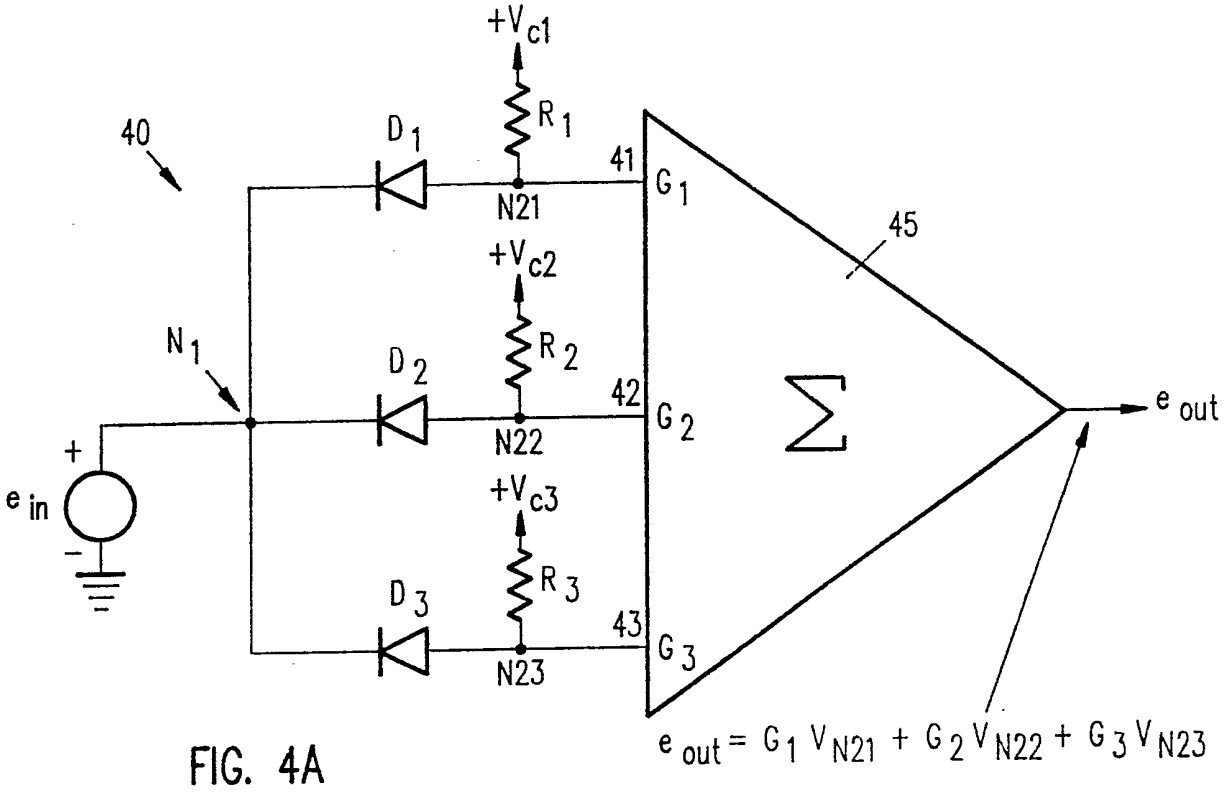

FIG. 4A

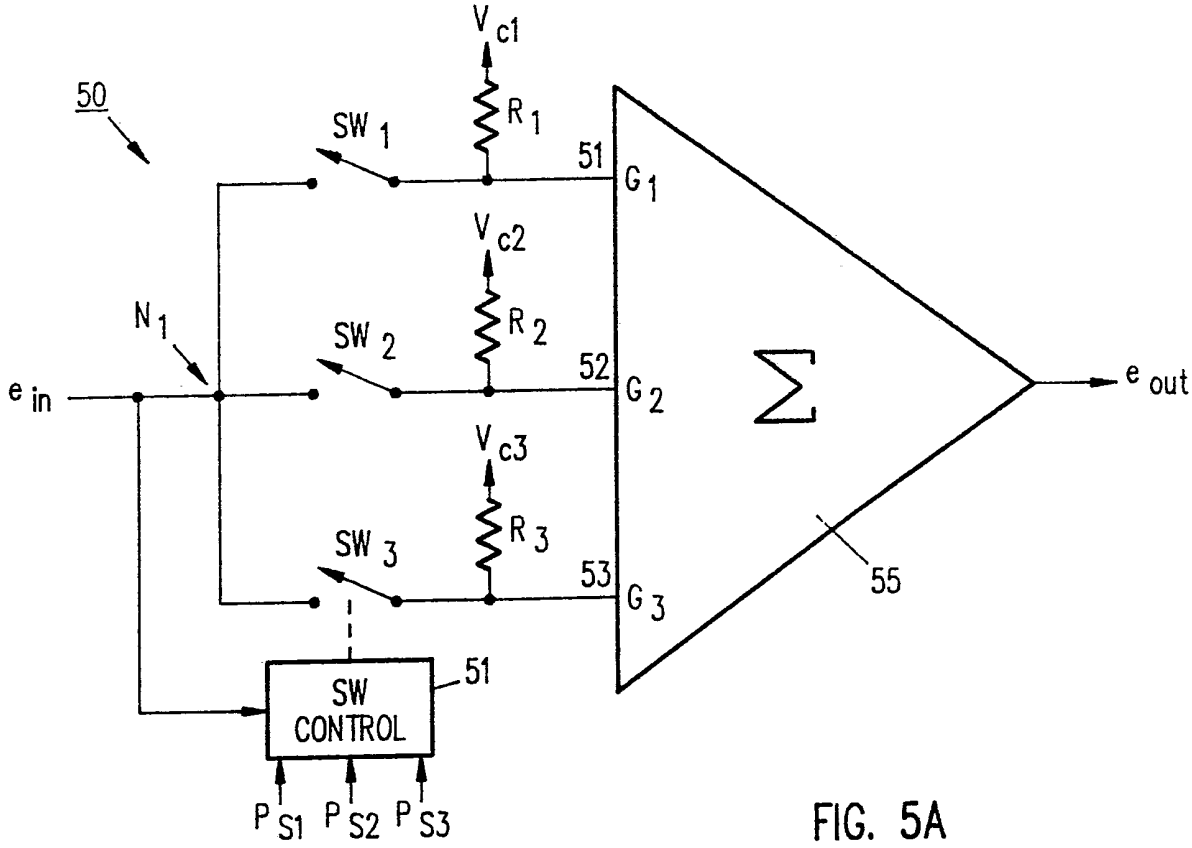

FIG. 5A

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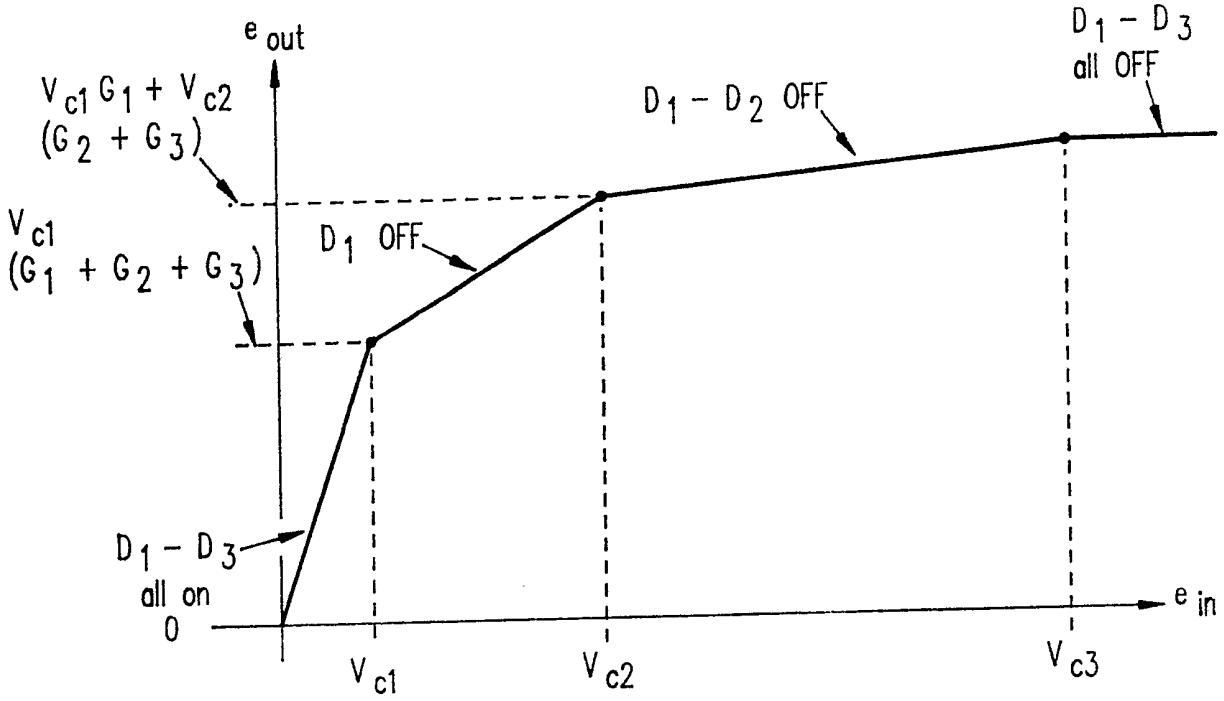

FIG. 4B

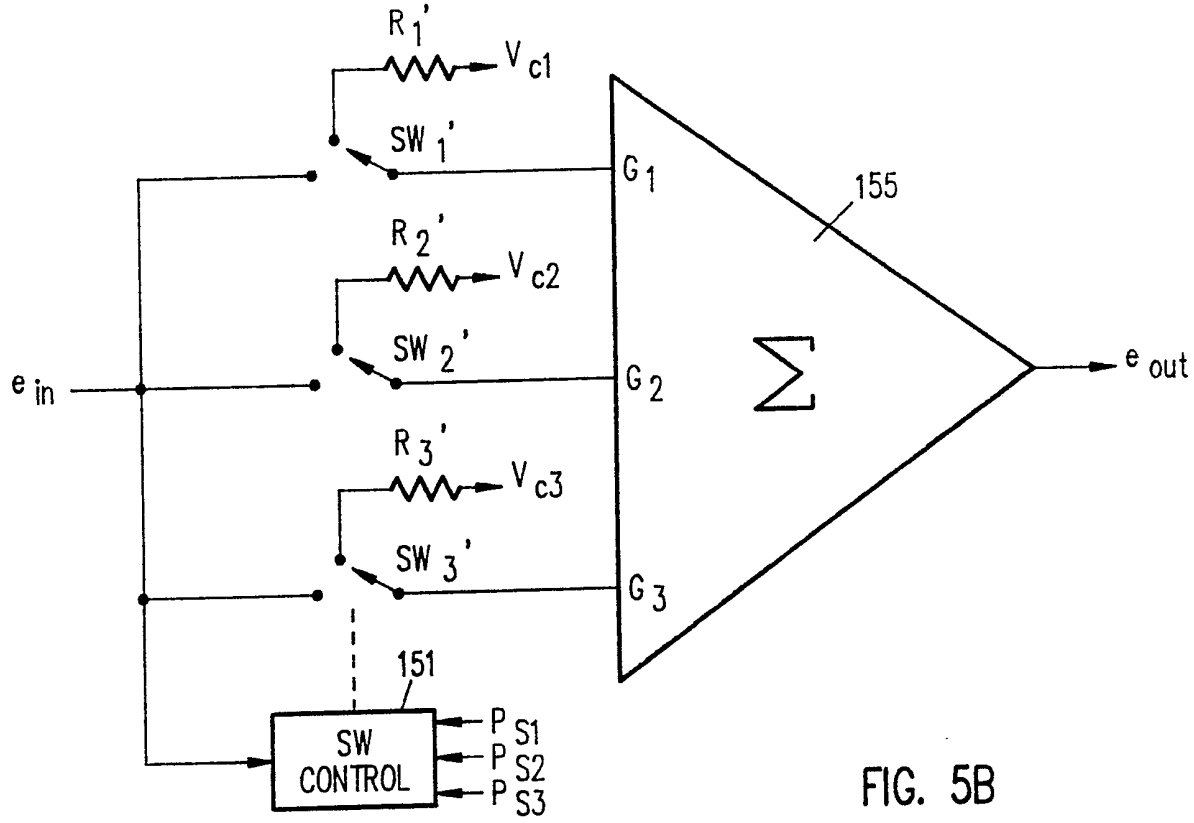

FIG. 5B

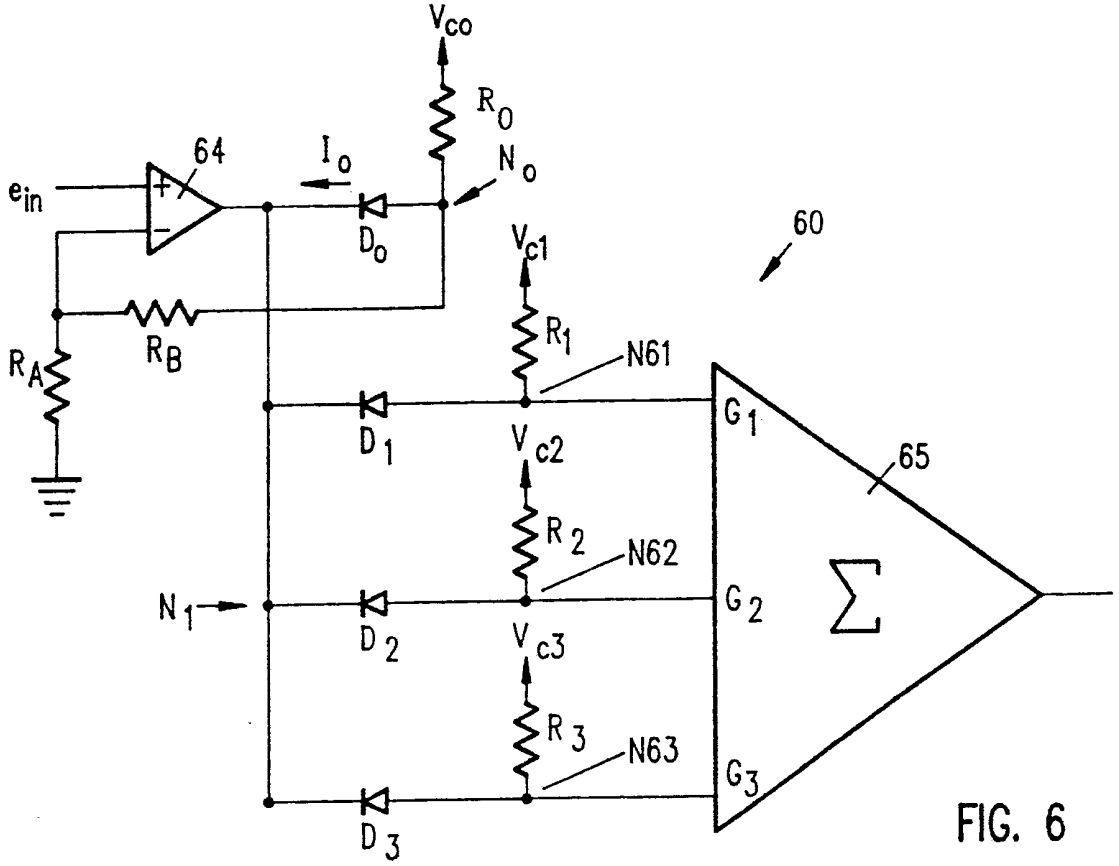
Vco
Ro
No
Io
64
ein
Do
60
Vc1
R1
N61
RA
RB
D1
G1
65
Vc2
R2
N62
N1
G2
D2
Vc3
R3
N63
G3
D3

FIG. 6

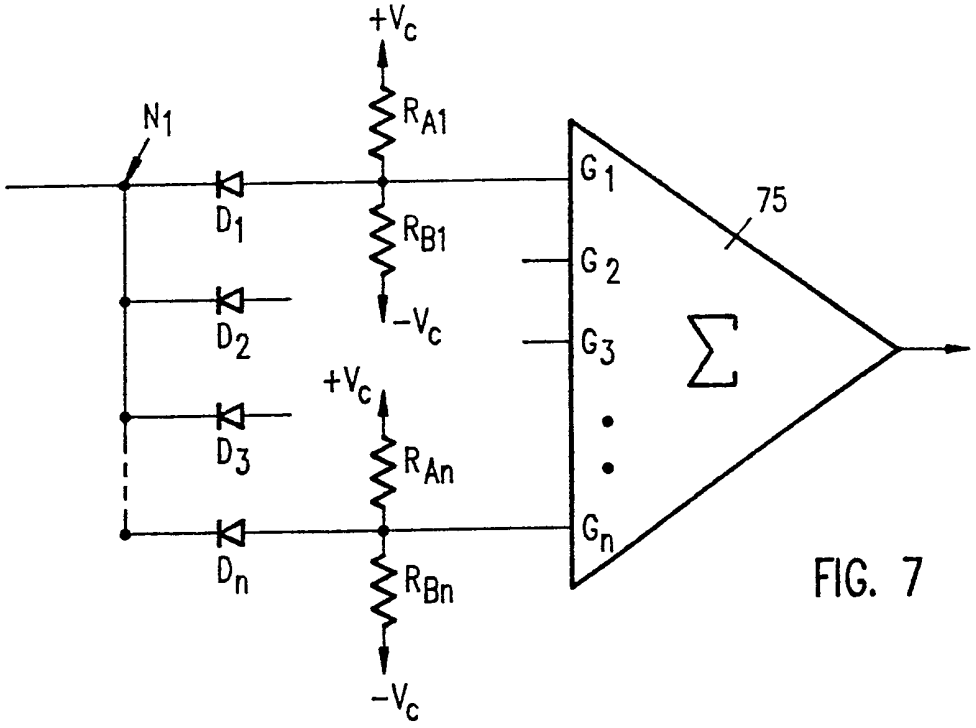
+Vc
RA1
N1
G1
75
D1
RB1
G2
D2
-Vc
G3
+Vc
D3
RAn
Gn
Dn
RBn
-Vc

FIG. 7

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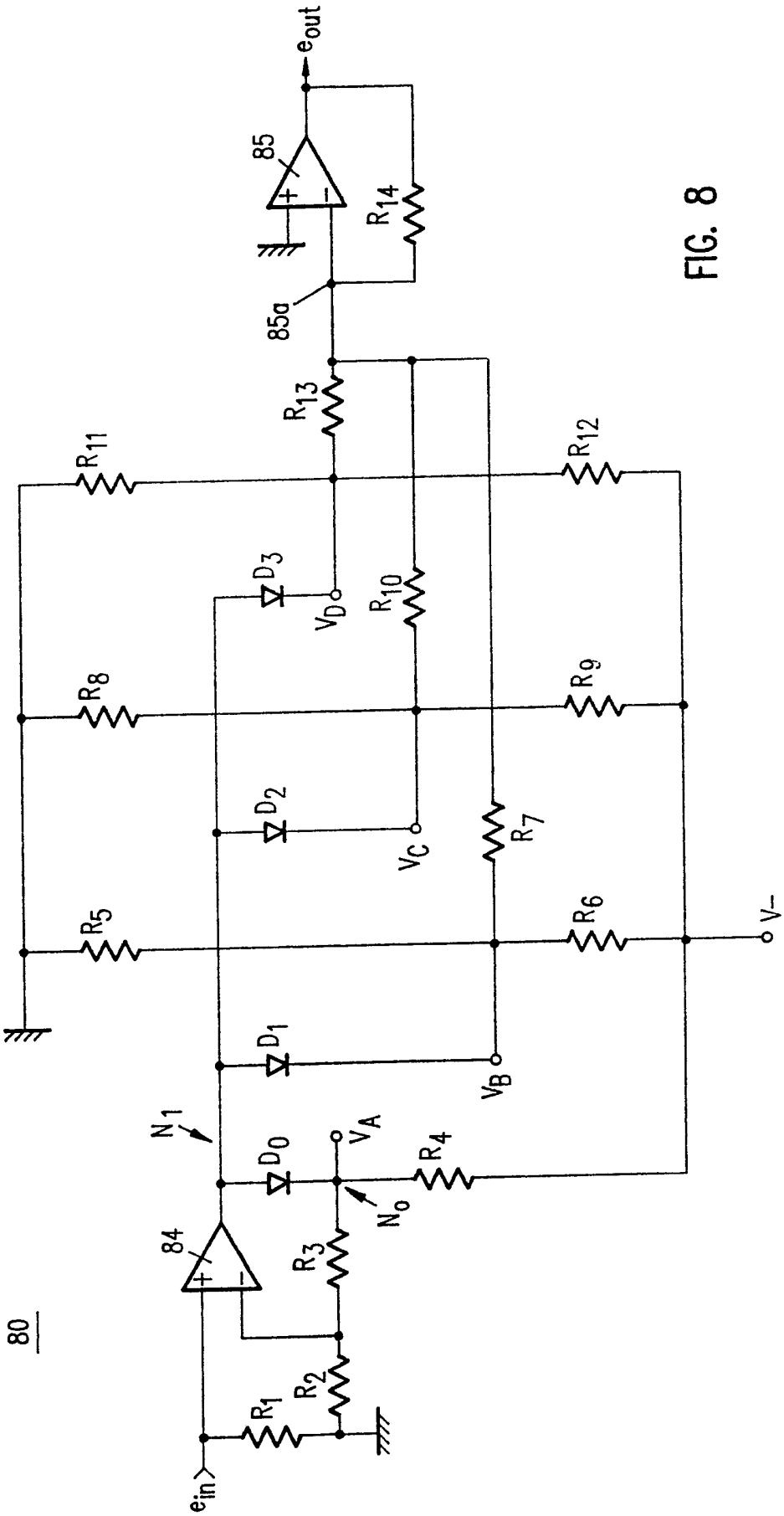


FIG. 8

CURVE APPROXIMATING CIRCUITS

DESCRIPTION

This invention relates to curve approximating circuits or logarithmic amplifiers, such as are used for dynamic range expansion in video frequency systems.

In many electronic circuits it is desirable to implement a non-linear or variable slope transfer function such as a logarithmic transfer function of the form $e_{out} = A_1 \log(e_{in})$, where e_{in} is an input voltage signal, e_{out} is an output voltage signal, and A_1 is an amplification constant. Such non-linear transfer functions are particularly useful for compressing and decompressing signals of wide dynamic range (e.g. 60dB) in telecommunication systems. Circuits which provide such transfer functions are sometimes referred to as log video amplifiers (LVA) because of their popularity in video frequency systems.

Reference is now made to Figures 1 and 2 of the accompanying drawings, in which:

Fig. 1 is a graph of a logarithmic transfer function,

Fig. 2A is a schematic diagram of a previous logarithmic circuit employing saturation-limited amplifiers,

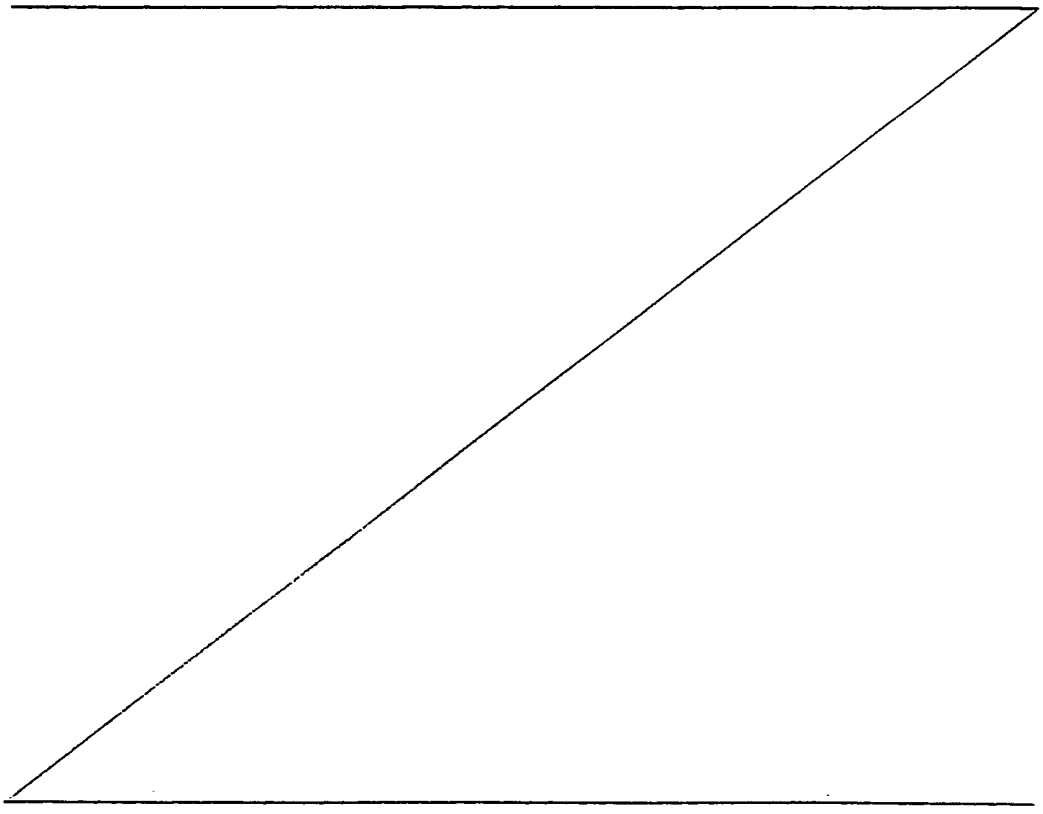
Fig. 2B is a graph of the transfer function of a previous saturation-limited amplifier,

Fig. 2C shows a saturation-limited amplifier comprising a diode clamping circuit,

Fig. 2D graphs the current versus voltage characteristics of a conventional clamping diode, and

Fig. 2E is a schematic of a differential amplifier sometimes used to form the saturation-limited amplifiers of Fig. 2A.

It can be seen, by referring to the logarithmic curve shown in Fig. 1, that the output signal versus input signal derivative, or slope, of the curve $e_{out} = \log(e_{in})$ decreases monotonically as the input voltage e_{in} increases. This means that the small signal gain $d(e_{out})/d(e_{in})$ of a circuit implementing the logarithmic transfer function (or other variable slope function) needs to change with input signal level. It is common practice to approximate variable slope curves of this nature by using a multiple section approximating circuit 20, such as shown in Fig. 2A. The multiple section approximating circuit 20 comprises a plurality of saturation-limited amplifiers SA_1, SA_2, SA_3, ..., SA_n, a voltage summing means 25 for summing



respective output signals e_{o1}, e_{o2}, e_{o3}, . . ., e_{on} of the saturation-limited amplifiers SA_1-SA_n, and a plurality of nonsaturable amplifiers NA_1, NA_2, . . . NA_{n-1} connected in series between input nodes of the saturation-limited amplifiers. The input voltage signal e_{in} is presented to the input node of the first saturation-limited amplifier SA_1 while a once amplified version of the input signal $e_{x1} = G_N e_{in}$ appears at the input node of the second saturation-limited amplifier SA_2, a twice amplified version of the input signal $e_{x2} = G_N^2 e_{in}$ appears at the input node of the third saturation-limited amplifier SA_3, and eventually, an (n-1) times amplified version of the input signal $e_{xn-1} = G_N^{(n-1)} e_{in}$ appears at the input node of the last saturation limited amplifier SA_n, amplification factor G_N here being the gain of nonsaturable amplifiers NA_1, NA_2, . . ., NA_{n-1}.

The saturation-limited amplifiers SA_1-SA_n each have an input/output characteristic curve 5 such as shown in Fig. 2B wherein the output signal e_{o1} of amplifier SA_1 for example, increases as a linear ramp function $e_{o1}=k_1 e_{in}$ while the input signal e_{in} is relatively small and then, at some saturation-limiting point P_s along the input scale, the magnitude of the output signal e_{o1} asymptotically flattens out towards a maximum level e_{max} as the magnitude of the input signal e_{in} is further increased. This type of curve 5 can be used to approximate a section of a log curve 6 to a maximum allowable approximation error as indicated by the separation between solid curve 5 and dash-dot curve 6 in Fig. 2B. Nonsaturable amplifiers NA_1-NA_{n-1} have linear ramp-like characteristics over the full range of input signal e_{in}.

Figure 2C illustrates one circuit SA' for implementing the saturation-limited amplifiers SA_1-SA_n. A first terminal of a clamping diode D_{clamp} is coupled to a low resistance output R_{out} (e.g. 4 ohms) of a linear amplifier 10 having a gain K_1. The circuit SA' is arranged in a manner which causes the diode D_{clamp} to be forward biased and driven into a saturated portion 12 (Figure 2D) of its current versus voltage characteristic curve 14 whenever the amplifier

output voltage V_0 exceeds a clamping voltage V_{clamp} provided at a second terminal of the diode D_{clamp}. The output resistance R_{out} is chosen sufficiently small so that its presence is negligible for low level outputs $V_o << V_{clamp}$ but sufficiently high such that the clamping diode D_{clamp} will be protected from burn out when high level output signals $V_o > V_{clamp}$ are developed.

The operation of diode based circuits such as SA' of Fig. 2C may be undesirably affected by an inherent temperature sensitivity characteristic of the clamping diode D_{clamp}, which is particularly pronounced near saturation, and by the inability of the diode D_{clamp} to quickly come out of saturation (recovery time) when the output voltage V_0 suddenly jumps from a level well above the clamping voltage, $V_o >> V_{clamp}$, to a level below the clamping voltage, $V_o < V_{clamp}$. The so-called recovery time of the clamping diode D_{clamp} tends to increase as the diode is driven further into saturation. Also the usable dynamic range of circuit SA' is generally limited to 6 db (for ±0.3 db approximation error) when approximating the log curve 6 (Fig. 2B).

Referring back to Fig. 1, it should be understood that if a 60 db dynamic range is desired, ten stages SA_1-SA_{10} of the SA' configuration would be required. Also it should be understood that when the input voltage signal e_{in} of circuit 20 is relatively small, all the saturation-limited amplifiers SA_1 - SA_n are expected to be operating in linear portions of their respective transfer curves so that the cumulative slope, $S_1 = d(e_{o1} + e_{o2} + e_{o3} + \ldots + e_{on})/d(e_{in})$ of the summed output signal, $e_{out} = e_{01} + e_{02} + \ldots + e_{on}$, is relatively steep at a first point P_1 along the abscissa of the Fig. 1 plot. As the magnitude of the input voltage signal e_{in} increases to a second point P_2, the n-1 times amplified input signal e_{xn} presented to the last saturation-limited amplifier SA_n forces that amplifier SA_n to clamp into a saturation mode. The corresponding slope term $d(e_{on})/d(e_{in})$ contributed to the total output gain $d(e_{out})/d(e_{in})$ by the last output signal e_{on} approaches zero

and a second, less steep slope $S_2 = d(e_{o1} + e_{o2} + \ldots + e_{on-1})/d(e_{in})$ results at second point P_2. When the magnitude of the input voltage signal e_{in} increases to yet a third point P_3, the next to last saturation-limited amplifier, e.g. SA_3, goes into a saturation mode and this further decreases the slope or small signal gain of the circuit 20. Eventually the first saturation-limited amplifier SA_1 of the series SA_1 - SA_n is also driven into a saturation mode and the slope $d(e_{out})/d(e_{in})$ flattens out to zero. A reverse process, of progressive increases in circuit gain, takes place when the magnitude of the input voltage signal e_{in} decreases past points P_3, P_2 and P_1.

The multiple section circuit 20 of Fig. 2A has a number of disadvantages, most notable of which is a requirement for a large number of amplifiers. Whenever further slope approximating steps, e.g., slopes S_4, S_5, . . . , are desired for the purpose of decreasing the approximation error and/or increasing the total dynamic range of the approximating circuit 20, the addition of individual saturation-limited amplifiers, e.g., SA_{n+1}, SA_{n+2}, . . . and nonsaturable amplifiers, e.g., NA_n, NA_{n+1}, . . . on a two amplifiers per step basis is required for each additional slope approximating step desired. This two-for-one amplifiers per step increase disadvantageously adds to the cost and complexity of the approximating circuit 20. It further exacerbates a signal propagation delay problem which is already inherent in the multiple section approximating circuit 20. The serial topology of nonsaturable amplifiers NA_1 through NA_{n-1} mandates that low level input signals (non-saturating signals) propagate through the summed time delays of all the nonsaturable amplifier stages NA_1-NA_{n-1} before a valid summed output signal e_{out} can be developed at output node 25a of the summing means 25. This additive type of time delay disadvantageously reduces the rise time of the summed output signal e_{out}. The delay due to the low level signal propagation problem is particularly annoying when the circuit 20 must handle very small but very fast changing input signals e_{in} such as may occur in video systems. The

serial ganging of amplifiers NA_1 - NA_{n-1} also disadvantageously acts to narrow the overall bandwidth of the system with respect to low level, high-frequency input signals. A bandwidth constriction effect is known to occur when multiple amplifiers having identical structures are strung together in serial fashion. Yet another problem associated with low level signals is that of adjusting the zero points of saturation-limited amplifiers SA_1-SA_n and non-saturable amplifiers NA_1-NA_{n-1} so all the amplifiers will produce zero level output signals e_{01}-e_{0n} simultaneously when the input signal e_{in} is at a zero level (zero offset adjustment problem).

At the other end of the input scale, where relatively large but again very fast changing input signals (saturating signals) e_{in} are presented (for example, input signals having step-like waveforms of large magnitude and steep falling edges), the response time of circuit 20 is limited by the time it takes for saturation-limited amplifiers SA_1-SA_n to recover out of saturation. The recovery time of each saturation-limited amplifier may be defined as the time needed to recover out of saturation and reenter the linear portion of its operating curve. This recovery time tends to increase as the amplifier is driven deeper and deeper into saturation. The last saturation-limited amplifier SA_n which receives the n-1 times amplified input signal $e_{nx} = G_N^{(n-1)}e_{in}$ will tend to be driven far more heavily into saturation than will front end amplifiers SA_2 or SA_1. As such the last amplifier SA_n will have the most difficulty in coming out of saturation when the input signal e_{in} shifts rapidly from a relatively high level to a relatively low level. This saturation recovery phenomenon can significantly limit the usable frequency range of the multiple section approximating circuit 20.

In cases where the circuit 20 is to operate with high frequency signals, such as present in video processing circuits (DC-20MH_z), all the amplifiers SA_1-SA_n and NA_1-NA_{n-1} need to be of a very high frequency variety (bandwidths > 20 MH_z) in order to compensate for the above-

described low level signal propagation problem and the high level saturation recovery problem. When this high frequency requirement is placed on all the amplifiers of circuit 20, it can greatly increase the cost and complexity of the overall circuit.

The multiple section circuit 20 of Figure 2A is sometimes referred to, when it is formed with amplifiers SA_1 - SA_n each having a diode clamped circuit configuration such as shown in Figure 2C, as a linear-limited log video amplifier circuit. Another circuit, referred to as a non-linear log amplifier, is disclosed in a book by Richard Smith Hughes, "Logarithmic Amplification", Artech House, 1986. The latter circuit is often used in place of the linear-limited log circuit for implementing logarithmic transfer functions. The non-linear log circuit utilizes differential amplifiers with constant current sources such as shown in Figure 2E in place of clamping diodes for limiting output voltage in a saturation-like manner. The advantages of such non-linear limiting circuits is that they can offer a greater dynamic range than diode clamping circuits (usually 13 db per stage for ±0.3 db error versus the 6 db range per stage of diode clamped circuit) and they can be designed to overcome the saturation recovery problem of clamping diodes as well as the need for larger number of stages. But the non-linear log amplifier circuits generally suffer from severe temperature instability (e.g. changes in gain and saturation knee point relative to temperature), problems with accurate alignment of knee points of multiple stages along a desired transfer function curve, and more importantly, they don't overcome the small signal propagation delay problem associated with serial ganging of video stages.

A third circuit for realizing the log transfer function uses multiple RF detectors coupled to tap points of a multiple stage microwave amplifier. The third circuit is often referred to either as an RFDLVA (radio frequency detector log video amplifier) or a successive detection LVA. While the RFDLVA may offer improved rise time

response, its primary disadvantages are linearity, cost, complexity and temperature sensitivity.

In accordance with the present invention, a logarithmic amplifier or other transfer function approximating circuit comprises a plurality of voltage dividers each formed of first and second resistive elements joined at a voltage generating node so as to produce different constant voltage levels at respective voltage generating nodes when no currents are supplied from other elements of the circuit to the voltage generating nodes. A plurality of level triggered switches, e.g. switching diodes, are each connected to respective ones of the voltage generating nodes so as to couple a voltage changing current to each of the nodes when the corresponding switch is closed (switching diode is forward biased) and to not couple a voltage changing current to the node when the switch is open (switching diode is reverse biased).

Each of the switches (or switching diodes) has a first terminal connected to its respective voltage generating node and a second terminal connected to the other switches at a common input node. As the magnitude of an input voltage supplied to the common input node changes, some of the switches (switching diodes) may be rendered non-conductive (reverse biased) because the input voltage causes the switches (diodes) to be triggered open (switched OFF) and other of the switches (switching diodes) may be rendered conductive (forward biased) because the input voltage causes them to be triggered closed (switched ON). As a result of

this action, the input voltage appears (ignoring minor voltage drops of closed switches) at the voltage generating nodes of the switches (diodes) that are switched ON (conductive) and the different constant voltages appear at the voltage generating nodes of the switches (diodes) that are switched OFF (nonconductive).

The voltage levels appearing at the plural voltage generating nodes, be they constant or input signal dependent, are passed through attenuation networks or amplifier input networks of preferably differing attenuation/amplification factors, and summed to produce a summed output voltage at an output node.

A different number of switches (diodes) will be switched ON or OFF as the input signal changes in magnitude. The small signal gain of the system will accordingly change in response to changes in the input signal magnitude because the constant voltages that appear at the voltage generating nodes of those of the switches (diodes) that open (become nonconductive) in response to a change in input signal magnitude will contribute only a zero term to the small signal gain of the system.

A transfer function of continuously decreasing slope with respect to increasing input signal magnitude may be obtained by suitably arranging the switches/diodes to become nonconductive in sequence so that the slope contribution of their corresponding voltage generating nodes sequentially converge toward zero. Only one summing amplifier with plural input terminals is needed for summing the constant or input signal dependent voltages developed at multiple voltage generating nodes. The problems of adding more approximating steps to the circuit transfer function, avoiding small signal propagation delay and/or minimizing large signal saturation recovery are obviated. A simple solution to the problem of approximating a multiple slope transfer function is made possible.

The present invention thus provides a curve approximating circuit of substantially simpler construction and of improved performance than prior art circuits. The invention avoids the saturation recovery problem of the prior art clamping diode system, and overcomes the time delay and bandwidth constriction problems associated with serially ganged amplifiers.

The invention is further described below, by way of example, with reference to the remaining Figures of the accompanying drawings, in which:

Fig. 3A is a schematic diagram of one portion of a variable slope approximating circuit in accordance with the invention,

Fig. 3B graphs the transfer function of the one portion shown in Fig. 3A,

Fig. 4A is a schematic diagram of a first curve approximating circuit in accordance with the present invention;

Fig. 4B graphs the transfer function of the circuit of Fig. 4A,

Fig. 5A is a block diagram of a second circuit in accordance with the present invention,

Fig. 5B shows a variation on the theme of Fig. 5A,

Fig. 6 is a schematic diagram of a third circuit including a temperature compensating and process variation compensating feature,

Fig. 7 shows a voltage divider version of the invention, and

Fig. 8 is a schematic of an embodiment employing the features of Figs. 6 and 7.

Referring to Fig. 3A, the operation of a sub-circuit 30 of one embodiment of the invention will be first explained. The sub-circuit 30 comprises a switching diode D_1, a resistor R_1 coupling the anode of diode D_1 to a constant voltage $+V_{C1}$, and a high input impedance amplifier A_1 having a predetermined gain G_1. Resistor R_1 and the anode of diode D_1 are joined at a voltage generating node N_2 which supplies intermediate voltage V_{N2} to the high impedance input of amplifier A_1. Input voltage V_{N1} is applied to the cathode of the diode D_1 through an input node N_1.

If the input voltage V_{N1} is sufficiently high relative to the constant voltage $+ V_{C1}$ at the anode of D_1 so as to cause diode D_1 to be reverse biased, the diode D_1 will not contribute any current to the voltage generating node N_2 and the intermediate voltage at that node will be a constant level $V_{N2} = + V_{C1}$. Resistor R_1 in essence couples the constant voltage $+V_{C1}$ to the voltage generating node N_2. If the input voltage V_{N1} is now decreased so that the switching diode D_1 comes into conduction, the diode D_1 will begin to withdraw a current I_1 from the voltage generating node N_2 and thereby decrease the intermediate voltage V_{N2} in accordance with the formula $V_{N2} = V_c - I_1R_1$. Under this condition, the intermediate voltage V_{N2} will equal the value of the applied input voltage V_{N1} plus the forward drop of switched-on diode D_1. Amplifier A_1 multiplies voltage V_{N2} by a predetermined gain factor G_1 to produce a final voltage V_{N3} at node N_3 in accordance with the formulas:

$$V_{N3} = G_1(V_C - I_1R_1) = G_1(V_{N1} + V_{D1}) \text{ for } V_{N1} < V_{N2}$$

$$V_{N3} = G_1V_C \text{ for } V_{N1} \geq V_{N2}$$

where V_{D1} is the forward drop across diode D_1. In many instances, e.g. AC signal analysis, the forward drop voltage V_{D1} can be assumed to be close to zero and neglected.

The behavior of this sub-circuit 30 is illustrated in Fig. 3B. It should be noted that the slope $d(V_{N3})/d(V_{N1})$ goes to zero when the input voltage V_{N1} increases beyond a switching point P_{S1} and that the location of this switching

point along the V_{N1} axis is determined by the value of the constant voltage $+V_{C1}$ produced at the voltage generating node N_2 as a result of potential coupling through resistor R_1. If an ideal switching diode which has no forward voltage drop is assumed for diode D_1, the switching point P_{S1} will be exactly equal to the constant voltage $+V_{C1}$.

Fig. 4A is a schematic diagram of a first curve approximating circuit 40 in accordance with the present invention. It can be seen that this curve approximating circuit 40 employs a plurality of diode/resistor sub-circuits D_1/R_1, D_2/R_2, D_3/R_3 such as the sub-circuit 30 shown in Fig. 3A. The cathodes of diodes D_1-D_3 are all connected to a common input node N_1. The anodes of diodes D_1-D_3, on the other hand, are individually coupled to different constant voltages $+V_{C1}$, $+V_{C2}$, $+V_{C3}$ by respective potential coupling resistors R_1, R_2 and R_3. Respective intermediate node voltages V_{N21}, V_{N22} and V_{N23} at the anodes of sub-circuits D_1/R_1 through D_3/R_3 are summed by a voltage summing amplifier 45 having a plurality of high-impedance input terminals 41, 42 and 43. Of importance, the switching points P_{S1}-P_{S3} of the three D/R sub-circuits are set to different values by suitable selection of constant voltages V_{C1}, V_{C2} and V_{C3} so that diodes D1-D3 become reverse biased at different points along the input signal voltage scale and they switch off in sequence as the magnitude of input signal V_{N1} increases. Input terminals 41, 42 and 43 of the summing amplifier are preferably each associated with different gain factors or signal weighting factors, G_1, G_2 and G_3 which are approximately one order of magnitude apart from one another (e.g., 10, 100, 1000) so as to develop a logarithmic-like transfer function. The transfer function of the circuit 40 may be expressed as:

$$e_{out}/e_{in} = [G_1V_{N21} + G_2V_{N22} + G_3V_{N23}]/e_{in}$$

where $V_{N2i} = e_{in}$ for $e_{in} \leq V_{ci}$ and $i = 1, 2, 3$;
and $V_{N2i} = V_{ci}$ for $e_{in} > V_{ci}$ and $i = 1, 2, 3$.

It will, of course, be understood that in cases where a summing amplifier 45 has input terminals 41-43 of finite input impedances that the Thevenin equivalency theorem can

be applied to draw an equivalent circuit having an amplifier with infinite input impedances and appropriate series resistances coupling the inputs to the Thevenin equivalent voltage sources of voltages $+V_{cl}$ and e_{in}.

The transfer function curve of circuit 40 is shown in Fig. 4B. It will of course be understood that additional linear ramp segments can be added to the curve simply by adding more input terminals to the single summing amplifier 45 and more D/R sub-circuits between common input node N_1 and the additional input terminals of the summing amplifier. This feature is a clear advantage over the expansion requirements of the previous serial circuit 20 shown in Fig. 2A. There is no need to add more amplifiers to circuit 40 when expansion is desired. There are no propagation delay penalties or saturation recovery time problems in circuit 40 similar to the problems encountered with circuit 20. Diodes D_1 - D_3 are not in saturation when switching occurs but rather coming into or out of reverse bias so very little charge needs to be moved about the diode junctions when a gain change is desired. Low level input signals do not need to propagate serially through a large number of stages in circuit 40. Instead, the input signal is split current-wise to pass in parallel through the diode switches D_1-D_3, when each of the latter is closed, to input terminals 41-43 of the summing amplifier. As such a remarkable simplification of the circuit is obtained together with improved performance.

Fig. 5A shows a block diagram of another curve approximating circuit 50 having generic switches SW_1 - SW_3 responsively coupled to a switch control 51 such that the switches respectively open or close when the magnitude of a supplied input signal e_{in} passes pre-set trip points P_{S1}, P_{S2} and P_{S3} of different values. Each of the switches, when closed, applies the input signal e_{in} to respective input terminals 51, 52 and 53 of summing amplifier 55. When one of the switches SW_1 - SW_3 opens, a corresponding one of resistors R_1, R_2 and R_3 pulls its corresponding one of input terminals 51, 52 and 53 to one of constant voltage levels

V_{C1}, V_{C2} and V_{C3}. Input gains G_1, G_2 and G_3 of input terminals 51-53 are preferably each set to a different value to produce a logarithmic-like variable gain transfer function. Switches SW_1 - SW_3 may be formed of any suitable components including for example, Schottky diodes, Schottky transistors and/or high speed field effect transistors having gates charged to different voltages V_{G1}-V_{G3} and sources/drains acting as opposed ends of dual terminal switches SW_1 - SW_3.

Fig. 5B shows a variation on the theme of Fig. 5A wherein three-terminal switches SW1'-SW3' couple input terminals of summing amplifier 155 either to receive input signal e_{in} or constant voltages V_{C1} - V_{C3} in accordance with the magnitude of input signal e_{in} relative to trip points P_{s1}, P_{s2} and P_{s3} set by control 151. Switches SW_1' through SW_3' may, again, be composed of various types of transistors and/or diodes as desired. It is within the contemplation of the present invention to include switches for programmably changing the constant voltages V_{c1}-V_{c3} or the trip-points P_{s1}-P_{s3} in response to computer generated instruction signals when such circuit programmability is desired.

Fig. 6 shows a temperature compensated version 60 of the invention. Diodes D_0 - D_3 are preferably all Schottky diodes (high speed metal-semiconductor junctions) integrally formed on a common substrate or otherwise matched during manufacture such that they have substantially identical voltage and/or current versus temperature dependencies. Input amplifier 64 forces the voltage at node N_0 to follow the magnitude of input voltage e_{in} in a mirror replicating-like linear manner as a result of a negative feedback loop formed by a temperature insensitive voltage divider comprised of resistors R_A and R_B. The voltage at node N_1 will include the temperature dependent forward drop V_{DO} of diode D_o. Temperature dependency cancellation occurs when one of the diodes D_1 - D_3 is switched on by an input signal e_{in} together with diode D_0 so that the voltage at the corresponding amplifier input terminals, terminal 61 for example, will be of the form $V_{N61} = V_{No} - V_{DO} + V_{D1}$.

Process and temperature variations in the terms V_{D0} and V_{D1} tend to cancel each other out both in the DC sense and AC sense because of the back-to-back relation between diode D_0 and diodes D_1-D_3 when moving from the input mirroring node N_0 to any one of amplifier input nodes N61, N62 or N63. Currents through diodes D_0 through D_3 are preferably kept high to minimize the small signal AC impedance dV_D/dI_D = $26mV/I_D(ma)$ @ 25°C of the diodes D_0-D_3.

The present invention contemplates the use of plural voltage dividers such the R_{A1}/R_{B1} divider shown in Figure 7 for generating voltages V_{C1} through V_{Cn} at the G_1 - G_n input terminals of a summing amplifier 75. Those skilled in the art will readily understand how power supply voltages $+V_C$ and $-V_C$ can be converted to different potential levels V_{C1} - V_{Cn}, free of temperature and manufacturing variations, using simple voltage division and how the circuit of Fig. 7 may be integrally fabricated on a semiconductive substrate (integrated circuit chip).

Figure 8 shows a circuit 80 employing the principles of Figs. 6 and 7. Operation amplifiers 84 and 85 are used for amplifying the input signal e_{in}. The negative input terminal 85a of amplifier 85 acts as a virtual ground point at which the currents of resistors R_7, R_{10} and R_{13} are summed. It will be noted that the diodes D_0 - D_3 of Fig. 8 are inverted in polarity relative to the ones discussed thus far. It should be understood from this that the input voltage signal e_{in} is of a negative polarity and that diodes D_0-D_3 are switched closed when the voltage at node N_1 is less negative than respective negative voltages V_A, V_B, V_C and V_D at the cathodes of diodes D_0-D_3. Operation amplifier 85 together with gain-determining resistors R_7, R_{10}, R_{13} and R_{14} forms the summing amplifier. In one embodiment of the circuit shown in Fig. 8 the components listed in the following table were used.

TABLE

R_1:	220 ohms	R_{10}:	1.0K
R_2:	220 ohms	R_{11}:	5.1K
R_3:	3.9K	R_{12}:	2.0K
R_4:	2.0K	R_{13}:	2.4K
R_5:	15 ohms	R_{14}:	820 ohms
R_6:	2.0K	D0-D3:	Motorla MBD101
R_7:	82 ohms	84-85:	Analog Devices Operational Amplifier AD5539
R_8:	470 ohms		
R_9:	5.1K	-V = -8 Volts	

Numerous variations and modifications of the circuits disclosed above will, of course, occur to those skilled in the art once the principles of the present invention are understood. As such, the scope of the invention is not to be limited to the above embodiments but rather defined to encompass the subject matter of the following claims.

CLAIMS

1. A curve approximating circuit comprising:

plural limiting networks including a voltage input node, a voltage output node, a constant voltage node, a resistor joining the voltage output node to the constant voltage node, and a switching diode connecting the voltage input node to the voltage output node, wherein the respective voltage input nodes of the limiting networks are coupled to receive a common input signal and wherein different constant voltages will appear at the voltage output nodes of the limiting networks when the diodes of the limiting networks are reverse biased; and

summing means having plurality input terminals coupled to the voltage output nodes of the limiting networks, for summing voltages developed at the respective voltage output nodes and producing a summed output voltage.

2. A circuit as claimed in claim 1 wherein the input terminals of the summing means are each coupled to signal attenuating/amplifying means which attenuate/amplify voltages developed at the input terminals in accordance with different attenuation/amplification factors.

3. A circuit as claimed in claim 1 or 2 wherein the switching diodes include Schottky barrier junctions.

4. A curve approximating circuit comprising:

a summing amplifier having first to nth input multiplier means of differing multiplier factors G_1 to G_n for multiplying the magnitude of a plurality of first to nth input voltage signals;

first to nth potential coupling means for respectively coupling first to nth constant

voltages V_{C1} - V_{Cn} to the first to nth input multiplier means; and

first to nth switches having respective first terminals coupled to the first to nth input multiplier means and second terminals all coupled to a common signal receiving node, the switches operating to open at different magnitude values of a common input signal supplied to the common signal receiving node.

5. A circuit as claimed in claim 4 wherein the summing amplifier comprises an operational amplifier and a plurality of resistors each having one terminal coupled to an input node of the operational amplifier and a second terminal forming a respective portion of first to nth input multiplier means.

6. A circuit as claimed in claim 4 wherein the first to nth switches include first to nth diodes which respectively become reverse biased when corresponding ones of the switches are open.

7. A circuit as claimed in claim 6 wherein the diodes are Schottky diodes.

8. A circuit as claimed in claim 4 wherein the first to nth potential coupling means respectively comprise first to nth voltage dividing networks supplying constant voltages V_{C1} - V_{Cn} to the first to nth summing amplifier input means.

9. A curve approximating circuit comprising:

summing means having first to nth weighted inputs for producing an output signal of the form $e_{out} = G_1e_1 = G_2e_2 + \ldots + G_ne_n$ where G_i is a weighting factor of input i, e_i is a signal applied to input i, and n is an integer greater than one; and

first to nth switching means each connected to selectively couple the first to nth weighted

inputs of the summing means so that the inputs respond substantially either to an input signal e_{in} supplied to the switching means or to corresponding ones of first to nth constant voltages V_{C1} - V_{Cn}, the first to nth switching means being responsive to the supplied input signal e_{in} so as to each switch at a different level of the supplied input signal e_{in}.

10. A circuit as claimed in claim 9 wherein the summing means includes first to nth attenuation/amplification networks for attenuating/amplifying the applied input signals e_1-e_n by attenuation/amplification factors corresponding to weighting factors G_1 to G^2_n and a current summing means coupled to the attenuation/amplification networks for summing currents of respective amplified/attenuated signals developed by the attenuation/amplification networks.

11. A circuit as claimed in claim 9 comprising temperature drift compensating means, interposed between an input node where the supplied input signal is produced or a mirror node where a mirror replica of the supplied input signal is produced and the first through nth switching means, for cancelling out temperature related voltage changes of the switching means, the compensating means including components that are temperature-wise substantially identical to those of the switching means.

12. A circuit as claimed in claim 11 wherein the first to nth switching means include first to nth switching diodes and the temperature drift compensating means includes a matched voltage drop cancelling diode which is voltage-wise in an opposed back-to-back relation with the first to nth switching diodes such that temperature related drifts in the forward bias

voltages of the first to nth switching diodes are matched by an equivalent voltage change across the opposed voltage drop cancelling diode.

13. A curve approximating circuit substantially as herein described with reference to Figures 4A & 4B, Figure 5A, Figure 5B, Figure 6, Figure 7 or Figure 8 of the accompanying drawings.

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