(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) **EP 3 493 285 B1**

(12) **EUROPEAN PATENT SPECIFICATION**

(45) Date of publication and mention of the grant of the patent:
06.11.2024 Bulletin 2024/45

(21) Application number: **18209266.8**

(22) Date of filing: **29.11.2018**

(51) International Patent Classification (IPC):
H10K 59/131 *(2023.01)* ***H10K 77/10*** *(2023.01)*
H10K 50/844 *(2023.01)* ***H01L 27/12*** *(2006.01)*
H10K 102/00 *(2023.01)*

(52) Cooperative Patent Classification (CPC):
H01L 27/1225; H10K 50/844; H10K 59/131; H10K 77/111; H10K 2102/311; Y02E 10/549; Y02P 70/50

(54) **DISPLAY PANEL AND METHOD FOR MANUFACTURING THE SAME**

ANZEIGETAFEL UND VERFAHREN ZUR HERSTELLUNG DAVON

PANNEAU D'AFFICHAGE ET SON PROCÉDÉ DE FABRICATION

(84) Designated Contracting States:
AL AT BE BG CH CY CZ DE DK EE ES FI FR GB GR HR HU IE IS IT LI LT LU LV MC MK MT NL NO PL PT RO RS SE SI SK SM TR

(30) Priority: **29.11.2017 KR 20170162011**

(43) Date of publication of application:
05.06.2019 Bulletin 2019/23

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(56) References cited:
EP-A1- 3 217 265
EP-A1- 3 236 309
US-A1- 2016 293 643
US-A1- 2017 125 505
US-A1- 2017 288 005
US-A1- 2017 288 007

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Description

[0001] The present invention relates to a display panel, and more particularly to a method for manufacturing the same.

[0002] A display panel may include a plurality of pixels and a driving circuit (e.g., scan driving circuit or a data driving circuit) controlling the plurality of pixels. Each of the plurality of pixels may include a display element and a driving circuit of the pixel, which may control the display element. The driving circuit of the pixel may include a plurality of thin-film transistors that are relatively closely connected to each other.

[0003] The display panel has been developed from a flat-type to various shapes such as a bending-type, a rollable-type, or a foldable-type. As the shape of the display panel is changed, a panel design may also be changed.

[0004] EP3236309, US2017/288005 and EP2217265 each relate to display devices having a first area including a display area and a second area forming a non-display area that extends from the first area and is configured to bend from the first area.

[0005] In accordance with an aspect of the present invention there is provided a display panel according to claim 1, having a pixel with increased speed and reliability, and the display panel may have increased flexibility. In accordance with another aspect of the present invention there is provided a method for manufacturing a display panel according to claim 13, with a reduced number of masks used in a manufacturing process. Further exemplary embodiments of the present invention are disclosed in the dependent claims, wherein: In an exemplary embodiment of the present invention, a portion of the signal line, which overlaps the second area, may be disposed on the organic layer.

[0006] In an exemplary embodiment of the present invention, the display panel may include a connection electrode disposed on the organic layer and connected to an output electrode of the first thin-film transistor through a contact hole formed in the organic layer.

[0007] In an exemplary embodiment of the present invention, a passivation layer may be disposed on the organic layer.

[0008] In an exemplary embodiment of the present invention, an electrode of the light emitting element may be connected to the connection electrode through a contact hole formed in the passivation layer.

[0009] In an exemplary embodiment of the present invention, the passivation layer may be disposed on the signal line. A portion of the passivation layer, which overlaps the second area, may be in direct contact with the signal line.

[0010] In an exemplary embodiment of the present invention, a first portion and a second portion of the oxide semiconductor pattern may be disposed on the input electrode and the output electrode of the second thin-film transistor, respectively.

[0011] In an exemplary embodiment of the present invention, the input electrode and the output electrode of the second thin-film transistor may be disposed above a first portion and a second portion of the oxide semiconductor pattern, respectively. A third portion of the oxide semiconductor pattern may be exposed from the input electrode and the output electrode of the second thin-film transistor.

[0012] In an exemplary embodiment of the present invention, the display panel may include an upper electrode disposed between the second insulation layer and the third insulation layer. The upper electrode may overlap the control electrode of the first thin-film transistor.

[0013] In an exemplary embodiment of the present invention, the display panel may include a light blocking pattern disposed on the organic layer. The light blocking pattern may overlap the oxide semiconductor pattern of the second thin-film transistor.

[0014] In an exemplary embodiment of the present invention, the at least one inorganic layer may include silicon oxide layers and silicon nitride layers disposed alternately with the silicon oxide layers.

[0015] In an exemplary embodiment of the present invention, a portion of a top surface of the at least one inorganic layer may be in direct contact with the organic layer.

[0016] In an exemplary embodiment of the present invention, after the forming of the oxide semiconductor pattern, forming the second input electrode and the second output electrode, which are spaced apart from each other and each of which may overlap the oxide semiconductor pattern along the direction orthogonal to the upper surface of the base layer.

[0017] The above and other features of the present invention will become more apparent by describing in detail exemplary embodiments thereof with reference to the accompanying drawings, in which:

FIGS. 1A and 1B are perspective views of a display panel according to an exemplary embodiment of the present invention;

FIG. 2 is a plan view of a display panel according to an exemplary embodiment of the present invention;

FIG. 3A is an equivalent circuit diagram of a pixel according to an exemplary embodiment of the present invention;

FIGS. 3B and 3C are cross-sectional views of a portion of a pixel according to an exemplary embodiment of the present invention;

FIGS. 4A and 4B are cross-sectional views of a bending area of a display panel according to an exemplary embodiment of the present invention;

FIGS. 5A, 5B, 5C, 5D, 5E, 5F, 5G, 5H, 5I, 5J, 5K, 5L, 5M, 5N and 5O are cross-sectional views of a process for manufacturing a display panel according to an exemplary embodiment of the present invention;

FIG. 6 is a cross-sectional view of a display panel

according to an exemplary embodiment of the present invention;

FIG. 7 is a cross-sectional view of a display panel according to an exemplary embodiment of the present invention;

FIGS. 8A, 8B, 8C, 8D and 8E are cross-sectional views illustrating a portion of a display panel according to an exemplary embodiment of the present invention; and

FIG. 9 is a cross-sectional view of a portion of a display panel according to an exemplary embodiment of the present invention.

[0018] Exemplary embodiments of the present invention will be described below in more detail with reference to the accompanying drawings. In this regard, the exemplary embodiments may have different forms and should not be construed as being limited to the exemplary embodiments of the present invention described herein.

[0019] It will be understood that when an element such as a region, layer, or portion is referred to as being "on" another element, it may be directly on the other element or intervening elements may also be present.

[0020] Like reference numerals may refer to like elements throughout the specification and drawings. Sizes of elements in the drawings may be exaggerated for clarity of description.

[0021] It will be understood that although the terms "first" and "second" may be used herein to describe various components, these components should not be limited by these terms.

[0022] FIGS. 1A and 1B are perspective views of a display panel according to an exemplary embodiment of the present invention. FIG. 2 is a plan view of the display panel according to an exemplary embodiment of the present invention. FIG. 2 schematically illustrates a connection relationship between pixels PX, a driving circuit GDC, and a signal line SGL.

[0023] In an unfolded state, a display panel DP may include a front surface DP-FS that is parallel to a surface defined by a first directional axis DR1 and a second directional axis DR2. As an example, the front surface DP-FS may have a substantially rectangular shape; however, exemplary embodiments of the present invention are not limited thereto. A normal direction of the front surface DP-FS of the display surface DS, for example, a thickness direction of the display panel DP, may extend a third directional axis DR3. Thus, the third directional axis DR3 may be orthogonal to the first direction axis DR1 and the second directional axis DR1. A front surface and a bottom surface (e.g., a rear surface) of the display panel DP may face along the third directional axis DR3. Thus, each of a plurality of stacked layers of the display panel DP may include front and rear surfaces facing along the third direction axis DR 3 (e.g., when the display panel DP is in an unfolded state). The first, second and third directional axes DR1, DR2, and DR3 may be respectively referred to as first, second and third directions herein, and may include like reference numerals herein.

[0024] Referring to FIG. 1A, the display panel DP may include a display area DP-DA on which the pixels PX are displayed and a non-display area DP-NDA on the front surface DP-FS. The non-display area DP-NDA may be an area on which the pixels are not disposed. Thus, each of the pixels PX may be positioned in the display area DP-DA. On the non-display area DP-NDA, a portion of the signal lines SGL and/or the driving circuit GDC may be disposed.

[0025] The display area DP-DA may have a rectangular shape. The non-display area DP-NDA may surround the display area DP-DA (e.g., on four sides of the display area DP-DA) when viewed in a plan view along the third direction DR3. However, exemplary embodiments of the present invention are not limited to particular shapes of the display area DP-DA or the non-display area DP-NDA. For example, the shapes of the display area DP-DA and the non-display area DP-NDA may each be modified, as desired. For example, the non-display area DP-NDA may be disposed on only areas facing each other in the first direction DR1. Alternatively, the non-display area DP-NDA may be disposed on three sides of the display area DP-DA (e.g., not on a side of the display area DP-DA on which a second area BA described in more detail below extends from). As an example, the display area DP-DA may have a circular shape.

[0026] According to an exemplary embodiment of the present invention, a portion of the non-display area DP-NDA may have a relatively narrow width (e.g., a length in the second direction DR2) in comparison with that of the display area DP-DA. Thus, a surface area of a bending area, which will be described in more detail below, may be reduced.

[0027] Referring to FIG. 1B, the display panel DP may be bent or curved (e.g., bent back on itself, for example to form a 'C' shape), and, as it is bent, the display panel DP may include a first area NBA (e.g., a non-bending area, also referred to as a planar area) and a second area BA (e.g., a bending area, also referred to as an area that has been bent). The second area BA may include a curvature area CA having a predetermined curvature in a bent state and a facing area FA facing the first area NBA in a bent state. As an example, the display panel DP may be bent along a bending axis BX. The bending axis BX may extend along the second direction DR2. The second direction DR2 may be perpendicular to each of the first direction DR1 and the third direction DR3.

[0028] Referring to FIG. 2, the display panel DP may include a driving circuit GDC, a plurality of signal lines SGL (e.g., which may be referred to herein as signal lines), a plurality of signal pads DP-PD (e.g., which may be referred to herein as signal pads), and a plurality of pixels PX (e.g., which may be referred to herein as pixels).

[0029] The pixels PX may be divided into a plurality of groups according to colors displayed thereon. The pixels PX may include, e.g., red pixels, green pixels, or blue

pixels. The pixels PX may include white pixels. Although the pixels may be divided into different groups according to colors displayed thereon, the pixel driving circuit of the pixels may be the same as each other.

[0030] The driving circuit GDC may include a scan driving circuit. The scan driving circuit may generate a plurality of scan signals (e.g., which may be referred to herein as scan signals) and may sequentially output the scan signals to a plurality of scan lines GL (e.g., which may be referred to herein as scan lines). The scan driving circuit may further output another control signal to the driving circuit of the pixels PX.

[0031] The scan driving circuits may include a plurality of thin-film transistors that are formed through substantially the same process as that of the driving circuit of the pixels PX, e.g., a low temperature polycrystalline silicon (LTPS) process or a low temperature polycrystalline oxide process.

[0032] The signal lines SGL may include scan lines GL, data lines DL, a power line PL, and/or control signal line CSL. Each of the scan lines GL may be connected to a corresponding pixel PX of the pixels PX, and each of the data lines DL may be connected to a corresponding pixel PX of the pixels PX. The power line PL may be connected to the pixels PX. The control signal line CSL may provide control signals to the scan driving circuit. Each of the signal pads DP-PD may be connected to the corresponding signal line of the signal lines SGL.

[0033] A circuit board may be electrically connected to the display panel DP. The circuit board may be a rigid circuit board or a flexible circuit board. A driving chip may be mounted to the circuit board.

[0034] The driving chip may be mounted to the display panel DP. When the driving chip is mounted to the display panel DP, the design of the signal lines SGL may be modified. The driving chip may be connected to the data lines DL, and a signal line connecting the driving chip to the signal pads DP-PD may be further provided.

[0035] FIG. 3A is an equivalent circuit diagram of a pixel according to an exemplary embodiment of the present invention. FIGS. 3B and 3C are cross-sectional views of a portion of a pixel PX according to an exemplary embodiment of the present invention.

[0036] FIGS. 4A and 4B are cross-sectional views of a bending area of a display panel according to an exemplary embodiment of the present invention.

[0037] Referring to FIG. 3A, any one scan line GL, any one data line DL, and a power line PL may be connected to a pixel PX. Although the pixel PX according to an exemplary embodiment of the present invention may be a light emitting type pixel, exemplary embodiments of the present invention are not limited thereto. For example, the pixel PX may include, as a light emitting element, an organic light emitting diode or a quantum dot light emitting diode. A light emitting layer of the organic light emitting diode may include an organic light emitting material. A light emitting layer of the quantum dot light emitting diode may include a quantum dot and a quantum rod. Below, as an example, the pixel PX will be described as an organic light emitting pixel.

[0038] The pixel PX may include an organic light emitting diode OLED and a pixel driving circuit for driving the organic light emitting diode OLED. The light emitting diode OLED may be referred to as a light emitting element herein. The organic light emitting diode OLED may be a front light emitting type diode or a rear light emitting type diode. In an exemplary embodiment of the present invention, the pixel driving circuit may include a first thin-film transistor T1 (e.g., a driving transistor), a second thin-film transistor T2 (e.g., a switching transistor), and a capacitor Cst. A first power voltage ELVDD may be provided to the first thin-film transistor T1, and a second power voltage ELVSS may be provided to the organic light emitting diode OLED. The second power voltage ELVSS may be less than the first power voltage ELVDD.

[0039] The first thin-film transistor T1 may be connected to the organic light emitting diode OLED. The first thin-film transistor T1 may control a driving current flowing in the organic light emitting diode OLED in correspondence to an electric charge quantity stored in the capacitor Cst. The second thin-film transistor T2 may output a data signal applied to the data line DL in response to a scan signal applied to the scan line GL. The capacitor Cst may hold a voltage corresponding to the data signal received from the second thin-film transistor T2.

[0040] Exemplary embodiments of the present invention are not limited to the configuration of the pixel PX described with reference to FIG. 3A. The configuration of the pixel PX may be varied within the scope of the appended claims. For example, the pixel circuit controlling the organic light emitting diode OLED may include, e.g., six or seven thin-film transistors. The organic light emitting diode OLED may be connected between the power line PL and the second thin-film transistor T2.

[0041] FIG. 3B, which is a partial configuration of the pixel PX, illustrates a cross-section corresponding to the first thin-film transistor T1, the second thin-film transistor T2, and the organic light emitting diode OLED. The first thin-film transistor T1 has a top-gate structure. The second thin-film transistor T2 has a bottom-gate structure. Referring to FIG. 3B, the display panel DP may include a base layer BL, a circuit element layer DP-CL disposed on the base layer BL, a display element layer DP-OLED, and a thin-film encapsulation layer TFE. The display panel DP may include functional layers such as a reflection protective layer and a refractive index adjusting layer. The circuit element layer DP-CL may include a plurality of insulation layers and a circuit element. As an example, the insulation layers may include an organic layer and/or an inorganic layer.

[0042] The circuit element may include a signal line SGL and a driving circuit of a pixel. The circuit element layer DP-CL may be formed through a process of forming an insulation layer, a semiconductor layer, and a conductive layer through coating and deposition and a process of patterning the insulation layer, the semiconductor

layer, and the conductive layer through a photolithography process.

[0043] The display element layer DP-OLED may include a light emitting element. The display element layer DP-OLED may further include an organic layer such as a pixel defining layer PDL.

[0044] The base layer BL may include a synthetic resin film. The synthetic resin layer may include a thermosetting resin. For example, although the synthetic resin layer may include a polyimide-based resin layer, exemplary embodiments of the present invention are not limited thereto. The synthetic resin layer may include at least one of an acryl-based resin, a methacryl-based resin, a polyisoprene-based resin, a vinyl-based resin, an epoxy-based resin, a urethane-based resin, a cellulose-based resin, a siloxane-based resin, a polyamide-based resin, or a perylene-based resin. The base layer BL may include a glass substrate, a metal substrate, and/or, an organic/inorganic composite substrate.

[0045] The areas of the display panel DP described with reference to FIGS. 1A, 1B and 2 may be defined in the base layer BL in substantially the same manner as described above for the display panel DP. For example, the base layer BL may include a first area NBA and a second area BA that is bent from the first area NBA.

[0046] According to an exemplary embodiment of the present invention, the second area BA does extend from the first area NBA. The second area BA does include the curvature area CA. The second area BA may have a smaller thickness (e.g., in the third direction DR3) than that of the first area NBA. Thus, bending or curving of the curvature area CA in the second area BA may be achieved with a relatively small amount of force applied to the second area BA, and a stress applied to a connection between the first area NBA and the second area BA may be relatively low. The curvature area CA may be permanently maintained in a curved state, or may remain bendable.

[0047] At least one inorganic layer is disposed on a top surface of the base layer BL. The inorganic layer may include at least one of an aluminum oxide, a titanium oxide, a silicon oxide, a silicon oxynitride, a zirconium oxide, or hafnium oxide. The inorganic layer may have a single layer or a multiple layer structure. The multi-layer inorganic layers may include a barrier layer BRL and/or a buffer layer BFL, which will be described in more detail below. The barrier layer BRL and the buffer layer BFL may be selectively disposed, as desired. Thus, either of the barrier layer BRL or the buffer layer BFL may be individually referred to as an inorganic layer. Alternatively, the barrier layer BRL and the buffer layer BFL may collectively be referred to as an inorganic layer.

[0048] The barrier layer BRL may prevent foreign substances from being introduced from the outside. The barrier layer BRL may include a silicon oxide layer and/or a silicon nitride layer. The silicon oxide layer and the silicon nitride layer may be provided as a plurality of layers. The silicon oxide layers and the silicon nitride layers may be alternately and repeatedly stacked.

[0049] The buffer layer BFL may be disposed on the barrier layer BRL. The buffer layer BFL may increase a coupling force between the base layer BL and conductive patterns or semiconductor patterns. The buffer layer BFL may include a silicon oxide layer and/or a silicon nitride layer. The silicon oxide layer and the silicon nitride layer may be alternately and repeatedly stacked.

[0050] A first semiconductor pattern OSP1 may be disposed on the buffer layer BFL. The first semiconductor pattern OSP1 may include a silicon semiconductor. Thus, the first semiconductor pattern OSP1 may be referred to as a silicon semiconductor pattern. The first semiconductor pattern OSP1 may include a polysilicon semiconductor. However, exemplary embodiments of the present invention are not limited thereto. For example, the first semiconductor pattern OSP1 may include amorphous silicon. The first semiconductor pattern OSP1 may include an input area (e.g., a first portion), an output area (e.g., a second portion), and a channel area (e.g., a third portion) defined between the input area and the output area. The channel area of the first semiconductor pattern OSP1 may be defined in correspondence to a first control electrode GE1 that will be described in more detail below. For example, the first control electrode GE1 and the first semiconductor pattern OSP1 may at least partially overlap each other (e.g., may be fully aligned with each other) along the third direction DR3. Each of the input area and the output area may have a conductivity relatively higher than that of the channel area because the input area and the output area are doped with a dopant. The input area and the output area may be doped with an n-type dopant. In an exemplary embodiment of the present invention, although the n-type first thin-film transistor T1 is exemplarily described, the first thin-film transistor T1 may be a p-type transistor.

[0051] A first insulation layer 10 may be disposed on the buffer layer BFL. The first insulation layer 10 may overlap each of the plurality of pixels PX (e.g., along the third direction DR3, which may be orthogonal to the upper surface of the base layer BL; see, e.g., FIG. 1A). The first insulation layer does cover upper and sides surfaces of the first semiconductor pattern OSP1. The upper surface of the first semiconductor pattern OSP1 may face away from the base layer in the third direction DR3 and the side surfaces of the first semiconductor pattern OSP1 may face along the first direction DR1 perpendicular to the third direction DR3. Upper and side surfaces of other layers described in more detail below may refer to surfaces facing in the third direction DR3 and the first direction DR1, respectively. The first insulation layer 10 may include an inorganic layer and/or an organic layer and may have a single-layer or multi-layer structure.

[0052] In an exemplary embodiment of the present invention, the first insulation layer 10 may include the inorganic layer and may include at least one of an aluminum oxide, a titanium oxide, a silicon oxide, a silicon oxynitride, a zirconium oxide, or hafnium oxide. In an ex-

emplary embodiment of the present invention, the first insulation layer 10 may be a single-layer including silicon oxide.

[0053] A first control electrode GE1 is disposed on the first insulation layer 10. The first control electrode GE1 may overlap the channel area of the first semiconductor pattern OSP1 (e.g., along the third direction DR3, which may be orthogonal to the upper surface of the base layer BL).

[0054] A second insulation layer 20 does cover upper and side surfaces of the first control electrode GE1 disposed on the first insulation layer 10. The second insulation layer 20 may overlap each of the plurality of pixels PX (e.g., along the third direction DR3, which may be orthogonal to the upper surface of the base layer BL; see, e.g., FIG. 1). The second insulation layer 20 may include an inorganic layer and/or an organic layer and may have a single-layer or multi-layer structure.

[0055] In an exemplary embodiment of the present invention, the second insulation layer 20 may include the inorganic layer and may include at least one of an aluminum oxide, a titanium oxide, a silicon oxide, a silicon oxynitride, a zirconium oxide, or hafnium oxide. In an exemplary embodiment of the present invention, the second insulation layer 20 may be a single-layer including silicon oxide.

[0056] A second control electrode GE2 is disposed on the second insulation layer 20. The second control electrode GE2 might not overlap the first control electrode GE1. Thus, the second control electrode GE2 may be spaced apart from the first control electrode (e.g., along the first direction DR1). In an exemplary embodiment of the present invention, an upper electrode UE may be disposed on the second insulation layer 20. The upper electrode UE may overlap the first control electrode GE1 (e.g., along the third direction DR3, which may be orthogonal to the upper surface of the base layer BL). Since the second control electrode GE2 and the upper electrode UE may be formed through the

[0057] same process as each other, the second control electrode GE2 and the upper electrode UE may include a same material as each other and may have the same lamination structure as each other. In an exemplary embodiment of the present invention, the upper electrode UE may be omitted.

[0058] A third insulation layer 30 substantially covering upper and side surfaces of the second control electrode GE2 and the upper electrode UE is disposed on the second insulation layer 20. The third insulation layer 30 may include an inorganic layer and/or an organic layer and may have a single-layer or multi-layer structure.

[0059] In an exemplary embodiment of the present invention, the third insulation layer 30 may include the inorganic layer and may include at least one of an aluminum oxide, a titanium oxide, a silicon oxide, a silicon oxynitride, a zirconium oxide, or hafnium oxide. In an exemplary embodiment of the present invention, the third insulation layer 30 may be a single-layer include silicon oxide.

[0060] A second semiconductor pattern OSP2 overlapping the second control electrode GE2 (e.g., along the third direction DR3, which may be orthogonal to the upper surface of the base layer BL) is disposed on the third insulation layer 30. The second semiconductor pattern OSP2 does include an oxide semiconductor. Thus, the second semiconductor pattern OSP2 may be referred to as an oxide semiconductor pattern. The second semiconductor pattern OSP2 may include a crystalline or non-crystalline oxide semiconductor. For example, the oxide semiconductor may include a metal oxide such as zinc (Zn), indium (In), gallium (Ga), tin (Sn) or titanium (Ti), metal such as zinc (Zn), indium In), gallium (Ga), tin (Sn), or titanium (Ti), or a mixture thereof. The oxide semiconductor may include an indium-tin oxide (ITO), an indium-gallium-zinc oxide (IGZO), a zinc oxide (ZnO), an indium-zinc oxide (IZnO), a zinc-indium oxide (ZIO), an indium oxide (InO), a titanium oxide (TiO), an indium-zinc-tin oxide (IZTO), or a zinc-tin oxide (ZTO).

[0061] The second semiconductor pattern OSP2 does may include an input area (e.g., a first portion), an output area (e.g., a second portion), and a channel area (e.g., a third portion) defined between the input area and the output area. Each of the input area and the output area may include impurities. The channel area of the second semiconductor pattern OSP2 may be defined as an area exposed from a second input electrode DE2 and a second output electrode SE2, which will be described in more detail below.

[0062] The impurities of the second semiconductor pattern OSP2 may be reduced metal materials. Each of the input area and the output area may include metal materials reduced from a metal oxide included in the channel area. Thus, the second thin-film transistor T2 may reduce a leakage current and may serve as a switching element having an on-off characteristic with increased accuracy and reliability.

[0063] A first input electrode DE1, a first output electrode SE1, a second input electrode DE2, and a second output electrode SE2 are disposed on the third insulation layer 30. Since the first input electrode DE1, the first output electrode SE1, the second input electrode DE2, and the second output electrode SE2 may be formed through the same process as each other, each of the first input electrode DE1, the first output electrode SE1, the second input electrode DE2, and the second output electrode SE2 may include a same material as each other and may have the same lamination structure as each other.

[0064] The first input electrode DE1 and the first output electrode SE1 may be respectively connected to the first semiconductor pattern OSP1 through a first contact hole CH1 and a second contact hole CH2 exposing the input area and the output area of the first semiconductor pattern OSP1, respectively. The first contact hole CH1 and the second contact hole CH2 may pass through the first insulation layer 10, the second insulation layer 20 and the third insulation layer 30.

[0065] The second input electrode DE2 and the second output electrode SE2 may respectively be connected to opposite ends of the second semiconductor pattern OSP2, respectively. At least a portion of the second input electrode DE2 may be directly disposed on the input area of the second semiconductor pattern OSP2, and at least a portion of the second output electrode SE2 may be directly disposed on the output area of the second semiconductor pattern OSP2.

[0066] The fourth insulation layer 40 substantially covering upper and sides surfaces of the first input electrode DE1, the first output electrode SE1, the second input electrode DE2, and the second output electrode SE2 is disposed on the third insulation layer 30. The fourth insulation layer 40 may include an inorganic layer and/or an organic layer and may have a single-layer or multi-layer structure.

[0067] In an exemplary embodiment of the present invention, the fourth insulation layer 40 including the inorganic layer and may include at least one of an aluminum oxide, a titanium oxide, a silicon oxide, a silicon oxynitride, a zirconium oxide, or hafnium oxide. The fourth insulation layer 40 may include a silicon oxide layer.

[0068] The fifth insulation layer 50 may be disposed on the fourth insulation layer 40. The fifth insulation layer 50 may include an organic layer. A connection electrode CNE may be disposed on the fifth insulation layer 50. The connection electrode CNE may be connected to the first output electrode SE1 through a third contact hole CH3 passing through the fourth insulation layer 40 and the fifth insulation layer 50. The sixth insulation layer 60 substantially covering upper and side surfaces of the connection electrode CNE may be disposed on the fifth insulation layer 50. The sixth insulation layer 60 may be referred to as a passivation layer. The sixth insulation layer 60 may include an organic layer and may have a single-layer or multi-layer structure.

[0069] In an exemplary embodiment of the present invention, each of the fifth insulation layer 50 and the sixth insulation layer 60 may have a single-layer structure including a polyimide-based resin layer. However, exemplary embodiments of the present invention are not limited thereto. For example, each of the fifth insulation layer 50 and the sixth insulation layer 60 may include at least one of an acryl-based resin, a methacryl-based resin, a polyisoprene-based resin, a vinyl-based resin, an epoxy-based resin, a urethane-based resin, a cellulose-based resin, a siloxane-based resin, a polyamide-based resin, or a perylene-based resin

[0070] The organic light emitting diode OLED may be disposed on the sixth insulation layer 60. An anode AE of the organic light emitting diode OLED may be disposed on the sixth insulation layer 60. The anode AE may be connected to the connection electrode CNE through a fourth contact hole CH4 passing through the sixth insulation layer 60. A pixel defining layer PDL may be disposed on the sixth insulation layer 60.

[0071] An opening of the pixel defining layer PDL may expose at least a portion of the anode AE. The opening OP of the pixel defining layer PDL may define a light emitting area PXA of the pixel. For example, the plurality of pixels PX (see, e.g., FIG. 1A) may be arranged under a predetermined rule on a plane of the display panel DP (see, e.g., FIG. 1A). For example, the plurality of pixels PX may be arranged in a matrix configuration having rows and columns extending along the first and second directions DR1 and DR2. An area on which the plurality of pixels PX are disposed may be defined as a pixel area, and one pixel area may include a light emitting area PXA and a non-light emitting area NPXA adjacent to the light emitting area PXA. The non-light emitting area NPXA may surround the light emitting area PXA (e.g., when viewed in a plan view along the third direction DR3, which may be orthogonal to the upper surface of the base layer BL).

[0072] The display area DP-DA (see, e.g., FIGS. 1A and 1B) may include a plurality of pixel areas. For example, the display area DP-DA may include a plurality of the light emitting areas PXA and the non-light emitting area NPXA surrounding the plurality of the light emitting areas PXA.

[0073] A hole control layer HCL may be disposed on the light emitting area PXA and the non-light emitting area NPXA in common. A common layer such as the hole control layer HCL may connect two or more pixels of the plurality of pixels PX to each other. The hole control layer HCL may include a hole transporting layer and a hole injection layer.

[0074] An organic light emitting layer EML may be disposed on the hole control layer HCL. The organic light emitting layer EML may be disposed on only an area corresponding to the opening OP. The organic light emitting layer EML may be separately provided on each of the plurality of pixels PX.

[0075] The organic light emitting layer EML may be disposed on two or more pixels of the plurality of pixels PX. The organic light emitting layer EML may generate white light. The organic light emitting layer EML may have a multi-layer structure.

[0076] An electron control layer ECL may be disposed on the organic light emitting layer EML. The electron control layer ECL may include an electron transporting layer and an electron injection layer. A cathode CE may be disposed on the electron control layer ECL. The electron control layer ELC and the cathode CE may be disposed on the plurality of pixels PX in common.

[0077] The thin-film encapsulation layer TFE may be disposed on the cathode. The thin-film encapsulation layer TFE may be disposed on two or more pixels of the plurality of pixels PX. According to an exemplary embodiment of the present invention, the thin-film encapsulation layer TFE may substantially cover an upper surface of the cathode CE. In an exemplary embodiment of the present invention, a capping layer may also substantially cover the upper surface of the cathode CE. The capping layer may include an organic layer. In an exemplary em-

bodiment of the present invention, an inorganic layer may be formed on the capping layer through a sputtering method. In an exemplary embodiment of the present invention, the lamination structure of the organic light emitting diode OLED may have a structure that is upside down from the structure described with reference to FIG. 3B.

[0078] The thin-film encapsulation layer TFE may include at least an inorganic layer or an organic layer. In an exemplary embodiment of the present invention, the thin-film encapsulation layer TFE may include two inorganic layers with an organic layer disposed therebetween. In an exemplary embodiment of the present invention, the thin-film encapsulation layer may include a plurality of inorganic layers and a plurality of organic layers, which are alternately and repeatedly stacked.

[0079] The encapsulation inorganic layer protects the organic light emitting diode OLED from moisture/oxygen, and the encapsulation organic layer protects the organic light emitting diode OLED from foreign substances such as dust particles. Although the encapsulation inorganic layer may include a silicon nitrite layer, a silicon oxynitride layer, a silicon oxide layer, a titanium oxide layer, or an aluminum oxide layer, exemplary embodiments of the present invention are not limited thereto. Although the encapsulation organic layer may include an acryl-based organic layer, exemplary embodiments of the present invention are not limited thereto.

[0080] According to an exemplary embodiment of the present invention, the first thin-film transistor T1 does include a silicon semiconductor, for example, a polysilicon semiconductor, and thus the first thin-film transistor T1 may have a relatively high electron mobility. The first thin-film transistor T1 may have an increased voltage-current accuracy and reliability. The second thin-film transistor T2 does include an oxide semiconductor, and thus an occurrence of a leakage current may be reduced. Thus, the driving voltage of the pixel PX (see, e.g., FIG. 3A) may be reduced, and an occurrence of a malfunction thereof may be reduced or prevented.

[0081] As the input electrode DE1 and the output electrode SE1 of the first thin-film transistor T1, which are disposed on the same layer as that of the input electrode DE2 and the output electrode SE2 of the second thin-film transistor T2, may be respectively directly connected to the first semiconductor pattern OSP1 through the first and second contact holes CH1 and CH2 passing through the first to third insulation layers 10 to 30, misalignment may decrease. When the input electrode DE1 and the output electrode SE1 are disposed on the same layer as that of the upper electrode UE (e.g., in a display panel according to a comparative example), a process of forming connection electrodes CNE on the same layer as that of the input electrode DE2 and the output electrode SE2 of the second thin-film transistor T2 may be performed. The connection electrodes CNE may be connected to the input electrode DE1 and the output electrode SE1, which are disposed on the same layer as that of the upper electrode UE. Thus, while the connection electrodes CNE are formed, the misalignment may occur. Since the input electrode DE2 and the output electrode SE2 of the second thin-film transistor T2 and the input electrode DE1 and the output electrode SE1 of the first thin-film transistor T1 are formed through separated processes, the number of masks used in the manufacturing process may increase.

[0082] Referring to FIG. 3C, the display panel according to an exemplary embodiment of the present invention may further include the capacitor Cst formed through the same process as that of the components of the first thin-film transistor T1.

[0083] A first electrode E1 of the capacitor Cst may be disposed on the first insulation layer 10. The first electrode E1 may be formed through the same process as that of the first control electrode GE1. The first electrode E1 may be connected to the first control electrode GE1.

[0084] The second insulation layer 20 may substantially cover upper and side surfaces of the first electrode E1. A second electrode E2 of the capacitor Cst may be disposed on the second insulation layer 20. In an exemplary embodiment of the present invention, the upper electrode UE may be electrically connected to the second electrode E2. The upper electrode UE and the second electrode E2 may be formed through the same process as each other, and thus the upper electrode UE and the second electrode E2 may include a same material as each other and may include a same structure (e.g., a single or multilayered structure) as each other. The third insulation layer 30 substantially covering the second electrode E2 and the upper electrode UE may be disposed on the second insulation layer 20.

[0085] FIGS. 4A and 4B are views illustrating a cross-section in the first direction DR1 of the curvature area CA in FIG. 2. FIG. 4A illustrates a cross-section overlapping the signal line DL, and FIG. 4B illustrates a cross-section of an area on which the signal line is not disposed. In FIG. 4A, the data line DL illustrated as the signal line DL.

[0086] Referring to FIGS. 4A and 4B, the second area BA may have a lamination structure that is similar to that of the first area NBA (see, e.g., FIGS. 1A, 1B and 2), for example, the display area DP-DA (see, e.g., FIGS. 1A, 1B and 2), in a cross-section. The barrier layer BRL, the buffer layer BFL, and the first to sixth insulation layers 10 to 60 may be sequentially arranged from the top surface of the base layer BL (e.g., along the third direction DR3, which may be orthogonal to the upper surface of the base layer BL).

[0087] A groove GV-1 (e.g., which may be referred to herein as a lower groove) overlapping the second area BA (e.g., along the third direction DR3, which may be orthogonal to the upper surface of the base layer BL) may define the barrier layer BRL and/or the buffer layer BFL. The lower groove GV-1 may be defined in the curvature area CA. Referring to FIGS. 1A, 1B and 2, the inorganic layers BRL and BFL disposed below the first semiconductor pattern OSP1 may overlap the display

area DP-DA (e.g., along the third direction DR3, which may be orthogonal to the upper surface of the base layer BL) and may extend to the second area BA. The lower groove GV-1 may be formed by removing portions of the inorganic layers BRL and BFL so that at least a portion of the inorganic layers BRL and BFL overlaps the second area BA (e.g., along the third direction DR3, which may be orthogonal to the upper surface of the base layer BL). The base layer BL exposed by the lower groove GV-1 may have a width in the first direction DR1, which is less than that of the curvature area CA in the first direction DR1.

[0088] A groove GV-2 (e.g., which may be referred to herein as an upper groove) overlapping the second area BA (e.g., along the third direction DR3, which may be orthogonal to the upper surface of the base layer BL) may be defined in the first to fourth insulation layers 10 to 40. The upper groove GV-2 may be defined in the curvature area CA. A top surface of an uppermost inorganic layer of the inorganic layers included in the barrier layer BRL and the buffer layer BFL may be exposed from the first to fourth insulation layers 10 to 40.

[0089] Each of side surfaces, which define the lower groove GV-1, of the barrier layer BRL and the buffer layer BFL may have a predetermined slope in a cross-section. Each of side surfaces, which define the upper groove GV-2, of the first to fourth insulation layers 10 to 40 may have a predetermined slope in a cross-section.

[0090] In an exemplary embodiment of the present invention, a width of the upper groove GV-2 in the first direction DR1, which corresponds to the fourth insulation layer 40, may be greater than that of the curvature area CA in the first direction DR1.

[0091] The fifth insulation layer 50 including an organic layer may be disposed in the upper groove GV-2 and the lower groove GV-1. Thus, the fifth insulation layer 50 may be referred to as an organic layer. The fifth insulation layer 50 may be in direct contact with a top surface of the base layer BL, an inclined surface of the lower groove GV-1, and an inclined surface of the upper groove GV-2. The fifth insulation layer 50 may be in direct contact with a portion of the top surface of the buffer layer BFL, which may be exposed from the first to fourth insulation layers 10 to 40.

[0092] As the grooves GV-1 and GV-2 are defined in the inorganic layers BRL, BFL, and insulation layers 10 to 40 of the curvature area CA, and the organic layer 50 is disposed in the grooves GV-1 and GV-2, the bending area BA may have increased flexibility. As the organic layer 50 is disposed on the bending area BA and the non-bending area NBA, the display panel DP may have a simplified structure. Thus, a relatively lower number of masks may be used in forming the organic layer 50. For example, the organic layer 50 may be formed by a single continuous process in the bending area BA and the non-bending area NBA. Thus, manufacturing costs may be reduced and an occurrence of defects may be reduced.

[0093] At least one portion of the signal line DL may be disposed on the fifth insulation layer 50. The sixth insulation layer 60 may substantially cover an upper surface of the signal line DL, which may protect the signal line DL. Another portion of the signal line DL, for example, another portion disposed on the display area DP-DA, may be disposed on a different layer from the sixth insulation layer 60. For example, another portion of the signal line DL may be disposed on the third insulation layer 30. The at least one portion and the another portion of the signal line DL may be connected through the contact hole passing through the fourth insulation layer 40 and the fifth insulation layer 50. The contact hole may be disposed on the non-display area DP-NDA of the first area NBA.

[0094] In an exemplary embodiment of the present invention, a layer extending from the layer disposed on the display area DP-DA may be further disposed on a top surface of the sixth insulation layer 60. In an exemplary embodiment of the present invention, the sixth insulation layer 60 might not be disposed in the curvature area CA.

[0095] FIGS. 5A, 5B, 5C, 5D, 5E, 5F, 5G, 5H, 5I, 5J, 5K, 5L, 5M, 5Nand 5O are cross-sectional views of a process of manufacturing a display panel according to an exemplary embodiment of the present invention. Each of FIGS. 5A to 5O comparatively illustrates areas corresponding to those described above with reference to FIGS. 3B and 4A. Thus, duplicative descriptions of components that are the same or substantially the same as those described above with reference to FIGS. 1A, 1B, 2, 3A, 3B, 3C, 4A and 4B may be omitted below.

[0096] Referring to FIG. 5A, at least one inorganic layer is formed on the first area NBA and the second area BA of the base layer BL. The base layer BL may be disposed on a working substrate during the manufacturing process. The working substrate may be removed after the display panel is manufactured.

[0097] The inorganic layers may be formed by depositing, coating, or printing an inorganic material. The barrier layer BRL may be formed by sequentially forming a silicon oxide layer and a silicon nitride layer. The buffer layer BFL may be formed by sequentially forming a silicon oxide layer and a silicon nitride layer on the barrier layer BRL.

[0098] A first preliminary semiconductor pattern OSP1-P is formed on the inorganic layer. The first preliminary semiconductor pattern OSP1-P may include a silicon semiconductor material. The semiconductor layer may be formed and then patterned to form the first preliminary semiconductor pattern OSP1-P. The semiconductor layer may be crystallized. For example, the semiconductor layer may be crystallized either before or after patterning the semiconductor layer to form the first preliminary semiconductor pattern OSP1-P. A doping process may be performed on the first preliminary semiconductor pattern OSP1-P.

[0099] Referring to FIG. 5B, the first insulation layer 10 is formed on the first area NBA and the second area BA of the inorganic layer. The first insulation layer 10 may

be formed through deposition, coating, or printing. Insulation layers disposed on the first insulation layer 10 may be also formed through deposition, coating, or printing.

[0100] The first control electrode GE1 is formed on the first insulation layer 10. The first control electrode GE1 may be formed by forming a conductive layer on the first insulation layer 10 and then pattering the same. The first electrode E1 (see, e.g., FIG. 3C) of the capacitor Cst may be formed through the same process as that of the first control electrode GE1.

[0101] The first preliminary semiconductor pattern OSP1-P may be doped by using the first control electrode GE1 as a mask. An area (e.g., which may be referred to herein as a channel area) overlapping the first control electrode GE1 (e.g., along the third direction DR3, which may be orthogonal to the upper surface of the base layer BL) might not be doped, and opposite side areas (e.g., an input area and an output area) of the channel area may be doped. In an exemplary embodiment of the present invention, the doping may be performed by using an n-type dopant, e.g., pentad. Thus, the first semiconductor pattern OSP1 may be formed.

[0102] Referring to FIG. 5C, the second insulation layer 20 is formed on the first area NBA and the second area BA of the first insulation layer 10 to substantially cover the first control electrode GE1. The second control electrode GE2 non-overlapping the first control electrode GE1 (e.g., along the third direction DR3, which may be orthogonal to the upper surface of the base layer BL) is formed on the second insulation layer 20. The upper electrode UE may be formed in the same process as that of the second control electrode GE2. The second electrode E2 (see, e.g., FIG. 3C) of the capacitor Cst may be formed through the same process as that of the upper electrode UE.

[0103] Referring to FIG. 5D, the third insulation layer 30 substantially covering the second control electrode GE2 and the upper electrode UE is formed on the first area NBA and the second area BA of the second insulation layer 20. Referring to FIG. 5E, a portion of the insulation layers 10 to 30 may be removed (e.g., which may be referred to herein as a first etching process). The contact holes CH1 and CH2 respectively exposing the input area and the output area of the first semiconductor pattern OSP1 may be defined. In the same process, a first upper groove GV-21 may be formed by partially removing the second area BA of the first to third insulation layers 10 to 30. As a process of forming the contact hole of the first area NBA and a process of forming the groove of the second area BA are performed in a single process, the number of masks used in the manufacturing process may be reduced.

[0104] Referring to FIG. 5F, a second preliminary semiconductor pattern OSP2-P is formed on the third insulation layer 30. The second preliminary semiconductor pattern OSP2-P may include a metal oxide semiconductor material. The second preliminary semiconductor pattern OSP_2-P may be formed from the metal oxide semiconductor layer through a photolithography process.

[0105] According to an exemplary embodiment of the present invention, a sequence of performing a process described with reference to FIG 5E and a process described with reference to FIG. 5F may be reversed. In an exemplary embodiment of the present invention, after the second preliminary semiconductor pattern OSP2-P is formed, the first and second contact holes CH1 and CH2 and the first upper groove GV-21 may be defined.

[0106] Referring to FIG. 5G, the electrodes DE1, SE1, SE2, and DE2 are formed on the third insulation layer 30 (e.g., which may be referred to herein as an electrode forming process). After the conductive layer is formed through a deposition process, the electrodes DE1, SE1, SE2, and DE2 may be formed through a patterning process.

[0107] The process of patterning the conductive layer may be performed by an etching gas including plasma. The etching gas may include plasma containing oxygen. The etching gas may decrease a hydrogen concentration of an area of the second preliminary semiconductor pattern OSP2-P, which is exposed from the second input electrode DE2 and the second output electrode SE2. Thus, the area of the second preliminary semiconductor pattern OSP2-P, which is exposed from the second input electrode DE2 and the second output electrode SE2, may be changed into the channel area having a semiconductor feature while having a resistance greater than that of the areas covered by the second input electrode DE2 and the second output electrode SE2. Thus, the second semiconductor pattern OSP2 including the input area and the output area, which are spaced apart from each other with a channel area therebetween may be formed from the second preliminary semiconductor pattern OSP2-P.

[0108] Referring to FIG. 5H, the fourth insulation layer 40 substantially covering the electrodes DE1, SE1, SE2, and DE2 is formed on the third insulation layer 30. A portion of the fourth insulation layer 40 may be disposed in the first upper groove GV-21.

[0109] Referring to FIG. 5I, a portion of the fourth insulation layers 40 may be removed (e.g., which may be referred to herein as a second etching process). A contact hole CH_3-40 exposing the first output electrode SE1 may be formed. In the same process, a second upper groove GV-22 may be formed by partially removing the second area BA of the fourth insulation layer 40. As a process of forming the contact hole of the first area NBA and a process of forming the groove of the second area BA are performed in a single process, the number of masks used in the manufacturing process may be reduced.

[0110] Although an inner surface of the second upper groove GV-22 and an inner surface of the first upper groove GV-21 may be aligned with each other, exemplary embodiments of the present invention are not limited thereto. For example, a top surface of the third insulation layer 30 may be exposed from the fourth insulation layer 40. For example, the inner surface of the second upper groove GV-22 may be spaced apart from the inner sur-

face of the first upper groove GV-21 along the first direction DR1 to expose the top surface of the third insulation layer 30 facing away from the base layer BL.

[0111] Referring to FIG. 5J, a portion of the inorganic layers BRL and BFL is removed (e.g., which may be referred to herein as a third etching process). The lower groove GV-1 may be formed by partially removing the second area BA of the barrier layer BRL and the buffer layer BFL by using an etching gas. The top surface of the uppermost inorganic layer of the inorganic layers included in the barrier layer BRL and the buffer layer BFL may be exposed from the first to fourth insulation layers 10 to 40. In an exemplary embodiment of the present invention, an inner surface of the lower groove GV-1 may be aligned with the inner surface of the first upper groove GV-21.

[0112] Referring to FIG. 5K, the fifth insulation layer 50 may be formed on the fourth insulation layer 40. The fifth insulation layer 50 may overlap the first area NBA and the second area BA (e.g., along the third direction DR3, which may be orthogonal to the upper surface of the base layer BL). The fifth insulation layer 50 is disposed in the lower groove GV-1 and the upper groove GV-2. The fifth insulation layer 50 may partially fill the contact hole CH3-40.

[0113] Referring to FIG. 5L, a portion of the fifth insulation layers 50 may be removed (e.g., which may be referred to herein as a fourth etching process). A contact hole CH3-50 may be formed in the fifth insulation layer 50 and a contact hole CH3-40 may be formed in the fourth insulation layer 40 to expose the first output electrode SE1 substantially covered by the fifth insulation layer 50 and the fourth insulation layer 40.. A contact hole CH3-50 of the fifth insulation layer 50 may be aligned with the contact hole CH3-40 of the fourth insulation layer 40. Thus, the contact holes CH3-40 and CH3-50 may define a third contact hole CH3.

[0114] Referring to FIG. 5M, the connection electrode CNE may be formed on the fifth insulation layer 50. A portion of the signal line DL overlapping the second area BA (e.g., along the third direction DR3, which may be orthogonal to the upper surface of the base layer BL) may be formed through the same process as that of the connection electrode CNE.

[0115] Referring to FIG. 5N, the sixth insulation layer 60 substantially covering the portion overlapping the second area BA of the connection electrode CNE and the signal line DL may be formed on the fifth insulation layer 50. A fourth contact hole CH4 exposing a top surface of the connection electrode CNE may be formed in the sixth insulation layer 60.

[0116] Referring to FIG. 5O, the organic light emitting diode OLED may be formed on the sixth insulation layer 60. The anode AE connected to the connection electrode CNE through a fourth contact hole CH4 may be formed on the sixth insulation layer 60. The pixel defining layer PDL exposing a central portion of the anode AE may be formed on the sixth insulation layer 60. After a preliminary pixel defining layer is formed on the sixth insulation layer 60, the opening OP may be formed in the preliminary pixel defining layer.

[0117] The hole control layer HCL, the light emitting layer EML, the electron control layer ECL, and the cathode CE may be sequentially formed on the first area NBA of the pixel defining layer PDL. The hole control layer HCL, the light emitting layer EML, the electron control layer ECL, and the cathode CE may overlap at least the display area DP-DA ((e.g., along the third direction DR3, which may be orthogonal to the upper surface of the base layer BL; see, e.g., FIG. 2).

[0118] The thin-film encapsulation layer TFE may be formed on the cathode CE. The encapsulation organic layer and/or the encapsulation inorganic layer may be formed through a deposition or inkjet printing process. Although the thin-film encapsulation layer TFE may be formed on the first area NBA and might not be formed on the second area BA, exemplary embodiments of the present invention are not limited thereto.

[0119] FIG. 6 is a cross-sectional view of a display panel according to an exemplary embodiment of the present invention. FIG. 7 is a cross-sectional view of a display panel according to an exemplary embodiment of the present invention. FIGS. 8A, 8B, 8C, 8D and 8E are cross-sectional views illustrating a portion of a display panel according to an exemplary embodiment of the present invention. FIG. 9 is a cross-sectional view of a portion of a display panel according to an exemplary embodiment of the present invention.

[0120] Duplicative descriptions of components that are the same or substantially the same as those described above with reference to FIGS. 1, 2, 3A, 3B, 3C, 4A, 4B, 5A, 5B, 5C, 5D, 5E, 5F, 5G, 5H, 5I, 5J, 5K, 5L, 5M, 5N and 5O may be omitted below.

[0121] Referring to FIG. 6, an arrangement relationship between the second semiconductor pattern OSP2 and both the second input electrode DE2 and the second output electrode SE2 may be varied. As the second semiconductor pattern OSP2 may be formed after the second input electrode DE2 and the second output electrode SE2 are formed, opposite ends of the second semiconductor pattern OSP2 may be directly disposed on the second input electrode DE2 and the second output electrode SE2.

[0122] Referring to FIG. 7, the connection electrode CNE and the sixth insulation layer 60 may be omitted. The anode AE may be directly disposed on the fifth insulation layer 50 and connected to the first output electrode SE1 through the third contact hole CH3. The portion of the signal line DL overlapping the second area BA (e.g., along the third direction DR3, which may be orthogonal to the upper surface of the base layer BL) may be directly disposed on the fifth insulation layer 50.

[0123] The portion of the data line DL overlapping the second area BA may be formed through the same process as that of the anode AE. Thus, the portion of the data line DL overlapping the second area BA and the anode

AE may include a same material and may have a same layer structure as each other.

[0124] FIGS. 8A, 8B, 8C, 8D and 8E illustrate display panels DP corresponding to the display panel DP described with reference to FIG. 5O. The display panels DP described with reference to FIGS. 8A to 8E and the display panel DP described with reference to FIG. 5O may be different in a shape of the signal line DL.

[0125] Referring to FIGS. 8A to 8E, the signal line (e.g., data lines DL) may include a first portion DL-P1, a second portion DL-P2, and a third portion DL-P3. The first portion DL-P1 may be connected to the pixel PX (see, e.g., FIG. 2), and the third portion DL-P3 may be connected to the corresponding signal pad DP-PD (see, e.g., FIG. 2) or a driving chip. The second portion DL-P2 may connect the first portion DL-P1 to the third portion DL-P3 through the fifth contact hole CH5 and the sixth contact hole CH6. The second portion DL-P2 may overlap the curvature area CA (e.g., along the third direction DR3, which may be orthogonal to the upper surface of the base layer BL).

[0126] Referring to FIGS. 8A to 8E, according to an exemplary embodiment of the present invention, the fifth contact hole CH5 may extend to substantially a same depth as the sixth contact hole CH6 along the direction orthogonal to the upper surface of the base layer BL. A bottom surface of the first portion DL-P1 of the signal line facing the base layer BL may be positioned at a first depth above the base layer BL which is substantially the same as a depth of a bottom surface of the third portion DL-P3 of the signal line facing the base layer BL.

[0127] Alternatively, according to an exemplary embodiment of the present invention, the bottom surface of the first portion DL-P1 of the signal line facing the base layer BL may be positioned at depth above the base layer BL that is different from a depth of a bottom surface of the third portion DL-P3 of the signal line facing the base layer BL.

[0128] Referring to FIG. 8A, the first portion DL-P1 and the third portion DL-P3 may be formed through the same process as that of the input electrodes and the output electrodes DE1, SE1, SE2, and DE2 and may be disposed on the same layer as that of the input electrodes and the output electrodes DE1, SE1, SE2, and DE2. Each of the fifth contact hole CH5 and the sixth contact hole CH6 may pass through the fourth insulation layer 40 and the fifth insulation layer 50. Each of the fifth contact hole CH5 and the sixth contact hole CH6 may be formed through the same process as that of the third contact hole CH3.

[0129] Referring to FIG. 8B, the first portion DL-P1 and the third portion DL-P3 may be formed through the same process as that of the upper electrode UE and may be disposed on the same layer as that of the upper electrode UE. Each of the fifth contact hole CH5 and the sixth contact hole CH6 may pass through the third insulation layer 30, the fourth insulation layer 40, and the fifth insulation layer 50. Each of the fifth contact hole CH5 and the sixth contact hole CH6 may be formed through the same process as that of the third contact hole CH3 and may further pass through the third insulation layer 30. In an exemplary embodiment of the present invention, a photolithography process for forming the fifth contact hole CH5 and the sixth contact hole CH6 may be performed.

[0130] Referring to FIG. 8C, the first portion DL-P1 and the third portion DL-P3 may be formed through the same process as that of the first control electrode GE1 and may be disposed on the same layer as that of the first control electrode GE1. Each of the fifth contact hole CH5 and the sixth contact hole CH6 may pass through the second insulation layer 20, the third insulation layer 30, the fourth insulation layer 40, and the fifth insulation layer 50. Each of the fifth contact hole CH5 and the sixth contact hole CH6 may be formed through the same process as that of the third contact hole CH3 and may further pass through the second and third insulation layers 20 and 30. In an exemplary embodiment of the present invention, the photolithography process for forming the fifth contact hole CH5 and the sixth contact hole CH6 may be performed.

[0131] One of the first portion DL-P1 and the third portion DL-P3 may be formed through the same process of that of one of the first input electrode DE1, the upper electrode UE, and the first control electrode GE1 and may be disposed on the same layer as that of the first input electrode DE1, the upper electrode UE, or the first control electrode GE1, and the other of the first portion DL-P1 and the third portion DL-P3 may be formed through the same process of that of one of the first input electrode DE1, the upper electrode UE, and the first control electrode GE1 and disposed on the same layer as that of the first input electrode DE1, the upper electrode UE, or the first control electrode GE1. According to the position of each of the first portion DL-P1 and the third portion DL-P3, the insulation layers through which each of the fifth contact hole CH5 and the sixth contact hole CH6 passes may be changed. Each of the fifth contact hole CH5 and the sixth contact hole CH6 may be formed through the same process as that of the third contact hole CH3. Thus, depths of the fifth contact hole CH5 and the sixth contact hole CH6 may be differently controlled.

[0132] For example, referring to FIG. 8D, the first portion DL-P1 may be formed through the same process as that of the upper electrode UE and may be disposed on the same layer as that of the upper electrode UE. The third portion DL-P3 may be formed through the same process as that of the first input electrode DE1 and may be disposed on the same layer as that of the s first input electrode DE1. The fifth contact hole CH5 may pass through the third insulation layer 30, the fourth insulation layer 40, and the fifth insulation layer 50, and the sixth contact hole CH6 may pass through the fourth insulation layer 40 and the fifth insulation layer 50.

[0133] Referring to FIG. 8E, the first portion DL-P1 may be formed through the same process as that of the first control electrode GE1 and may be disposed on the same layer as that of the first control electrode GE1. The third

portion DL-P3 may be formed through the same process as that of the upper electrode UE and may be disposed on the same layer as that of the upper electrode UE. The fifth contact hole CH5 may pass through the second insulation layer 20, the third insulation layer 30, the fourth insulation layer 40, and the fifth insulation layer 50, and the sixth contact hole CH6 may pass through the third insulation layer 30, the fourth insulation layer 40, and the fifth insulation layer 50.

[0134] Although the second portion DL-P2 may be formed through the same process as that of the connection electrode CNE and may be disposed on the same layer as that of the connection electrode CNE, exemplary embodiments of the present invention are not limited thereto. The second portion DL-P2 may be formed through the same process as that of the anode AE and may be disposed on the same layer as that of the anode AE. Referring to FIG. 9, the display panel DP may include a light blocking pattern LSP disposed between the fifth insulation layer 50 and the sixth insulation layer 60 and overlapping the second semiconductor pattern OSP2 (e.g., along the third direction DR3, which may be orthogonal to the upper surface of the base layer BL).

[0135] The light blocking pattern LSP may include a material having a relatively high light absorption rate or a relatively high light reflection rate. The light blocking pattern LSP may be disposed above the second semiconductor pattern OSP2 to block light that is generated from the organic light emitting diode OLED and then reflected from being incident into the second semiconductor pattern OSP2.

[0136] The light blocking pattern LSP may include a same material as that of the connection electrode CNE. For example, the light blocking pattern LSP may include a metal.

[0137] As described above, the leakage current of the switching transistor may decrease. Thus, the accuracy and reliability of the voltage-current of the driving transistor may be increased. As the input electrode and the output electrode of the driving transistor, which are disposed on the same layer as that of the input electrode and the output electrode of the switching transistor, may be directly connected to the silicon semiconductor pattern through the contact hole passing through the insulation layers, an occurrence of a misalignment may be reduced or eliminated.

[0138] As the groove may be defined in the inorganic layers of the bending area, and the organic layer may be disposed in the corresponding groove, the bending area of the display panel may have increased flexibility. As the organic layer may be disposed in each of the bending area and the non-bending area, the display panel may have a simplified structure (e.g., may be manufactured using a relatively lower number of etching masks).

[0139] As the process of forming the contact hole exposing a portion of the semiconductor pattern disposed on the display area and the process of removing the insulation layer of the bending area may be performed in the single process, the number of masks used in the manufacturing process may decrease. As the input electrode and the output electrode of the switching transistor and the input electrode and the output electrode of the driving transistor may be formed by the single process, the manufacturing process may be simplified.

[0140] While the present invention has been shown and described with reference to the exemplary embodiments thereof, it will be apparent to those of ordinary skill in the art that various changes in form and detail may be made thereto without departing from the scope of the present invention as defined by the claims.

Claims

1. A display panel comprising:

a base layer (BL) comprising a first area (NBA) and a second area (BA) extending and bent from the first area (NBA), wherein the second area comprises a curvature area (CA);

at least one inorganic layer (BRL, BFL) disposed on the base layer (BL) overlapping the first area (NBA) and the second area (BA) and comprising a lower groove (GV-1) disposed in the curvature area (CA);

a first thin-film transistor (T1) disposed on the at least one inorganic layer and comprising a silicon semiconductor pattern (OSP1) overlapping the first area (NBA);

a second thin-film transistor (T2) disposed on the at least one inorganic layer and comprising an oxide semiconductor pattern (OSP2) overlapping the first area (NBA);

a plurality of insulation layers (10, 20, 30, 40) overlapping the first area (NBA) and the second area (BA) and comprising an upper groove (GV-2) extending from the lower groove (GV-1);

a signal line (SGL) electrically connected to the second thin-film transistor (T2);

an organic layer (50) disposed on the first area (NBA) and the second area (BA) and disposed in the lower groove (GV-1) and the upper groove (GV-2); and

a light emitting element (OLED) disposed on the organic layer (50) and overlapping the first area (NBA),

wherein the insulation layers (10, 20, 30, 40) comprise:

a first insulation layer (10) substantially covering an upper surface of the silicon semiconductor pattern (OSP1) of the first thin-film transistor (T1);

a second insulation (20) layer disposed on the first insulation layer (10) and substantially covering upper and side surfaces of a

control electrode (GE1) of the first thin-film transistor (T1);
a third insulation layer (30) disposed on the second insulation layer (20) and substantially covering upper and side surfaces of a control electrode (GE2) of the second thin-film transistor (T2); and
a fourth insulation layer (40) disposed on the third insulation layer (30) and substantially covering upper and side surfaces of an input electrode (DE2) of the second thin-film transistor (T2), substantially covering upper and side surfaces of an output electrode (SE2) of the second thin-film transistor (T2), and substantially covering an upper surface of the oxide semiconductor pattern (OSP2) of the second thin-film transistor (T2),
wherein the oxide semiconductor pattern (OSP2) of the second thin-film transistor (T2) is disposed on the third insulation layer (30), and
wherein the first thin-film transistor (T1) is a top-gate type thin-film transistor and the second thin-film transistor (T2) is a bottom-gate type thin-film transistor.

2. The display panel of claim 1, wherein a portion of the signal line (SGL), which overlaps the second area (BA), is disposed on the organic layer (50).

3. The display panel of claim 1 or 2, further comprising a connection electrode (CNE) disposed on the organic layer (50) and connected to an output electrode (SE1) of the first thin-film transistor (T1) through a contact hole (CH3) formed in the organic layer (50).

4. The display panel of any one of the preceding claims, further comprising a passivation layer (60) disposed on the organic layer (50).

5. The display panel of claim 4, wherein an electrode (AE) of the light emitting element (OLED) is connected to the connection electrode (CNE) through a contact hole (CH4) formed in the passivation layer (60).

6. The display panel of claim 4 or 5, wherein the passivation layer (60) is disposed on the signal line (SGL), and
a portion of the passivation layer (60), which overlaps the second area (BA), is in direct contact with the signal line (SGL).

7. The display panel of claim 1, wherein a first portion and a second portion of the oxide semiconductor pattern (OSP2) are disposed on the input electrode (DE2) and the output electrode (SE2) of the second thin-film transistor (T2), respectively.

8. The display panel of claim 1 or 7, wherein the input electrode (DE2) and the output electrode (SE2) of the second thin-film transistor (T2) are disposed above a first portion and a second portion of the oxide semiconductor pattern (OSP2), respectively, and a third portion of the oxide semiconductor pattern (OSP2) is exposed from the input electrode (DE2) and the output electrode (SE2) of the second thin-film transistor (T2).

9. The display panel of claim 1, 7 or 8, further comprising an upper electrode (UE) disposed between the second insulation layer (20) and the third insulation layer (30), and overlapping the control electrode (GE1) of the first thin-film transistor (T1).

10. The display panel of any one of the preceding claims, further comprising a light blocking pattern (LSP) disposed on the organic layer (50) and overlapping the oxide semiconductor pattern (OSP2) of the second thin-film transistor (T2).

11. The display panel of any one of the preceding claims, wherein the at least one inorganic layer comprises silicon oxide layers and silicon nitride layers disposed alternately with the silicon oxide layers.

12. The display panel of any one of the preceding claims, wherein a portion of a top surface of the at least one inorganic layer is in direct contact with the organic layer (50).

13. A method for manufacturing a display panel, comprising:

forming, on a base layer (BL) comprising a first area (NBA) and a second area (BA), extending and bent from the first area (NBA), wherein the second area comprises a curvature area (CA), at least one inorganic layer overlapping the first area (NBA) and the second area (BA) along a direction orthogonal to an upper surface of the base layer (BL);
forming a silicon semiconductor pattern (OSP1) on the at least one inorganic layer to overlap the first area (NBA) along the direction orthogonal to the upper surface of the base layer (BL);
forming a first control electrode (GE1) on a first insulation layer (10) to overlap the silicon semiconductor pattern (OSP1) along the direction orthogonal to the upper surface of the base layer (BL), wherein the first insulation layer (10) overlaps the first area (NBA) and the second area (BA) along the direction orthogonal to the upper surface of the base layer (BL);
forming a second control electrode (GE2)

spaced apart from the first control electrode (GE1) on a second insulation layer (20) overlapping the first area (NBA) and the second area (BA) along the direction orthogonal to the upper surface of the base layer (BL), wherein the second insulation layer (20) substantially covers upper and side surfaces of the first control electrode (GE1);
forming a third insulation layer (30) overlapping the first area (NBA) and the second area (BA) along the direction orthogonal to the upper surface of the base layer (BL), wherein the third insulation layer (30) substantially covers upper and side surfaces of the second control electrode (GE2);
performing a first etching partially removing the first, second and third insulation layers (10, 20, 30) to form a first contact hole (CH1) and a second contact hole (CH2) exposing a first portion and a second portion of the silicon semiconductor pattern (OSP1), respectively, and to form a first upper groove (GV-21) exposing the at least one inorganic layer in the second area (BA);
forming an oxide semiconductor pattern (OSP2) overlapping the second control electrode (GE2) on the third insulation layer (30) along the direction orthogonal to the upper surface of the base layer (BL);
forming a first input electrode (DE1) and a first output electrode (SE1), which are connected to the silicon semiconductor pattern (OSP1) through the first contact hole (CH1) and the second contact hole (CH2), respectively, on the third insulation layer (30) and forming a second input electrode (DE2) and a second output electrode (SE2), which are connected to the oxide semiconductor pattern (OSP2), on the third insulation layer (30);
forming a fourth insulation layer (40) on the third insulation layer (30), wherein the fourth insulation layer (40) overlaps the first area (NBA) and the second area (BA) along the direction orthogonal to the upper surface of the base layer (BL);
performing a second etching partially removing the fourth insulation layer (40) to form a third contact hole (CH3-40) exposing the first output electrode (SE1) in the fourth insulation layer (40), and to form a second upper groove (GV-22) exposing the at least one inorganic layer in the second area (BA);
performing a third etching removing a portion of the at least one inorganic layer, which overlaps the second area (BA), to form a lower groove (GV-1) in the curvature area (CA) and aligned with the first upper groove (GV-21) along the direction orthogonal to the upper surface of the base layer (BL) in the at least one inorganic layer;
forming an organic layer (50) disposed on the fourth insulation layer (40) within the first area (NBA) and disposed in the first upper groove (GV-21), the second upper groove (GV-22), and the lower groove (GV-1) within the second area (BA);
performing a fourth etching partially removing the organic layer (50) to form a fourth contact hole (CH3-50) connected to the third contact hole (CH3) in the organic layer (50); and
forming a light emitting element (OLED) electrically connected to the first output electrode (CNE) on the organic layer (50),
wherein a first thin-film transistor (T1) of the display panel is a top-gate type thin-film transistor and comprises the silicon semiconductor pattern (OSP1) and a second thin-film transistor (T2) of the display panel is a bottom-gate type thin-film transistor and comprises the oxide semiconductor pattern (OSP2).

14. The method of claim 13, wherein, after forming the oxide semiconductor pattern (OSP2), forming the second input electrode (DE2) and the second output electrode (SE2), which are spaced apart from each other and each of which overlaps the oxide semiconductor pattern (OSP2) along the direction orthogonal to the upper surface of the base layer (BL).

Patentansprüche

1. Anzeigetafel, umfassend:

eine Basisschicht (BL), die einen ersten Bereich (NBA) und einen zweiten Bereich (BA) umfasst, der sich von dem ersten Bereich (NBA) erstreckt und gebogen ist, wobei der zweite Bereich einen Krümmungsbereich (CA) umfasst;
mindestens eine auf der Basisschicht (BL) angeordnete anorganische Schicht (BRL, BFL), die den ersten Bereich (NBA) und den zweiten Bereich (BA) überlappt und eine in dem Krümmungsbereich (CA) angeordnete untere Rille (GV-1) umfasst;
einen ersten Dünnschichttransistor (T1), der auf der mindestens einen anorganischen Schicht angeordnet ist und ein Silizium-Halbleitermuster (OSP1) umfasst, das den ersten Bereich (NBA) überlappt;
einen zweiten Dünnschichttransistor (T2), der auf der mindestens einen anorganischen Schicht angeordnet ist und ein Oxid-Halbleitermuster (OSP2) umfasst, das den ersten Bereich (NBA) überlappt;
eine Vielzahl von Isolierschichten (10, 20, 30, 40), die den ersten Bereich (NBA) und den zweiten Bereich (BA) überlappen und eine obere Ril-

le (GV-2) umfassen, die sich von der unteren Rille (GV-1) erstreckt;
eine Signalleitung (SGL), die elektrisch mit dem zweiten Dünnschichttransistor (T2) verbunden ist;
eine organische Schicht (50), die auf dem ersten Bereich (NBA) und dem zweiten Bereich (BA) und in der unteren Rille (GV-1) und der oberen Rille (GV-2) angeordnet ist; und
ein lichtemittierendes Element (OLED), das auf der organischen Schicht (50) angeordnet ist und den ersten Bereich (NBA) überlappt,
wobei die Isolierschichten (10, 20, 30, 40) umfassen:

eine erste Isolierschicht (10), die im Wesentlichen eine obere Fläche der Silizium-Halbleitermuster (OSP1) des ersten Dünnschichttransistors (T1) bedeckt;
eine zweite Isolierschicht (20), die auf der ersten Isolierschicht (10) angeordnet ist und im Wesentlichen obere und seitliche Flächen einer Steuerelektrode (GE1) des ersten Dünnschichttransistors (T1) bedeckt;
eine dritte Isolierschicht (30), die auf der zweiten Isolierschicht (20) angeordnet ist und im Wesentlichen obere und seitliche Flächen einer Steuerelektrode (GE2) des zweiten Dünnschichttransistors (T2) bedeckt; und
eine vierte Isolierschicht (40), die auf der dritten Isolierschicht (30) angeordnet ist und im Wesentlichen obere und seitliche Flächen einer Eingangselektrode (DE2) des zweiten Dünnschichttransistors (T2) bedeckt, im Wesentlichen obere und seitliche Flächen einer Ausgangselektrode (SE2) des zweiten Dünnschichttransistors (T2) bedeckt und im Wesentlichen eine obere Fläche des Oxid-Halbleitermusters (OSP2) des zweiten Dünnschichttransistors (T2) bedeckt,
wobei das Oxid-Halbleitermuster (OSP2) des zweiten Dünnschichttransistors (T2) auf der dritten Isolierschicht (30) angeordnet ist, und
wobei der erste Dünnschichttransistor (T1) ein Dünnschichttransistor vom Typ Top-Gate ist und der zweite Dünnschichttransistor (T2) ein Dünnschichttransistor vom Typ Bottom-Gate ist.

2. Anzeigetafel nach Anspruch 1, wobei ein Abschnitt der Signalleitung (SGL), der den zweiten Bereich (BA) überlappt, auf der organischen Schicht (50) angeordnet ist.

3. Anzeigetafel nach Anspruch 1 oder 2, ferner umfassend eine Verbindungselektrode (CNE), die auf der organischen Schicht (50) angeordnet und über ein in der organischen Schicht (50) ausgebildetes Kontaktloch (CH3) mit einer Ausgangselektrode (SE1) des ersten Dünnfilmtransistors (T1) verbunden ist.

4. Anzeigetafel nach einem der vorhergehenden Ansprüche, ferner umfassend eine Passivierungsschicht (60), die auf der organischen Schicht (50) angeordnet ist.

5. Anzeigetafel nach Anspruch 4, wobei eine Elektrode (AE) des lichtemittierenden Elements (OLED) mit der Verbindungselektrode (CNE) durch ein in der Passivierungsschicht (60) ausgebildetes Kontaktloch (CH4) verbunden ist.

6. Anzeigetafel nach Anspruch 4 oder 5, wobei die Passivierungsschicht (60) auf der Signalleitung (SGL) angeordnet ist, und
ein Abschnitt der Passivierungsschicht (60), der den zweiten Bereich (BA) überlappt, in direktem Kontakt mit der Signalleitung (SGL) ist.

7. Anzeigetafel nach Anspruch 1, wobei ein erster Abschnitt und ein zweiter Abschnitt des Oxid-Halbleitermusters (OSP2) jeweils auf der Eingangselektrode (DE2) und der Ausgangselektrode (SE2) des zweiten Dünnschichttransistors (T2) angeordnet sind.

8. Anzeigetafel nach Anspruch 1 oder 7, wobei die Eingangselektrode (DE2) und die Ausgangselektrode (SE2) des zweiten Dünnschichttransistors (T2) jeweils über einem ersten Abschnitt und einem zweiten Abschnitt des Oxid-Halbleitermusters (OSP2) angeordnet sind und ein dritter Abschnitt des Oxid-Halbleitermusters (OSP2) von der Eingangselektrode (DE2) und der Ausgangselektrode (SE2) des zweiten Dünnschichttransistors (T2) freigelegt ist.

9. Anzeigetafel nach Anspruch 1, 7 oder 8, ferner umfassend eine obere Elektrode (UE), die zwischen der zweiten Isolierschicht (20) und der dritten Isolierschicht (30) angeordnet ist und die Steuerelektrode (GE1) des ersten Dünnschichttransistors (T1) überlappt.

10. Anzeigetafel nach einem der vorhergehenden Ansprüche, ferner umfassend ein Lichtblockierungsmuster (LSP), das auf der organischen Schicht (50) angeordnet ist und das Oxid-Halbleitermuster (OSP2) des zweiten Dünnschichttransistors (T2) überlappt.

11. Anzeigetafel nach einem der vorhergehenden Ansprüche, wobei die mindestens eine anorganische Schicht Siliziumoxidschichten und Siliziumnitrid-

schichten, die abwechselnd mit den Siliziumoxidschichten angeordnet sind, umfasst.

12. Anzeigetafel nach einem der vorhergehenden Ansprüche, wobei ein Abschnitt einer oberen Fläche der mindestens einen anorganischen Schicht in direktem Kontakt mit der organischen Schicht (50) ist.

13. Verfahren zum Herstellen einer Anzeigetafel, umfassend:

Ausbilden, auf einer Basisschicht (BL), die einen ersten Bereich (NBA) und einen zweiten Bereich (BA) umfasst, der sich von dem ersten Bereich (NBA) erstreckt und gebogen ist, wobei der zweite Bereich einen Krümmungsbereich (CA), mindestens eine anorganische Schicht, die den ersten Bereich (NBA) überlappt, und den zweiten Bereich (BA) entlang einer Richtung orthogonal zu einer oberen Fläche der Basisschicht (BL) umfasst;

Ausbilden eines Silizium-Halbleitermusters (OSP1) auf der mindestens einen anorganischen Schicht, um den ersten Bereich (NBA) entlang der Richtung orthogonal zur oberen Fläche der Basisschicht (BL) zu überlappen;

Ausbilden einer ersten Steuerelektrode (GE1) auf einer ersten Isolierschicht (10), um das Silizium-Halbleitermuster (OSP1) entlang der Richtung orthogonal zur oberen Fläche der Basisschicht (BL) zu überlappen, wobei die erste Isolierschicht (10) den ersten Bereich (NBA) und den zweiten Bereich (BA) entlang der Richtung orthogonal zur oberen Fläche der Basisschicht (BL) überlappt;

Ausbilden einer zweiten Steuerelektrode (GE2), die von der ersten Steuerelektrode (GE1) im Abstand ist, auf einer zweiten Isolierschicht (20), die den ersten Bereich (NBA) und den zweiten Bereich (BA) entlang der Richtung orthogonal zur oberen Fläche der Basisschicht (BL) überlappt, wobei die zweite Isolierschicht (20) im Wesentlichen obere und seitliche Flächen der ersten Steuerelektrode (GE1) bedeckt;

Ausbilden einer dritten Isolierschicht (30), die den ersten Bereich (NBA) und den zweiten Bereich (BA) entlang der Richtung orthogonal zur oberen Fläche der Basisschicht (BL) überlappt, wobei die dritte Isolierschicht (30) im Wesentlichen obere und seitliche Flächen der zweiten Steuerelektrode (GE2) bedeckt;

Durchführen eines ersten Ätzens zum teilweisen Entfernen der ersten, zweiten und dritten Isolierschicht (10, 20, 30), um ein erstes Kontaktloch (CH1) und ein zweites Kontaktloch (CH2) auszubilden, die jeweils einen ersten Abschnitt und einen zweiten Abschnitt des Silizium-Halbleitermusters (OSP1) freilegen, und um eine erste obere Rille (GV-21) auszubilden, die die mindestens eine anorganische Schicht in dem zweiten Bereich (BA) freilegt;

Ausbilden eines Oxid-Halbleitermusters (OSP2), das die zweite Steuerelektrode (GE2) auf der dritten Isolierschicht (30) entlang der Richtung orthogonal zur oberen Fläche der Basisschicht (BL) überlappt;

Ausbilden einer ersten Eingangselektrode (DE1) und einer ersten Ausgangselektrode (SE1), die mit dem Silizium-Halbleitermuster (OSP1) jeweils durch das erste Kontaktloch (CH1) und das zweite Kontaktloch (CH2) auf der dritten Isolierschicht (30) verbunden sind, und

Ausbilden einer zweiten Eingangselektrode (DE2) und einer zweiten Ausgangselektrode (SE2), die mit dem Oxid-Halbleitermuster (OSP2) verbunden sind, auf der dritten Isolierschicht (30);

Ausbilden einer vierten Isolierschicht (40) auf der dritten Isolierschicht (30), wobei die vierte Isolierschicht (40) den ersten Bereich (NBA) und den zweiten Bereich (BA) entlang der Richtung orthogonal zur oberen Fläche der Basisschicht (BL) überlappt;

Durchführen eines zweiten Ätzens zum teilweisen Entfernen der vierten Isolierschicht (40), um ein drittes Kontaktloch (CH3-40) auszubilden, das die erste Ausgangselektrode (SE1) in der vierten Isolierschicht (40) freilegt, und um eine zweite obere Rille (GV-22) auszubilden, die die mindestens eine anorganische Schicht in dem zweiten Bereich (BA) freilegt;

Durchführen eines dritten Ätzens zum Entfernen eines Abschnitts der mindestens einen anorganischen Schicht, der den zweiten Bereich (BA) überlappt, um eine untere Rille (GV-1) in dem Krümmungsbereich (CA) auszubilden, die mit der ersten oberen Rille (GV-21) entlang der Richtung orthogonal zur oberen Fläche der Basisschicht (BL) in der mindestens einen anorganischen Schicht ausgerichtet ist;

Ausbilden einer organischen Schicht (50), die auf der vierten Isolierschicht (40) innerhalb des ersten Bereichs (NBA) angeordnet ist und in der ersten oberen Rille (GV-21), der zweiten oberen Rille (GV-22) und der unteren Rille (GV-1) innerhalb des zweiten Bereichs (BA) angeordnet ist;

Durchführen eines vierten Ätzens zum teilweisen Entfernen der organischen Schicht (50), um ein viertes Kontaktloch (CH3-50) auszubilden, das mit dem dritten Kontaktloch (CH3) in der organischen Schicht (50) verbunden ist; und

Ausbilden eines lichtemittierenden Elements (OLED), das elektrisch mit der ersten Ausgangselektrode (CNE) auf der organischen Schicht (50) verbunden ist,

wobei ein erster Dünnschichttransistor (T1) der Anzeigetafel ein Dünnschichttransistor vom Typ Top-Gate ist und das Silizium-Halbleitermuster (OSP1) umfasst und ein zweiter Dünnschichttransistor (T2) der Anzeigetafel ein Dünnschichttransistor vom Typ Bottom-Gate ist und das Oxid-Halbleitermuster (OSP2) umfasst.

14. Verfahren nach Anspruch 13, wobei nach dem Ausbilden des Oxid-Halbleitermusters (OSP2), das die zweite Eingangselektrode (DE2) und die zweite Ausgangselektrode (SE2) bildet, die voneinander im Abstand sind und von denen jede das Oxid-Halbleitermuster (OSP2) entlang der Richtung orthogonal zur oberen Fläche der Basisschicht (BL) überlappt.

Revendications

1. Panneau d'affichage comprenant :

une couche de base (BL) comprenant une première zone (NBA) et une seconde zone (BA) s'étendant et courbée à partir de la première zone (NBA), ladite seconde zone comprenant une zone de courbure (CA) ;
au moins une couche inorganique (BRL, BFL) disposée sur la couche de base (BL) chevauchant la première zone (NBA) et la seconde zone (BA) et comprenant une rainure inférieure (GV-1) disposée dans la zone de courbure (CA) ;
un premier transistor en couches minces (T1) disposé sur la au moins une couche inorganique et comprenant un motif semi-conducteur en silicium (OSP1) chevauchant la première zone (NBA) ; un second transistor en couches minces (T2) disposé sur la au moins une couche inorganique et comprenant un motif oxyde-semi-conducteur (OSP2) chevauchant la première zone (NBA) ;
une pluralité de couches d'isolation (10, 20, 30, 40) chevauchant la première zone (NBA) et la seconde zone (BA) et comprenant une rainure supérieure (GV-2) s'étendant à partir de la rainure inférieure (GV-1) ;
une ligne de signal (SGL) connectée électriquement au second transistor en couches minces (T2) ; une couche organique (50) disposée sur la première zone (NBA) et la seconde zone (BA) et disposée dans la rainure inférieure (GV-1) et la rainure supérieure (GV-2) ; et
un élément électroluminescent (OLED) disposé sur la couche organique (50) et chevauchant la première zone (NBA),
lesdites couches d'isolation (10, 20, 30, 40) comprenant :
une première couche d'isolation (10) recouvrant sensiblement une surface supérieure du motif semi-conducteur en silicium (OSP1) du premier transistor en couches minces (T1) ;
une deuxième couche d'isolation (20) disposée sur la première couche d'isolation (10) et recouvrant sensiblement les surfaces supérieure et latérales d'une électrode de commande (GE1) du premier transistor en couches minces (T1) ;
une troisième couche d'isolation (30) disposée sur la deuxième couche d'isolation (20) et recouvrant sensiblement les surfaces supérieure et latérales d'une électrode de commande (GE2) du second transistor en couches minces (T2) ; et
une quatrième couche d'isolation (40) disposée sur la troisième couche d'isolation (30) et recouvrant sensiblement les surfaces supérieure et latérales d'une électrode d'entrée (DE2) du second transistor en couches minces (T2), recouvrant sensiblement les surfaces supérieure et latérales d'une électrode de sortie (SE2) du second transistor en couches minces (T2), et
recouvrant sensiblement une surface supérieure du motif oxyde-semi-conducteur (OSP2) du second transistor en couches minces (T2),
ledit motif oxyde-semi-conducteur (OSP2) du second transistor en couches minces (T2) étant disposé sur la troisième couche d'isolation (30), et
ledit premier transistor en couches minces (T1) étant un transistor en couches minces de type à grille supérieure et ledit second transistor en couches minces (T2) étant un transistor en couches minces de type à grille inférieure.

2. Panneau d'affichage de la revendication 1, une partie de la ligne de signal (SGL), qui chevauche la seconde zone (BA), étant disposée sur la couche organique (50).

3. Panneau d'affichage de la revendication 1 ou 2, comprenant en outre une électrode de connexion (CNE) disposée sur la couche organique (50) et connectée à une électrode de sortie (SE1) du premier transistor en couches minces (T1) à travers un trou de contact (CH3) formé dans la couche organique (50).

4. Panneau d'affichage de l'une quelconque des revendications précédentes, comprenant en outre une couche de passivation (60) disposée sur la couche organique (50).

5. Panneau d'affichage de la revendication 4, une électrode (AE) de l'élément électroluminescent (OLED) étant connectée à l'électrode de connexion (CNE) par l'intermédiaire d'un trou de contact (CH4) formé dans la couche de passivation (60).

6. Panneau d'affichage de la revendication 4 ou 5, ladite couche de passivation (60) étant disposée sur la ligne de signal (SGL), et
une partie de la couche de passivation (60), qui chevauche la seconde zone (BA), étant en contact direct avec la ligne de signal (SGL).

7. Panneau d'affichage de la revendication 1, une première partie et une seconde partie du motif oxyde-semi-conducteur (OSP2) étant disposées respectivement sur l'électrode d'entrée (DE2) et l'électrode de sortie (SE2) du second transistor en couches minces (T2).

8. Panneau d'affichage de la revendication 1 ou 7, ladite électrode d'entrée (DE2) et ladite électrode de sortie (SE2) du second transistor en couches minces (T2) étant disposées, respectivement, au-dessus d'une première partie et d'une seconde partie du motif oxyde-semi-conducteur (OSP2) et une troisième partie du motif oxyde-semi-conducteur (OSP2) étant exposée à partir de l'électrode d'entrée (DE2) et de l'électrode de sortie (SE2) du second transistor en couches minces (T2).

9. Panneau d'affichage de la revendication 1, 7 ou 8, comprenant en outre une électrode supérieure (UE) disposée entre la deuxième couche d'isolation (20) et la troisième couche d'isolation (30), et chevauchant l'électrode de commande (GE1) du premier transistor en couches minces (T1).

10. Panneau d'affichage de l'une quelconque des revendications précédentes, comprenant en outre un motif de blocage de lumière (LSP) disposé sur la couche organique (50) et chevauchant le motif oxyde-semi-conducteur (OSP2) du second transistor en couches minces (T2).

11. Panneau d'affichage de l'une quelconque des revendications précédentes, ladite au moins une couche inorganique comprenant des couches d'oxyde de silicium et des couches de nitrure de silicium disposées en alternance avec les couches d'oxyde de silicium.

12. Panneau d'affichage de l'une quelconque des revendications précédentes, une partie d'une surface supérieure de la au moins une couche inorganique étant en contact direct avec la couche organique (50).

13. Procédé permettant la fabrication d'un panneau d'affichage, comprenant :

la formation, sur une couche de base (BL) comprenant une première zone (NBA) et une seconde zone (BA) s'étendant et courbée à partir de la première zone (NBA), ladite seconde zone comprenant une zone de courbure (CA), au moins une couche inorganique chevauchant la première zone (NBA) et la seconde zone (BA) le long d'une direction orthogonale à une surface supérieure de la couche de base (BL) ;
la formation d'un motif semi-conducteur en silicium (OSP1) sur la au moins une couche inorganique pour chevaucher la première zone (NBA) le long de la direction orthogonale à la surface supérieure de la couche de base (BL) ;
la formation d'une première électrode de commande (GE1) sur une première couche d'isolation (10) pour chevaucher le motif semi-conducteur en silicium (OSP1) le long de la direction orthogonale à la surface supérieure de la couche de base (BL), ladite première couche d'isolation (10) chevauchant la première zone (NBA) et la seconde zone (BA) le long de la direction orthogonale à la surface supérieure de la couche de base (BL) ;
la formation d'une seconde électrode de commande (GE2) espacée de la première électrode de commande (GE1) sur une deuxième couche d'isolation (20) chevauchant la première zone (NBA) et la seconde zone (BA) le long de la direction orthogonale à la surface supérieure de la couche de base (BL), ladite deuxième couche d'isolation (20) recouvrant sensiblement les surfaces supérieure et latérales de la première électrode de commande (GE1) ;
la formation d'une troisième couche d'isolation (30) chevauchant la première zone (NBA) et la seconde zone (BA) le long de la direction orthogonale à la surface supérieure de la couche de base (BL), ladite troisième couche d'isolation (30) recouvrant sensiblement des surfaces supérieure et latérale de la seconde électrode de commande (GE2) ;
la réalisation d'une première gravure enlevant partiellement les première, deuxième et troisième couches d'isolation (10, 20, 30) pour former un premier trou de contact (CH1) et un deuxième trou de contact (CH2) exposant respectivement une première partie et une deuxième partie du motif semi-conducteur en silicium (OSP1), et pour former une première rainure supérieure (GV-21) exposant la au moins une couche inorganique dans la seconde zone (BA) ;
la formation d'un motif oxyde-semi-conducteur (OSP2) chevauchant la seconde électrode de commande (GE2) sur la troisième couche d'iso-

lation (30) le long de la direction orthogonale à la surface supérieure de la couche de base (BL) ;

la formation d'une première électrode d'entrée (DE1) et d'une première électrode de sortie (SE1), qui sont connectées, respectivement, au motif semi-conducteur en silicium (OSP1) à travers le premier trou de contact (CH1) et le deuxième trou de contact (CH2) sur la troisième couche d'isolation (30) et la formation d'une seconde électrode d'entrée (DE2) et d'une seconde électrode de sortie (SE2), qui sont connectées au motif oxyde-semi-conducteur (OSP2), sur la troisième couche d'isolation (30) ;

la formation d'une quatrième couche d'isolation (40) sur la troisième couche d'isolation (30), ladite quatrième couche d'isolation (40) chevauchant la première zone (NBA) et la seconde zone (BA) le long de la direction orthogonale à la surface supérieure de la couche de base (BL) ;

la réalisation d'une deuxième gravure enlevant partiellement la quatrième couche d'isolation (40) pour former un troisième trou de contact (CH3-40) exposant la première électrode de sortie (SE1) dans la quatrième couche d'isolation (40), et pour former une seconde rainure supérieure (GV-22) exposant la au moins une couche inorganique dans la seconde zone (BA) ;

la réalisation d'une troisième gravure enlevant une partie de la au moins une couche inorganique, qui chevauche la seconde zone (BA), pour former une rainure inférieure (GV-1) dans la zone de courbure (CA) et alignée avec la première rainure supérieure (GV-21) le long de la direction orthogonale à la surface supérieure de la couche de base (BL) dans la au moins une couche inorganique ;

la formation d'une couche organique (50) disposée sur la quatrième couche d'isolation (40) dans la première zone (NBA) et disposée dans la première rainure supérieure (GV-21), la seconde rainure supérieure (GV-22) et la rainure inférieure (GV-1) dans la seconde zone (BA) ;

la réalisation d'une quatrième gravure enlevant partiellement la couche organique (50) pour former un quatrième trou de contact (CH3-50) connecté au troisième trou de contact (CH3) dans la couche organique (50) ; et

la formation d'un élément électroluminescent (OLED) connecté électriquement à la première électrode de sortie (CNE) sur la couche organique (50),

un premier transistor en couches minces (T1) du panneau d'affichage étant un transistor en couches minces de type à grille supérieure et comprenant le motif semi-conducteur en silicium (OSP1) et un second transistor en couches minces (T2) du panneau d'affichage étant un transistor en couches minces de type à grille inférieure et comprenant le motif oxyde-semi-conducteur (OSP2).

14. Procédé de la revendication 13, après la formation du motif oxyde-semi-conducteur (OSP2), la formation de la seconde électrode d'entrée (DE2) et de la seconde électrode de sortie (SE2), qui sont espacées l'une de l'autre et dont chacune chevauche le motif oxyde-semi-conducteur (OSP2) le long de la direction orthogonale à la surface supérieure de la couche de base (BL).

FIG. 1A

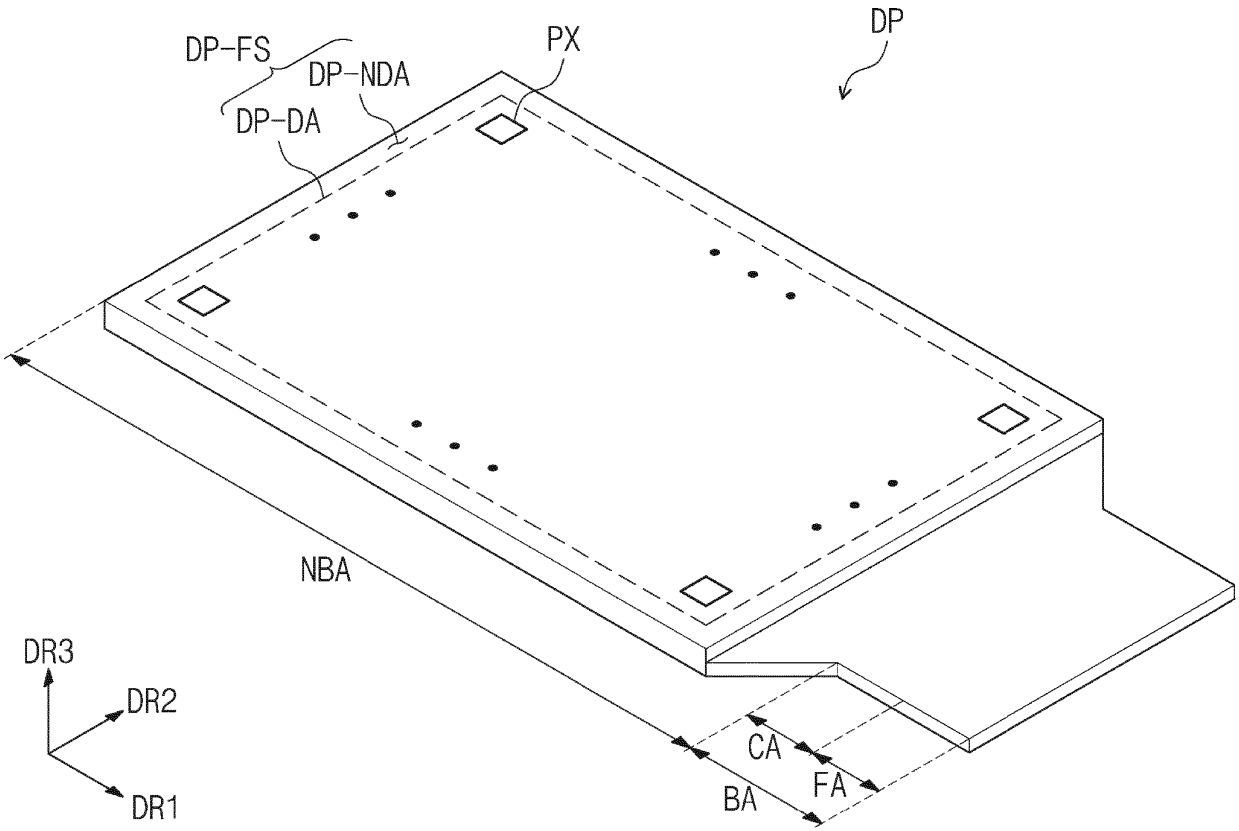


FIG. 1B

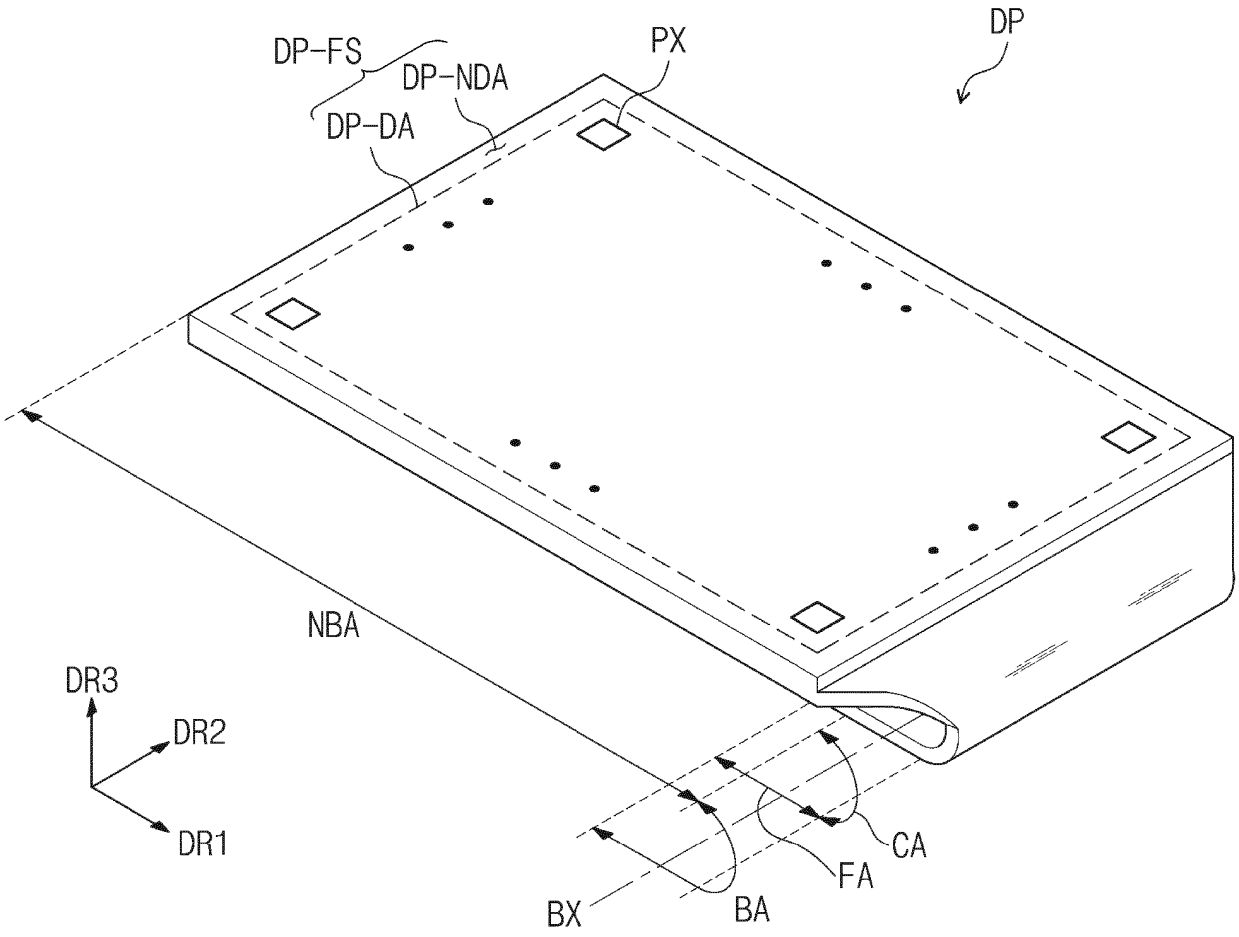


FIG. 2

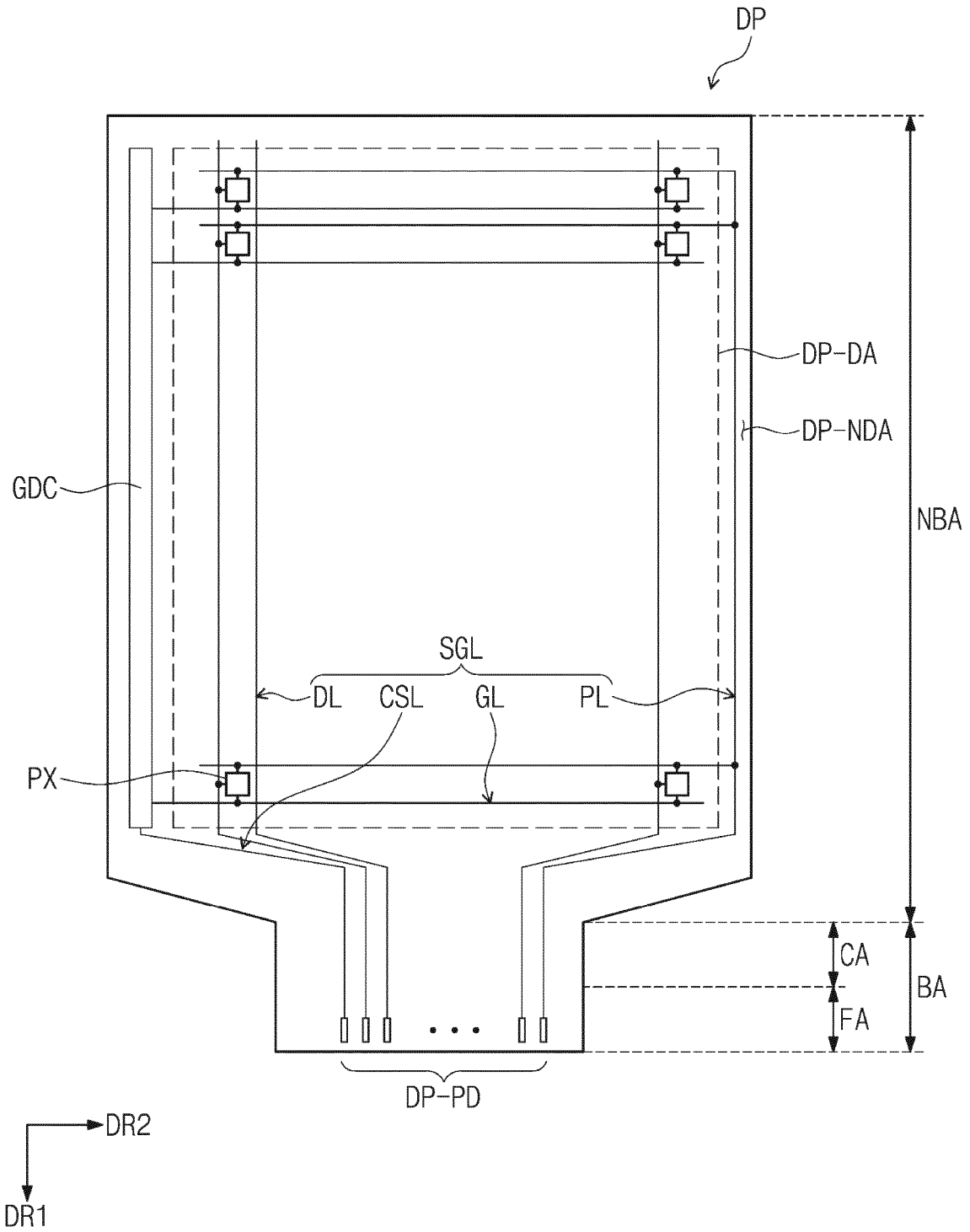


FIG. 3A

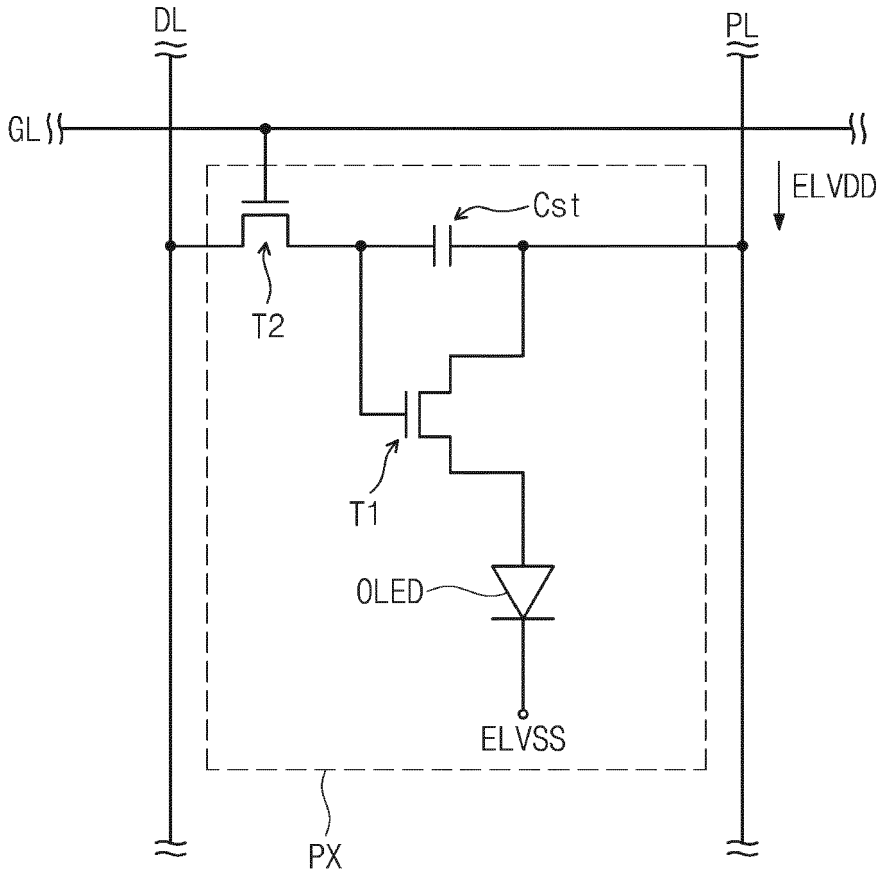


FIG. 3B

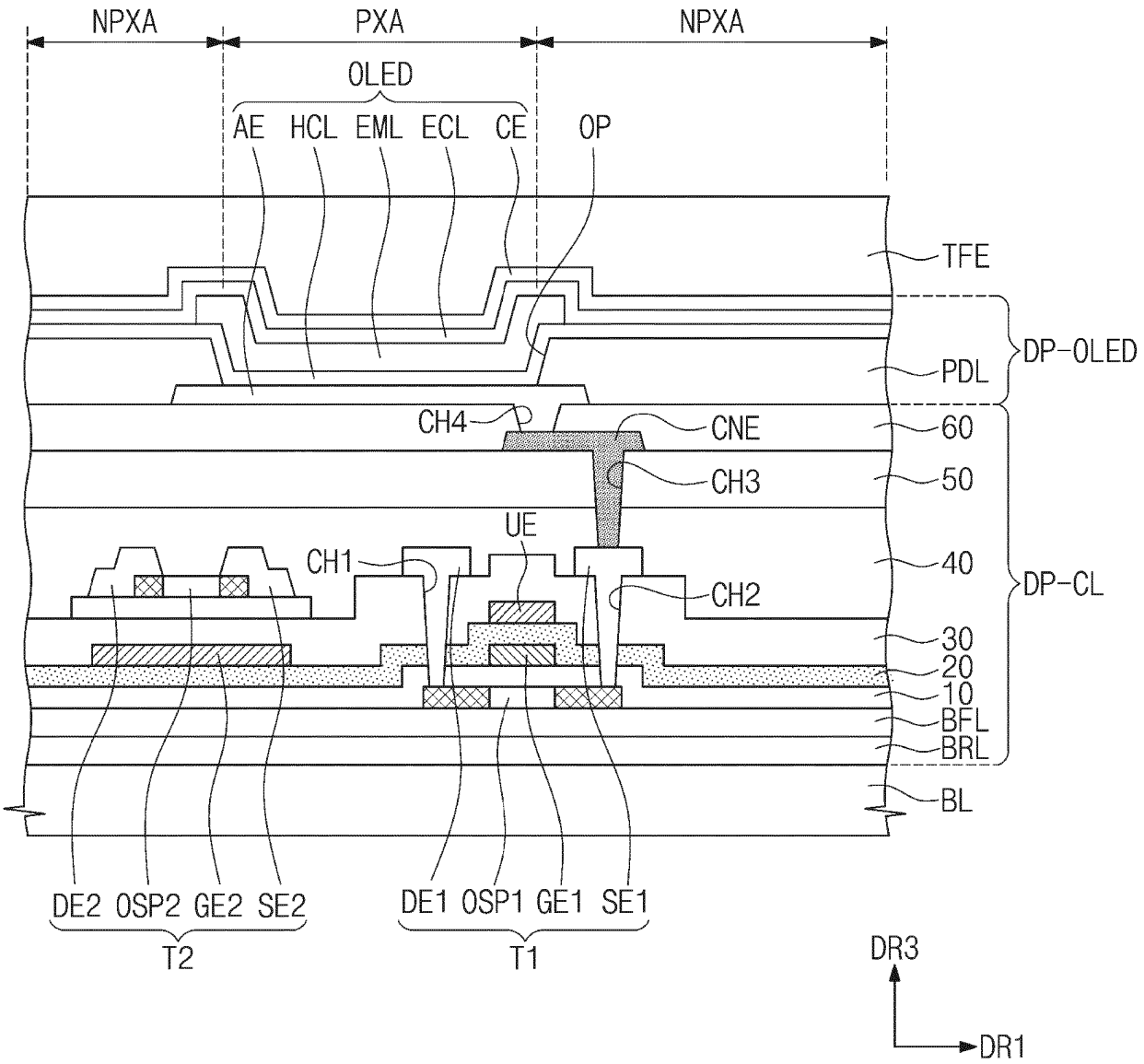

NPXA
PXA
NPXA
OLED
AE
HCL
EML
ECL
CE
OP
TFE
PDL
DP-OLED
CH4
CNE
60
CH3
50
UE
CH1
40
DP-CL
CH2
30
20
10
BFL
BRL
BL
DE2
OSP2
GE2
SE2
T2
DE1
OSP1
GE1
SE1
T1
DR3
DR1

FIG. 3C

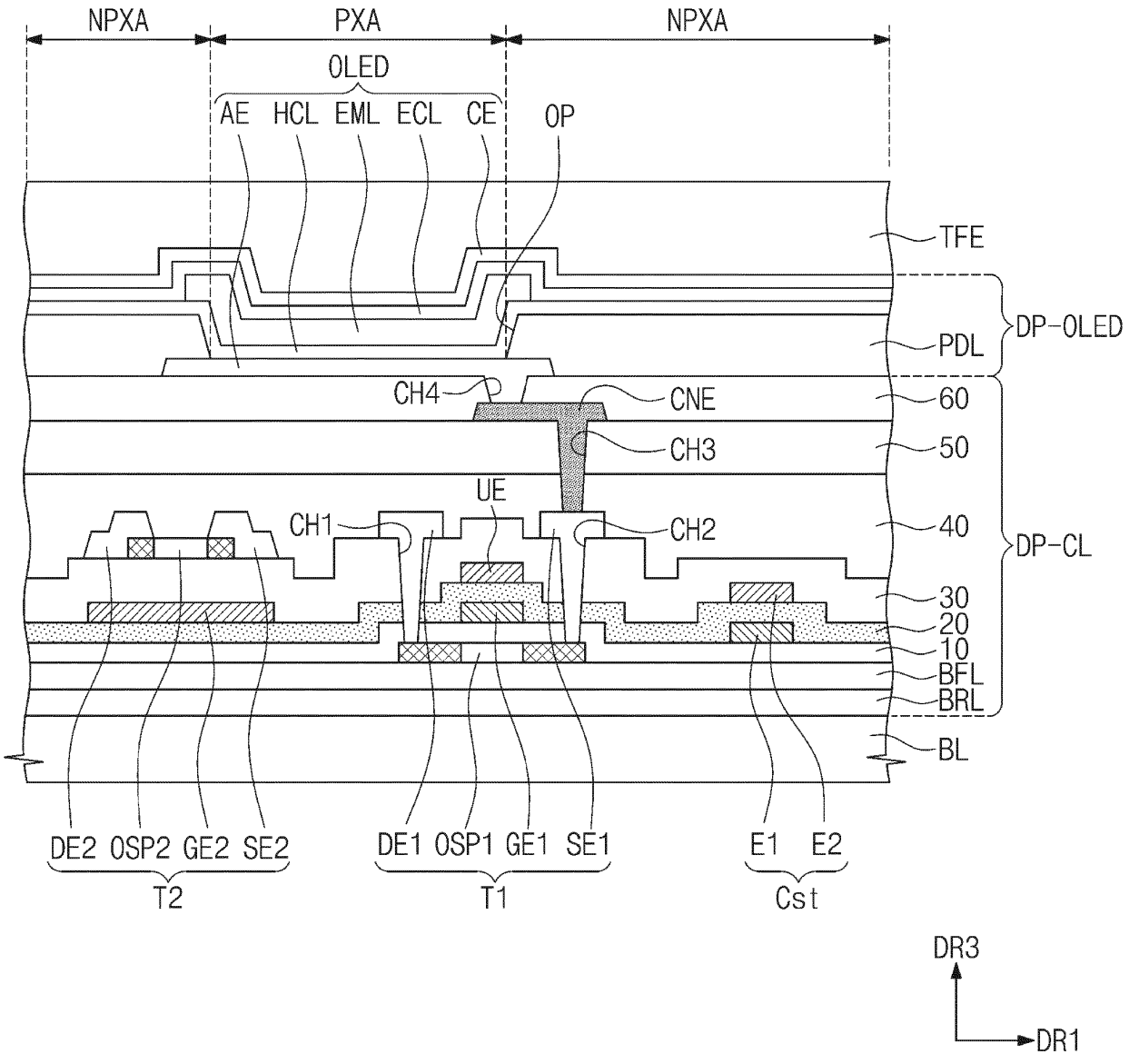

NPXA
PXA
NPXA
OLED
AE
HCL
EML
ECL
CE
OP
TFE
PDL
DP-OLED
CH4
CNE
60
CH3
50
UE
CH1
CH2
40
DP-CL
30
20
10
BFL
BRL
BL
DE2
OSP2
GE2
SE2
T2
DE1
OSP1
GE1
SE1
T1
E1
E2
Cst
DR3
DR1

FIG. 4A

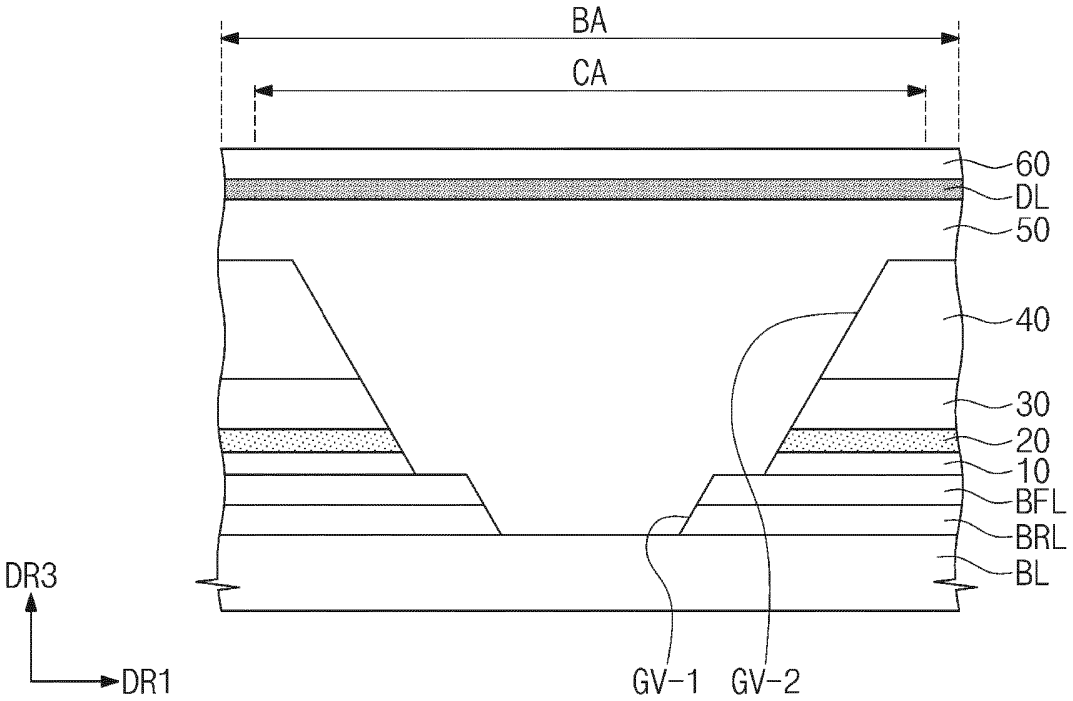

BA
CA
60
DL
50
40
30
20
10
BFL
BRL
BL
DR3
DR1
GV-1
GV-2

FIG. 4B

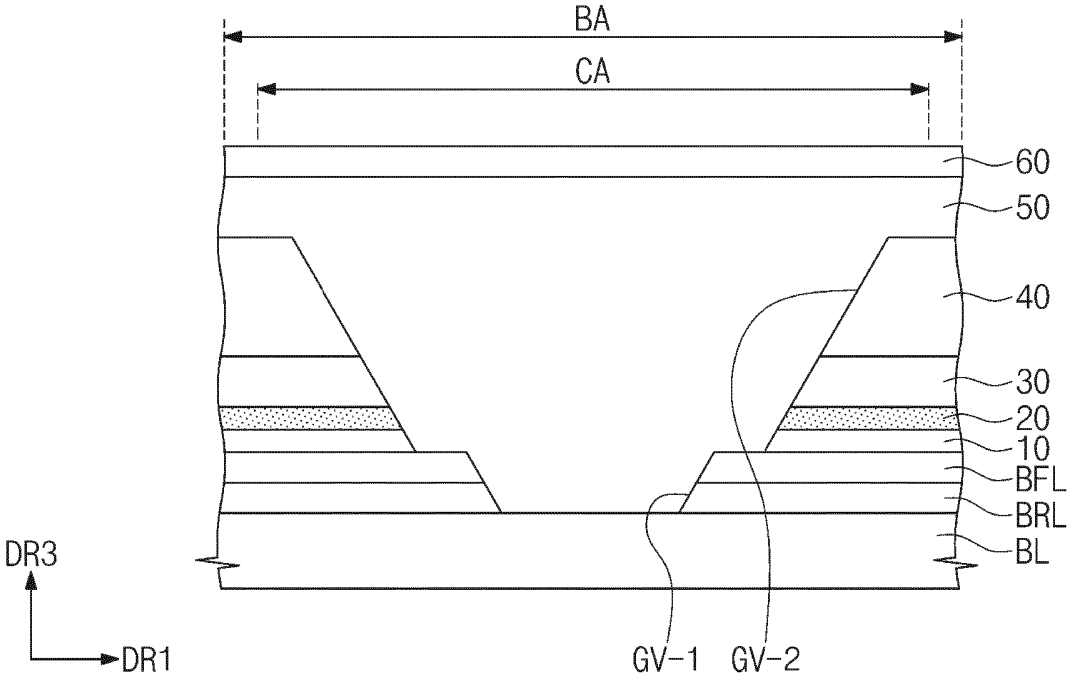

BA
CA
60
50
40
30
20
10
BFL
BRL
BL
DR3
DR1
GV-1
GV-2

FIG. 5A

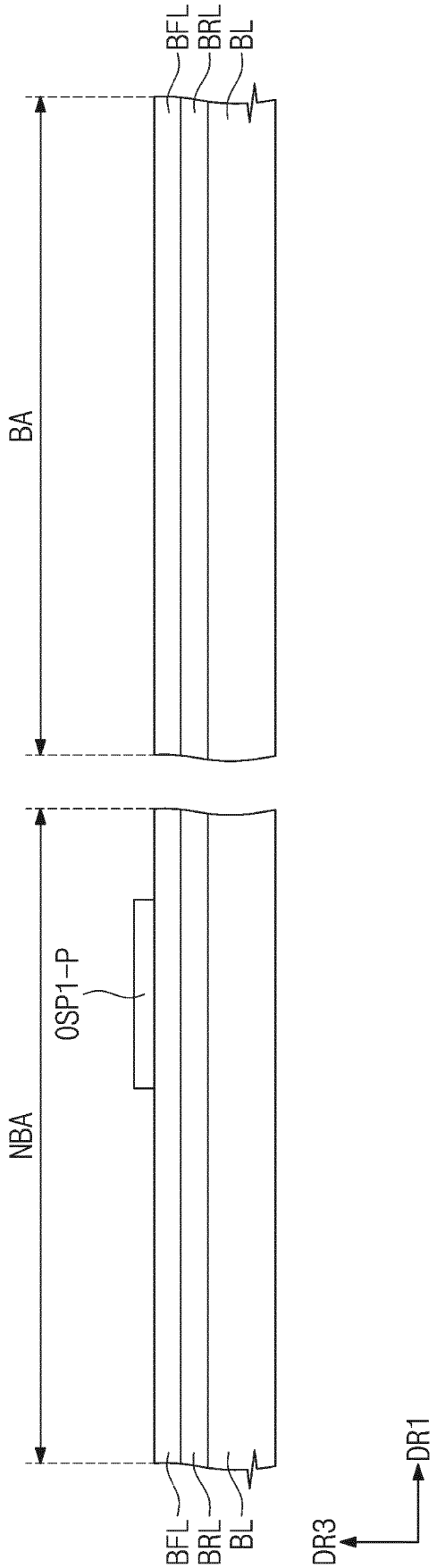

BFL
BRL
BL
BA
NBA
OSP1-P
BFL
BRL
BL
DR3
DR1

FIG. 5B

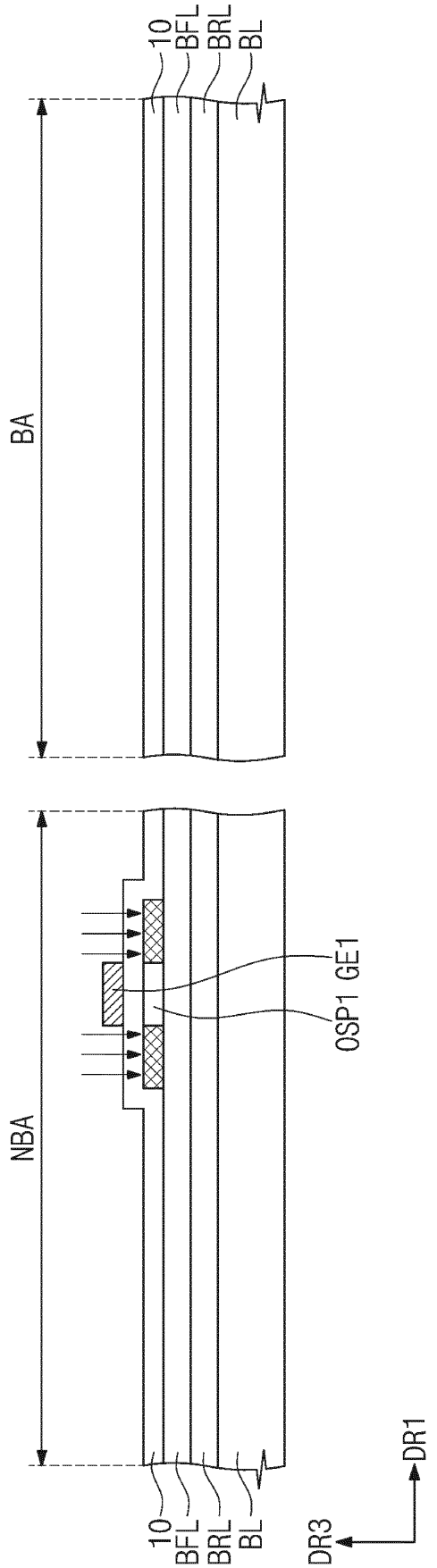

10
BFL
BRL
BL
BA
NBA
OSP1 GE1
10
BFL
BRL
BL
DR3
DR1

FIG. 5C

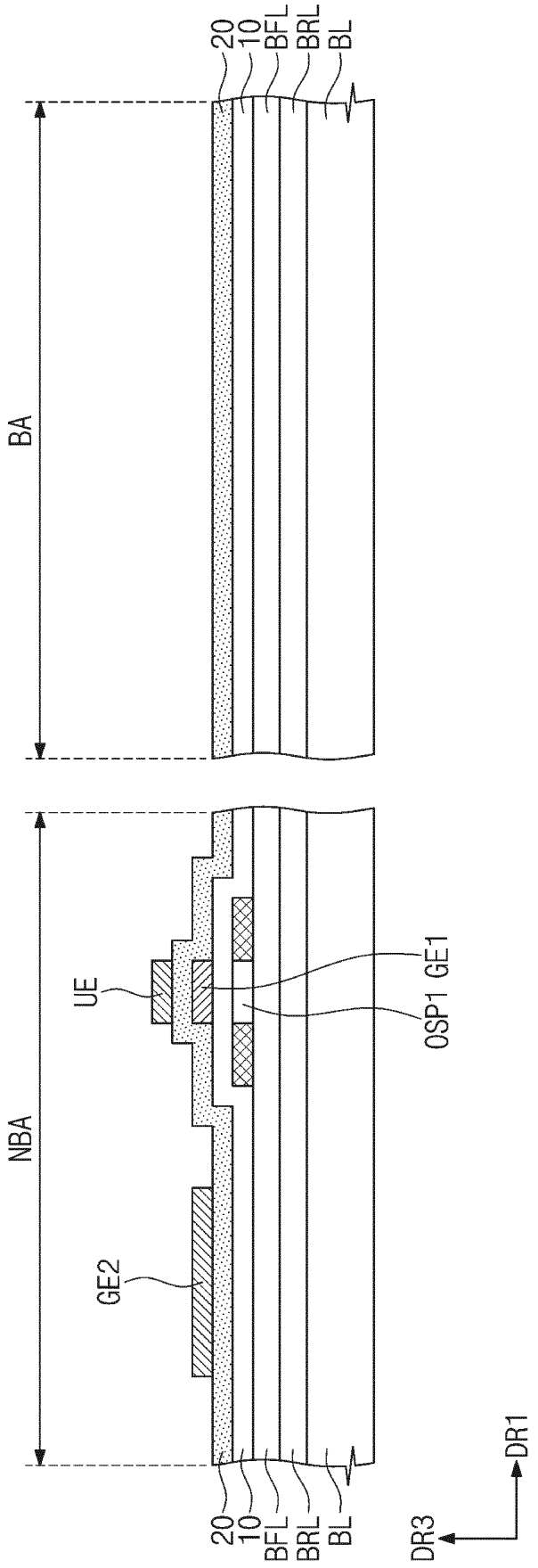


FIG. 5D

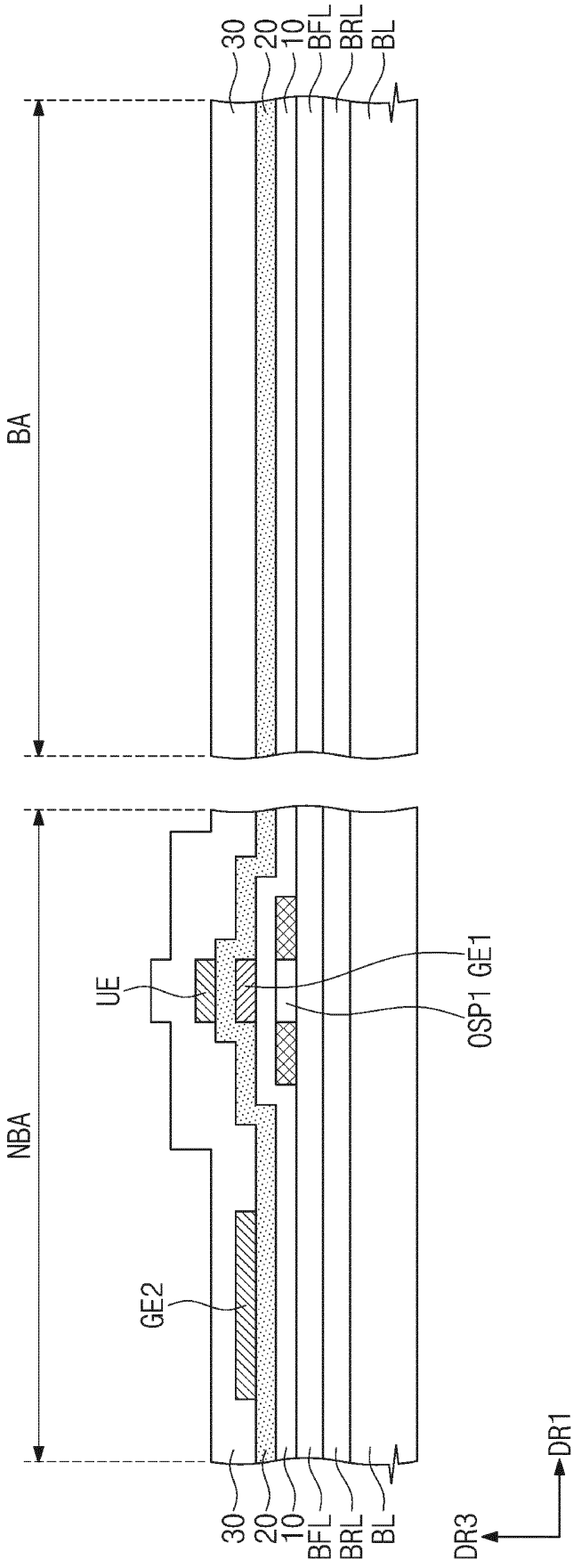


FIG. 5E

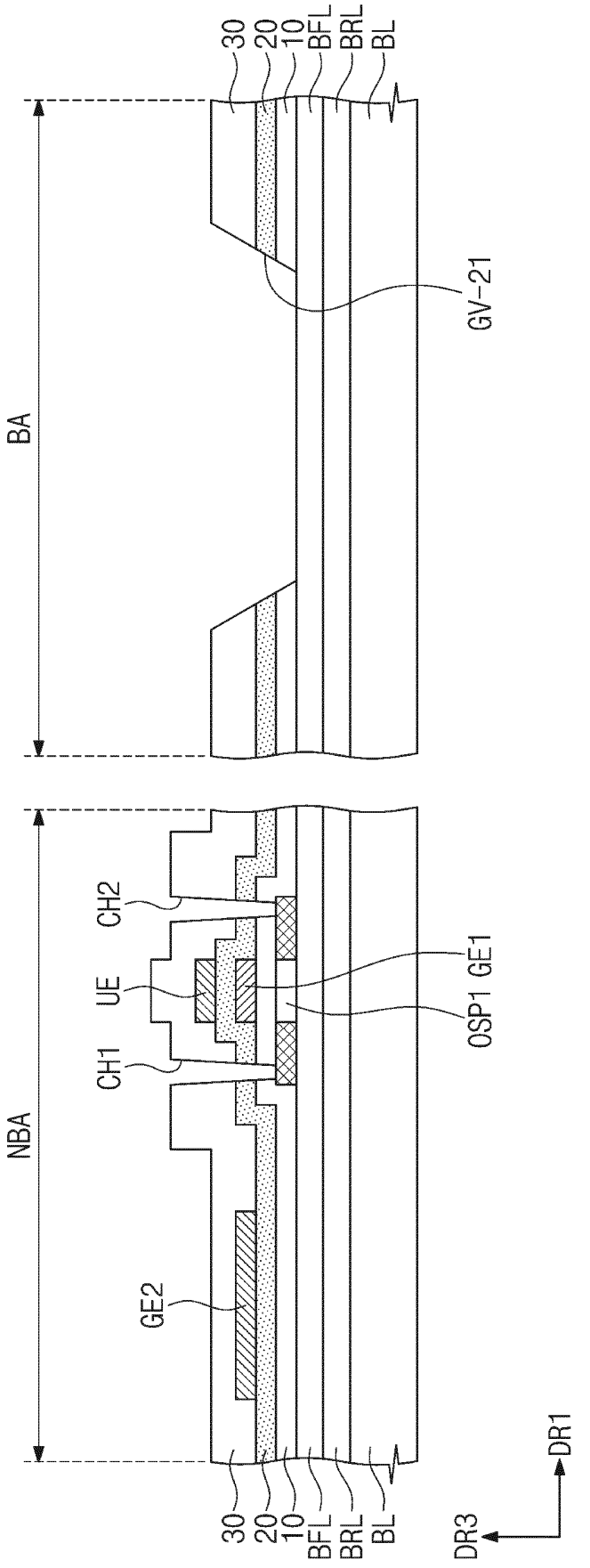


FIG. 5F

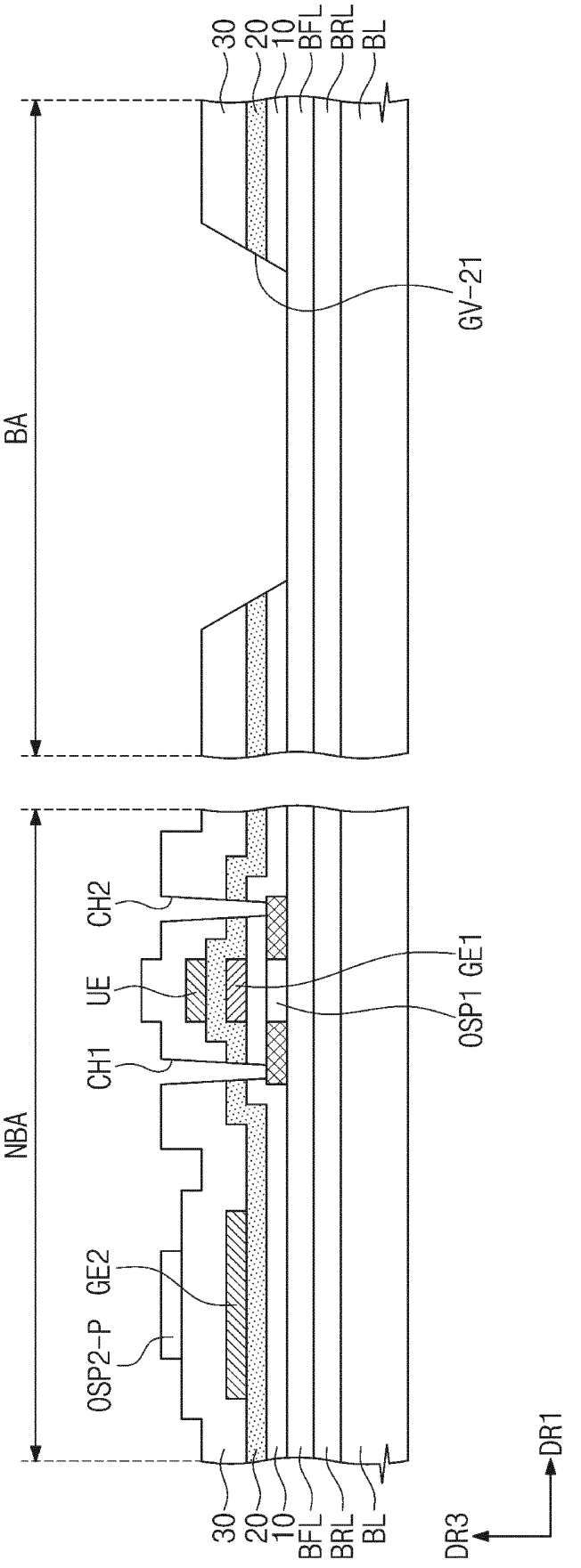

30
20
10
BFL
BRL
BL
BA
GV-21
NBA
CH2
UE
CH1
OSP1
GE1
GE2
OSP2-P
DR1
DR3

FIG. 5G

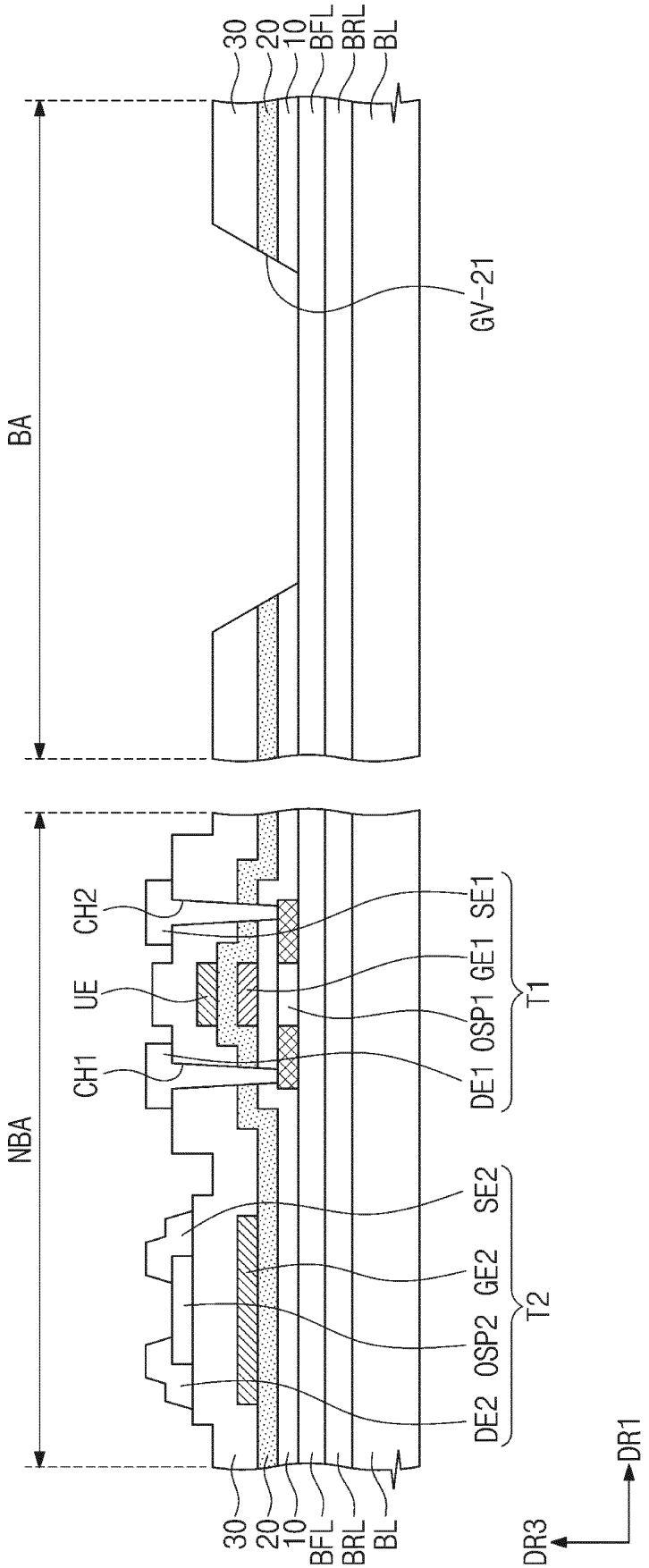

30
20
10
BFL
BRL
BL
GV-21
BA
NBA
CH2
UE
CH1
SE1
GE1
OSP1
DE1
T1
SE2
GE2
OSP2
DE2
T2
DR1
DR3

FIG. 5H

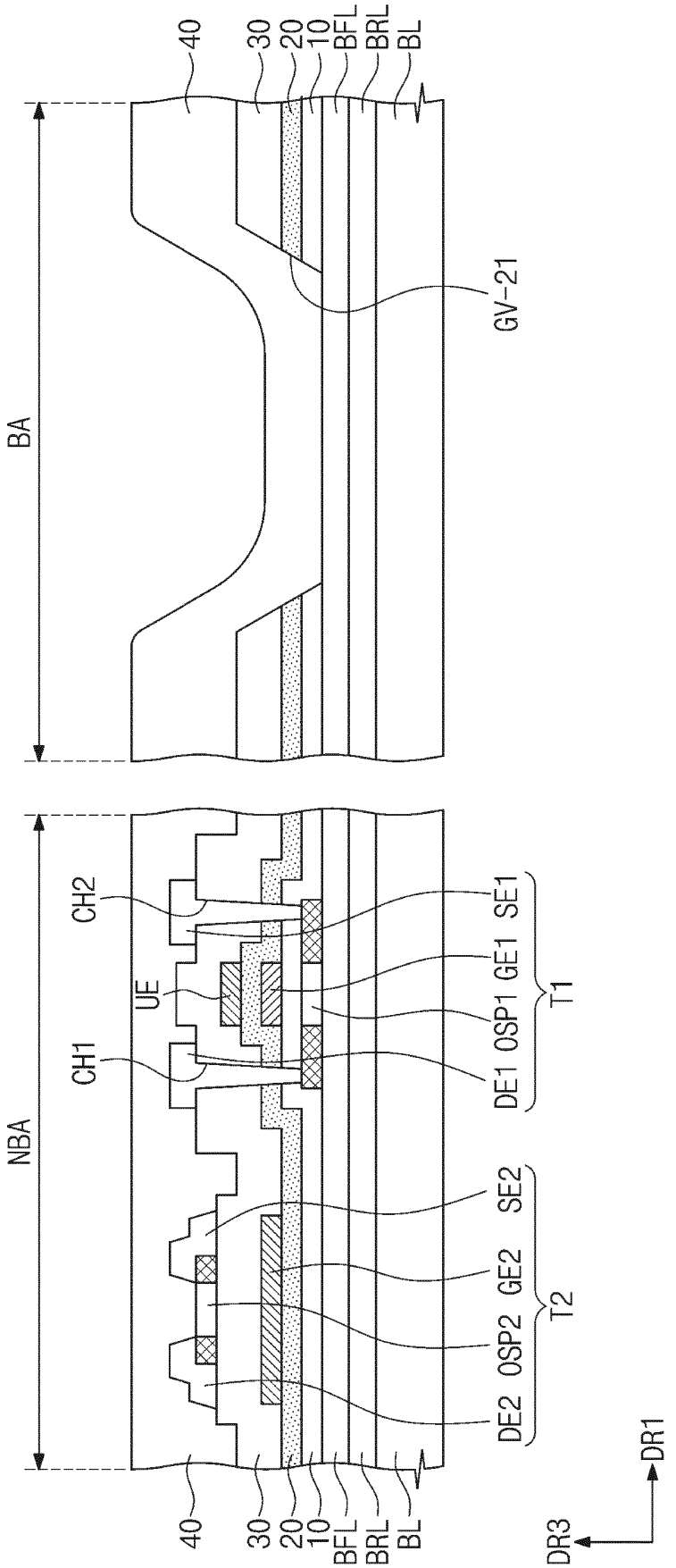

40
30
20
10
BFL
BRL
BL
BA
GV-21
NBA
CH2
CH1
UE
SE1
GE1
OSP1
DE1
T1
SE2
GE2
OSP2
DE2
T2
DR1
DR3

FIG. 5I

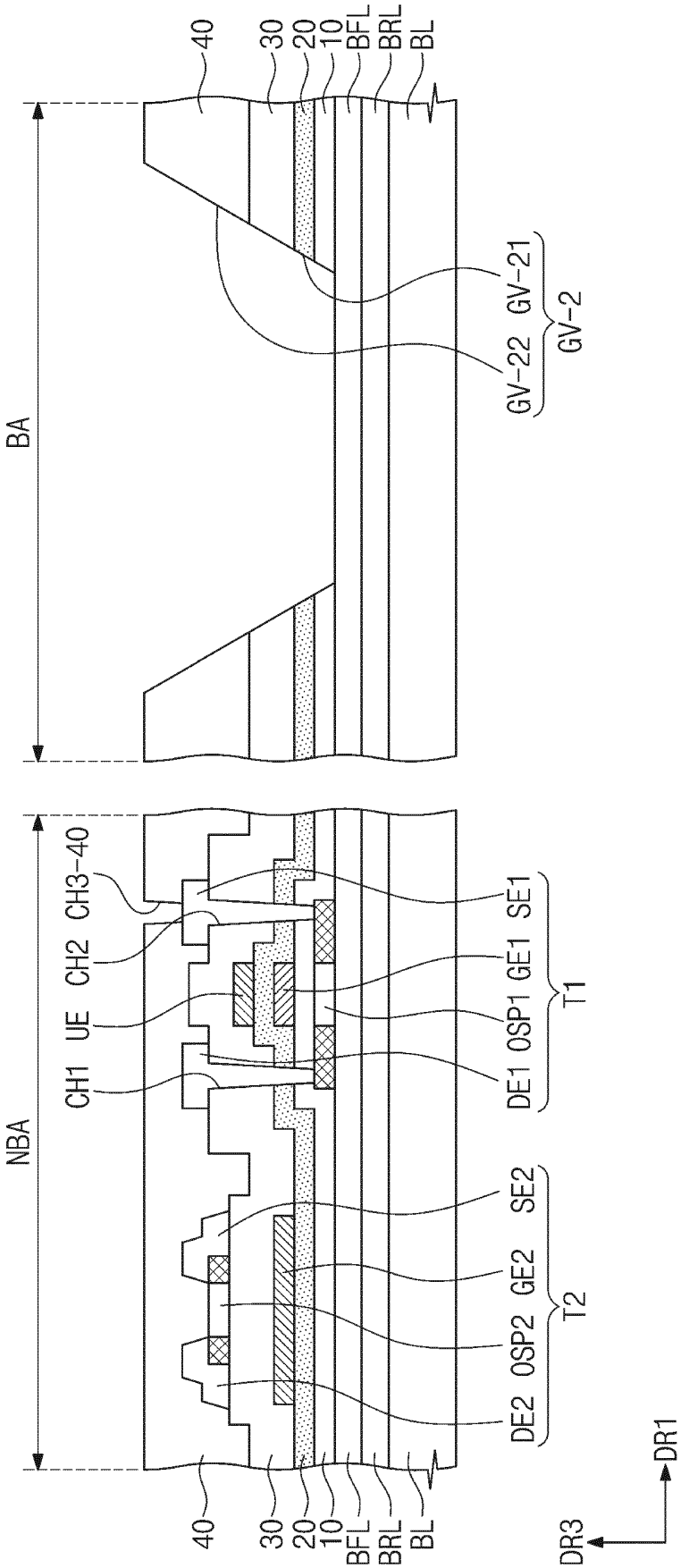

BA
NBA
40
30
20
10
BFL
BRL
BL
GV-21
GV-22
GV-2
CH3-40
CH2
UE
CH1
SE1
GE1
OSP1
DE1
T1
SE2
GE2
OSP2
DE2
T2
DR1
DR3

FIG. 5J

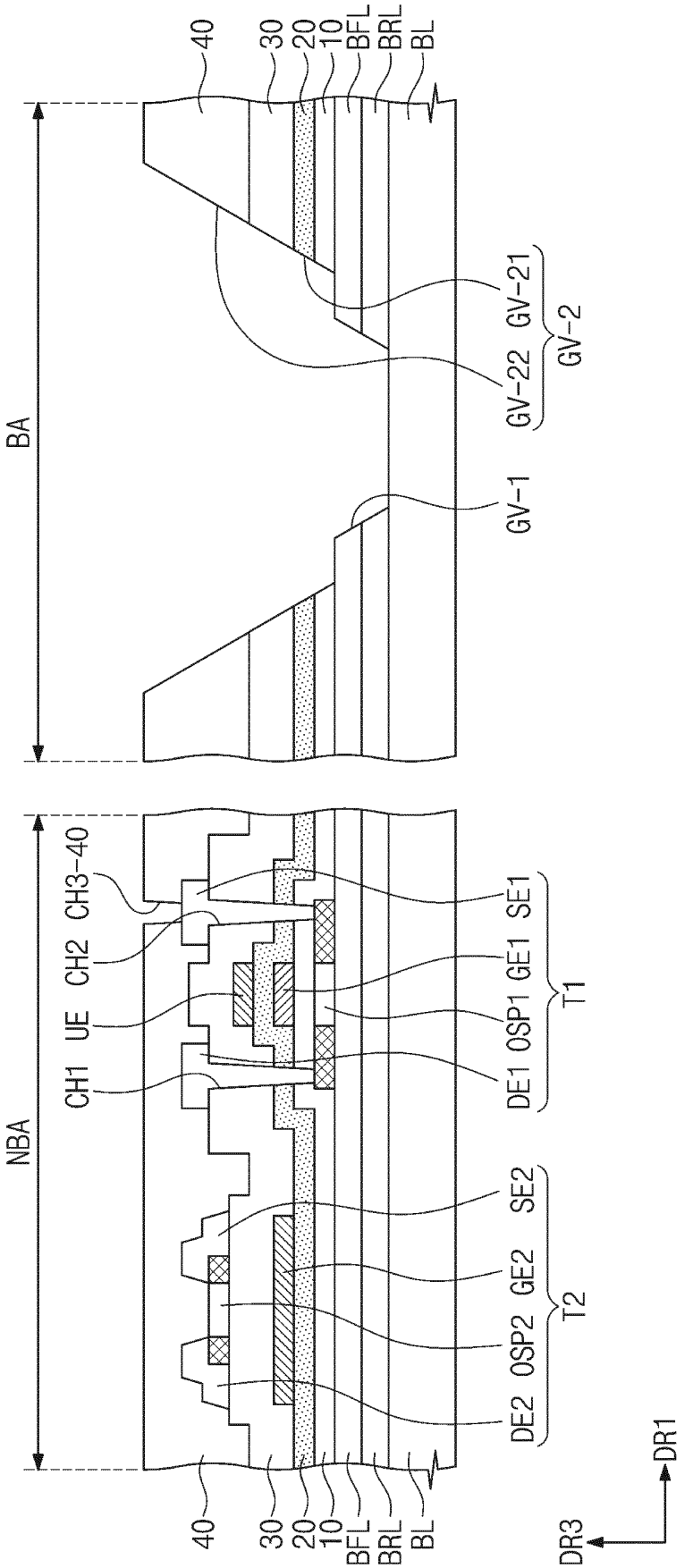

BA
NBA
40
30
20
10
BFL
BRL
BL
GV-21
GV-22
GV-2
GV-1
CH3
CH2
CH1
UE
SE1
GE1
OSP1
DE1
T1
SE2
GE2
OSP2
DE2
T2
DR1
DR3

FIG. 5K

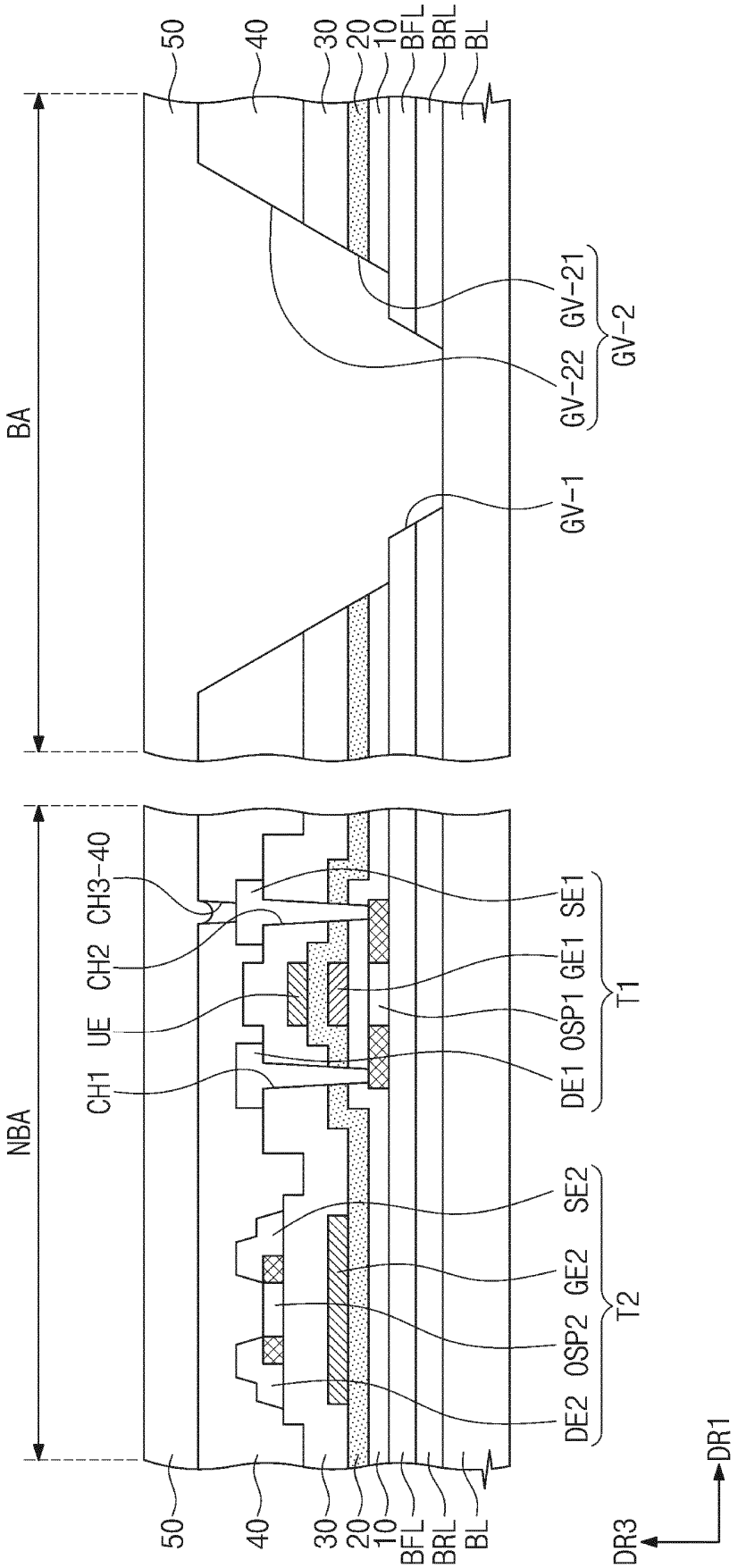

BA
NBA
50
40
30
20
10
BFL
BRL
BL
GV-1
GV-2
GV-21
GV-22
CH1
UE
CH2
CH3-40
DE1
OSP1
GE1
SE1
T1
DE2
OSP2
GE2
SE2
T2
DR1
DR3

FIG. 5L

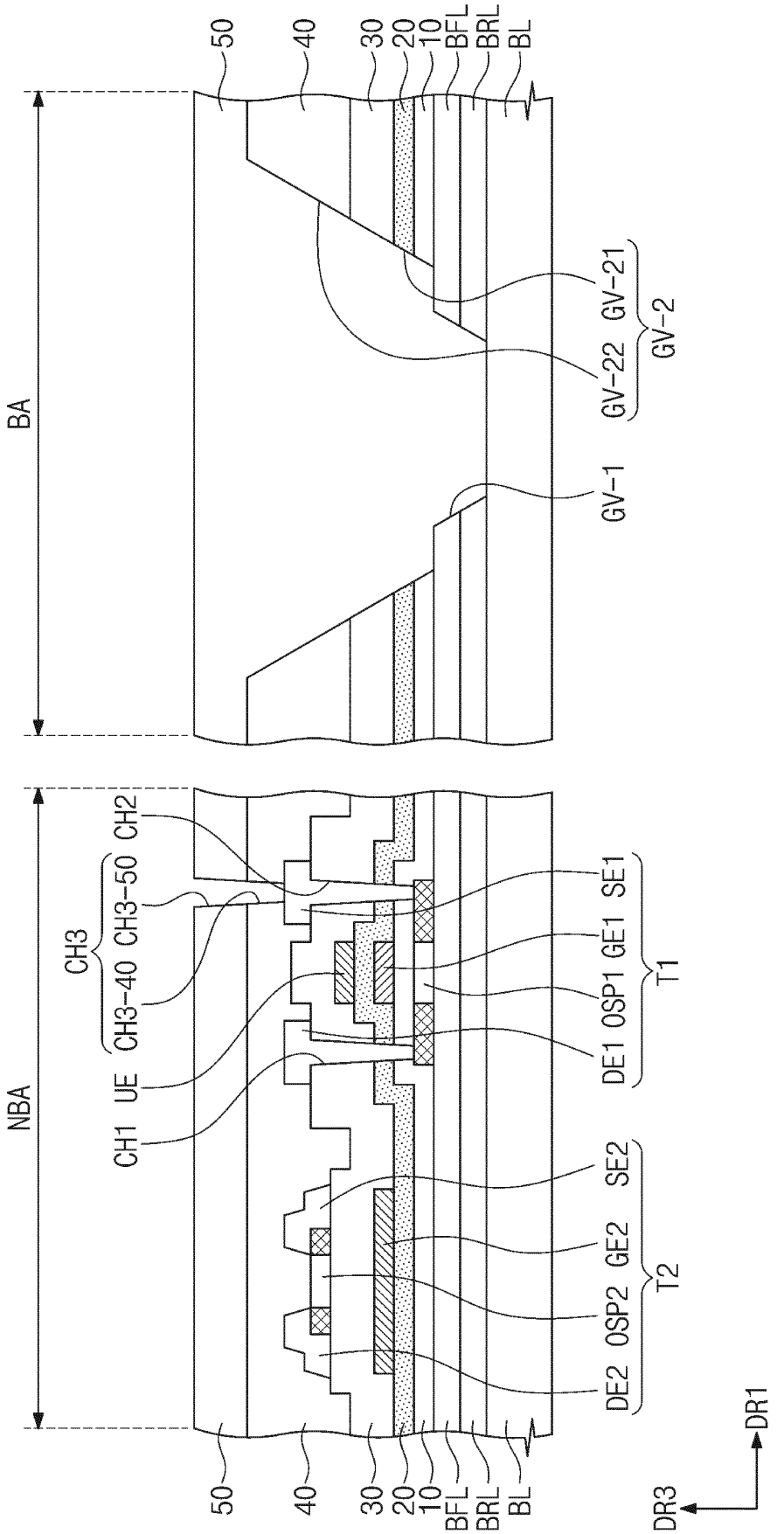

BA
NBA
50
40
30
20
10
BFL
BRL
BL
GV-21
GV-22
GV-2
GV-1
CH2
CH3-50
CH3
CH3-40
UE
CH1
SE1
GE1
OSP1
DE1
T1
SE2
GE2
OSP2
DE2
T2
DR1
DR3

FIG. 5M

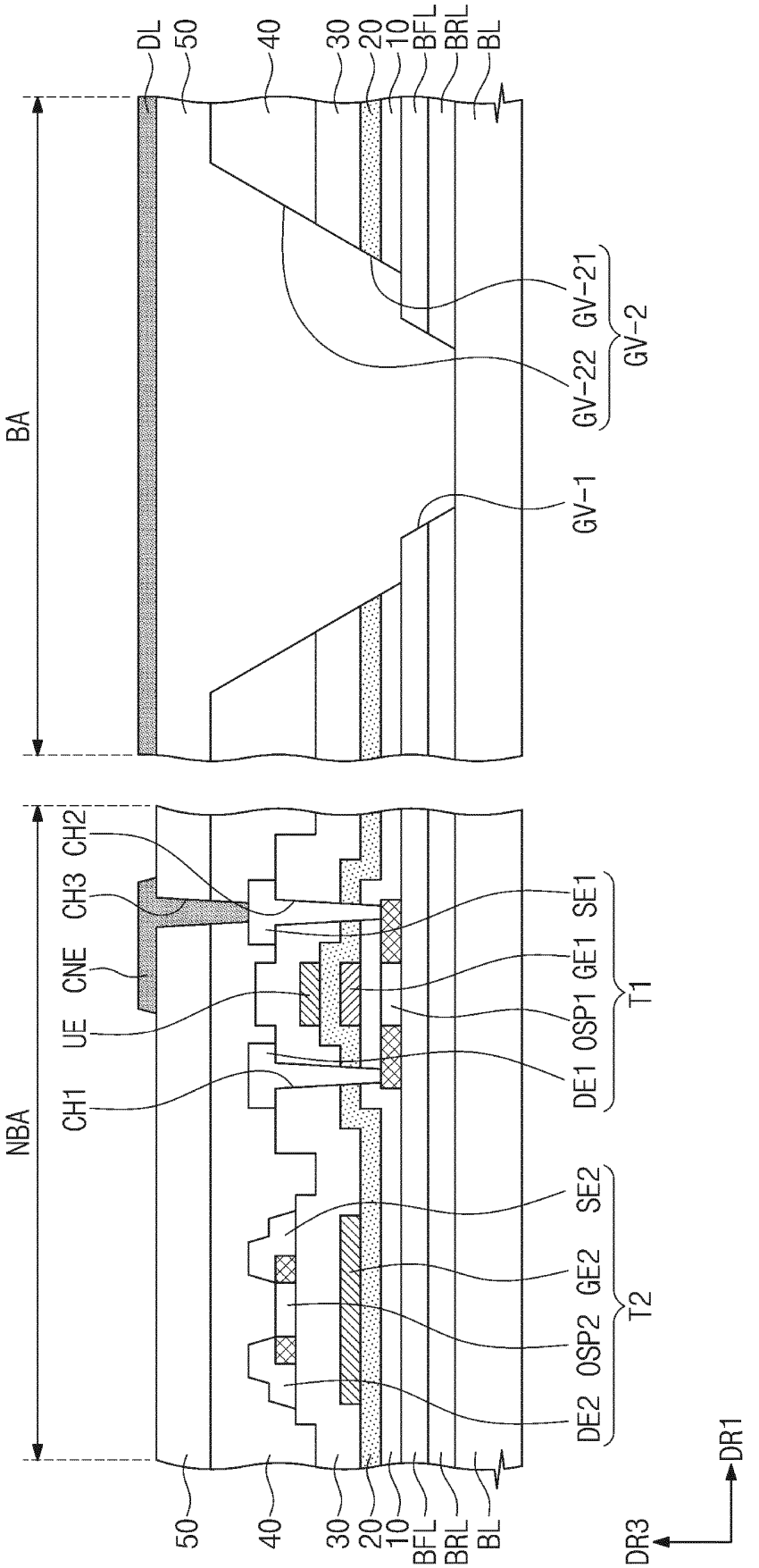

BA
NBA
DL
50
40
30
20
10
BFL
BRL
BL
GV-1
GV-2
GV-21
GV-22
CH1
UE
CNE
CH3
CH2
DE1
OSP1
GE1
SE1
T1
DE2
OSP2
GE2
SE2
T2
DR1
DR3

FIG. 5N

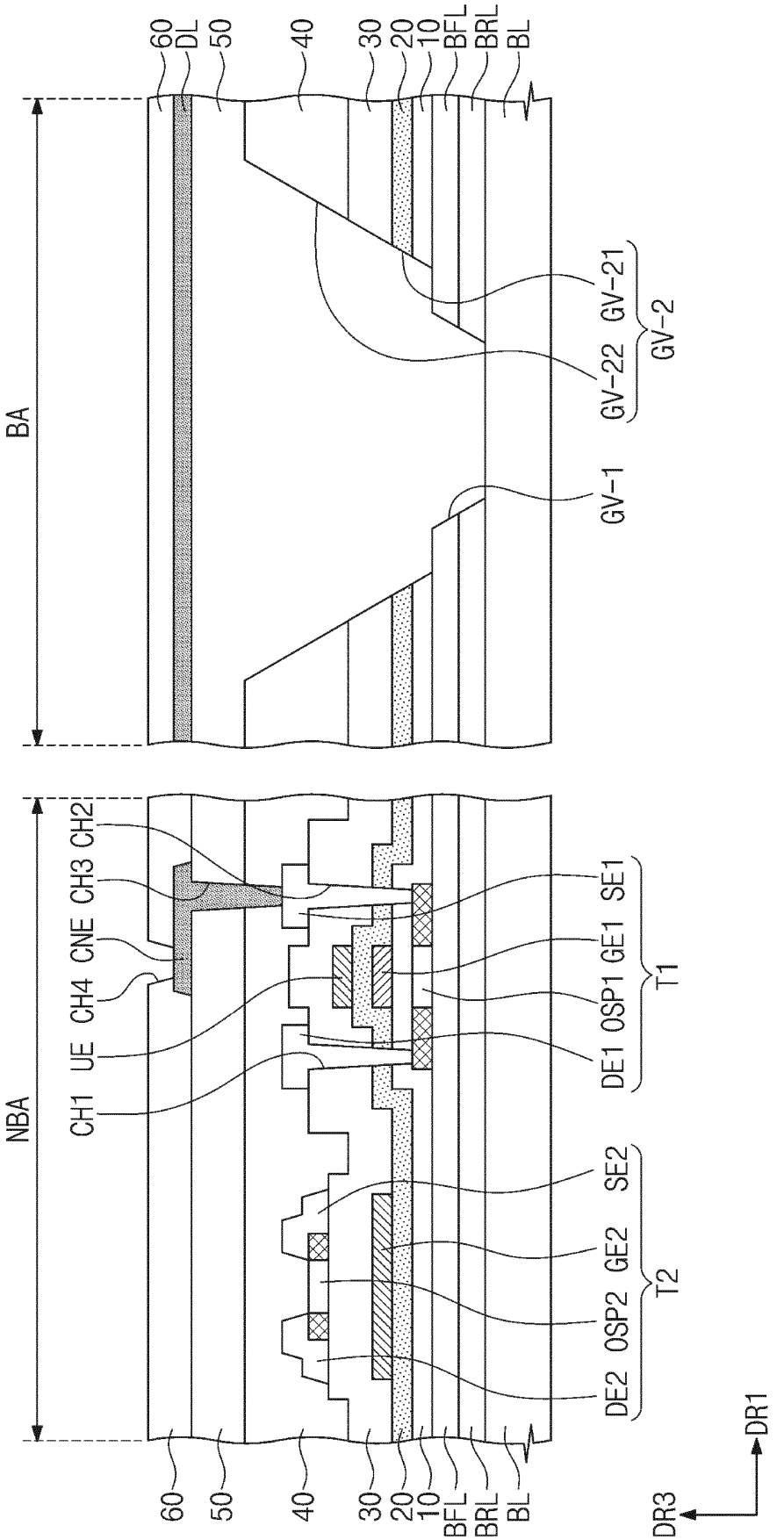

BA
NBA
60
DL
50
40
30
20
10
BFL
BRL
BL
GV-21
GV-22
GV-2
GV-1
CH2
CH3
CNE
CH4
UE
CH1
SE1
GE1
OSP1
DE1
T1
SE2
GE2
OSP2
DE2
T2
DR1
DR3

FIG. 50

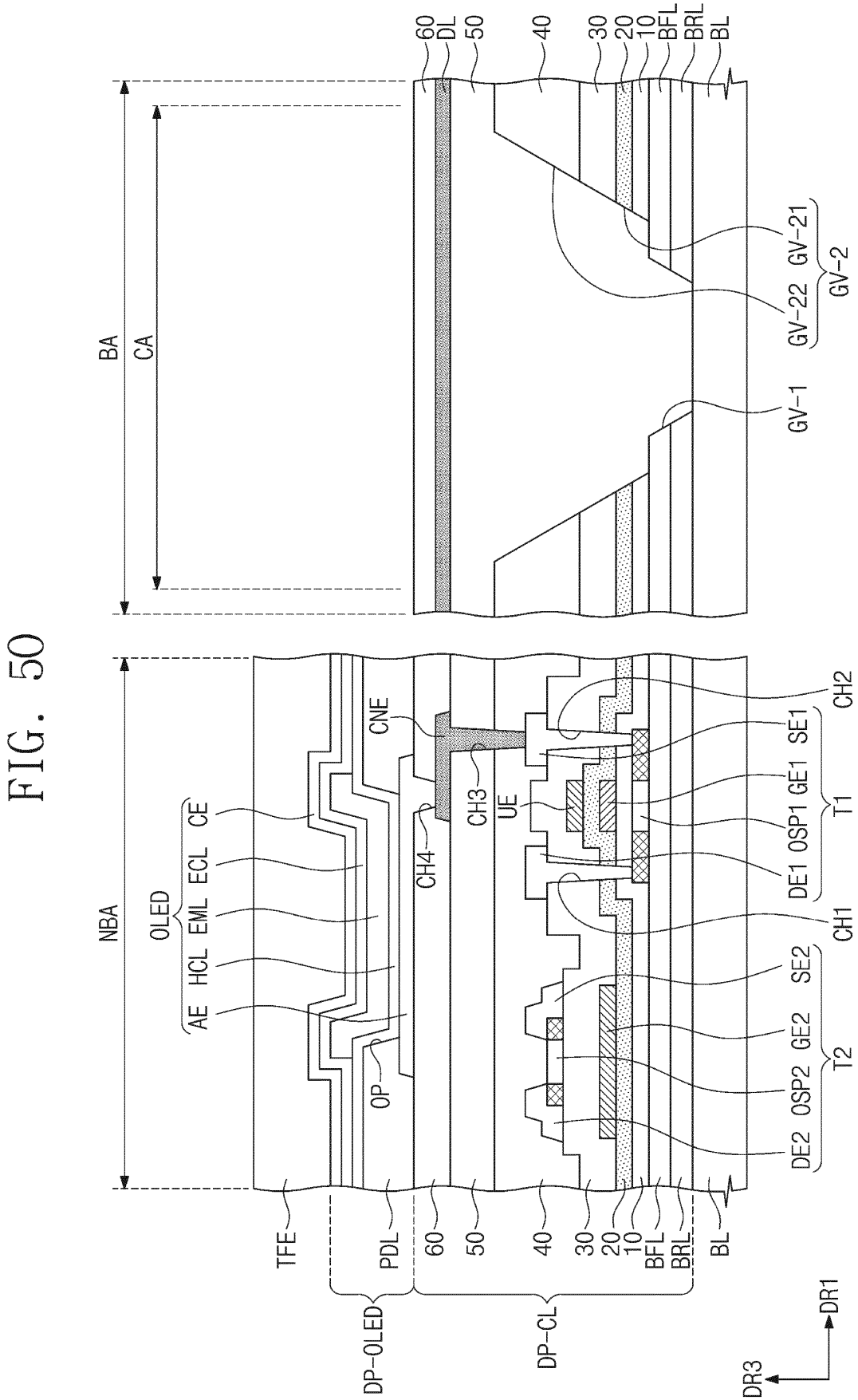
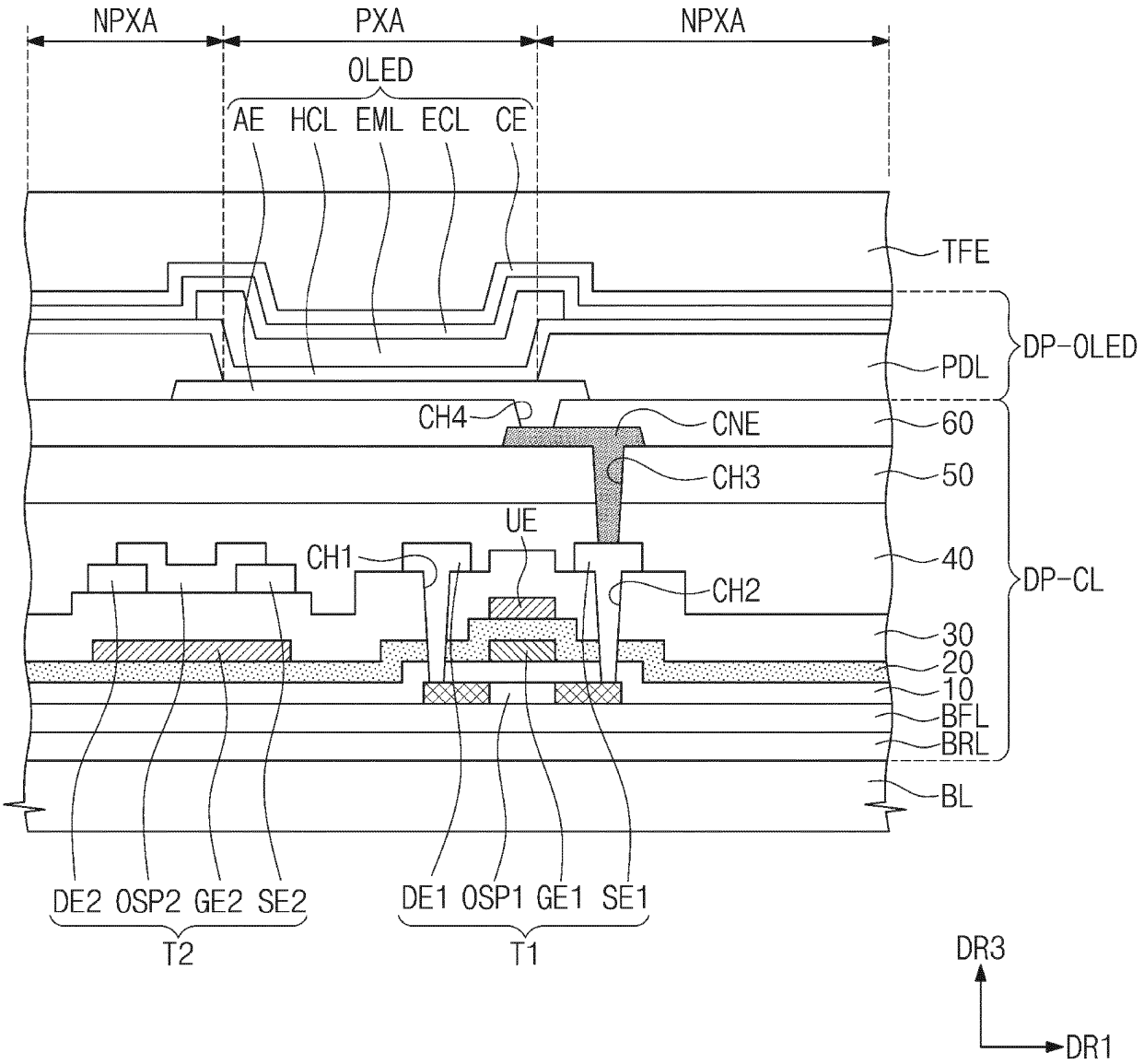

BA
CA
60
DL
50
40
30
20
10
BFL
BRL
BL
GV-21
GV-22
GV-2
GV-1
NBA
OLED
AE
HCL
EML
ECL
CE
CNE
CH3
CH4
UE
OP
CH2
SE1
GE1
OSP1
DE1
T1
CH1
SE2
GE2
OSP2
DE2
T2
TFE
PDL
DP-OLED
DP-CL
DR1
DR3

FIG. 6


NPXA
PXA
NPXA
OLED
AE HCL EML ECL CE
TFE
PDL
DP-OLED
CH4
CNE
60
CH3
50
UE
CH1
40
CH2
DP-CL
30
20
10
BFL
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DR1

FIG. 7

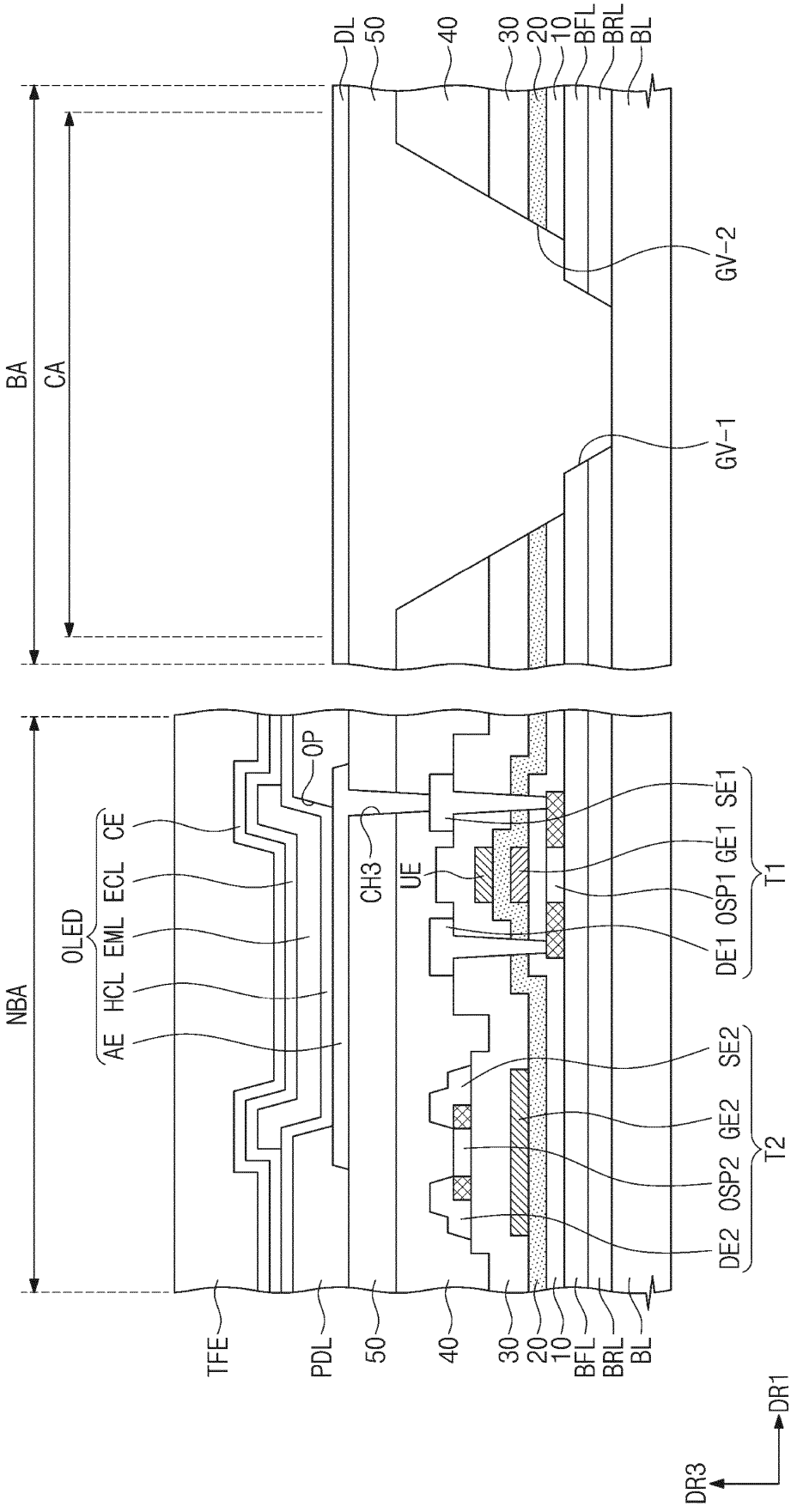
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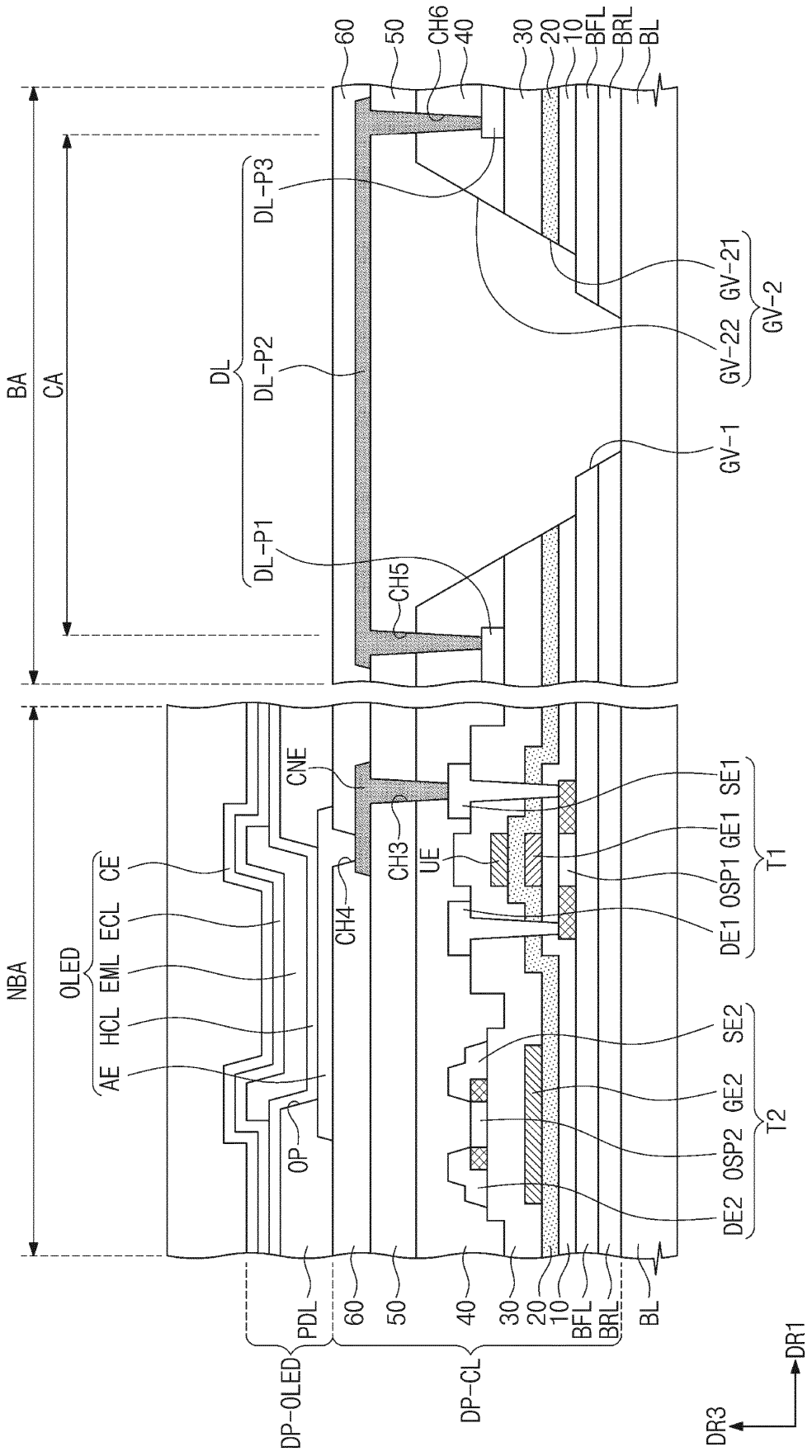
FIG. 8A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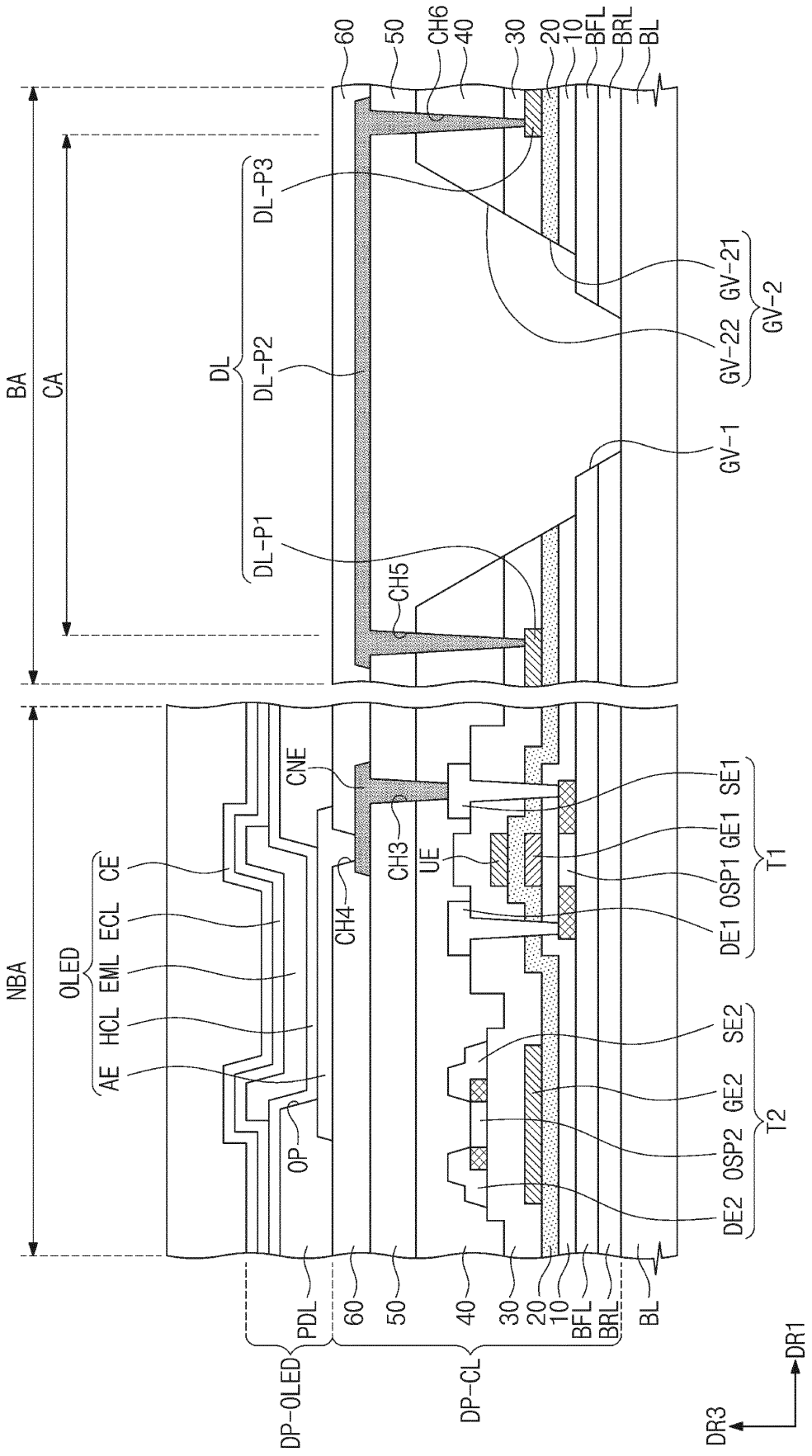
DR1
DR3

FIG. 8B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PDL
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T2
DP-OLED
DP-CL
DR1
DR3

FIG. 8C

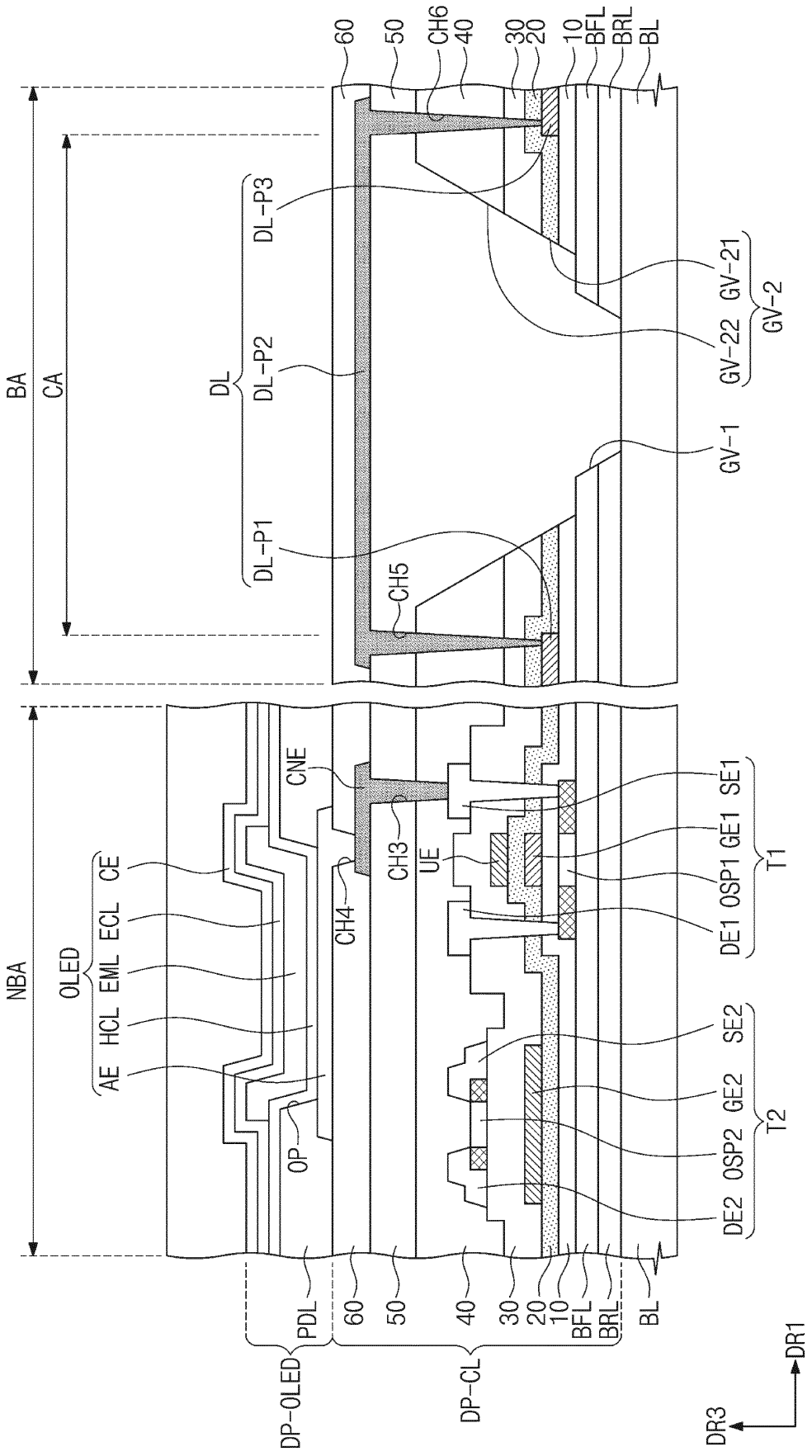
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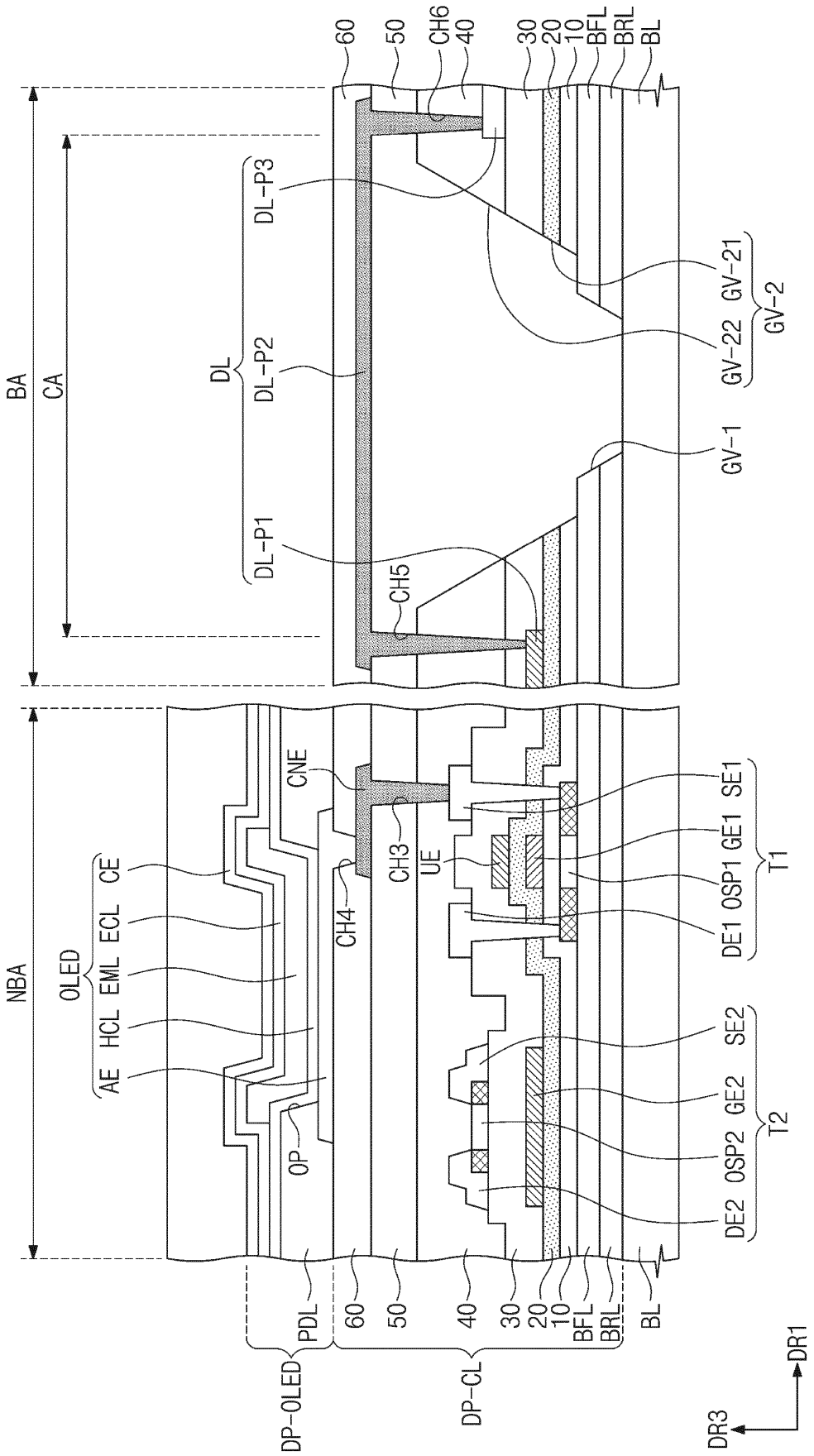
FIG. 8D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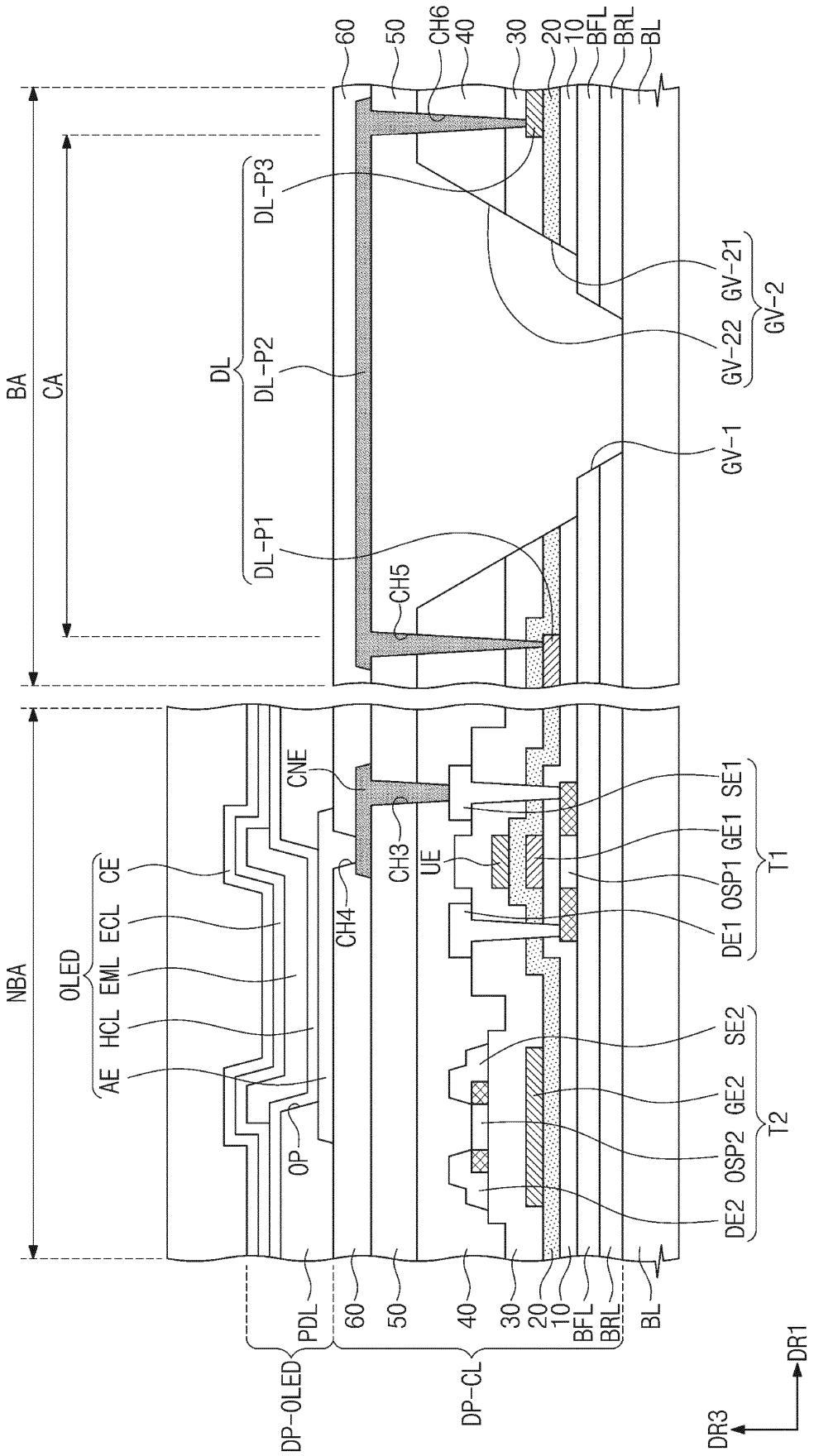
DR3

FIG. 8E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OSP2
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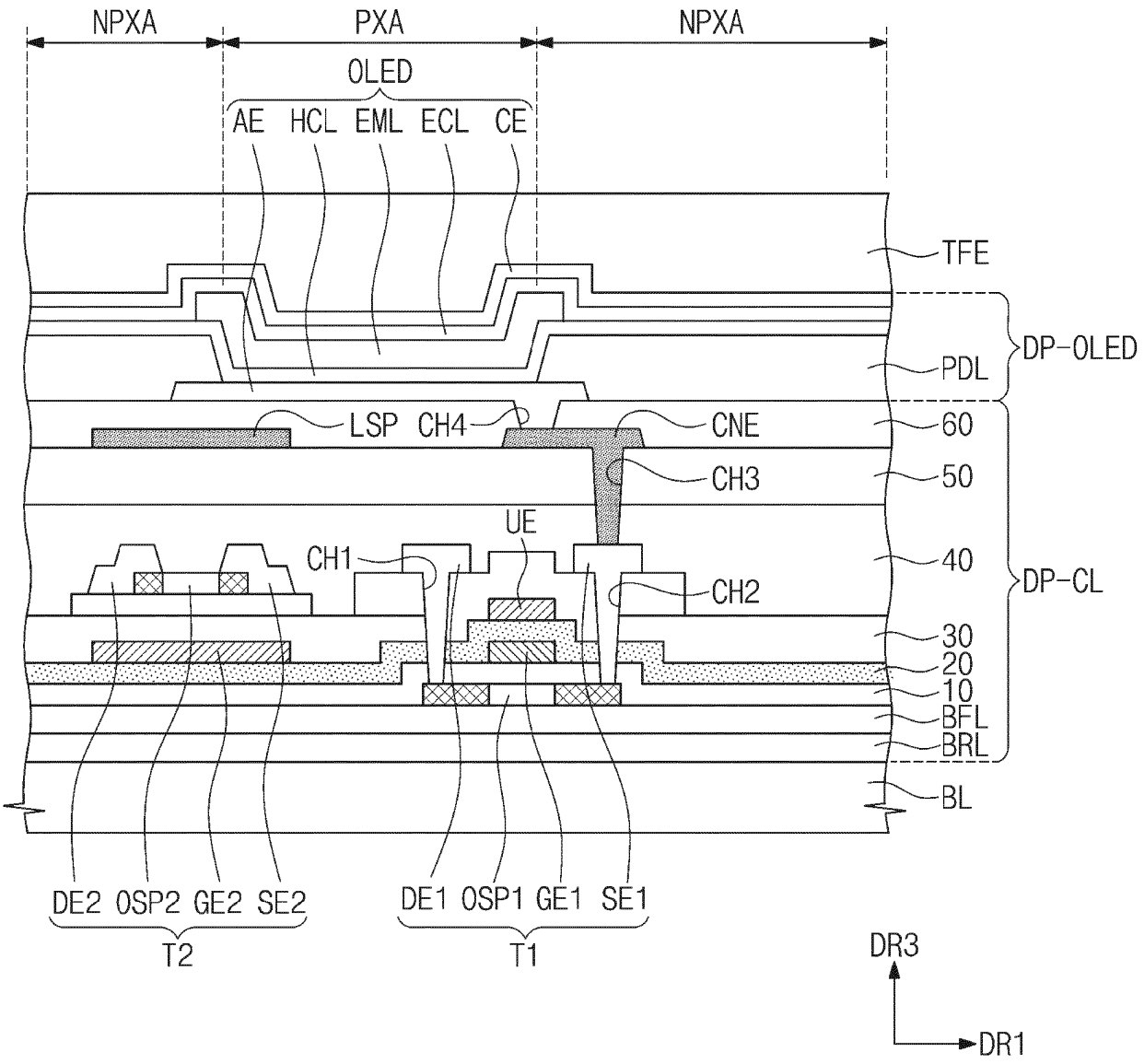
DP-OLED
DP-CL
DR1
DR3

FIG. 9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BFL
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DE2 OSP2 GE2 SE2
T2
DE1 OSP1 GE1 SE1
T1
DR3
DR1

REFERENCES CITED IN THE DESCRIPTION

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Patent documents cited in the description

- EP 3236309 A **[0004]**
- US 2017288005 A **[0004]**
- EP 2217265 A **[0004]**