# United States Patent [19]

**Dobrzanski et al.**

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[54] **RESIDENTIAL ALARM SYSTEM**


[75] Inventors: **John J. Dobrzanski,** New Britain, Conn.; **Willaim J. Doyle,** La Habra, Calif.

[73] Assignee: **Emhart Corporation,** Bloomfield, Conn.



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[52] **U.S. Cl.** ..... **340/276,** 340/213 R, 340/274

[51] **Int. Cl.** ..... **G08b 13/00**

[58] **Field of Search** ..... 340/274, 276, 214, 411, 340/409, 213 R



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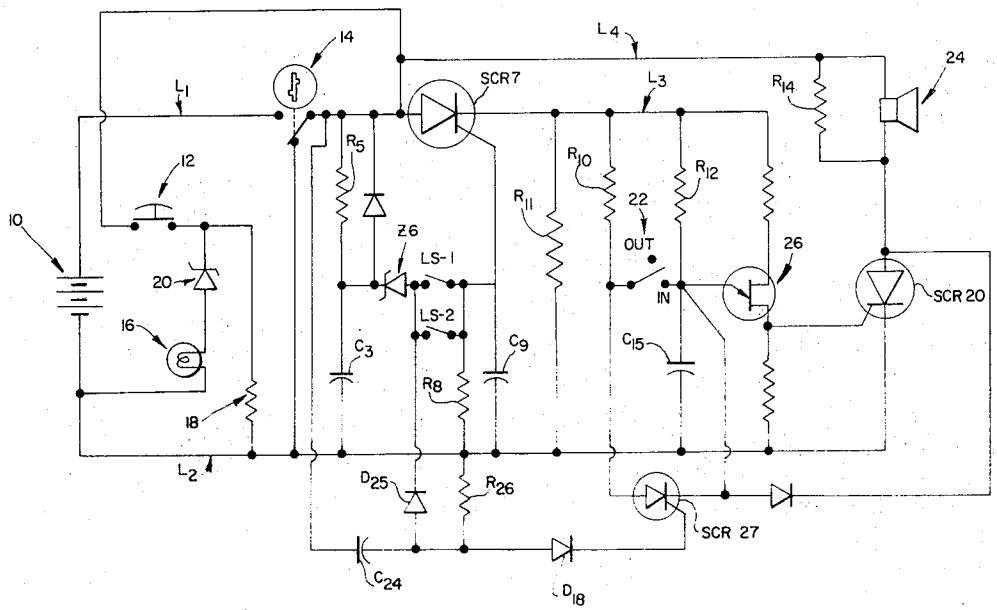
*Primary Examiner*—John W. Caldwell
*Assistant Examiner*—Scott F. Partridge
*Attorney, Agent, or Firm*—McCormick, Paulding & Huber

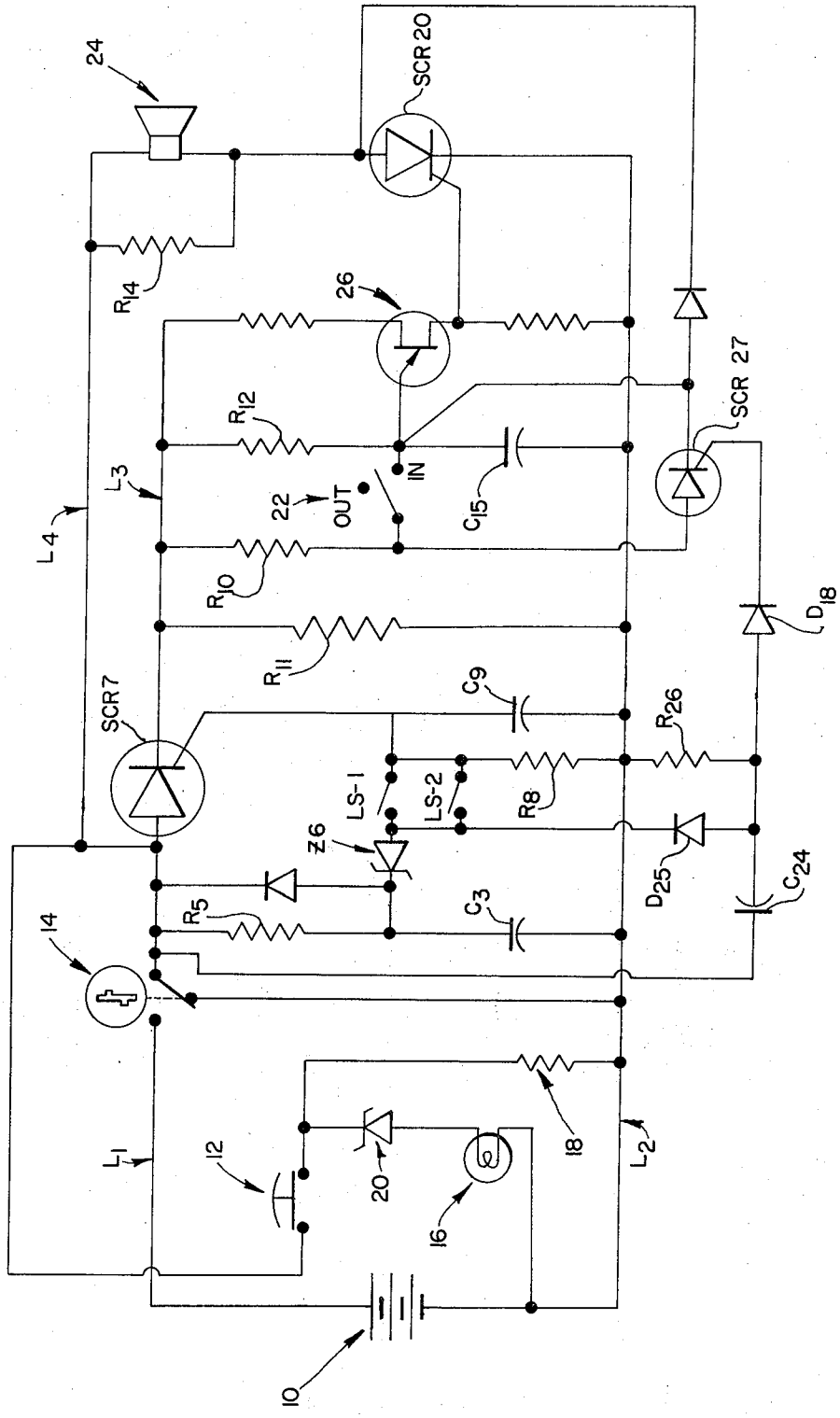


[57] **ABSTRACT**

Circuitry is disclosed for sounding an alarm horn when a window or door is opened, and an associated limit switch is closed, the circuitry providing for predetermined time delays suitable for use in either one of two possible modes of operation. A console is provided in the residence to be protected, and contains a battery power source for operating the circuitry, a key control switch, and a mode selector switch. One mode is suitable for use at night when the occupant of the residence is at home, and the circuitry provides for a time delay in sounding the alarm following closing of one of the limit switches, in order to allow the occupant time to close any open exit door or window. The second mode is for use when the occupant leaves his residence unattended, and two time delays are provided for in this second mode prior to sounding any alarm, and after switching the system on. One of these delays is the same as that outlined above, the other delay being of variable duration and in sequence with the first mentioned delay. The occupant has the same nine seconds to re-enter and deactivate the system once he has left his residence, but he also has the benefit of a secondary delay on leaving his residence. Thus, he may activate the system in mode two, open an exit door within a certain time, and procrastinate for any amount of time before leaving and closing the door behind him. Having closed the door behind him he will have the benefit of a short delay on re-entry to allow him to deactivate the system.


**5 Claims, 1 Drawing Figure**




24
SCR 20
R14
26
R12
SCR 27
L3
22
OUT
IN
C15
L4
R10
D18
R11
C9
SCR7
R26
LS-1
LS-2
R8
Z6
D25
C24
R5
C3
14
18
L1
12
20
16
L2
10

# RESIDENTIAL ALARM SYSTEM

## SUMMARY OF INVENTION

This invention relates to residential alarm systems, and deals more particularly with a circuit capable of two modes of operation, one for use when the occupant is at home, and the second when he intends to leave, and return at a later time.

Normally closed sensor switches are mounted at the various doors and windows, and these switches are held open when these various exit openings are suitably secured. A control console located inside the residence contains a battery, a mode selector switch, and a keylock control switch for energizing circuitry which includes these sensor switches arranged in parallel.

The system also includes an alarm device, selectively operated from the battery by a sensing circuit, and the sensing circuit has solid state gate means which can be triggered following a known delay by a threshold device. The sensing switches are preferably arranged between a resistance-capacitance grouping associated with and the gate, in order to minimize drain on the battery when the system is operating, and to permit the alarm to operate only after a known delay following reclosing of the sensing switch in the second mode. This feature permits the occupant to close the keylock or control switch allowing him time to open one of his exit doors within the known delay period, and to then have an undetermined length of time within which to exit and reclose the door. Once the door, or any other secured opening has been tampered with, reclosing an associated sensing switch, the alarm device will operate normally, that is with the limited delay period built into the circuit as described above.

In both mode one and in mode two following the above preliminary situation, the alarm will be energized from the battery following the brief delay dictated in mode one, and in mode two be a secondary gate and triggering circuit network.

## BRIEF DESCRIPTION OF THE DRAWING

The single view shows in schematic fashion the circuitry included in an alarm system constructed in accordance with the present invention.

## DETAILED DESCRIPTION

In order to equip a typical residence with a burglar alarm system in accordance with the present invention, a plurality of normally closed limit switches, or other sensing devices with contacts arranged so as to close in response to a condition to be detected, are provided at the various exits and windows of the residence to be secured in such a way as to close when the exit door or window is opened or otherwise tampered with. As shown in FIG. 1 these sensing devices may comprise limit switches, such as LS 1 and LS 2, arranged in parallel with respect to one another, or may comprise contacts engageable by a deadbolt, or latch bolt, or may comprise contacts in a magnetic motion detector or sensor or any other known intrusion device. Such devices will be arranged so as to be held in a normally open circuit condition, and are adapted to close whenever the secured condition is violated. The electrical connection of these devices, in parallel, back to a control console located within the residence may be accomplished in a well known manner, and the remaining



elements shown in FIG. 1 are provided in the control console.

Turning now to the system components shown in FIG. 1 a self-contained battery pack **10** is provided to achieve a voltage potential between the lines L-1 and L-2. A push to test switch **12** is provided to check the status of the battery when the key control lock switch **14** is turned on by an appropriately shaped key. A gallium arsenide light emitting diode **16** is mounted on the console and adapted to be energized when the push to test switch is closed and a resistive load is applied across the battery as shown at **18.** If the load resistor drops the battery voltage below horn operating specifications, the blocking zener **20** connected in series with the light emitting diode **16** will not function below its threshold and the light will not indicate telling the occupant of the house to replace the battery as soon as possible.

A mode selector switch **22** is provided on the console, and permits the occupant to select an "in" mode or an "out" mode. This selection will be dictated by virtue of whether the occupant intends to remain in his residence or to go out for any reason. For example, when the system is activated at night when the occupant retires for the evening, the mode selector switch **22** would be placed in the "in" position. The control switch **14** can be closed from the open position shown and a nine second time delay provided for last minute checking of doors and windows. An alarm will occur after a lapse of nine seconds if entry is attempted. The alarm device **24** is also provided in the console, and the sensing circuit for operation of the horn **24** from the battery source **10** with the mode selector switch in the in position will now be described in detail.

With the system turned on as described above battery voltage is applied across a time delay network consisting of a resistor $R_5$ and capacitor $C_3$. When a conventional 6 volt battery is used as the power source for a typical circuit, $R_5$ preferably comprises a relatively large resistance as for example 690K ohms. The capacitor $C_3$ is chosen to have a capacitance of **22** microfarads. When the capacitor $C_3$ is fully charged the only current being drawn from the battery, will be due to minute capacitor leakage. The capacitor, when charged above the threshold voltage of zener $Z_6$, will provide a triggering voltage to a silicon control rectifier $SCR_7$ or solid state gate means through one or more of the sensing devices which may have been closed as for example by an intruder in opening or otherwise tampering with a window or door. If one or more of the limit switches $LS_1$ and $LS_2$ are closed momentarily prior to the nine second time delay, achieved through the capacitive resistive grouping mentioned above, the zener threshold voltage level will not have been reached, resulting in continual blocking of the triggering circuit associated with the gate means $SCR_7$. Thus, the occupant might close control key switch **14,** and subsequently close an exit door within the nine second time delay provided for, and no alarm will be sounded. Capacitor $C_9$ preferably has a capacitance of **.05** microfarads and serves only to assure the proper operation of the triggering circuitry described above. Resistor $R_8$ serves to cooperate with the resistor $R_5$ to define a voltage dividing network in combination with the zener $Z_6$, and one or more of the limit switches $LS_1$, $LS_2$, for a purpose to be described in greater detail hereinbelow.

Once an intrusion occurs, and a limit switch such as $LS_1$ closes, capacitor $C_3$ discharges through the zener $Z_6$, triggering the silicon control rectifier $SCR_7$ allowing current to be conducted through this SCR gate, providing battery voltage in the line $L_3$ with respect to the ground line $L_2$. Resistor $R_{11}$ serves to latch $SCR_7$ in its conductive state. If the "in" position of the mode switch **22** has been selected, the horn **24** will sound immediately or nearly so. A voltage dividing network is formed by resistors $R_{12}$ and $R_{10}$, through the mode switch **22** providing a triggering voltage for a unijunction transistor **26**, charging of capacitor $C_{15}$ in this particular mode of operation of the system is accomplished virtually instantaneously due to the fact that resistor $R_{10}$ comprises only 6,8K ohms. The unijunction transistor **26** comprises a threshold voltage device which triggers a secondary gate means, in the form of silicon control rectifier $SCR_{20}$, to conduct with the result that the horn **24** will have one side grounded by line $L_2$, and the other side provided with six volts through the line $L_4$. The resistor $R_{14}$ associated with the vibrating horn **24** allows its satisfactory operation, and also serves to latch the gate $SCR_{20}$ in its conductive state. Thus, in the case of a forced entry, with the occupant in his residence, and the "in" position of the mode switch selected, as mentioned above the alarm will sound virtually instantaneously following any intrusion. Actually, with the capacitances and resistances mentioned above a delay time of approximately 1/10 of a second will occur. The operation of the above-described circuitry in the "out" mode position of selector switch **22** will now be described.

Upon leaving this residence the occupant uses his key to close key control switch **14** allowing capacitor $C_3$ to charge as described above, with the resistor $R_5$ serving to limit the current flow to approximately $9\mu$ amperes with the result that when capacitor $C_3$ is fully charged a 9 second delay will have occured. Within this 9 second delay the occupant may open one of the secured exits, his front door for example if he intends to exit through the front door, and having opened one of the limit switches, such as $LS_1$ during this 9 second delay, no alarm will sound. This important feature of the present invention is possible by virtue of the placement of the limit switches $LS_1$ and $LS_2$ between the zener $Z_6$ and the gate means $SCR_7$. As mentioned above a voltage dividing network is formed consisting of resistor $R_5$ zener $Z_6$, one or more of the limit switches $LS_1$ and resistor $R_8$, to prevent the capacitor $C_3$ from charging above the required zener threshold voltage until one or the other limit switches, $LS_1$ and $LS_2$ for example, is again closed. In other words, the front door, or other exit through which the occupant intends to leave his premises may be held open as long as desired. The system only being armed when this door is reclosed and capacitor $C_3$ is recharged.

Once this door is closed, the capacitor $C_3$ is charged within the nine seconds mentioned above. The next entry will of course close one or more of the limit switches $LS_1$ providing a discharge path for the capacitor $C_3$ through the zener $Z_6$ triggering the silicon control rectifier gate $SCR_7$. As mentioned above, this will provide lines $L_2$ and $L_3$ at different potentials with respect to one another with no time delay.

With the "out" mode of selector switch **22** selected resistor $R_{10}$ with its limited resistance of 6.8K ohms is out of circuit, and resistor $R_{12}$ at 270K ohms controls the charging of capacitor $C_{15}$. At the expiration of a predetermined time delay, dictated by this capacitor resistive group $C_{15}$ and $R_{12}$, the unijunction transistor **26** will conduct triggering the gate $SCR_{20}$, when the threshold voltage of the unijunction transistor is exceeded. The horn **24** will thus be grounded, and line $L_4$ will carry the audio horn to sound, resistor $R_{14}$ serving not only to provide the necessary voltage on the intermittent horn device but also serving to latch the $SCR_{20}$ in its conductive state, and to retain this condition until key control switch **14** is switched to its "off" position.

Assuming that the key control switch **14** is turned on with the mode switch **22** in its "out" position the predetermined time delay mentioned in the preceeding paragraph will allow the occupant to secure any open door or window, after which time the alarm device will function so as to sound the alarm whenever an unauthorized entry closes one of the limit switches $LS_1$ or $LS_2$, or more particularly after the nine second delay following such unauthorized entry. This latter 9 second delay is intended to allow the occupant to return to his residence, to open the door with his usual household key, and to give him 9 seconds within which to get to the key control switch **14** and to turn it off. Once turned off, the occupant can reclose the door by which he just entered, and switch the mode selector switch to the "in" position, and reclose the key control switch **14** thereby activating the alarm system for the continued security of his residence.

A status check circuit is provided when the control switch **14** is first turned on, a timing network consisting of capacitor $C_{24}$ and resistor $R_{26}$ providing a short duration pulse via the charging of the capacitor $C_{24}$ to be applied through diode $D_{25}$ to the limit switches $LS_1$ and $LS_2$. If any such switch is closed, indicating that a door or window is not secure, a pulse path is provided to the gate $SCR_7$. The triggering of $SCR_7$ will of course initiate an alarm immediately if the mode switch is positioned to "in."

The timing network pulse of capacitor $C_{24}$ is also applied simultaneously through diode $D_{18}$ to a test circuit gate $SCR_{27}$. Triggering gate $SCR_{27}$ initiates an effective bridge of the mode switch, permitting capacitor $C_{15}$ to be charged in a reduced time since the normal timing network for triggering $SCR_{20}$ will have been parallelled by the combination of resistance $R_{10}$ and resistance $R_{12}$ leading to capacitor $C_{15}$. Thus, this circuitry performs in the same manner as the night "in" mode selector switch position. In conclusion then, the status network described above in affect overrides the time delay networks in both the primary sensing circuit and the secondary sensing circuit described above to provide an immediate audio alarm if any limit switch $LS_1$ or $LS_2$ is closed indicating an unsecure condition at a door or window or the like.

We claim:

**1.** An alarm system comprising:

a. a source of electrical energy,

b. a sensing circuit having at least one sensing device with contacts adapted to close in response to a condition to be detected,

c. a control switch for connecting said sensing circuit to said source,

d. an electrically energizable alarm device,

e. said sensing circuit further including selectively conductive solid state gate means for operating said sensing circuit to said alarm device,

f. said sensing circuit further including a first gate triggering network which includes said sensing device contacts,

g. said gate triggering network including a capacitive resistance group for delaying said first gate from conducting for a first predetermined time delay,

h. second solid state gate means in said sensing circuit and including a second triggering network which network includes a second capacitive resistance group for delaying said second gate from conducting for a second predetermined time delay, and

i. a mode switch forming a part of a paralleled resistive network to reduce said second delay when said mode switch is closed and to provide said second time delay following closing of said control switch and one of said sensing device contacts when said mode switch is opened.

**2.** The alarm system of claim **1** further characterized by a voltage threshold device in each of said gate triggering networks for controlling the voltage at which said gate is triggered by its associated capacitive resistance group.

**3.** The alarm system of claim **2** wherein at least one of said threshold devices comprises a zener so arranged that when the capacitive portion of said group is charged above the threshold associated with said zener, triggering voltage is available at the first solid state gate means via the closed contacts of said sensing device.

**4.** The alarm system of claim **3** further characterized in that said mode switch is more particularly located between said second threshold device and said second capacitive resistance group, and said parallel resistance network comprising a by-pass resistor so arranged as to increase the rate at which the capacitance portion of said second group is charged to the threshold voltage of said threshold device.

**5.** The alarm system of claim **4** further characterized by a sensing device status check circuit which permits said first gate triggering network to be by-passed in checking for closed contacts in said sensing device without encountering said first delay.

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# UNITED STATES PATENT OFFICE

# CERTIFICATE OF CORRECTION

Patent No. 3,803,576 Dated April 9, 1974

Inventor(s) John J. Dobrzanski and William J. Doyle

It is certified that error appears in the above-identified patent and that said Letters Patent are hereby corrected as shown below:

Inventor's name: Willaim J. Doyle should be

William J. Doyle

Col. 1, line 39, "be" should be --by--.

Col. 3, line 15, "6,8K" should be --6.8K--.

Signed and sealed this 1st day of October 1974.

(SEAL)
Attest:

McCOY M. GIBSON JR.
Attesting Officer

C. MARSHALL DANN
Commissioner of Patents

FORM PO-1050 (10-69)

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