



US006605962B2

(12) **United States Patent**
Lee et al.

(10) **Patent No.: US 6,605,962 B2**
(45) **Date of Patent: Aug. 12, 2003**

(54) **PLD ARCHITECTURE FOR FLEXIBLE
PLACEMENT OF IP FUNCTION BLOCKS**

(75) Inventors: **Andy L. Lee**, San Jose, CA (US);
Cameron McClintock, Mountain View,
CA (US); **Brian Johnson**, Sunnyvale,
CA (US); **Richard Cliff**, Los Altos, CA
(US); **Srinivas Reddy**, Fremont, CA
(US); **Chris Lane**, San Jose, CA (US);
Paul Leventis, Toronto (CA); **Vaughn
Timothy Betz**, Toronto (CA); **David
Lewis**, Toronto (CA)

(73) Assignee: **Altera Corporation**, San Jose, CA
(US)

(*) Notice: Subject to any disclaimer, the term of this
patent is extended or adjusted under 35
U.S.C. 154(b) by 0 days.

(21) Appl. No.: **10/057,442**

(22) Filed: **Jan. 25, 2002**

(65) **Prior Publication Data**

US 2002/0163356 A1 Nov. 7, 2002

Related U.S. Application Data

(60) Provisional application No. 60/289,311, filed on May 6,
2001.

(51) **Int. Cl.⁷** **H03K 19/177; H01L 21/182**

(52) **U.S. Cl.** **326/41; 326/38; 326/39;**
716/1; 716/16; 716/17

(58) **Field of Search** 326/38–41; 716/1,
716/16, 17

(56) **References Cited**

U.S. PATENT DOCUMENTS

4,870,302 A 9/1989 Freeman
4,871,930 A 10/1989 Wong et al.
5,121,006 A 6/1992 Pedersen
5,241,224 A 8/1993 Pedersen et al.
5,243,238 A 9/1993 Kean

5,260,611 A 11/1993 Cliff et al.
5,455,525 A 10/1995 Ho et al.
5,485,103 A 1/1996 Pedersen et al.
5,537,057 A 7/1996 Leong et al.
5,541,530 A 7/1996 Cliff et al.
5,550,782 A 8/1996 Cliff et al.
5,557,217 A 9/1996 Pedersen
5,581,199 A 12/1996 Pierce et al.
5,592,106 A 1/1997 Leong et al.
5,682,107 A 10/1997 Tavana et al.
5,689,195 A 11/1997 Cliff et al.
5,701,091 A 12/1997 Kean
5,705,939 A 1/1998 McClintock et al.
5,760,604 A 6/1998 Pierce et al.
5,847,579 A 12/1998 Trimberger
5,880,598 A 3/1999 Duong
5,903,165 A 5/1999 Jones et al.
5,907,248 A 5/1999 Bauer et al.
5,909,126 A 6/1999 Cliff et al.
5,914,616 A 6/1999 Young et al.
5,942,913 A 8/1999 Young et al.
5,977,793 A 11/1999 Reddy et al.
6,084,429 A 7/2000 Trimberger
6,107,824 A 8/2000 Reddy et al.

(List continued on next page.)

OTHER PUBLICATIONS

Altera Corporation (Jun. 1996). "Max 7000: Programmable
logic device family" *Data Book, A-DB-0696-01*, version 4,
pp. 193–261.

(List continued on next page.)

Primary Examiner—Michael Tokar

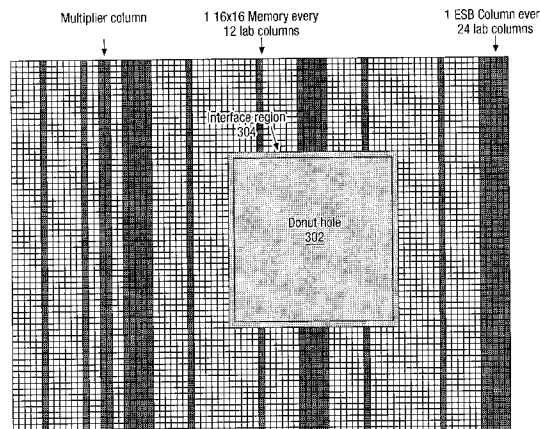
Assistant Examiner—Vibol Tan

(74) *Attorney, Agent, or Firm*—Morrison & Foerster LLP

(57) **ABSTRACT**

In accordance with one aspect of the invention, a hole is
formed within an LE array of a PLD by interrupting the LE
array base signal routing architecture such that a hole is left
for IP function block to be incorporated. An interface region
is provided for interfacing the remaining LE array base
signal routing architecture to the IP function block.

20 Claims, 7 Drawing Sheets



U.S. PATENT DOCUMENTS

6,204,690	B1	3/2001	Young et al.	
6,218,859	B1	4/2001	Pedersen	
6,278,291	B1	8/2001	McClintock et al.	
6,289,412	B1 *	9/2001	Yuan et al.	703/14
6,292,018	B1	9/2001	Kean	
6,300,794	B1	10/2001	Reddy et al.	
6,484,291	B1 *	11/2002	Amiya et al.	716/1
2001/0033188	A1	10/2001	Aung et al.	
2002/0163358	A1 *	11/2002	Johnson et al.	326/41

OTHER PUBLICATIONS

Altera Corporation (Oct. 2001). Excalibur “Description of the The Floor plan”, pp. 1–1 through 1–10.

Betz, V. et al., eds. (1999) “Background and Previous Work,” Chapter 2 *In Architecture and CAD for Deep-Submicron FPGAs*, Kluwer Academic, Boston pp. 12–18.

Betz, V. et al., eds. (1999). “Routing Tools and Routing Architecture Generation,” Chapter 4 *In Architecture and CAD for Deep-Submicron FPGAs*, Kluwer Academic, Boston, pp. 63–95.

Betz, V. et al., eds. (1999). “Detailed Routing Architecture,” Chapter 7 *In Architecture and CAD for Deep-Submicron FPGAs*, Kluwer Academic, Boston, pp. 151–190.

Betz, V. et al., eds. (1999). “Global Routing Architecture,” Chapter 7 *In Architecture and CAD for Deep-Submicron FPGAs*, Kluwer Academic, Boston, pp. 105–126.

Xilinx. (Nov. 2000). “Programmable Logic: News and Views, a montly report on developments in the PLD/FPGA industry” *Electronic Trend Publications, Inc.*, IX(11):14–15. (Includes Table of Contents).

Xilinx. (Oct. 2000) “Putting It All the Together. The Vitrex-II Series Platform FPGA: World fastest logic and routing” Xilinx brochure, p. 83.

* cited by examiner

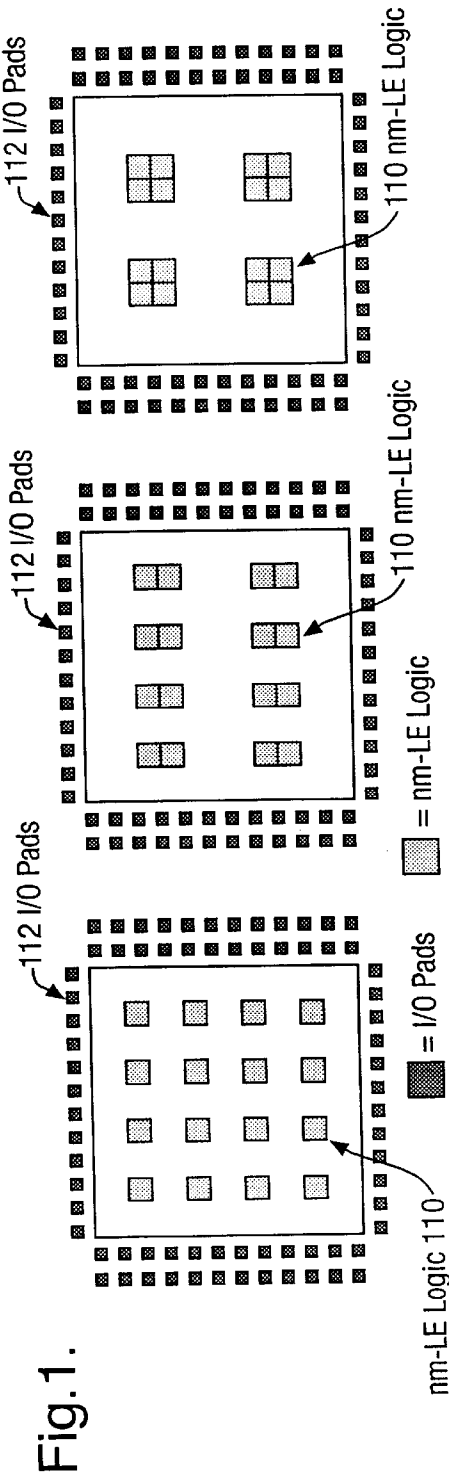
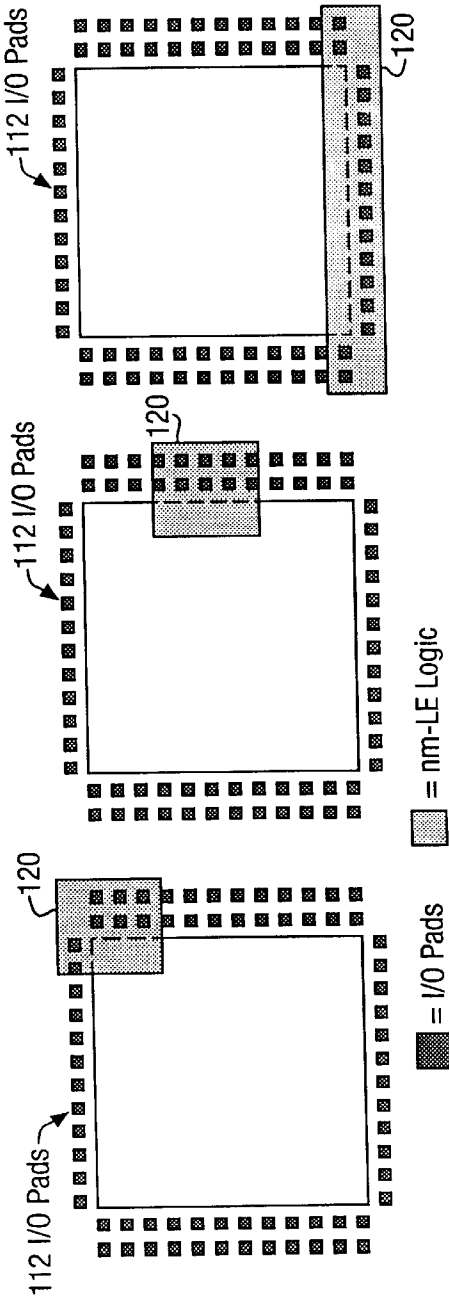


Fig. 2. C

Fig. 2. B

Fig. 2. A



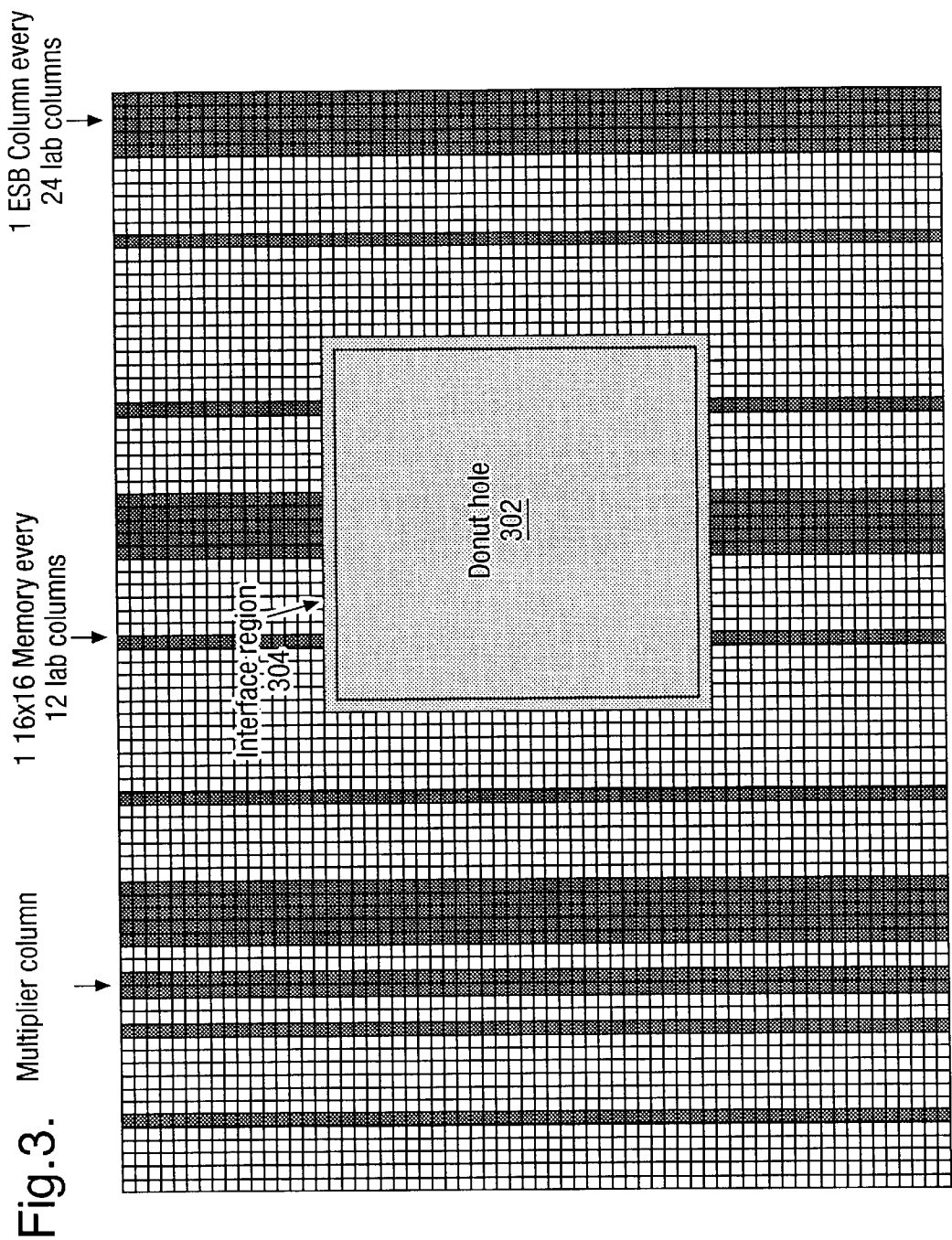


Fig.4.

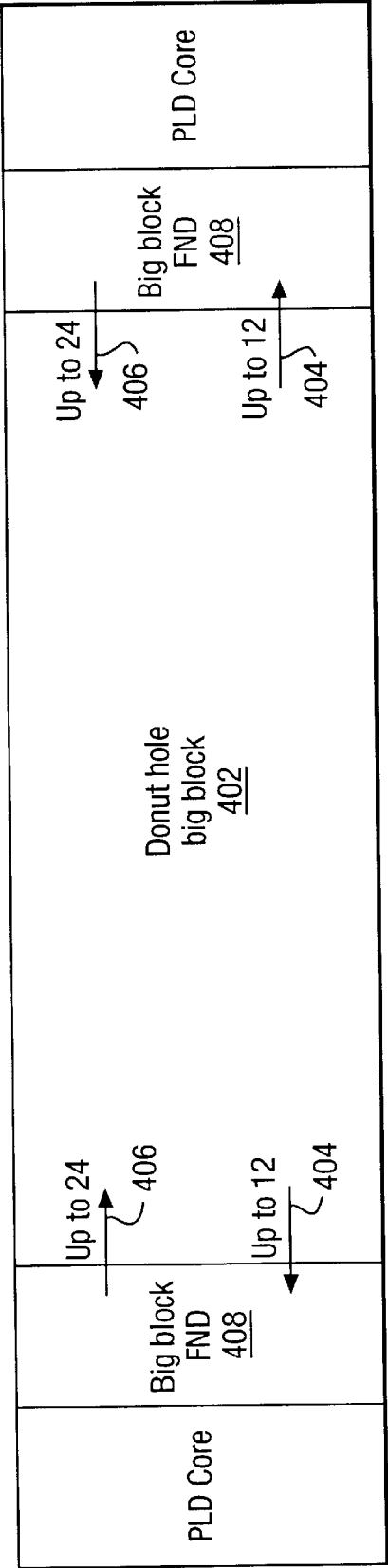


Fig.5.

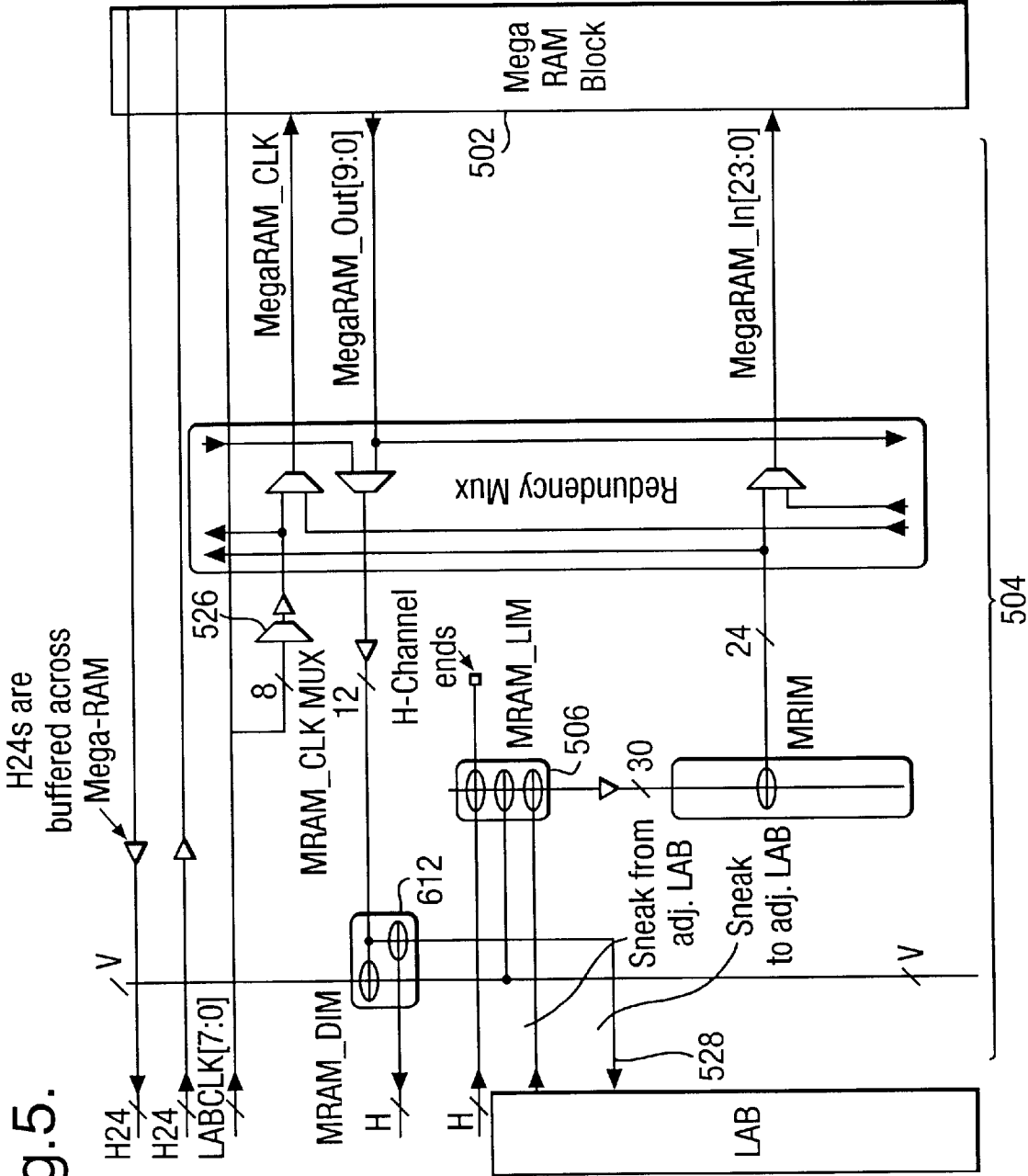


Fig. 6.

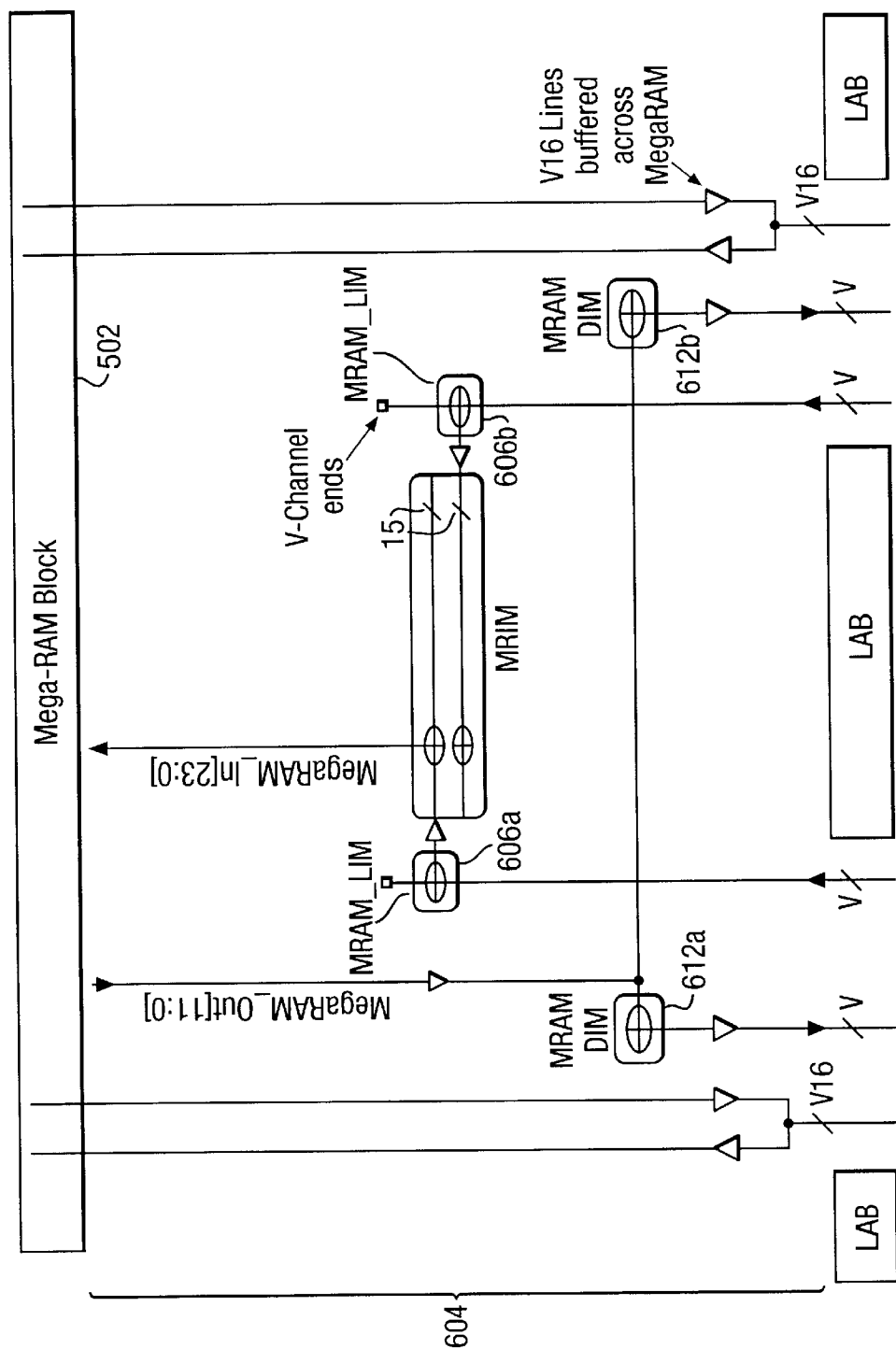


Fig.7.

	Horizontal MegaRAM Interface		Vertical MegaRAM Interface	
	Ways in per line	Connections per MRAM_LIM	Ways in per line	Connections per MRAM_LIM
H4	3	8	0	0
H8	3 or 4	2 or 3	0	0
H24	0	0	0	0
V4	1 or 2	4	4 or 5	12
V8	1 or 2	1 or 2	3 or 4	4
V16	0	0	0	0
Sneak path from adjacent LAB	1	0 or 1	0	0
Total MRAM LIM fanin		16		16
Total number MRAM LIM muxes	30		30	

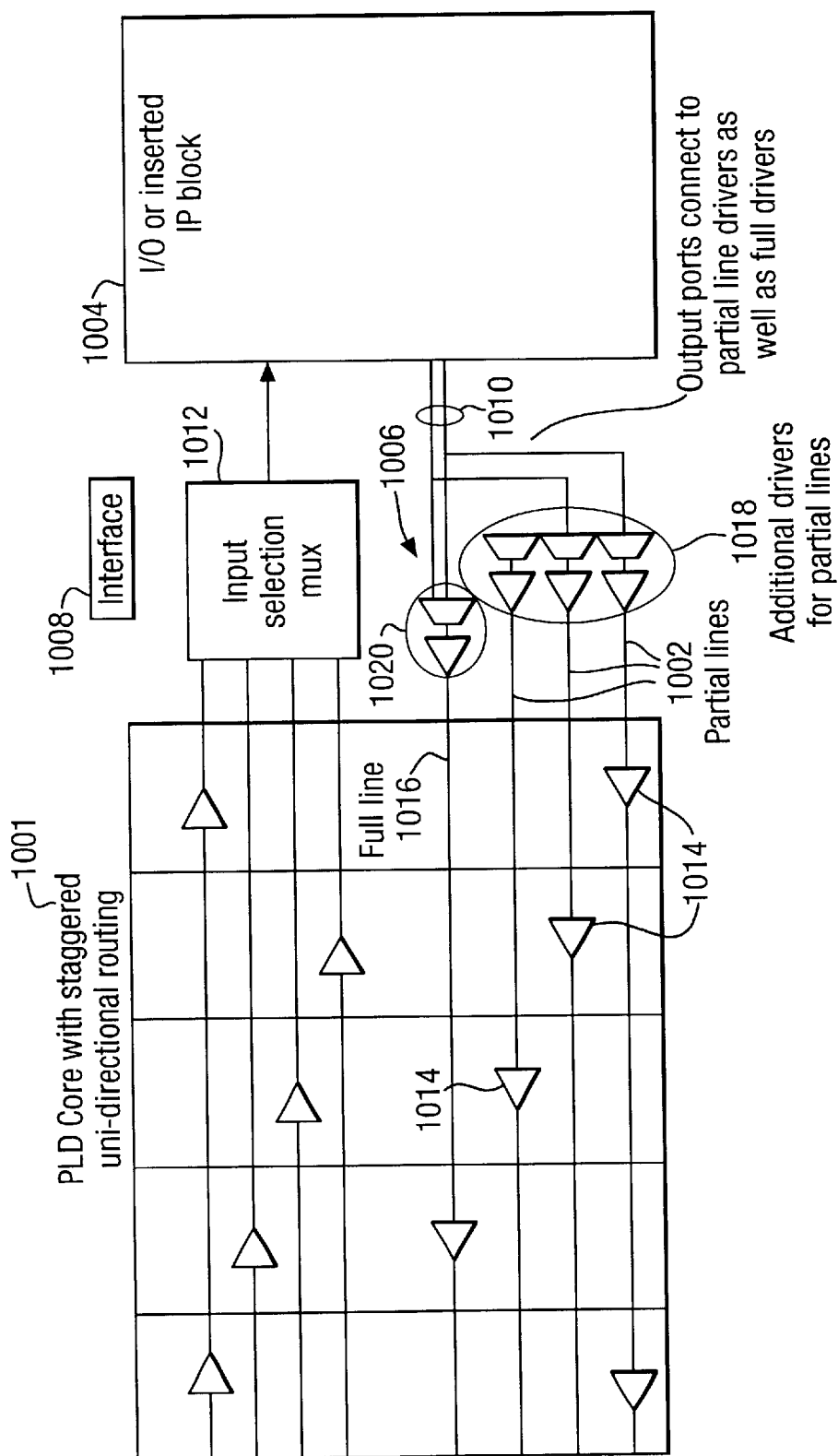
Fig.8.

	Mega-RAM Horizontal Interface	Mega-RAM Vertical Interface
H4 DIM	9 or 10	N/A
H8 DIM	1, 2 or 3	N/A
H24 DIM	0	N/A
V4 DIM	5	5
V8 DIM	2 or 3	1
V16 DIM	0	N/A
Total ways out per MegaRAM Out	17 to 21	6

Fig.9.

	Mega-RAM Horizontal Interface	Mega-RAM Vertical Interface
Lablines	30	30
MRIMs	24	24
H4 Drivers	20	0
H8 Drivers	3	0
H24 Drivers	0 or 1	0
V4 Drivers	10 + 10 redundant	20
V8 Drivers	2 + 2 redundant	4
V16 Drivers	0 or 1 + 0 or 1 redundant	0

Fig. 10.



1

PLD ARCHITECTURE FOR FLEXIBLE
PLACEMENT OF IP FUNCTION BLOCKS

RELATED APPLICATIONS

This application claims priority to provisional patent application No. 60/289,311, filed May 6, 2001.

TECHNICAL FIELD

The present invention is in the field of programmable logic devices (PLD's) and, more particularly, relates to a flexible architecture by which logic elements (LE's) of a PLD having an array of logic elements are replaced with intellectual property (IP) function blocks.

BACKGROUND

Conventional programmable logic devices (PLD's) comprise one or more arrays of logic elements (LE's), and the base signal routing architecture between LE's is designed such that LE-to-LE routing (typically performed by software programs that convert hardware design language program instructions into such routing) is optimized. Examples of PLD's having more than one array include PLD's in the APEX family of devices, by Altera Corporation of San Jose, Calif. It is sometimes desired to add one or more IP function blocks among an LE array. For the purposes of this disclosure, an LE is considered to be a basic—or most common—logic element that functions, for example, with respect to look-up table or macrocell logic. The LE's of an array are nominally connected by a base signal routing architecture. An IP function block is a functional block that is not constrained by the function of the most common logic element. For example, by way of illustration and not by limitation, an IP function block may be a high-speed serial interface (HSSI), a digital signal processor or other microprocessor, ALU, memory, or a multiplier.

Conventionally, when an IP function block is added to an LE array, the IP function block is placed at an edge of the LE array and spanning the entire edge of the LE array. This minimizes the disruption in the base routing. Furthermore, by placing the IP function block at an edge of the array, the performance degradation that would otherwise be caused by routing over the IP function block is minimized. A disadvantage of placing the IP function block at an edge of the LE array, however, is that the input/output (I/O) cells (for communication off the LE array) are conventionally located at the edge of the LE array. The IP function block may not even require access to the I/O cells at that edge but, nonetheless, impedes access by other elements (LE's, or even other IP function block) to the I/O cells at the edge where the IP function block is placed. In some cases, such as is described in U.S. Pat. No. 5,550,782, a block such as an embedded array block (EAB) completely replaces a logic array block (LAB) of LE's. In this case, the routing connects to the EAB in much the same way that the routing interfaces with the conventional logic block and, thus, there is no corresponding performance degradation.

Clearly, placement of an IP function block within an LE array of a PLD has commonly been an afterthought such that, typically, an IP function block was merely placed where it could best fit to minimize the disruption to the base signal routing architecture. What is desired is a PLD architecture by which the placement of an IP function block is not dictated by the goal of minimizing the disruption to the base signal routing architecture.

SUMMARY

In accordance with one aspect of the invention, a “hole” is formed within an LE array of a PLD by interrupting the

2

base signal routing architecture such that a hole is left for the IP function block to be incorporated. An interface region is provided for interfacing the remaining base signal routing to the IP function block. This provides for flexible placement of IP function block within the regular LE-routing structure of the PLD.

BRIEF DESCRIPTION OF FIGURES

FIG. 1 illustrates possible placements of “big” IP function blocks within a PLD and not adjacent to an edge of the LE array, for a “big” IP function block such as a memory for which direct I/O access is not a requirement.

FIGS. 2A, 2B and 2C illustrate possible placements of big IP function blocks within a PLD and adjacent to an edge of the LE array such that direct I/O access is provided.

FIG. 3 illustrates a “donut hole” within the context of a PLD, for placement of a “big” IP function block within a PLD and not adjacent to an edge of the LE array.

FIG. 4 illustrates, in greater detail, a “big block” interface region as used in FIGS. 1, 2 and 3.

FIG. 5 illustrates the horizontal interface to a “big block” that is a large random access memory (“MRAM”).

FIG. 6 illustrates the vertical interface to the MRAM.

FIG. 7 is a table illustrating connectivity details of the MRAM_LIM

FIG. 8 is a table illustrating the MegaRAM_Out signal connections.

FIG. 9 is a table illustrating the Mega-RAM interface specifications.

FIG. 10 illustrates an embodiment of a staggered routing architecture, in which the partial lines at the boundary of the staggered routing architecture are driven.

DETAILED DESCRIPTION

FIGS. 1 and 2 illustrate possible floorplans for a PLD architecture in accordance with an aspect of the invention. The illustrations in FIG. 1 are examples only, and the invention is not limited to the examples shown in FIG. 1. In accordance with the invention, a method of creating the FIG. 1 floorplans (and other floorplans within the scope of the invention) is now described.

The base signal routing architecture is defined and optimized for LE's. For example, an array of LE's is created for a particular target die size. For variants of the created LE array, as discussed in the Background, it is desired to place the IP function block within the LE array. In some embodiments, the IP function block is added as IP function blocks at some desired uniform density, although the density of IP function blocks need not be uniform. For IP function blocks added to the LE array, LE's are replaced. Thus, there is a tradeoff between LE's and the amount of IP added to the die. The array of LE's for which a particular base signal routing architecture is optimized may occupy substantially an entire target die. Alternately, a base signal routing architecture may be optimized for an array of LE's that coexists on a die with other circuitry, including other LE's.

FIGS. 1A, 1B and 1C illustrate IP function block 110 incorporated within the interior of an LE array, for an IP function block that does not require direct I/O pad 112 access. FIGS. 2A and 2B illustrate an IP function block 120 incorporated at the edge of the LE array but not spanning the entire edge of the LE array, such that I/O pad 112 access is provided to the IP function block 120. Furthermore, while not shown in FIGS. 2A and 2B, the IP function block can even displace I/O pads 112, if desired.

FIG. 3 illustrates how an IP function block is incorporated as a “donut hole” **302** as applied to the FIG. 1 examples. That is, within the region where the IP function block is incorporated, the base signal routing architecture is interrupted, and a hole **302** is left (at least in one layer of the metal) for the IP function block to be incorporated. In addition, an interface region **304** is provided completely surrounding the hole **302** for interfacing the remaining base signal array routing to the IP function block. A very specific example of one such interface block is described later with reference to FIGS. 5 and 6. It should be noted that some of the lines of the base signal routing architecture may be routed around the hole **302** by being raised from the interface region **304** at one side of the hole **302** to a different layer of the metal not occupied by the hole **302** and lowered back into the interface region **304** at another side of the hole **302**, typically the opposite side of the hole **302**. To generalize, signal routing lines for driving shorter distances are terminated, and routing lines for driving longer distances are raised to a different layer of metal, buffered across the hole, and lowered into the interface region at the opposite side of the donut hole. What is “shorter” and “longer” is variable for any particular embodiment and is discussed later with respect to the size of the interruption—“small” or “large.” Typically, those routing lines buffered across a hole do so without being connected to the IP function block in the hole region.

An interface region is provided even when the IP function block is not to be bordered on all four sides by the base signal routing architecture as illustrated in the FIG. 3 embodiment but, rather, is to be bordered on two sides (an example of which is shown in FIG. 2A), three sides (an example of which is shown in FIG. 2B), or even one side (an example of which is shown in FIG. 2C). The interface region is typically provided on each side of the hole that borders the base signal routing architecture.

FIG. 4 illustrates an embodiment of the interface region **304**. That is, in accordance with the FIG. 4, it is shown that, for some level of granularity, the interface region **408** includes up to 24 signal lines into the hole **402** and up to 12 signal lines out of the hole **402**. The interface region **408** is built modularly, at a particular level of granularity. In one embodiment, the particular level of granularity is one width or height of the logic array block (LAB) of the LE array.

A design consideration for the placement of a hole is the number of signal lines in and out of a hole that would result from a particular placement, primarily as a result of the extent to which the hole would border the base signal routing architecture. This can be seen with reference again to FIGS. 2A and 2B.

FIGS. 5 and 6 illustrate a situation where the IP function block is a RAM block (designated in FIGS. 5 and 6 as a “Mega-RAM” **502**). FIG. 5 illustrates the situation from the horizontal routing perspective, and FIG. 6 illustrates the situation from the vertical routing perspective. The Mega-RAM block **502** spans multiple columns and multiple rows of the LE array, and therefore interfaces with many lines (“channels”) of routing. The general routing does not cross the Mega-RAM **502**. Rather, the general routing “dead ends” at the Mega-RAM Interface (a specific instance of the FIG. 3 interface region) to form the donut hole for the Mega-RAM. The H24 (FIG. 5) and V16 (FIG. 6) routing lines are buffered across the Mega-RAM block. The Mega-RAM horizontal interface **504** (FIG. 5) allows the Mega-RAM to interface to logic to the left or to the right of the Mega-RAM. The Mega-RAM vertical interface **604** (FIG. 6) allows the Mega-RAM to interface to logic above and below the

Mega-RAM. In the Mega-RAM vertical interface (FIG. 6), there are two groups of fifteen MRAM_LIM’s (Not all are shown). Each of the two groups is fed by a different V-Channel. One Mega-RAM interface is provided on each of the left and right hand edges of the MegaRAM for every LAB row it spans, and one Mega-RAM interface is provided on each of the top and bottom edges of the Mega-Ram for every pair of LAB columns it spans.

Driving into the Mega-RAM **502** is now described. H and V routing lines in a typical embodiment connect into MRAM_LIM’s **506**, **606a** and **606b** (LAB input multiplexers). The MRAM_LIM’s **506**, **606a** and **606b** is a two stage 4-way sharing multiplexer. Of the portion of the routing that terminates at the boundaries of the Mega-RAM **502**, only the routing able to carry signals toward the Mega-RAM **502** feeds the MRAM_LIM’s **506**, **606a** and **606b**. Therefore, if the routing is unidirectional (i.e., each line can carry a signal in one direction), then routing able to carry signals away from the MRAM will not be coupled to the input interface. In another embodiment, bi-directional lines are used in addition to, or in place of, unidirectional lines.

Connectivity details of the MRAM_LIM **506**, **606a** and **606b** are listed in the table of FIG. 7. Briefly, FIG. 7 lists the number of “ways in per line” and the number of “connections per MRAM_LIM” for each of the Horizontal Mega-RAM interface (FIG. 5) and the Vertical MegaRAM interface (FIG. 6). At the bottom of the FIG. 7 table, the listed totals include the total number of MRAM_LIM fan in signals, and the total number of MRAM_LIM multiplexers, for each of the Horizontal MegaRAM interface and the Vertical MegaRAM interface.

Clock inputs **524** are taken into the Mega-RAM block **502** from the global clock network at the side of the Mega-RAM block **502** through the Mega-RAM horizontal interface **504** in (FIG. 5). The MRAM_CLOCK_MUX **526** chooses one of the eight LABCLK’s that are feeding through the adjacent LABs. There is one clock input to the Mega-RAM **502** per row, although the Mega-RAM **502** typically would not use every clock input available to it.

The Mega-RAM input mux (“MRIM”) is a fully populated 4-way mux-sharing mux that connects thirty LAB lines onto twenty-four I/O block inputs.

Driving out of the Mega-RAM **502** is now described. At the edge of the Mega-RAM, routing lines driving into the core do not have LAB’s to drive them and are left as partial length lines. The Mega-RAM interface uses the full-length and partial length (i.e., length four and length eight lines, in this embodiment) to connect to the core via the MRAM_DIM. The Mega-RAM interface provides similar resources as are provided for a LAB to drive onto the core routing. For example, H4 lines extending four LAB’s into the core are driven, and H4 lines extending three LAB’s in or less are not driven. These partial length lines are driven to Vcc. In another embodiment, the partial length lines connect to the MRAM_LIM’s as described below with reference to FIG. 10.

The Mega-RAM horizontal interface can also drive signals out onto the adjacent V-channel routing. Ten partial length sneak paths (H4, H8, V16, H24) (e.g., as collectively designated by line **528**) are driven directly into adjacent LAB’s by ten of the twelve MegaRAM_Out signals for a “quick” path to logic.

Each MRAM driver input multiplexer (“MRAM DIM”) **612a**, **612b** supports the V-channel at the edge of the core and the half H-channel able to carry signals from the MRAM

5

in the direction of the core. The Mega-RAM vertical interface **604** drives the full-length routing resources of two full V-channels. These drivers are dedicated to the MegaRAM_Out signals and do not support turns from other routing resources. The DIM's **612a** and **612b** associated with the V-line drivers in the Mega-RAM vertical interface **604** are used to choose between MegaRAM_Out signals. Each DIM **612a**, **612b** in the vertical interface is a 4:1 mux that can be implemented in one or more stages, and each input to the DIM is a MegaRAM_Out signal. The connection pattern from the MegaRAM_Out signals to the DIM **612a**, **612b** is typically spread equally between the two V-channels.

The number of MegaRAM_Out signal connections per DIM for each of the Mega_RAM Horizontal Interface (FIG. 5) and the Mega_RAM Vertical Interface (FIG. 6) are set forth in FIG. 8. FIG. 9 is a summary of the Mega_RAM interface specifications for each of the Mega_RAM Horizontal Interface and the Mega_RAM Vertical Interface, and lists the total number of the various interface components described above.

It is noted that, typically, not all IP function blocks need be incorporated into an LE array using the hole concept. For example, the IP function block may be of two types—small and large. In general, the terms small and large as used here can be thought of as indicating size. One actual design consideration, however, in determining whether to consider particular IP function block as small or large is a consideration of how much disruption to the timing of signal routing is to be tolerated. For example, in accordance with one embodiment, a small block is an IP function block whose layout can be drawn at a width on the order of an LE width. In accordance with this embodiment, the width of small blocks may be wider than an LE so long as the timing of signal routing over the block does not get significantly larger than for routing over an LE. For example, in one 0.13 μm architecture, it has been deemed that the timing of the signal routing over a block of roughly 5 LE widths does not get significantly larger than for routing over an LE. Typically, additional inputs and/or outputs may be added that exceed the width of an LE, so long as the base signal routing architecture across the IP function block is maintained with the LE's surrounding the small block. Another consideration for determining whether an IP function block is large (implemented using the hole concept) or small is the size of the IP function block relative to the overhead associated with employing an interface region. In one embodiment, small blocks include MEAB's (medium sized embedded array blocks), SEAB's (small sized embedded array blocks) and a DSP block. By contrast, large blocks are IP function blocks that typically have dimensions much larger than that of an LE. Extending the base signal routing architecture across these blocks without modification would cause routing over these blocks to be significantly larger than routing over an LE, forming a boundary in the PLD timing model. Such large blocks may be inserted into the LE array as holes in the base signal routing architecture, as described above. In some sense, what occurs at the boundary between the base signal routing architecture and a hole is similar to the base signal routing architecture ending at the edge of an LE array.

In some embodiments, shown with reference to FIG. 10, the LE routing lines are part of a staggered, uni-directional routing architecture. As a result of the staggering, as can be seen from FIG. 10, there are partial lines **1002** at boundaries formed by, for example, the I/O interface **1008** at the edge of the PLD **1001** or by an inserted IP function block (designated by reference numeral **1004**). In accordance with some such staggered architecture embodiments, routing

6

drivers **1006** are included in the interface region **1008** (whether the I/O interface region or the hole interface region) to drive both the full and partial lines. The output ports **1010** of the logic block **1004** connect to the drivers of both the "full" lines and the "partial" lines. Signal selection muxes may be used in front of the drivers to add routing flexibility. As described above, the routing may also be implemented with segmented bi-directional lines.

The partial lines **1002** driving out of the PLD core **1001** feed an input selection mux **1012** to drive into the logic block **1004**. These partial lines **1002** impose a smaller load on the drivers **1014** than do full lines **1016**, and having a small load makes the partial line **1002** a faster path into the PLD core **1001**. If area is a concern, drivers **1018** for partial lines **1002** may be smaller than drivers **1020** for full lines **1016**, and still not be at a speed disadvantage due to the smaller load.

Furthermore, by driving even the partial lines **1002**, additional routing flexibility is provided for signals from the PLD core **1001** to the PLD boundaries. Allowing the partial lines **1002** headed out of the PLD **1001** to drive into an IP function block **1004** increases the routability from the PLD core **1001** to the logic block **1004**. In addition, the additional drivers **1018** may be used to provide the core **1001** access to more signals, or the signals may be used to provide more paths into the PLD core **1001** for a given signal. Thus, quite simply, lines that would have otherwise been unused are utilized to provide needed access to the PLD core **1001**.

While the present invention has been particularly described with respect to the illustrated embodiments, it will be appreciated that various alterations, modifications and adaptations may be based on the present disclosure, and are intended to be within the scope of the present invention. While the invention has been described in connection with what are presently considered to be the most practical and preferred embodiments, it is to be understood that the present invention is not limited to the disclosed embodiment but, on the contrary, is intended to cover various modifications and equivalent arrangements included within the scope of the claims. For example, the techniques described herein may be applied to other types of fixed blocks or routing structures.

What is claimed is:

1. A programmable logic device (PLD), comprising:
a plurality of logic elements (LE's) arranged in an array;
a base signal routing architecture including a plurality of signal routing lines to route signals among the LE's,
wherein

a hole is formed in the array of LE's, and the hole is characterized by a perimeter portion and a central portion;

the base signal routing architecture is, at least in part, interrupted at the hole; and

the PLD further comprises interface circuitry within the perimeter portion of the hole, configurable to couple circuitry within the hole to the signal routing architecture; and

the PLD further comprises an IP function block within the hole and electrically coupled to the interface circuitry.

2. The PLD of claim 1, wherein:

a portion of the base signal routing architecture is routed across the hole.

3. The PLD of claim 2, wherein:

the portion of the signal routing architecture routed across the hole is routed across the hole in a physical layer of the PLD other than the physical layer where the base routing architecture is routed in the remainder of the PLD.

4. The PLD of claim 3, wherein:
the IP function block is a first IP function block;
the PLD further comprises a second IP function block, and
the second IP function block is not within a hole formed
in the array of LE's, such that the base signal routing
architecture is not interrupted at the second IP function
block.
5. The PLD of claim 4, wherein:
the first IP function block circuitry is of a size such that,
if all of the base signal routing architecture were routed
across the first IP function block, the signal timing of
the base signal routing architecture would be inter-
rupted more than a predetermined threshold; and
the timing of the base signal routing architecture routing
across the second IP function block is interrupted less
than the predetermined threshold.
6. The PLD of claim 1, wherein the hole is completely
surrounded by the base signal routing architecture.
7. The PLD of claim 1, wherein the hole is surrounded by
the base signal routing architecture on at least two sides.
8. The PLD of claim 1, wherein the hole does not displace
or replace any I/O pads to the base signal routing architec-
ture.
9. The PLD of claim 2, wherein the hole displaces or
replaces I/O pads in the base signal routing architecture.
10. The PLD of claim 1, wherein the IP function block
includes circuitry for input/output between the IP function
block and other than the base signal routing architecture.
11. A programmable logic device (PLD), comprising:
a plurality of logic elements (LE's) arranged in an array;
a base signal routing architecture including a plurality of
signal routing lines to route signals among the LE's, the
signal routing lines including short lines and long lines,
at least one IP function block inserted into the array in
place of a portion of the LE's, wherein a first subset of
the short lines connect to the IP function block and
second subset of the short lines terminate at the IP
function block while at least one long line passes by the
IP function block.
12. The PLD of claim 11, where in the short lines have a
length less than the length of 8 LE's and the long lines have
a length greater than or equal to the length of 8 LE's.

13. The PLD of claim 11, wherein a third subset of the
short lines passes by the IP function block.
14. A semiconductor integrated circuit, comprising:
a plurality of logic elements (LE's) arranged in an array
with at least one IP function block inserted into the
array.
a base signal routing architecture connected to the LE's
and at least partially interrupted by the IP function
block, such that a first portion of the base routing
architecture is terminated at the IP function block and
a second portion of the base signal routing architecture
continues past the IP function block.
15. The semiconductor integrated circuit of claim 14,
wherein:
the semiconductor integrated circuit further comprises an
interface portion; and
a third portion of the base signal routing architecture
connects to the IP function block via the interface
portion.
16. The semiconductor integrated circuit of claim 15,
wherein base signal routing architecture includes long rout-
ing lines and short routing lines, wherein at least some of the
long routing lines continue by the IP function block and at
least some of the short routing lines terminate or connect to
the IP function block.
17. The semiconductor integrated circuit of claim 14,
wherein some of the IP function blocks are placed so as not
to interrupt the base signal routing architecture.
18. The semiconductor integrated circuit of claim 17,
wherein a decision as to whether the IP function block is
placed to interrupt the base signal routing architecture is
based on the physical size of the IP function block.
19. The semiconductor integrated circuit of claim 18,
wherein the decision is based on the physical size as
indicated by the die space occupied by the IP function block.
20. The semiconductor integrated circuit of claim 18,
wherein the decision is based on the physical size as
indicated by timing parameters.

* * * * *