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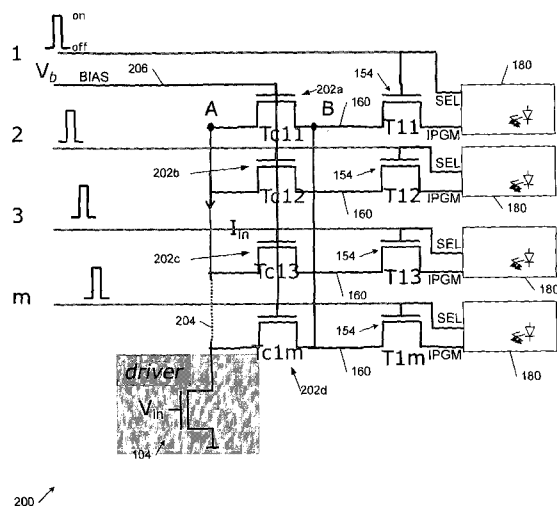
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Figure 2

(57) **Abstract:** An active matrix display comprises a plurality of OLED pixels each having an associated current-programmed pixel drive circuit, the pixel drive circuit having a pixel select line and a current programming input for programming the associated OLED pixel when said pixel select line is active. The display further comprises at least one distributed cascode transistor shared between a set of said pixel drive circuits, the distributed transistor comprising a set of transistors each having an input connection, an output connection and a control connection. Each of the transistors of the set is in physical proximity to a respective pixel drive circuit and has its output connection connected to the current programming input of said respective pixel drive circuit. The input connections of the transistors of said set are connected together in parallel, the output connections of the transistors of the set are connected together in parallel, and the control connections of the transistors of the set are connected together in parallel. The parallel-connected input connections are connected to a common current programming line for said set of said pixel drive circuits.



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OLED DISPLAY DRIVE CIRCUITS AND TECHNIQUES

FIELD OF THE INVENTION

- 5 This invention relates to improved pixel drive techniques for organic light emitting diode (OLED) displays.

BACKGROUND TO THE INVENTION

- 10 It is known to drive an OLED display using an 'active matrix' arrangement in which individual pixels of a display are activated by an associated thin film transistor. In one drive technique an analogue current is employed to program the drive current of an active matrix OLED pixel so that the current through the pixel, and hence the luminance, is proportional to the programmed level. Thus in a standard current
15 programmed pixel circuit a data line supplies a current which is copied, either on a 1:1 basis or with a fixed scaling, to an output stage.

- As OLED displays become larger the length of backplane pixel interconnects increases and, for HDTV (high definition television) can be of order 1 metre in length. Further, the
20 gamma function results in a dynamic range for such a display of 1000:1 between the maximum grey-level and minimum non-zero grey level and in sRGB standard displays this increases to approximately 200,000:1. The minimum grey-level current may typically be less than 10 nA for the ITU Rec709 standard used for HDTV, and may be less than 100 pA for sRGB.

- 25 With large displays and hence long current programming lines such small currents present a significant challenge, in particular because of the relatively large capacitance associated with such lines. The programming time τ_{pgm} is proportional to the line and other associated capacitance C_x , to the change in voltage, ΔV , on the line imposed by
30 (current) programming of a pixel, and is inversely proportional to the programming current, I_{prog} , as follows:

$$\tau_{pgm} \propto \frac{C_x \Delta V}{I_{prog}}$$

We have described in our co-pending patent application (GB1102949.3) techniques for, in effect, increasing the value of I_{prog} , and in our co-pending UK patent application GB 2,462,646 the use of negative capacitance circuits to decrease C_x . We now describe
5 techniques for addressing the ΔV term in the above equation.

SUMMARY OF THE INVENTION

10 According to a first aspect of the invention there is therefore provided an active matrix OLED display panel, the panel comprising: a plurality of OLED pixels each having an associated current-programmed pixel drive circuit, said pixel drive circuit having a pixel select line and a current programming input for programming an OLED pixel for the associated OLED pixel when said pixel select line is active; and wherein said OLED
15 display panel further comprises at least one distributed cascode transistor shared between a set of said pixel drive circuits, wherein said distributed cascode transistor comprises a set of transistors each having an input connection, an output connection and a control connection, wherein each of said transistors of said set is in physical proximity to a respective one of said set of said pixel drive circuits and has said output
20 connection connected to said current programming input of said respective one of said pixel drive circuits, wherein said input connections of said transistors of said set are connected together in parallel, said output connections of said transistors of said set are connected together in parallel, and said control connections of said transistors of said set are connected together in parallel, and wherein said parallel-connected input
25 connections of said transistors of said set are connected to a common current programming line for said set of said pixel drive circuits.

Broadly speaking, use of a cascode transistor stabilises the voltage on the constant current source or sink programming the pixel current, in effect reducing the output
30 impedance of the current source/sink. This reduces voltage variations on the current programming line, and hence decreases programming time. More particularly, however, the cascode transistor is distributed amongst a set of the pixel drive circuits and the cascode functionality is shared between these pixel drive circuits.

35 In embodiments each of the pixel drive circuits is provided with a respective cascode transistor, and the cascode transistors of the set of pixel drive circuits are connected

together in parallel, the collective input (source or drain) to this distributed cascode transistor being connected to a common current programming line for the set of pixel drive circuits. This has the effect of stiffening the voltage on the common current programming line. In principal a separate cascode transistor could be employed for each pixel drive circuit, but an improved cascode functionality can be achieved by providing a high transconductance, and thus the (cascode) device should have a relatively wide channel. Such a device is not necessarily practical but an effective wider channel for the distributed cascode transistor can be achieved by connecting a plurality of (standard size) cascode transistors in parallel. These parallel-connected devices may be distributed amongst the pixel drive circuits to achieve the desired effect without the need for a single very 'fat' transistor.

Although the input capacitance for the set of parallel connected transistors is slightly larger than for a single, wide-channel device, the benefits outweigh this small disadvantage. Distributing the cascode transistors also means that there is a little more (column) capacitance at the further end of the common current programming line for the cascode transistor connected at this point, but again the deleterious effect of this is small.

In embodiments each source connection of a cascode transistor of the set is directly connected to the common current programming line, and each drain connection of a transistor of the set is connected directly to a switch or select transistor of the pixel drive circuit. The parallel-connected gates of the transistors are, in embodiments, connected to a bias voltage line. This may comprise either a local connection for the set of pixel drive circuits sharing the distributed cascode transistor, or a global line for the display panel. Where a local, preset bias voltage connection is provided this enables the set of pixel drive circuits (associated with the paralleled cascode transistors) effectively to be disconnected or made inactive. Thus this line may, for example, be used as a form of select line and/or to reduce charge injection/input capacitance. In still other embodiments a bias voltage for a cascode transistor of the set may be generated locally, or potentially even by the transistor itself (for example in a depletion-mode junction FET the gate may simply be grounded).

In embodiments the display panel comprises at least one bias circuit to provide a bias voltage for the distributed cascode transistor. The bias voltage is selected so that the cascode transistor is in a minimal required on-state so that it provides a channel to the

programming current supplied/taken by the driver to/from the pixel circuit. The voltage on the common current programming line is set by the bias voltage of the cascode transistor, with an offset dependent on the threshold voltage of the distributed cascode transistor. Thus the common programming line voltage is held approximately a
5 threshold voltage different to the applied bias voltage, more particularly less than (in case of n-type TFT pixel circuits) or greater than (in case of p-type pixel circuits) the applied bias voltage.

10 In some preferred embodiments the transistors are thin film transistors (TFTs), in particular n-type TFTs fabricated on the display panel. The techniques we describe are particularly useful for such transistors, which are fabricated from amorphous silicon, in part because of the relatively high parasitic capacitance with such devices.

15 The techniques we describe are particularly useful for so-called top emitting OLED structures. These structures emit through the top of the OLED structure rather than through the panel substrate and, in general, have a transparent cathode. Use of such a structure facilitates arranging the pixel drive circuits and associated cascode transistors under the OLED structures, providing greater design freedom. However the circuits we describe may also be employed with bottom-emitting devices.

20 In embodiments a display panel comprises a plurality of sets of pixel drive circuits each with a respective distributed cascode transistor. A set of pixel drive circuits may comprise, for example, between 10 and 100 pixel drive circuits. Arranging the row or column pixel drive circuits into sets in this way mitigates effects of capacitance of the
25 common current programming line – with a single set of pixel drive circuits for an entire row or column one would, to a degree, reproduce the original problem. As a rule of thumb, the pixel drive circuits may be arranged into a number of sets determined by the square root of the number of rows or columns of the display, for example of order 30 for a 1000 line display.

30 In embodiments a pixel drive circuit comprises a current copying pixel drive circuit in which, when the pixel select line is active, a current on the current programming input is copied to provide a corresponding output current to drive an OLED pixel. In one embodiment of a pixel drive circuit the circuit comprises an OLED drive transistor with a
35 capacitor connected to its gate to store a gate voltage defining the programmed OLED drive current. A select transistor is provided connected in series between this gate

connection and the distributed cascode transistor, more particularly the transistor of the set of transistors comprising the distributed cascode transistor which is physically part of the pixel drive circuit. In this way the connection between the transistor of the distributed cascode transistor and the pixel drive transistor, in embodiments, carries the same programming current as the common programming line and has a corresponding voltage change during programming. (However the physical length of this connection is short (smaller number of transistors drain-connected) and thus has a low capacitance. By contrast the common programming line has a larger capacitance, because it is relatively long (and many transistors connected to it contribute with overlap capacitances), and also carries the same programming current, but it has a reduced voltage swing.

The skilled person will appreciate that, in embodiments, more than one select transistor may be employed depending upon the detailed implementation of the current copying pixel drive circuit.

In a related approach the pixel drive circuit may comprise a current mirror circuit. Then, in embodiments, the parallel-connected control (gate) connections of the transistors comprising the distributed cascode transistor are connected to the parallel-connected input or output (drain or source) connections, so that the distributed cascode transistor is diode connected. This multi-element transistor may then be used as an input transistor for the current mirror, more particularly as a shared or distributed common input transistor for each current mirror of each respective pixel drive circuit. In this way the pixel drive circuits may, in embodiments, each comprise a current mirror in which the output stage comprises the OLED drive transistor and in which the input stage/transistor is shared and is provided by the distributed 'cascode' transistor (in this arrangement acting as a diode-connected current mirror input transistor).

Thus in a related aspect the invention provides an active matrix OLED display panel, the panel comprising a plurality of OLED pixels each having an associated pixel drive circuit, wherein a said pixel drive circuit comprises: a current mirror having a diode-connected input transistor; a current output transistor, wherein said current output transistor is a pixel drive transistor to drive an OLED with a mirror output current; a capacitor coupled to a gate connection of said pixel drive transistor to store a gate voltage for said pixel drive transistor to program said output current; and a select transistor connected in series between said current mirror input transistor and said

pixel drive transistor; and wherein said diode-connected input transistor comprises a distributed transistor shared between a set of said pixel driver circuits, said distributed transistor comprising a separate physical diode-connected transistor in each of said pixel drive circuits of said set, wherein said separate physically diode connected transistors of said set have their respective input, output and control connections connected in parallel, and wherein each said diode-connected transistor has one of said input and output connections connected to the respective control connection of the transistor and to said select transistor.

10 In embodiments of this arrangement a common, second select transistor is provided connected between the common current programming line for the set of pixel drive circuits and a row or column current programming data line for a plurality of such sets of pixel drive circuits. As before the distributed transistor comprises a set of physically separate transistors, one in each respective pixel drive circuit, connected together in
15 parallel to provide the distributed, diode-connected transistor functionality. Again, preferably each row or column is divided into a plurality of sets of such pixel drive circuits each with a respective distributed transistor. The number of parallel-connected transistors comprising the distributed transistor may, similarly, be between 10 and 100 (although useful advantages may also be provided, as before, with between 1 and 10
20 parallel-connected transistors).

In a further related aspect the invention provides a method of providing an active matrix OLED display panel, the panel comprising: a plurality of OLED pixels each having an associated current-programmed pixel drive circuit, said pixel drive circuit having a pixel
25 select line and a current programming input for programming an OLED pixel for the associated OLED pixel when said pixel select line is active, the method comprising: providing each of a set of said pixel drive circuits with a programming current for said current programming inputs via a respective input transistor; connecting at least input, output and control connections respectively, of said input transistors of said set of pixel
30 drive circuits, in parallel to provide an input transistor functionality which is electrically shared between said set of pixel drive circuits and physically distributed such that part of said functionality of said shared input transistor is physically located in conjunction with each said pixel drive circuit of said set; and providing a common current programming line for said set of pixel drive circuits, connected to said parallel-
35 connected input connections of said input transistors.

In embodiments of the method the pixel programming time of a pixel drive circuit is reduced by biasing the input transistors such that they operate as cascode transistors. Each input transistor is located adjacent, or associated with, a respective pixel drive circuit, so that they provide an electrically shared but physically distributed cascode transistor functionality. Then a programming current for the programming line input of a pixel drive circuit may be provided from the common current programming line via this shared, distributed cascode transistor, to thereby reduce programming time.

In other arrangements the input transistors are diode-connected and used as a shared but distributed input transistor for a set of pixel drive circuits each comprising a (portion of a) current mirror circuit. Then a select transistor may be provided between the common current programming line and a current data line of the OLED display panel.

In a further aspect the invention provides an active matrix OLED display panel comprising: a plurality of OLED pixels each having an associated current-programmed pixel drive circuit, said pixel drive circuit having a pixel select line and a current programming input for programming an OLED pixel for the associated OLED pixel when said pixel select line is active; an input transistor for providing a programming current to said current programming input of each of set of said pixel drive circuits; wherein at least said input connections, said output connections and said control connections of said input transistors are respectively connected in parallel with one another to provide an input transistor functionality which is electrically shared between said set of pixel drive circuits and physically distributed such that part of said functionality of said shared input transistor is physically located in conjunction with each said pixel drive circuit of said set; said display panel further comprising: a common current programming line for said set of pixel drive circuits connected to said parallel-connect input connections of said input transistors.

In embodiments of the above described display panels and methods, a current driver circuit (source or sink) for a data line or common current programming line of the display may comprise a single (FET) transistor connected at the end of a line, and provided with a current-programming control voltage.

BRIEF DESCRIPTION OF THE DRAWINGS

The invention will now be described, by way of example only, with reference to the accompanying figures in which:

5 Figures 1a and 1b show, respectively, an example of a current-programmed OLED pixel drive circuit, and an example of a current-programmed pixel drive circuit with an added cascode transistor;

10 Figure 2 shows an example of a set of current-programmed pixel drive circuits with a shared, distributed cascode transistor according to an embodiment of a first aspect of the invention;

Figure 3 shows a set of current-programmed pixel drive circuits with a shared, distributed current mirror input transistor according to an embodiment of a second aspect of the invention; and

15 Figure 4 shows an example of an OLED display incorporating an OLED display panel according to an embodiment of the invention.

DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS

20 Two requirements for OLED displays are related to:

- a. Programming/settling time – the need to programme the luminance within the allocated programming time, which reduces with the increase of resolution. If programming of the luminance is not completed within the allocated time this can cause either a loss of greyscale information or contrast or both.
- 25 b. Aging (V_t shift) – the desire to compensate for shifts in V_t (and μ). If not successful, this can reduce the luminance and/or cause image sticking.

The main schemes for programming the pixel circuits can be divided into voltage programming (VP) and current programming (CP). The voltage programming schemes provide fast programming times and it are therefore suitable for higher resolution
30 displays. However such techniques need additional functionality to compensate for OLED aging (which changes the luminance ~ voltage characteristic) and voltage drop on a power supply line.

A current programming scheme automatically compensates for aging (the luminance is proportional to the charge flowing through the OLED structure). However a current programming scheme has problems with the programming of small luminance levels within the allocated programming time and it is therefore difficult to support higher resolution displays.

We will describe techniques which extend the applicability of current programming schemes, which intrinsically cope with the aging issues, to high resolution displays. In embodiments the techniques include a pixel circuit modification which reduces the required programming time, enabling a faster programming than a standard current programming scheme.

Referring first to Figure 1a (which is taken from our earlier patent application WO03/038790), this shows one example of a "current copying" current-programmed pixel driver circuit 100. In this circuit the current through an OLED 152 is programmed by setting a drain source current for OLED driver transistor 158 using current generator 102, for example a reference current sink, and copying/memorising the driver transistor gate voltage required for this drain-source current. Thus the brightness of OLED 152 is determined by the current, I_{DAT} , flowing into reference current sink 102, which may be adjustable and set as desired for the pixel being addressed. A switching transistor 114 is connected between drive transistor 158 and OLED 152 to inhibit OLED illumination during the programming phase. In general one current sink 102 is provided for each column data line. To copy the programming current, switch transistor 110 is "closed" and switch transistor 114 is "opened" so that the programming current flows through drive transistor 158, and switch transistor 112 is also closed to set V_g on drive transistor 158 for the programmed current and to store this V_g value on capacitor 120.

Broadly speaking, we will describe cascode based current programming schemes for driving OLED displays. More particularly, in embodiments of the techniques we describe a cascode thin film transistor (TFT) device is shared among pixels inside a block of pixel circuits in a column to: (a) alleviate the effect of the data line capacitance on a pixel programming time and provide a room for faster programming of pixels using current programming methods as well as (b) to accommodate compensation of larger V_t shift values with the current programming schemes (with the set pre-charge scheme). In this way the techniques we describe reduce the impedance of a dataline

(and hence the voltage swing on the line), and thus reduce the panel loading effect in a current programmed scheme.

Referring now to Figure 1b, in which like elements to those of Figure 1a are indicated by like reference numerals, this shows a current-programmed pixel drive circuit 150 including a cascode TFT device 156, operating in a common gate mode. The pixel drive circuit is a current-programmed circuit copying a current I_{pgm} on a current-programming line for driving the same current, I_{OLED} , through OLED 152. The programming current is copied when the select line SEL is activated to control a pair of select/switch TFT transistors 152, 154. A cascode transistor 156 is connected in series between a current-programming line 160 of the circuit and a current dataline 162 for the display panel. The gate of cascode TFT 156 is connected to a bias voltage line 158 connected to a bias voltage generator (now shown in Figure 1b) to bias transistor 156 into a linear region of operation. The cascode transistor 156 reduces variations in voltage on the current data line 162 when the (programming) current on this line changes. This facilitates using a relatively simple constant current generator, for example comprising a single transistor 104 with an appropriate input voltage, as illustrated in Figure 1b.

Figure 2 shows a portion of an active matrix OLED display panel 200 comprising a set of current-programmed pixel drive circuits 180 each, for example, as illustrated by the dashed line 180 of Figure 1b. Each pixel drive circuit 180 and associated select transistor 154 is physically located adjacent a respective OLED pixel, and in the arrangement of Figure 2, a respective cascode transistor 202a-d is also provided in the pixel drive circuit physically adjacent each OLED pixel. However the drain connections of the cascode devices 202a-d are all connected together, to node B and line 160 in the illustrated example; the source connections of transistors 202a-d are also all connected together, to node A and common current-programming line 204; and the gate connections of the cascode transistors are also all connected together in parallel, to a common cascode bias voltage line 206.

In this way although each of cascode transistors 202a-d is fabricated as a separate physical device, the transistors are connected in parallel to provide a distributed cascode transistor functionality with, in effect, a wider channel for a block of m -pixels, a channel of m times the effective width. The true situation is slightly complicated by the different input capacitances of the cascode transistors because of the different lengths

of line connecting them to the common programming line 204, but to a first approximation this can be disregarded. Thus, broadly speaking, transistors 202a-d can be regarded as constituting a distributed cascode transistor shared between the set of pixels.

5

The arrangement of Figure 2 shows one set of OLED pixels, but in a display panel the pixels are preferably grouped together, for example in groups of around 10 to 30, each sharing a distributed cascode transistor 202 and having a respective common current programming line 204. Optionally each common cascode bias voltage line 206 may be used as a further select line for a set of pixels. Providing a distributed cascode transistor in this way facilitates patterning and fabrication of a display panel whilst also providing a large cascode device, which is desirable for good performance (a reduced voltage swing on line 204).

15

Thus, in embodiments, a block of m pixels in a column share, effectively, one large cascode TFT device comprising m smaller TFT's (common gate devices), each in a respective current-programmed pixel circuit, and these are connected in parallel. The distributed cascode connected device 202 reduces the impedance at node A, thus reducing the voltage swing on data line 204. The cascode device should be large in order to provide the desired functionality improvement, and by constructing this using a plurality (m) of smaller devices in parallel this can be provided in a manner which facilitates layout and patterning of the panel. Furthermore susceptibility to failures due to process issues is reduced because each individual TFT cascode device has a smaller area.

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Continuing to refer to Figure 2, node B represents a high impedance point but by comparison with a current programmed arrangement of the type shown in Figure 1a its capacitance is reduced by a factor of: $2 \times \text{number of blocks [sets of pixel drive circuits]}$ in a column (or row) of the display panel.

30

Consider, for example, a panel with $N_r=1000$ rows in which $m=40$ rows (pixels in a column) are connected together in each block to share a distributed cascade transistor as we have described. With this example we have $N_b=25$ blocks and thus the reduction in a capacitive loading will be $N_r/N_b/2 = 40/2 = m/2 = 20$ times. (We presume that the cascode device and switch TFTs in a block have similar gate-drain

35

and gate source capacitance). This is the factor by which the programming time is reduced for the same programming current.

It can therefore be appreciated that the techniques we describe facilitate programming of higher resolution displays. The techniques we describe also facilitate achieving a higher dynamic range. To appreciate this latter point, consider that for the ITU Rec709 standard (used for high definition television) the gamma function results in a dynamic range of 1000:1 between the maximum grey level and the minimum non-zero grey level, and for the sRGB standard the dynamic range is approximately 200,000:1. Where the programming current is changed to control the current driven to the OLED this creates a particular problem in driving long lines (with large capacitance) using an imperfect constant current generator when the programming current is very small (the minimum grey-level current is typically less than 10nA for Rec709, and potentially less than 50 pA for sRGB). Thus controlling (reducing) the voltage swing on the current programming line is particularly important when the OLED/pixel is driven with a controllable current of less than 10 nA or less than 1 nA. The techniques we describe facilitate accurate driving with such low currents.

The fabrication of OLED display panels can entail (cathode related) processing issues with OLEDs and the techniques we describe are particularly suitable for n-type TFT technology and n-type TFT pixel circuits.

Referring now to Figure 3, this shows a portion of an active matrix OLED display panel configured to implement a variation of the above described techniques in which the shared, distributed TFT device is configured as a shared input transistor of a distributed current mirror. In this arrangement each respective pixel drive circuit of the set comprises, effectively, a separate output stage for the shared current mirror, each driving a respective OLED pixel. Again like elements to those previously described are indicated by like reference numerals.

Thus, referring to Figure 3, each of the pixel drive circuits comprises a thin film transistor 302a,b-n, and each of these transistors is diode-connected (the gate is connected to the drain). Further, gate, drain and source connections of these transistors are all respectively connected in parallel to provide a distributed, diode-connected transistor. Each of transistors 302a,b-n forms the input of a current mirror having a common current-programming line 304, the current mirror having a set of

outputs each comprising a respective driver transistor 158. In this way the current I_{PGM} on line 304 is mirrored to current I_{OLED} driving the respective OLED pixels.

The skilled person will appreciate that the ratio of each current mirror may be substantially 1:1 or, by choosing different size ratios for the transistors 302, 158, different to 1:1. Thus, for example the current mirrors may be configured to provide an output current which is a fraction of the input current, for example an N/M fraction where N and M are integers (and N/M is less than unity), to facilitate accurate programming of small OLED drive currents.

As illustrated, each pixel drive circuit is also provided with a select transistor 306 for programming the voltage on capacitor 120 to maintain the mirrored OLED drive current. In embodiments a further select transistor 308 is provided to selectively connect the common current programming line 304 for the set of pixels to a (column) current data line 310 of the display panel. Data line 310 may be programmed by a controllable constant current generator 102 as illustrated.

The skilled person will appreciate that in one implementation of the type of arrangement shown in Figure 3, the cascode transistors of Figure 2 are diode-connected and used in conjunction with mirror-based pixel drive circuits. Thus, effectively, the arrangements of Figures 2 and 3 may be combined.

Figure 4 shows an OLED display system 400 comprising an OLED display 450 incorporating a display panel comprising sets of pixel drive circuits as described with reference to Figures 2 and/or 3. A controller 410 accepts RGB (red, green, blue) input data on line 402 and provides current programming data for the pixel drive circuits on lines 404 and pixel drive circuit select data on column select lines 406. As illustrated the OLED display 450 includes one or more bias voltage generator circuits 452 for biasing the cascode transistors; alternatively these may be part of the controller 410.

For the avoidance of doubt, references to pixels in this specification may refer to a pixel that is only a single colour, or to a pixel which comprises a plurality of individually addressable sub-pixels that together enable the pixel to emit a range of colours to provide a colour display.

We have thus described, in general terms, techniques using blocks of transistors connected in parallel and, more specifically, connecting cascode transistor devices in this way. The addition of a (distributed) cascode TFT (with a common gate TFT connection) facilitates faster programming of the pixel circuits using a current programming scheme, in particular due to the reduced voltage swing at a current programming dataline (that is, reduced impedance). This in turn facilitates the fabrication of higher resolution displays using current programming schemes, and also facilitates faster programming of lower currents, which allows an increase in the programmable dynamic range and therefore the number of greyscale levels.

Optionally an arrangement of the type we describe may be combined with a preset pre-charge scheme in which a current programming line is pre-charged to a defined voltage value, preferably a transistor (TFT) threshold voltage. Such a pre-charge arrangement can also help to reduce the change in voltage needed on the current-programming line when programming a current for an OLED pixel. However, one difficulty with pre-charging is that the threshold voltage of a TFT transistor can change with time (because of charge trapping at the dielectric interface), this effectively adding a gate voltage offset. The techniques we describe facilitate more effective use of a pre-charge scheme because they effectively enable compensation of a shift in transistor threshold voltage (for example, by changing the bias voltage applied to the cascode transistors), and are thus potentially able to accommodate relatively large shifts in threshold voltage.

No doubt many other effective alternatives will occur to the skilled person. It will be understood that the invention is not limited to the described embodiments and encompasses modifications apparent to those skilled in the art lying within the scope of the claims appended hereto.

CLAIMS

1. An active matrix OLED display panel, the panel comprising:
a plurality of OLED pixels each having an associated current-programmed pixel
5 drive circuit, said pixel drive circuit having a pixel select line and a current programming
input for programming an OLED pixel for the associated OLED pixel when said pixel
select line is active; and
wherein said OLED display panel further comprises at least one distributed
cascode transistor shared between a set of said pixel drive circuits, wherein said
10 distributed cascode transistor comprises a set of transistors each having an input
connection, an output connection and a control connection, wherein each of said
transistors of said set is in physical proximity to a respective one of said set of said
pixel drive circuits and has said output connection connected to said current
programming input of said respective one of said pixel drive circuits, wherein said input
15 connections of said transistors of said set are connected together in parallel, said
output connections of said transistors of said set are connected together in parallel,
and said control connections of said transistors of said set are connected together in
parallel, and wherein said parallel-connected input connections of said transistors of
said set are connected to a common current programming line for said set of said pixel
20 drive circuits.
2. An active matrix OLED display panel as claimed 1 wherein said set of pixel
drive circuits has an associated pixel block bias line, and wherein said parallel
connected control connections of said transistors of said set are connected to said pixel
25 block bias line.
3. An active matrix OLED display panel as claimed in claim 2 further comprising
at least one bias circuit connected to said pixel block bias line, wherein said bias circuit
is configured to bias said distributed cascode transistor such that a nominally constant
30 voltage is maintained on the common current programming data line when current is
being programmed.
4. An active matrix OLED display panel as claimed in claim 1, 2 or 3 wherein each
row or column of said display panel comprises a plurality of said sets of pixel drive
35 circuits each with a respective said distributed cascode transistor.

5. An active matrix OLED display panel as claimed in claim 4 wherein a said set of pixel drive circuits comprises between 10 and 100 said pixel drive circuits.

5 6. An active matrix OLED display panel as claimed in any preceding claim wherein said transistors are n-type thin film transistors.

7. An active matrix OLED display panel as claimed in any preceding claim wherein said OLED pixels comprise top-emitting OLED structures having a transparent cathode, and wherein at least a portion of one or both of a said pixel drive circuit and said distributed cascode transistor is under a said OLED structure between a said OLED structure and a substrate of said display panel.

10

8. An active matrix OLED display panel as claimed in any one of claims 1 to 7 wherein said pixel drive circuit comprises a current copying pixel drive circuit in which, when said pixel select line is active, a current on said current programming input is copied to provide a corresponding output current to drive a said OLED pixel.

15

9. An active matrix OLED display panel as claimed in claim 8 wherein a said pixel drive circuit comprises an OLED drive transistor, a capacitor coupled to a gate connection of said pixel drive transistor to store a gate voltage for said pixel drive transistor to program said output current, and at least one select transistor having a gate connector coupled to said pixel select line and having drain and source connections connected in series between an output connection of one of said set of transistors of said distributed cascode transistor and said gate connection of said pixel drive transistor.

20

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10. An active matrix OLED display panel as claimed in any one claims 1 to 8 wherein a said pixel drive circuit comprises a current mirror circuit, wherein said parallel-connected control connections of said transistors of said set are connected to one of said parallel-connected input and output connections of said transistors of said set such that said distributed cascode transistor is diode-connected, and wherein distributed cascode transistor is a common input transistor for each said current mirror circuit of each said pixel driver circuit of said set of said pixel drive circuits.

30

11. An active matrix OLED display panel, the panel comprising a plurality of OLED pixels each having an associated pixel drive circuit, wherein a said pixel drive circuit comprises: a current mirror having a diode-connected input transistor; a current output transistor, wherein said current output transistor is a pixel drive transistor to drive an
5 OLED with a mirror output current; a capacitor coupled to a gate connection of said pixel drive transistor to store a gate voltage for said pixel drive transistor to program said output current; and a select transistor connected in series between said current mirror input transistor and said pixel drive transistor; and wherein said diode-connected input transistor comprises a distributed transistor shared between a set of said pixel
10 driver circuits, said distributed transistor comprising a separate physical diode-connected transistor in each of said pixel drive circuits of said set, wherein said separate physically diode connected transistors of said set have their respective input, output and control connections connected in parallel, and wherein each said diode-connected transistor has one of said input and output connections connected to the
15 respective control connection of the transistor and to said select transistor.

12. An active matrix OLED display panel as claimed in claim 11 further comprising a common, second select transistor common to said set of pixel drive circuits, and wherein the other of said input and output parallel-connected connections of each said
20 diode-connected transistor of said distributed transistor is connected to an input/output connection of said common select transistor.

13. *An active matrix OLED matrix display panel as claimed in claim 11 or 12 wherein each row or column of said display panel comprises a plurality of said sets of*
25 *pixel drive circuits each with a respective said distributed transistor.*

14. A method of providing an active matrix OLED display panel, the panel comprising:
a plurality of OLED pixels each having an associated current-programmed pixel
30 drive circuit, said pixel drive circuit having a pixel select line and a current programming input for programming an OLED pixel for the associated OLED pixel when said pixel select line is active, the method comprising:
providing each of a set of said pixel drive circuits with a programming current for
said current programming inputs via a respective input transistor;
35 connecting at least input, output and control connections respectively, of said input transistors of said set of pixel drive circuits, in parallel to provide an input

transistor functionality which is electrically shared between said set of pixel drive circuits and physically distributed such that part of said functionality of said shared input transistor is physically located in conjunction with each said pixel drive circuit of said set; and

- 5 providing a common current programming line for said set of pixel drive circuits, connected to said parallel-connected input connections of said input transistors.

15. A method as claimed in claim 14 for reducing the pixel programming time of a said pixel drive circuit, wherein said input transistors comprise cascode transistors
10 providing an electrically shared and physically distributed cascode transistor functionality, the method comprising providing a programming current for a said current programming input of a said pixel drive circuit from said common current programming line via said electronically shared and physically distributed cascode transistor functionality, such that when driving said common current programming line with a
15 variable current a voltage swing on said common current programming line is reduced to reduce said pixel programming time of a said pixel drive circuit.

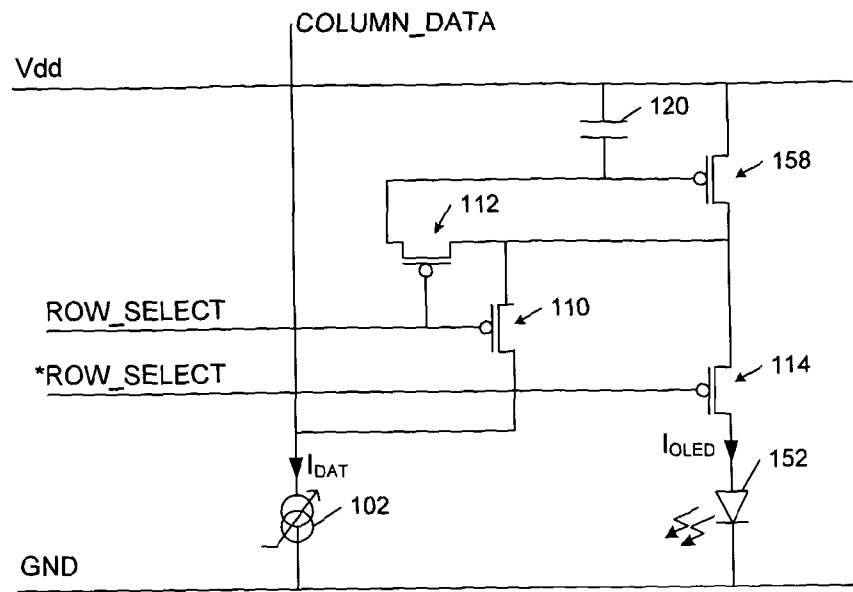
16. A method as claimed in claim 14 or 15 wherein said pixel drive circuits comprise current mirror circuits and wherein said input transistors comprise diode-connected
20 current mirror input transistors, the method further comprising connecting said parallel-connected control connections to said parallel-connected input connections of said input transistors, and providing a select transistor between said common current programming line and a current data line of said OLED display panel.

25 17. An active matrix OLED display panel comprising:
 a plurality of OLED pixels each having an associated current-programmed pixel drive circuit, said pixel drive circuit having a pixel select line and a current programming input for programming an OLED pixel for the associated OLED pixel when said pixel select line is active;

30 an input transistor for providing a programming current to said current programming input of each of set of said pixel drive circuits; wherein
 at least said input connections, said output connections and said control connections of said input transistors are respectively connected in parallel with one another to provide an input transistor functionality which is electrically shared between
35 said set of pixel drive circuits and physically distributed such that part of said

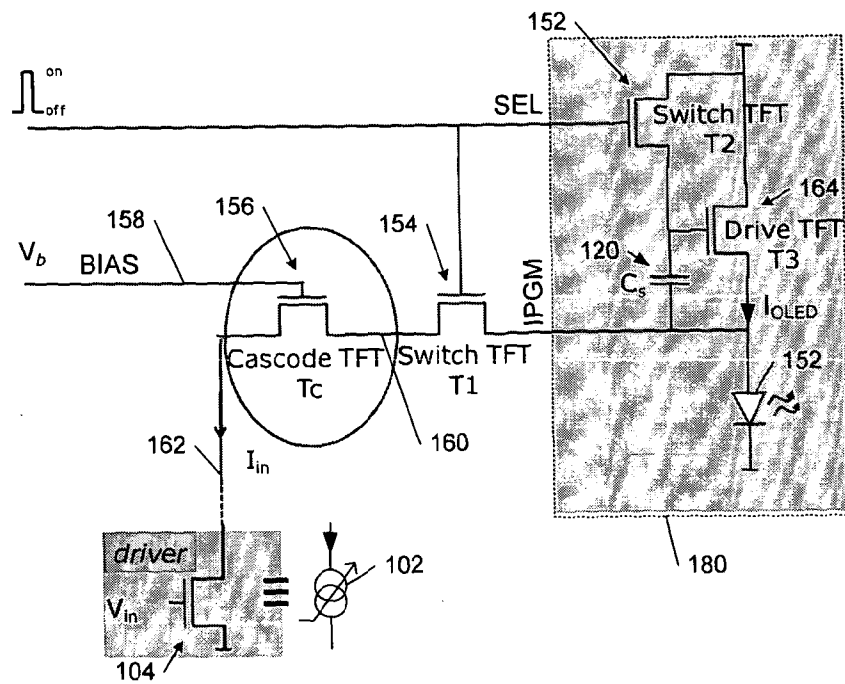
functionality of said shared input transistor is physically located in conjunction with each said pixel drive circuit of said set; said display panel further comprising:
a common current programming line for said set of pixel drive circuits connected to said parallel-connect input connections of said input transistors.

1/4



100 ↗

Figure 1a



150 ↗

Figure 1b

2/4

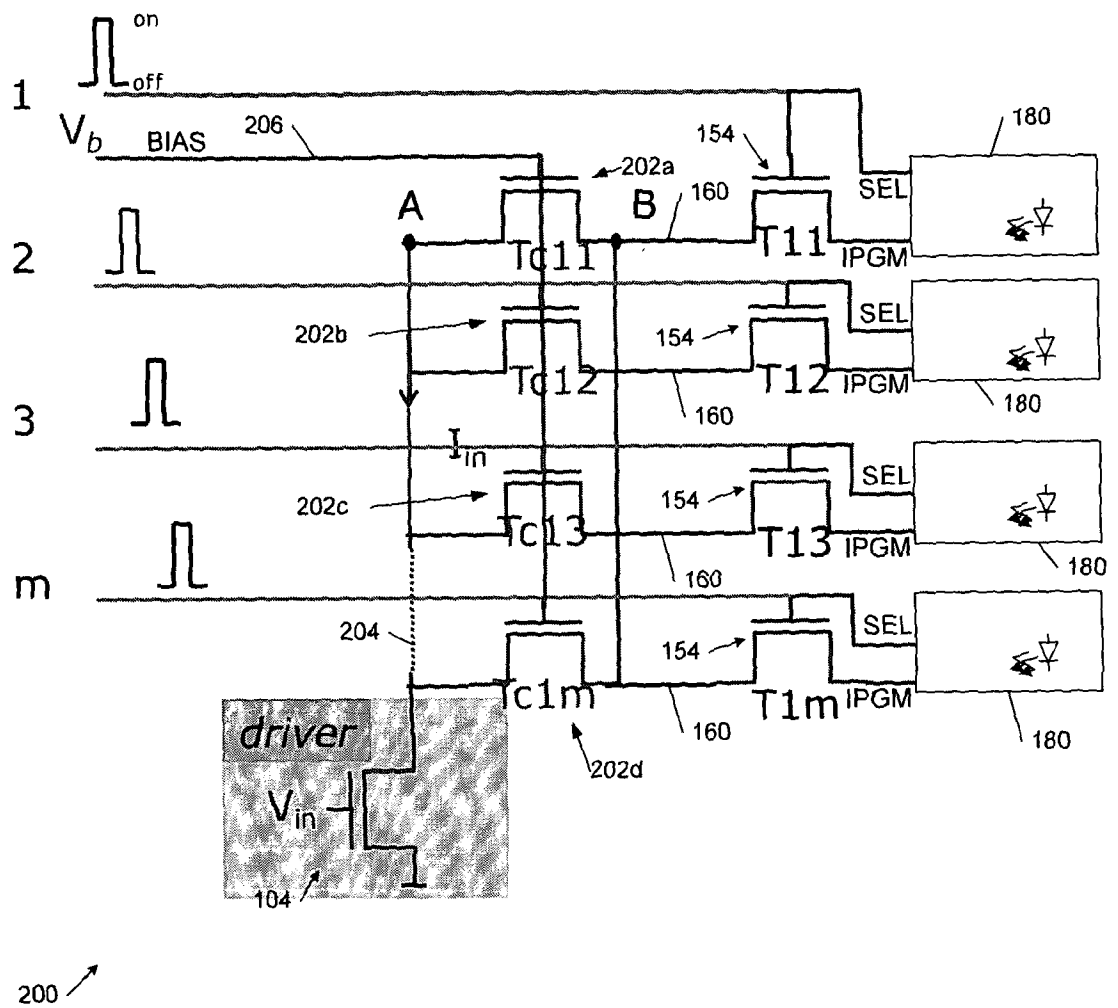


Figure 2

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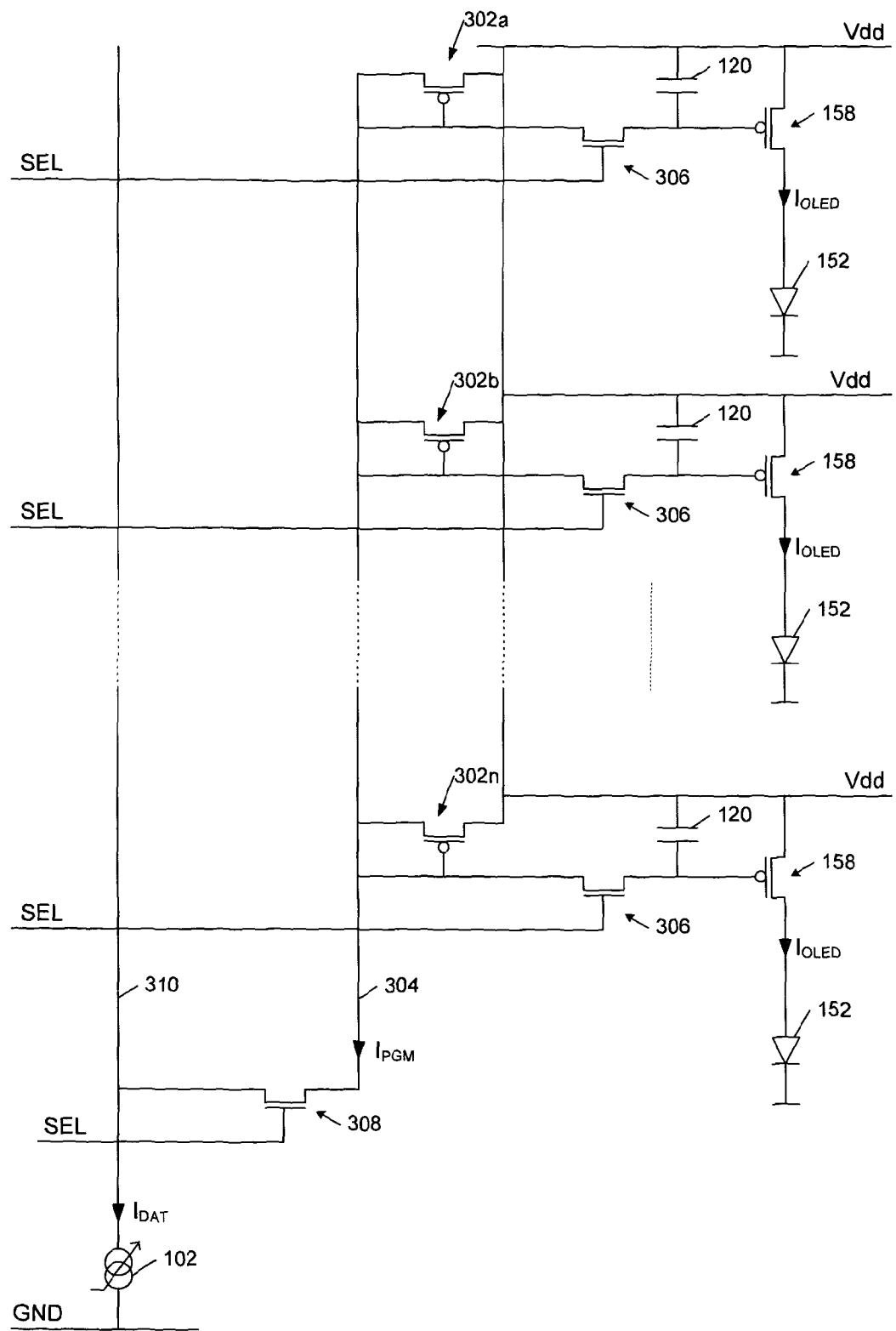


Figure 3

300 ↗

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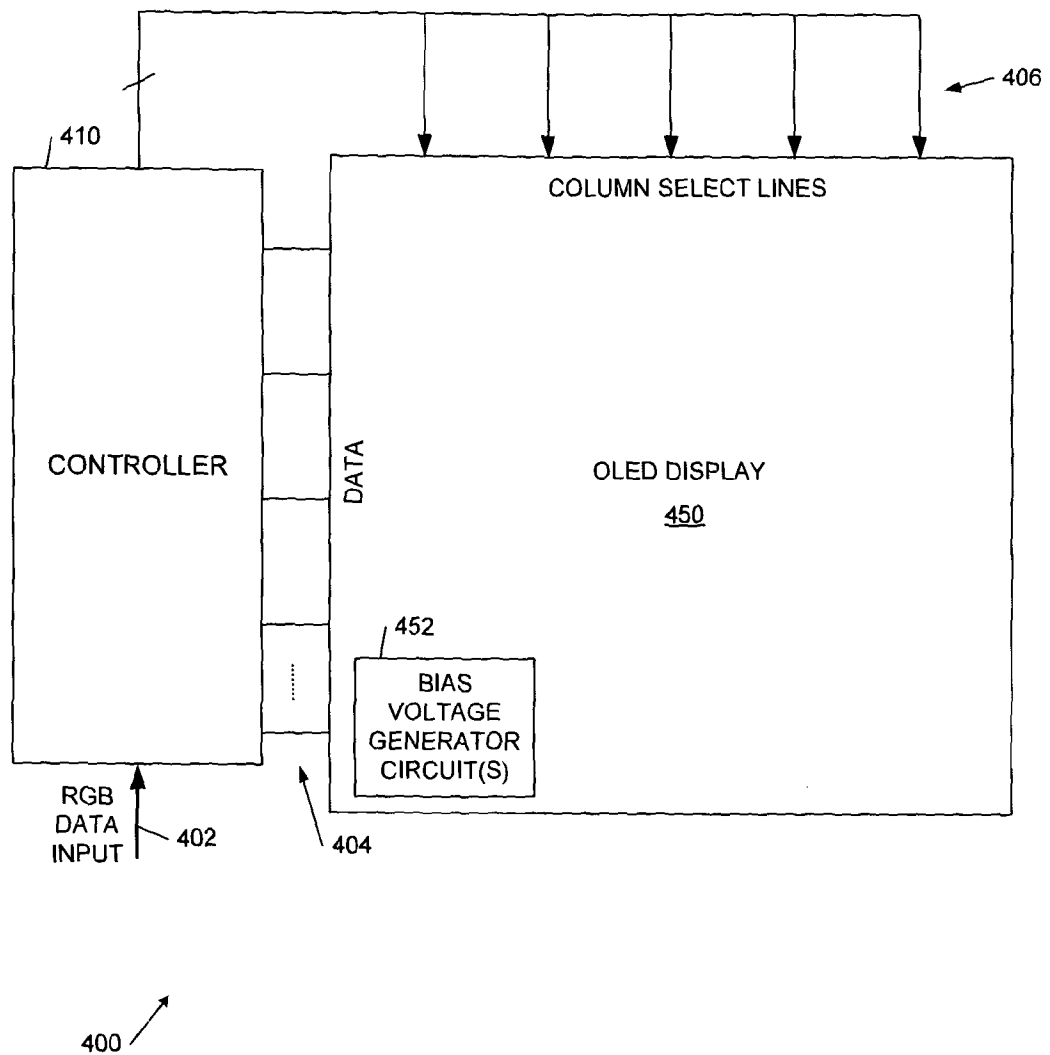


Figure 4