(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
30 April 2009 (30.04.2009)

PCT

(10) International Publication Number
WO 2009/055181 A1

(51) International Patent Classification:
B82B 3/00 (2006.01)

(21) International Application Number:
PCT/US2008/077419

(22) International Filing Date:
24 September 2008 (24.09.2008)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
11/877,016 23 October 2007 (23.10.2007) US

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(81) Designated States *(unless otherwise indicated, for every kind of national protection available)*: AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BR, BW, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IS, JP, KE, KG, KM, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LT, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PG, PH, PL, PT, RO, RS, RU, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(84) Designated States *(unless otherwise indicated, for every kind of regional protection available)*: ARIPO (BW, GH, GM, KE, LS, MW, MZ, NA, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MT, NL, NO, PL, PT, RO, SE, SI, SK, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Declarations under Rule 4.17:
— *as to applicant's entitlement to apply for and be granted a patent (Rule 4.17(ii))*
— *as to the applicant's entitlement to claim the priority of the earlier application (Rule 4.17(iii))*

Published:
— *with international search report*

(54) Title: CONTROLLED DOPING OF SEMICONDUCTOR NANOWIRES

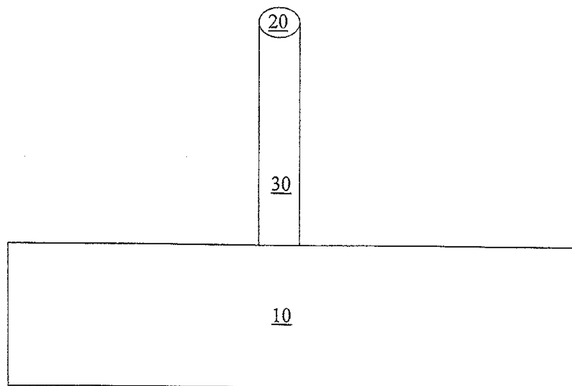

FIG. 1 (Prior Art)

(57) Abstract: A catalyst particle on a substrate is exposed to reactants containing a semiconductor material in a reactor. An intrinsic semiconductor nanowire having constant lateral dimensions is grown at a low enough temperature so that pyrolysis of the reactant is suppressed on the sidewalls of the intrinsic semiconductor nanowire. Once the intrinsic semiconductor nanowire grows to a desired length, the temperature of the reactor is raised to enable pyrolysis on the sidewalls of the semiconductor nanowire, and thereafter dopants are supplied into the reactor with the reactant. A composite semiconductor nanowire having an intrinsic inner semiconductor nanowire and a doped semiconductor shell is formed. The catalyst particle is removed, followed by an anneal that distributes the dopants uniformly within the volume of the composite semiconductor nanowire, forming a semiconductor nanowire having constant lateral dimensions and a substantially uniform doping.

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CONTROLLED DOPING OF SEMICONDUCTOR NANOWIRES

Field of the Invention

[0001] The present invention relates to semiconductor structures, and particularly to doped semiconductor nanowires and methods of manufacturing the same.

Background of the Invention

[0002] A nanowire refers to a wire having a diameter from about 1 nm to about 1,000 nm. Implied in the use of the term “nanowire” is the assumption that the length of the nanowire is substantially greater than the diameter of the nanowire. Nanowires having a diameter at a low end of the range, i.e., a diameter from about 1 nm to about 100 nm, exhibit quantum mechanical properties, and are also called "quantum wires." A nanowire may comprise a metallic material, a semiconductor material, or an insulator material. Both organic nanowires, e.g., deoxyribonucleic acid (DNA), and inorganic nanowires are known in the art.

[0003] The ratio of the length of a nanowire to the diameter of the nanowire is referred to as an aspect ratio. Typical aspect ratios for nanowires range from about 10 to about 1,000,000. As such, one dimension, i.e., the length, of a nanowire may be considered to be virtually infinite for practical purposes, while the diameter of the nanowire determines predominant physical and chemical characteristics of the nanowire. Quantum mechanical properties of nanowires due to the limited dimension of the nanowire in the plane perpendicular to the length of the nanowire have been observed in many types of nanowires.

[0004] Devices employing semiconductor nanowires have been proposed in the art. One of the challenges in the manufacture of the semiconductor devices employing semiconductor nanowires has been the difficulty in forming doped semiconductor nanowires. Particularly, controlled doping of semiconductor nanowires comprising silicon or germanium presents a significant challenge.

[0005] Prior art publications propose doping of semiconductor nanowires by a dopant gas such as phosphene, diborane, etc. with a reactant gas such as silane or germane during the growth of the nanowire. One such example is U.S. Patent No. 6,962,823 to Empedocles et al., which describes in-situ doping of isolated bands in a semiconductor nanowire by changing of dopant level during growth of the semiconductor nanowire. Application of this approach to form a silicon nanowire or a geranium nanowire faces severe problems that hamper its usefulness. In particular, a relatively low temperature range from about 350 °C to about 450 °C is required to grow certain types of semiconductor nanowires, such as silicon nanowires and germanium nanowires, with diameters less than 30 nm. At an elevated temperature above 500 °C, such semiconductor nanowires grow laterally.

[0006] Unfortunately, a relatively high temperature above 500 °C is required to successfully incorporate dopant atoms at a significant level, i.e., at a concentration of about $1.0 \times 10^{17}/cm^3$ or above, into the semiconductor nanowire during growth. However, at such a temperature, the semiconductor nanowire also grows laterally since the elevated temperature enables pyrolysis of reactants on the exposed surfaces of the semiconductor nanowire. Suppression of pyrolysis of reactants on sidewall surfaces of semiconductor nanowires and doping of the sidewall surfaces of the semiconductor wires are mutually incompatible in many semiconductor nanowires. In other words, doping of the sidewall surfaces of the semiconductor wires necessarily causes pyrolysis of reactants on the sidewall surfaces the semiconductor nanowires.

[0007] This situation is illustrated in FIGS. 1 and 2. In FIG. 1, a catalyst particle 20, such as a gold particle, is placed on a substrate 10, which may comprise an insulator material or a semiconductor material. In a temperature range from about 350 °C to about 450 °C, a semiconductor nanowire 30 is grown as reactants containing a semiconductor material, e.g., SiH_4, Si_2H_6, GeH_4, etc., are supplied into a reactor, such as a low pressure chemical vapor deposition (LPCVD) chamber or an ultra-high vacuum chemical vapor deposition (UHVCVD) chamber. The catalyst particle 20 forms a thin moving eutectic region (not shown) at the interface between the catalyst particle 20 and the top region of the

semiconductor nanowire 30, and travels at the top of the semiconductor nanowire throughout the growth process. The diameter, or the lateral dimensions, of the semiconductor nanowire 30 is substantially the same as the lateral dimensions of the catalyst particle 20. At this temperature range, dopant incorporation into the semiconductor nanowire 30 is negligible. Thus, even if a high partial pressure is maintained for dopant gases in a reactor, dopant incorporation into the semiconductor nanowire 30 is insignificant, and the semiconductor nanowire 30 remains essentially undoped.

[0008] Referring to FIG. 2, to force incorporation of dopants, the temperature of the reactor must be increased above 500 °C in the case of some semiconductor wires such as a silicon nanowire and a germanium wire. In this case, however, pyrolysis occurs on the sidewalls of a doped semiconductor nanowire 40. While dopants are incorporated into the doped semiconductor nanowire 40 during the growth, lateral growth of the doped semiconductor wire 40 is unavoidable. Further, a bottom portion of the doped semiconductor wire 40, being exposed to the reactants for a longer time, has a larger diameter than a top portion of the doped semiconductor wire 40, which is exposed to the reactants for a shorted period of time, and has lateral dimensions close to lateral dimensions of the catalyst particle 20. Thus, the doped semiconductor wire 40 has a taper in the diameter, i.e., a constant diameter for the doped semiconductor wire 40 cannot be achieved.

[0009] An alternate approach to forming doped semiconductor wires is to implant dopants into nanowires. However, ion implantation tends to be an inherently violent process due to the high energy of the implanted ions, and causes amorphization of the nanowire crystalline structure and sputtering of the nanowire itself. Thus, the ion implantation tends to cause wire deformation and/or wire breakage during the ion implantation process. Subsequent anneals are required to recrystallize the nanowire, which may not be wholly effective if the structural damage is extensive.

[0010] While prior art publications, such as U.S. Patent No. 7,105,428 to Pan et al., and U.S. Patent No. 7,211,464 to Lieber et al., disclose useful applications of doped semiconductor

nanowires, methods of forming such useful structures still need to be provided to enable such structures.

[0011] Thus, there exists a need for methods of forming a semiconductor wire having constant lateral dimensions and a significant level of doping, i.e., at a concentration of about $1.0 \times 10^{17}/cm^3$ or above.

[0012] Further, there exists a need for methods of forming a doped semiconductor wire having constant lateral dimensions, such as a diameter, of less than 30 nm.

[0013] In this disclosure we describe a simple method for controllably incorporating dopant atoms into semiconductor nanowires. This process separates the initial growth of the nanowire from the doping process, thereby allowing the growth of the nanowire to be decoupled from dopant incorporation into the nanowire crystalline structure.

Summary of the Invention

[0014] The present invention addresses the needs described above by providing a method for controllably incorporating dopant atoms into a semiconductor nanowire of constant lateral dimensions. This method separates the initial growth of the semiconductor nanowire from a subsequent doping process, thereby allowing the growth of the semiconductor nanowire to be decoupled from dopant incorporation into the semiconductor nanowire.

[0015] In the present invention, a catalyst particle is formed on a substrate, which is exposed to reactants containing a semiconductor material in a reactor. An intrinsic semiconductor nanowire having constant lateral dimensions is grown as the catalyst particle moves on top of the intrinsic semiconductor nanowire. The intrinsic semiconductor nanowire is grown at a low enough temperature so that pyrolysis of the reactant is suppressed on the sidewalls of the intrinsic semiconductor nanowire. Once the intrinsic semiconductor nanowire grows to a desired length, the temperature of the reactor is raised to enable pyrolysis on the sidewalls of the semiconductor nanowire, and thereafter dopants are supplied into the reactor with the

reactant. A composite semiconductor nanowire having an intrinsic inner semiconductor nanowire and a doped semiconductor shell is formed. The catalyst particle is removed, followed by an anneal that distributes the dopants uniformly within the volume of the composite semiconductor nanowire, forming a semiconductor nanowire having constant lateral dimensions and a substantially uniform doping.

[0016] According to an aspect of the present invention, a method of forming a semiconductor nanowire is provided, which comprises:

forming a catalyst particle on a substrate;

growing an undoped semiconductor nanowire between the catalyst particle and the substrate by subjecting the catalyst particle to a first reactant gas at a first temperature, wherein pyrolysis of the first reactant gas on sidewalls of the semiconductor nanowire is suppressed at the first temperature; and

growing a shell of a doped semiconductor material around sidewalls of the undoped semiconductor nanowire by subjecting the undoped semiconductor nanowire to a second reactant and a dopant at a second temperature, wherein the second reactant and the dopant is incorporated into the shell by pyrolysis.

[0017] In one embodiment, the undoped semiconductor nanowire comprises a group IV semiconductor material, a III-V compound semiconductor material, a II-VI compound semiconductor material, and an alloy thereof.

[0018] In another embodiment, the doped semiconductor material comprises a group IV semiconductor material, a III-V compound semiconductor material, a II-VI compound semiconductor material, and an alloy thereof.

[0019] In even another embodiment, the doped semiconductor material further comprises at least one of B, Ga, In, P, As, and Sb.

[0020] In yet another embodiment, the undoped semiconductor nanowire has a substantially constant cross-sectional area across an entire length of the undoped semiconductor nanowire.

Lateral dimensions of the undoped semiconductor nanowire may be from about 1 nm to about 1,000 nm, and further, may be less than 30 nm.

[0021] In still another embodiment, the shell has a substantially constant cross-sectional area across an entire length of the shell. The shell may have a thickness from about 0.3 nm to about 10 nm.

[0022] In a further embodiment, the shell has a doping concentration from about 1.0 x $10^{18}/cm^3$ to about $5.0x10^{21}/cm^3$.

[0023] In an even further embodiment, the catalyst particle has a lateral dimension from about 1 nm to about 1,000 nm. Further, the the lateral dimension of the catalyst particle may be less than 30 nm.

[0024] In a yet further embodiment, the catalyst particle comprises one of Au, Ag, Cu, Pt, Fe, Co, Ni, In, Ta, Ti, Zn, Cd, and Sn.

[0025] In a still further embodiment, the first reactant comprises at least one of SiH_4, Si_2H_6, SiH_2Cl_2, $SiHCl_3$, $SiCl_4$, GeH_4, Ge_2H_6, GeH_3Cl, GeH_2Cl_2, $GeHCl_3$, and $GeCl_4$.

[0026] In a still yet further embodiment, the first temperature is from about 350 °C to about 450 °C.

[0027] In further another embodiment, the second reactant comprises at least one of SiH_4, Si_2H_6, SiH_2Cl_2, $SiHCl_3$, $SiCl_4$, GeH_4, Ge_2H_6, GeH_3Cl, GeH_2Cl_2, $GeHCl_3$, and $GeCl_4$.

[0028] In even further another embodiment, the dopant comprises one of B_2H_6, GaH_3, $GaCl_3$, Ga_2Cl_6, PH_3, $POCl_3$, AsH_3, SbH_3, and SbF_3.

[0029] In yet further another embodiment, the second temperature is from about 500 °C to about 1,100 °C.

[0030] In still further another embodiment, the method further comprises annealing the undoped semiconductor nanowire and the shell at an elevated temperature from about 600 °C to about 1,200 °C, wherein the undoped semiconductor nanowire and the shell have a substantially uniform doping concentration after the anneal.

[0031] In still yet further another embodiment, the substantially uniform doping concentration is from about $1.0 \times 10^{17}/cm^3$ to about $5.0 \times 10^{20}/cm^3$.

[0032] In a further embodiment, the substantially uniform doping concentration is the product of a doping concentration of said shell and a ratio of a volume of said shell to a sum of volumes of said shell and said undoped semiconductor nanowire.

[0033] In still further embodiment, a doping concentration of said shell is set by a partial pressure of a dopant gas in a process chamber or a ratio between a partial pressure of said dopant gas to a partial pressure of a reactant.

[0034] The substantially uniform doping concentration may be changed either by adjusting a doping concentration of the shell, adjusting of thickness of the shell, or a combination of both.

[0035] According to another aspect of the present invention, a semiconductor nanowire formed by the methods described above is provided.

[0036] A semiconductor nanowire structure according to the present invention comprises:

an undoped semiconductor nanowire formed by subjecting the catalyst particle to a first reactant gas at a first temperature, wherein pyrolysis of the first reactant gas on sidewalls of the semiconductor nanowire is suppressed at the first temperature; and

a shell of a doped semiconductor material abutting and surrounding sidewalls of the undoped semiconductor nanowire and formed by subjecting the undoped semiconductor

nanowire to a second reactant and a dopant at a second temperature, wherein the second reactant and the dopant is incorporated into the shell by pyrolysis.

Brief Description of the Drawings

[0037] FIG. 1 is a vertical cross-sectional view of an exemplary prior art undoped semiconductor nanowire.

[0038] FIG. 2 is a vertical cross-sectional view of an exemplary prior art in-situ doped semiconductor nanowire.

[0039] FIG. 3A is a vertical cross-sectional view of an exemplary semiconductor nanowire according to the present invention after formation of an undoped semiconductor nanowire.

[0040] FIG. 3B is a horizontal cross-sectional view of the exemplary semiconductor nanowire in FIG. 3A along the plane X-X'.

[0041] FIG. 4A is a vertical cross-sectional view of an exemplary semiconductor nanowire according to the present invention after formation of a doped shell.

[0042] FIG. 4B is a horizontal cross-sectional view of the exemplary semiconductor nanowire in FIG. 4A along the plane X-X'.

[0043] FIG. 5A is a vertical cross-sectional view of the exemplary semiconductor nanowire according to the present invention after an anneal for dopant distribution.

[0044] FIG. 5B is a horizontal cross-sectional view of the exemplary semiconductor nanowire in FIG. 5B along the plane X-X'.

[0045] FIG. 6 is a schematic view of the transformation of the assembly of an undoped semiconductor nanowire and a shell into a doped semiconductor nanowire according to the present invention.

[0046] FIG. 7 shows photoelectron spectra for an undoped 20 nm diameter nanowire and a boron-doped 29 nm diameter nanowire according to the present invention.

[0047] FIG. 8A-8C show band diagrams for an undoped semiconductor nanowire, a p-type semiconductor nanowire, and an n-type semiconductor nanowire according to the present invention, respectively.

Detailed Description of the Invention

[0048] As stated above, the present invention relates to doped semiconductor wires having constant lateral dimensions and methods of manufacturing the same, which are now described in detail with accompanying figures. It is noted that like and corresponding elements are referred to by like reference numerals, and that the figures are not drawn to scale.

[0049] Referring to FIG. 3A and 3B, an exemplary semiconductor nanowire structure according to the present invention is shown, which comprises a substrate 10, an undoped semiconductor nanowire 50, and a catalyst particle 20. The exemplary semiconductor nanowire is provided by first growing an undoped semiconductor nanowire 50 on the substrate 10 by catalytic growth induced by the catalyst particle 20.

[0050] The substrate 10 may comprise a semiconductor material, or an insulator material. Semiconductor materials that may be employed in the substrate 10 include group IV semiconductor materials, III-V compound semiconductor materials, II-VI compound semiconductor materials, and alloys thereof. The insulator materials that may be employed in the substrate include dielectric oxides and dielectric nitrides. Exemplary dielectric oxides include silicon oxide and dielectric metal oxides including high dielectric constant dielectric material having a dielectric constant greater than 4.0 such as HfO_2, ZrO_2, La_2O_3, Al_2O_3, TiO_2,

$SrTiO_3$, $LaAlO_3$, and Y_2O_3. Exemplary dielectric nitrides include silicon nitride and ceramic nitrides such as aluminum nitride, strontium nitride, boron nitride, and beryllium nitride. The substrate 10 may be single crystalline, polycrystalline, or amorphous.

[0051] The catalyst particle 20 comprises a material that induces catalytic growth of a semiconductor nanowire in a suitable environment. Exemplary materials for the catalyst particle 20 include, but are not limited to, Au, Ag, Cu, Pt, Fe, Co, Ni, In, Ta, Ti, Zn, Cd, and Sn. The catalyst particle 20 has lateral dimensions from about 1 nm to about 1,000 nm, and preferably from about 1 nm to about 30 nm. The catalyst particle 20 may, or may not have a radial symmetry, i.e., horizontal cross-sectional areas may, or may not be, a circle. The catalyst particle 20 may be a sphere, an ellipsoid, a cylinder, a cone, a regular polyhedron, an irregular polyhedron, or a combination thereof. The lateral dimensions of the catalyst particle 20 refer to characteristic dimensions of the catalyst particle 20 if such a characteristic dimension exists. For example, in case a horizontal cross-sectional area is a circle or an ellipse, the characteristic dimension may be a diameter, a major axis, and/or a minor axis. In case the catalyst particle 20 does not have a regular shaped cross-sectional area, the lateral dimensions refer to the maximum of lateral extent of a cross-sectional area. If multiple cross-sectional areas provide different lateral extents, the cross-sectional area that provides the maximum lateral extent is employed to characterize the lateral dimensions of the catalyst particle 20.

[0052] Once the catalyst particle 20 is placed on the substrate 10, the catalyst particle 20 and the substrate 10 are subjected to a condition conducive to the growth of the undoped semiconductor nanowire 50 in a process chamber, which may be a low pressure chemical vapor deposition (LPCVD) chamber or an ultra-high vacuum chemical vapor deposition (UHVCVD) chamber. The undoped semiconductor nanowire 50 is grown by catalytic growth of a semiconductor material, which is known in the art and described, for example, in U.S. Patent Nos. 7,105,428; 7,211,464; and 6,962,823 *supra*. Specifically, the catalytic growth of the undoped semiconductor wire 50 is effected by supplying a reactant containing a semiconductor material to be incorporated into the undoped semiconductor wire 50 at an elevated temperature, which is herein referred to as a first temperature.

[0053] The semiconductor material of the undoped semiconductor nanowire 50 may be a group IV semiconductor material such as silicon and germanium. In case the semiconductor material comprises silicon, the reactant may be SiH_4, Si_2H_6, SiH_2Cl_2, $SiHCl_3$, $SiCl_4$, GeH_4, or a combination thereof. In case the semiconductor material comprises germanium, the reactant may be one of GeH_4, GeH_4, Ge_2H_6, GeH_3Cl, GeH_2Cl_2, $GeHCl_3$, and $GeCl_4$. Alternately, the semiconductor material of the undoped semiconductor nanowire 50 may be a III-V compound semiconductor material, or a II-VI compound semiconductor material. In this case, the reactant comprises a mixture of precursors that provide the semiconductor material to the undoped semiconductor nanowire upon reaction with the catalyst particle 20. The semiconductor material of the undoped semiconductor nanowire 50 may be a mixture of any semiconductor material, in which case the reactant is a combination of the various gases and/or precursors described above.

[0054] The first temperature, which is the temperature employed for growth of the undoped semiconductor nanowire 50, is selected to avoid lateral growth of the semiconductor material on sidewalls of the undoped semiconductor nanowire. Pyrolysis of the reactant in the absence of the catalyst particle 20 is effected at a higher temperature than catalytic pyrolysis effected on the surface of the catalyst particle 20. In other words, one of the functions of the catalyst particle 20 is to enable catalytic pyrolysis of the reactant at a temperature at which normal pyrolysis of the reactant would not occur without the catalyst particle 20. The first temperature is selected so that catalytic pyrolysis of the reactant occurs directly beneath the catalyst particle 20, while pyrolysis of the reactant does not occur on normal surfaces including sidewalls of the undoped semiconductor nanowire 50. In case the undoped semiconductor nanowire 50 comprises silicon or germanium, the first temperature may be from about 350 °C to about 500 °C, and preferably from about 350 °C to about 450 °C, and most preferably from about 350 °C to about 400 °C. Typically, the undoped semiconductor nanowire 50 is entirely single crystalline since the catalytic growth induces epitaxial alignment of the semiconductor atoms during the growth.

[0055] The lateral dimensions of the undoped semiconductor nanowire 50 may be substantially the same as the lateral dimensions of the catalyst particle 20. Lack of pyrolysis on sidewalls of the undoped semiconductor nanowire 50 preserves the lateral dimensions of portions of the undoped semiconductor nanowire even after the catalyst particle 20 moves away from the portion as the growth of the undoped semiconductor nanowire 50 continues. Thus, the undoped semiconductor nanowire 50 has a constant cross-sectional area independent of the location within the undoped semiconductor nanowire 50. The cross-sectional area of the undoped semiconductor nanowire 50 may be circular, elliptical, polygonal, or may be a composite shape of a curved portion and a polygonal portion. In case the cross-sectional area of the undoped semiconductor nanowire 50 is a circle, the radius R1 of the circle may be from about 0.5 nm to about 500 nm with a corresponding radius from about 1 nm to about 1,000 nm, and preferably from about 0.5 nm to about 15 nm with a corresponding radius from about 1 nm to about 30 nm.

[0056] The undoped semiconductor nanowire 50 is substantially undoped, i.e., any dopant, if present, is at a trace level or at a level that does not increase conductivity of the undoped semiconductor nanowire to any significant level. Dopants herein refer to electrical dopants that confer p-type doping or n-type doping on a semiconductor material as well known in the art. P-type dopants include B, Ga, and In. N-type dopants include P, As, and Sb. Typically, a doping concentration of less than $1.0 \times 10^{17}/cm^3$ is insufficient to induce any significant increase in the conductivity of a semiconductor material. Preferably, no dopant is supplied into the process chamber during the growth of the undoped semiconductor nanowire 50, and any dopant in the undoped semiconductor nanowire 50 is at a trace level.

[0057] It is to be noted that even if dopant gases are provided within the process chamber during the growth of the undoped semiconductor nanowire 50 at the first temperature, the first temperature is insufficient to effect any significant level of dopant incorporation of the dopant gases into the undoped semiconductor nanowire. This is because the catalytic growth selectively incorporates the semiconductor material at the expense of dopant atoms that may be provided from the dopant gases. Thus, even if any dopant gas is supplied into the gas stream along with the reactant, the doping concentration of the undoped semiconductor

nanowire 50 is much less than $1.0x10^{17}/cm^3$, thus rendering the undoped semiconductor nanowire 50 "undoped," i.e., having a doping at a level that renders the properties of the undoped semiconductor nanowire 50 essentially the same as the corresponding properties of a semiconductor nanowire with no doping.

[0058] Referring to FIGS. 4A and 4B, a shell 60 of a doped semiconductor material is grown directly on and around the sidewall of the undoped semiconductor nanowire 50 by exposing the undoped semiconductor nanowire 50 to a mixture of a reactant and a dopant gas at another elevated temperature, which is herein referred to as a second temperature. This processing step may employ the same process chamber as, or a different process chamber from, the process chamber employed for the growth of the undoped semiconductor nanowire 50. Use of the same process chamber provides the advantage of preventing exposure of the surfaces of the undoped semiconductor wire 50 to an ambient gas outside the process chamber.

[0059] The doped semiconductor material may comprise the same semiconductor material as, or a different semiconductor material from, the undoped semiconductor nanowire 50. In general, any of the semiconductor material that may be employed for the undoped semiconductor nanowire 50 as listed above may be employed for the doped semiconductor material for the shell 60. The reactant for the growth of the shell 60 is selected based on the material of the shell, and may be the same as the reactants listed above, i.e., SiH_4, Si_2H_6, SiH_2Cl_2, $SiHCl_3$, $SiCl_4$, GeH_4, GeH_4, Ge_2H_6, GeH_3Cl, GeH_2Cl_2, $GeHCl_3$, $GeCl_4$, and other precursors for compound semiconductors.

[0060] The dopant gas comprises a gas phase compound of a dopant atom. Exemplary dopant gases include, but are not limited to, B_2H_6, GaH_3, $GaCl_3$, Ga_2Cl_6, PH_3, $POCl_3$, AsH_3, SbH_3, and SbF_3. The dopant gas may be supplied concurrently and continuously with the reactant into the process chamber so that the composition of the shell 60 is uniform, or alternately, may be supplied intermittently into the process chamber so that the shell 60 has a layered structure with modulations in the dopant concentration within the shell 60. Dopant concentration in the shell 60 may be controlled by adjusting the partial pressure of the dopant

gas and/or the ratio of the partial pressure of the dopant gas to the partial pressure of the reactant.

[0061] The shell 60 grows on sidewalls of the undoped semiconductor wire 50 and at the top of the undoped semiconductor wire 50. The catalyst particle 20 may be separated from the undoped semiconductor nanowire 50 by the growth of the shell 60. Due to the *in-situ* doping of the shell, i.e., the incorporation of dopants into the shell 60 during the growth, the shell 60 comprises both a semiconductor material and a dopant. Preferably, the doping concentration of the shell is from about $1.0 \times 10^{18}/cm^3$ to about $5.0 \times 10^{21}/cm^3$, more preferably, from about $5.0 \times 10^{19}/cm^3$ to about $5.0 \times 10^{21}/cm^3$ to effect a high doping concentration level in the undoped semiconductor wire 50 after an anneal to be subsequently performed.

[0062] The growth of the shell 60 is not catalytic, i.e., the presence of the catalyst particle 20 is not necessary for precipitating the growth of the shell, although the catalyst particle 20 may enhance deposition rate of the shell 60 over the undoped semiconductor nanowire 50. To insure that growth of the shell 60 occurs on the sidewalls of the undoped semiconductor nanowire 50, the second temperature, i.e., the temperature of the growth of the shell 60, is set at a sufficiently high temperature at which pyrolysis of the reactant proceeds even without the catalyst particle 20. In the case the shell 60 comprises silicon or germanium, the second temperature may be from about 500 °C to about 1,100 °C, and preferably from about 500 °C to about 700 °C. The shell is typically single crystalline as the doped semiconductor material of the shell 60 is grown in epitaxial registry with the underlying undoped semiconductor nanowire 50.

[0063] The cross-sectional area of the shell 60 is independent of the location along the shell 60. Since the shell 60 laterally encloses the undoped semiconductor nanowire 50, the inner surface of the shell 60 conforms to the outer surface of the undoped semiconductor nanowire 50. The cross-sectional area of the shell 60 may be annular, or may comprise an expanded shape of the cross-sectional area of the undoped semiconductor nanowire 50 from which the shape of the cross-sectional area of the undoped semiconductor nanowire is subtracted. The thickness of the shell 60 may be from about 0.5 nm to about 100 nm, and typically from about

1 nm to about 10 nm. The thickness of the shell 60 may be from about 5 % to about 100 % of the lateral dimensions of the undoped semiconductor nanowire 50, and preferably from about 20 % to about 50% of the lateral dimensions of the undoped semiconductor nanowire 50, although lesser and greater percentages are explicitly contemplated herein also. In case the cross-sectional area of the undoped semiconductor nanowire 50 is a circle, the cross-sectional area of the shell is an annulus or a ring having an inner radius and an outer radius R2. The inner radius is the same as the radius R1 of the circle of the cross-sectional area of the inner semiconductor nanowire 50.

[0064] Referring to FIGS. 5A and 5B, the catalyst particle 20 may be removed by a heating cycle, during which the catalyst 20 is separated from the assembly of the undoped semiconductor nanowire 50 and the shell 60. Methods of separating a catalyst particle from a nanowire after formation of the nanowire are known in the art.

[0065] Concurrently with the heating cycle, or subsequent to the heating cycle, the assembly of the undoped semiconductor nanowire 50 and the shell 60 is subjected to an anneal at an elevated temperature, which is typically performed at a higher temperature than the second temperature to induce diffusion of dopants in the shell 60 into the undoped semiconductor nanowire 50, thereby converting the assembly into a uniformly doped semiconductor nanowire 70. If the undoped semiconductor nanowire 50 and the shell 60 are single crystalline, the resulting structure after the anneal, which is the uniformly doped semiconductor nanowire 70, is also single crystalline.

[0066] The temperature of the anneal is selected to effect sufficient bulk diffusion of the dopants in the shell 60 into the undoped semiconductor nanowire 50 so that the dopant concentration in the uniformly doped semiconductor nanowire 70 is substantially uniform. For example, the anneal temperature may be from about 600 °C to about 1,200 °C. The anneal may be performed in a furnace or in a rapid thermal anneal chamber. The duration of the anneal may be from about 1 second to about 12 hours, and typically from about 10 seconds to about 1 hour. Typically, use of a high anneal temperature requires a short duration

of the anneal process, while use a low anneal temperature requires a long duration of the anneal process.

[0067] The doping concentration of the uniformly doped semiconductor nanowire 70 is the volume weighted average of the doping concentration of the undoped semiconductor nanowire 50 prior to the anneal, which is substantially zero, and the doping concentration of the shell 60 prior to the anneal. For example, if the volume of the undoped semiconductor nanowire 50 is V1, the volume of the shell 60 is V2, and the doping concentration of the shell 60 before the anneal is Cb, the doping concentration of the uniformly doped semiconductor nanowire 70 after the anneal Ca is given by: Ca = Cb x V2 / (V1 + V2). In case the doping concentration of the shell is from about $1.0 \times 10^{18}/cm^3$ to about $5.0 \times 10^{21}/cm^3$, the doping concentration of the uniformly doped semiconductor nanowire 70 may be from about $1.0 \times 10^{17}/cm^3$ to about $5.0 \times 10^{20}/cm^3$, although higher and lower doping concentrations for the uniformly doped semiconductor nanowire 70 may be obtained by manipulation of the dimensions of the undoped semiconductor nanowire 50 and/or the dimensions of the shell 60.

[0068] Thus, the present invention provides a method of forming a semiconductor nanowire having a high doping level, i.e., a doping concentration of about $1.0 \times 10^{17}/cm^3$ or greater, while maintaining the diameter of the semiconductor constant. Further, the lateral dimensions of the uniformly doped semiconductor nanowire 70 may be kept at a small dimension, i.e. from about 1 nm to about 30 nm, by keeping the lateral dimensions of the undoped semiconductor nanowire 50 at such a small dimension and avoiding pyrolysis of reactants at sidewalls of the undoped semiconductor nanowire 50.

[0069] Referring to FIG. 6. the conversion process of the assembly of the undoped semiconductor nanowire 50 and the shell 60 into the uniformly doped semiconductor nanowire 70 by an anneal is schematically shown. The anneal homogenizes the dopant distribution within the assembly of the semiconductor nanowire 50 and the shell 60 so that the uniformly doped semiconductor nanowire 70 has a substantially "uniform" doping concentration.

[0070] Referring to FIG. 7, two measured photoelectron spectra are shown as a demonstration of the present invention. In this experimental set up, two nanowires were subjected to a beam of photons having 6.2 eV of kinetic energy. Photoemitted electrons were extracted with a bias potential of 15 eV so that 15 eV of energy would be added to the initial kinetic energy of the photoemitted electrons through the electrical biasing of the set up. The first nanowire comprised an undoped silicon nanowire having a diameter of 20 nm. The second nanowire comprised a uniformly doped silicon nanowire having a diameter of 29 nm and manufactured by the methods of the present invention by first forming an undoped silicon nanowire of diameter of 20 nm, followed by formation of a 4.5 nm thick doped silicon shell and a subsequent anneal. The doped silicon shell contained boron (a p-type dopant) as a doping material.

[0071] A shift in the energy of the photoemitted electrons is observed in the photoelectron spectrum of the second nanowire, which is the doped silicon nanowire, relative to the photoelectron spectrum of the first nanowire, which is the undoped silicon nanowire. The shift in the energy of the photoelectron spectrum shows that the Fermi level of the second nanowire shifted due to the doping of the second nanowire. In other words, the shift in the photoelectron spectra demonstrates that the second silicon nanowire is indeed doped with p-type dopants as disclosed in the present invention.

[0072] Referring to FIGS. 8A-8C, Fermi level diagrams for an undoped semiconductor nanowire, a p-doped semiconductor nanowire, and an n-doped semiconductor nanowire are shown, respectively. The present invention enables formation of p-type or n-type doped semiconductor nanowires having a shifted Fermi level relative to the Fermi level of the undoped semiconductor nanowire shown in FIG. 8A. Thus, the manipulation of the Fermi level according to the present invention enables changes in the conductivity of a semiconductor nanowire as well as determination of charge carrier types in the semiconductor nanowire.

[0073] While the invention has been described in terms of specific embodiments, it is evident in view of the foregoing description that numerous alternatives, modifications and

variations will be apparent to those skilled in the art. Accordingly, the invention is intended to encompass all such alternatives, modifications and variations which fall within the scope and spirit of the invention and the following claims.

Claims

What is claimed is:

1. A method of forming a semiconductor nanowire comprising:

forming a catalyst particle on a substrate;

growing an undoped semiconductor nanowire between said catalyst particle and said substrate by subjecting said catalyst particle to a first reactant gas at a first temperature, wherein pyrolysis of said first reactant gas on sidewalls of said semiconductor nanowire is suppressed at said first temperature; and

growing a shell of a doped semiconductor material around sidewalls of said undoped semiconductor nanowire by subjecting said undoped semiconductor nanowire to a second reactant and a dopant at a second temperature, wherein said second reactant and said dopant is incorporated into said shell by pyrolysis.

2. The method of Claim 1, wherein said undoped semiconductor nanowire comprises a group IV semiconductor material, a III-V compound semiconductor material, a II-VI compound semiconductor material, and an alloy thereof.

3. The method of Claim 1, wherein said doped semiconductor material comprises a group IV semiconductor material, a III-V compound semiconductor material, a II-VI compound semiconductor material, and an alloy thereof.

4. The method of Claim 1, wherein said doped semiconductor material further comprises at least one of B, Ga, In, P, As, and Sb.

5. The method of Claim 1, wherein said undoped semiconductor nanowire has a substantially constant cross-sectional area across an entire length of said undoped semiconductor nanowire.

6. The method of Claim 5, wherein lateral dimensions of said undoped semiconductor nanowire is from about 1 nm to about 1,000 nm.

7. The method of Claim 6, wherein said lateral dimensions of said undoped semiconductor nanowire are less than 30 nm.

8. The method of Claim 1, wherein said shell has a substantially constant cross-sectional area across an entire length of said shell.

9. The method of Claim 8, wherein said shell has a thickness from about 0.3 nm to about 10 nm.

10. The method of Claim 1, wherein said shell has a doping concentration from about $1.0 \times 10^{18}/cm^3$ to about $5.0 \times 10^{21}/cm^3$.

11. The method of Claim 1, wherein said catalyst particle has a lateral dimension from about 1 nm to about 1,000 nm.

12. The method of Claim 11, wherein said lateral dimension of said catalyst particle is less than 30 nm.

13. The method of Claim 1, wherein said catalyst particle comprises one of Au, Ag, Cu, Pt, Fe, Co, Ni, In, Ta, Ti, Zn, Cd, and Sn.

14. The method of Claim 1, wherein said first reactant comprises at least one of SiH_4, Si_2H_6, SiH_2Cl_2, $SiHCl_3$, $SiCl_4$, GeH_4, Ge_2H_6, GeH_3Cl, GeH_2Cl_2, $GeHCl_3$, and $GeCl_4$, and wherein said first temperature is from about 350 °C to about 450 °C.

15. The method of Claim 1, wherein said second reactant comprises at least one of SiH_4, Si_2H_6, SiH_2Cl_2, $SiHCl_3$, $SiCl_4$, GeH_4, Ge_2H_6, GeH_3Cl, GeH_2Cl_2, $GeHCl_3$, and $GeCl_4$.

16. The method of Claim 15, wherein said dopant comprises one of B_2H_6, GaH_3, $GaCl_3$, Ga_2Cl_6, PH_3, $POCl_3$, AsH_3, SbH_3, and SbF_3.

17. The method of Claim 15, wherein said second temperature is from about 500 °C to about 1,100 °C.

18. The method of Claim 1, further comprising annealing said undoped semiconductor nanowire and said shell at an elevated temperature from about 600 °C to about 1,200 °C, wherein said undoped semiconductor nanowire and said shell have a substantially uniform doping concentration after said anneal.

19. The method of Claim 18, wherein said substantially uniform doping concentration is from about $1.0 \times 10^{17}/cm^3$ to about $5.0 \times 10^{20}/cm^3$, and is the product of a doping concentration of said shell and a ratio of a volume of said shell to a sum of volumes of said shell and said undoped semiconductor nanowire.

20. The method of Claim 1, wherein a doping concentration of said shell is set by a partial pressure of a dopant gas in a process chamber or a ratio between a partial pressure of said dopant gas to a partial pressure of a reactant.

21. A semiconductor nanowire formed by the method of Claim 1.

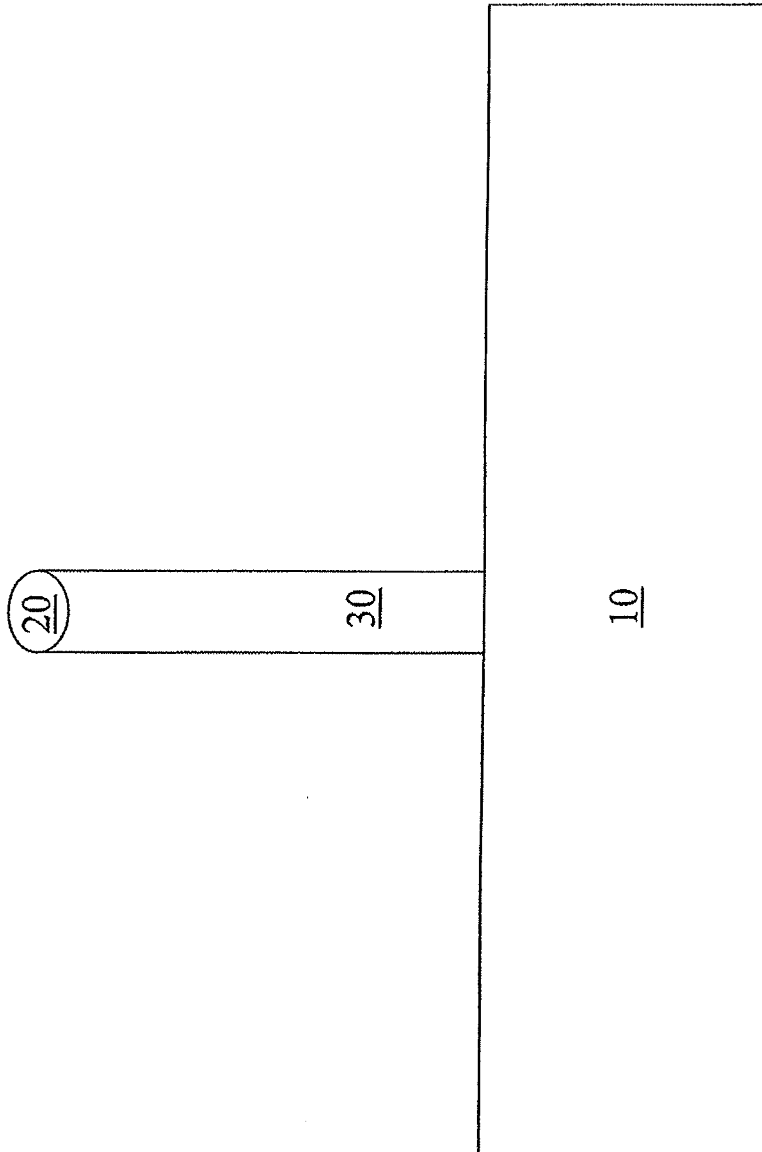


FIG. 1 (Prior Art)

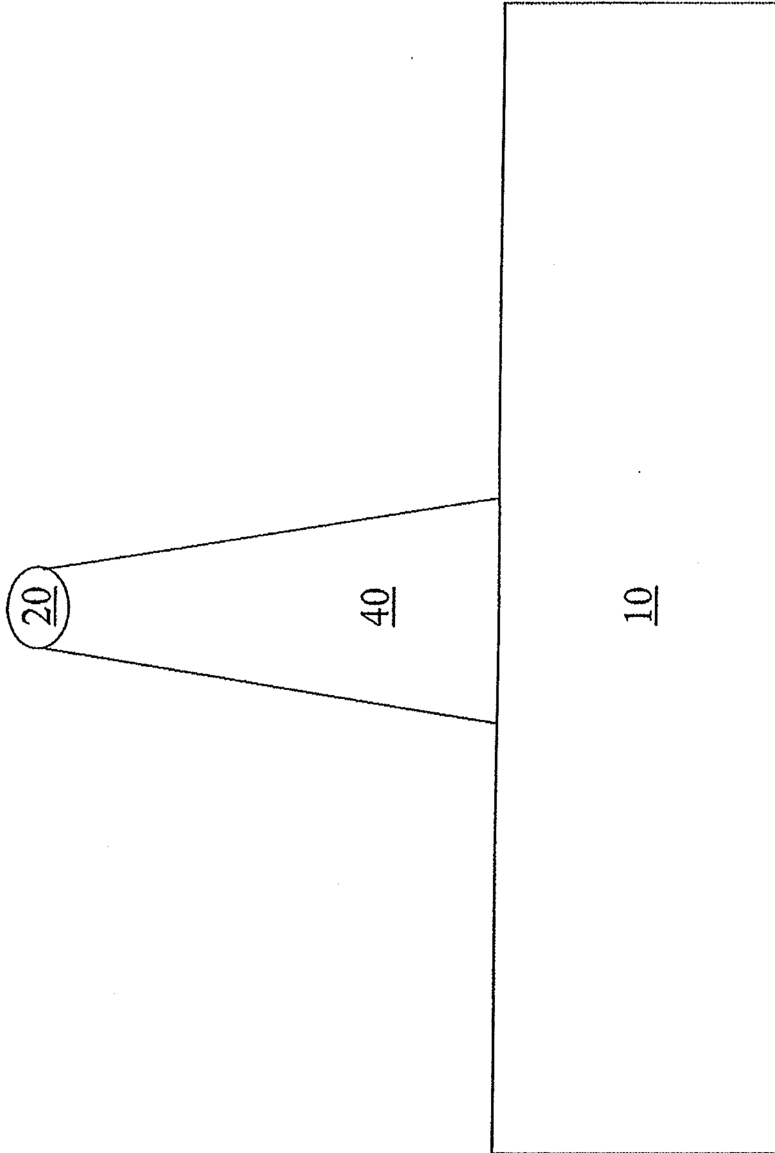


FIG. 2 (Prior Art)

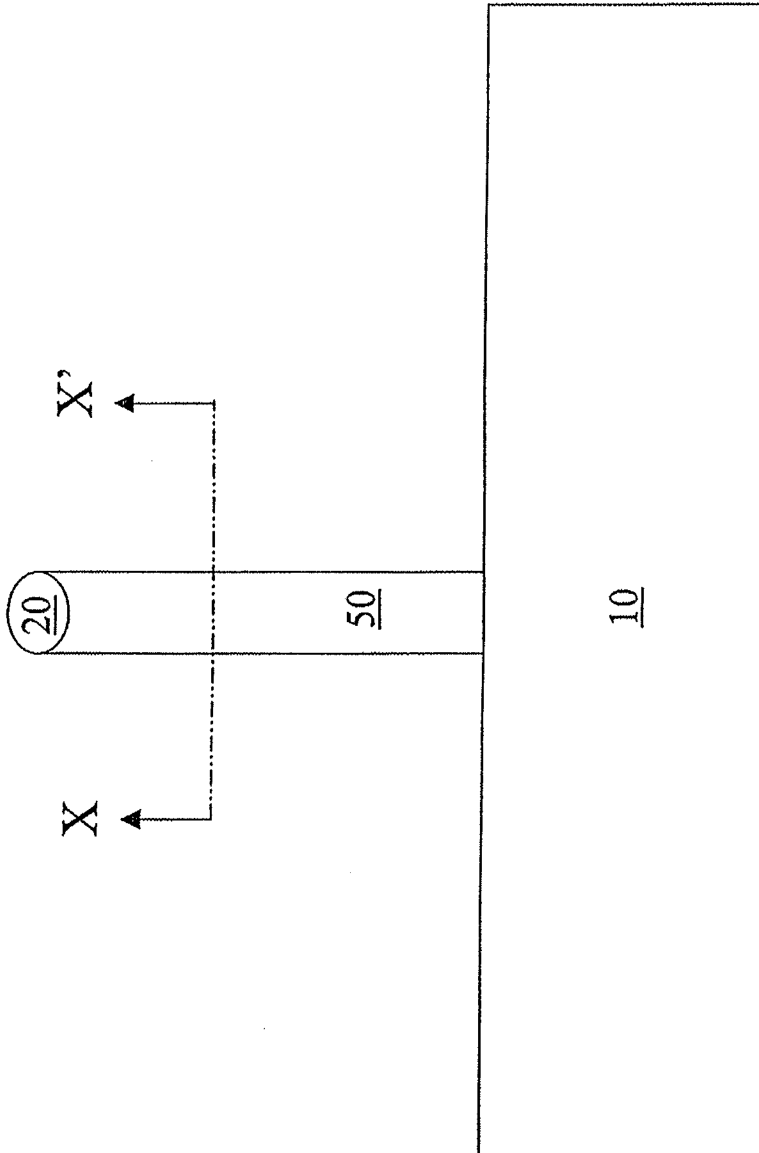


FIG. 3A

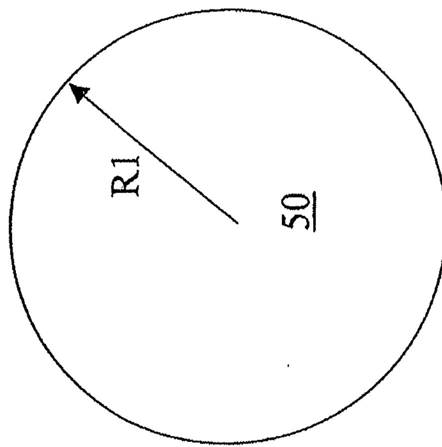


FIG. 3B

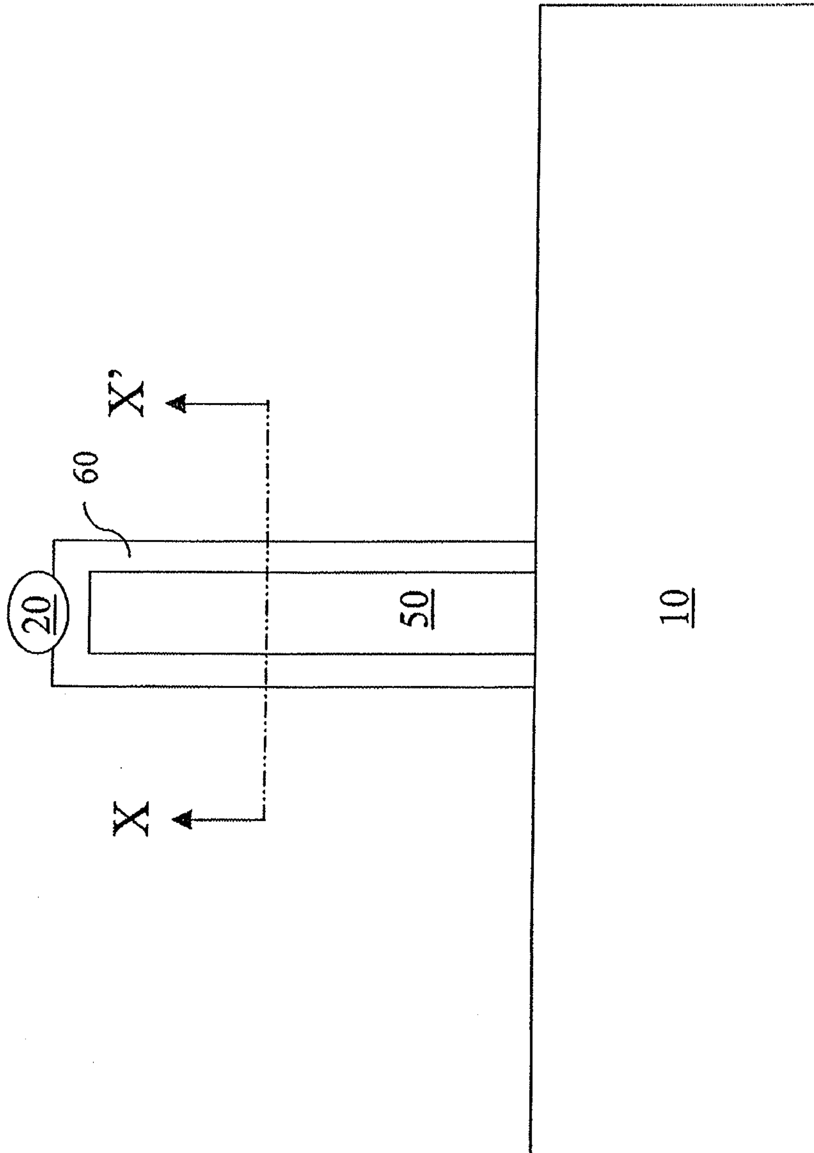


FIG. 4A

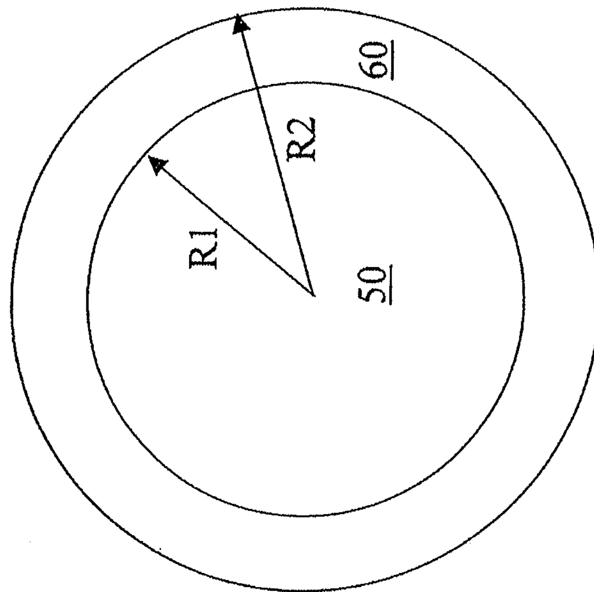


FIG. 4B

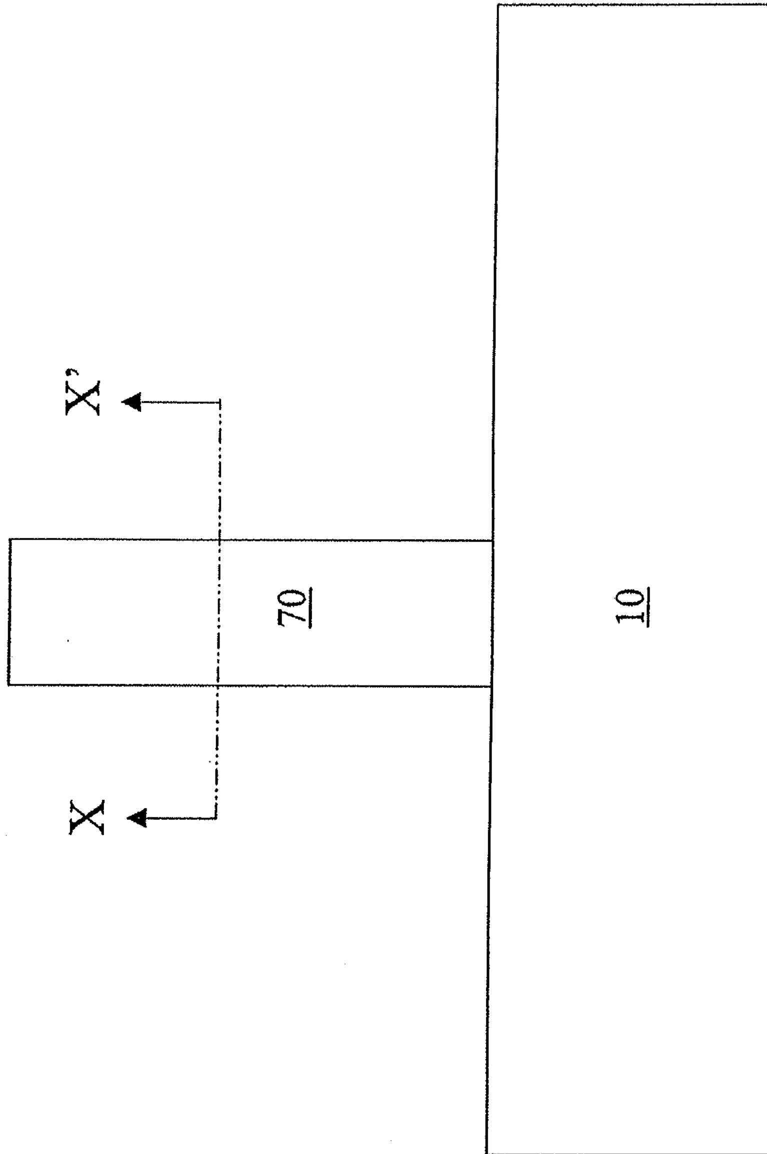


FIG. 5A

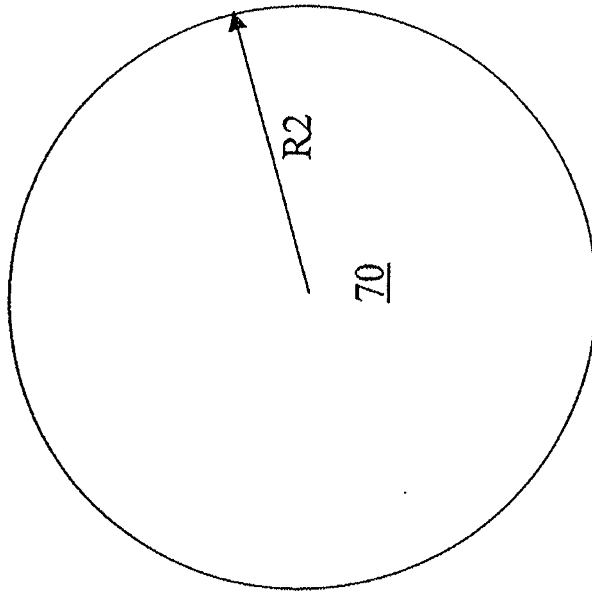


FIG. 5B

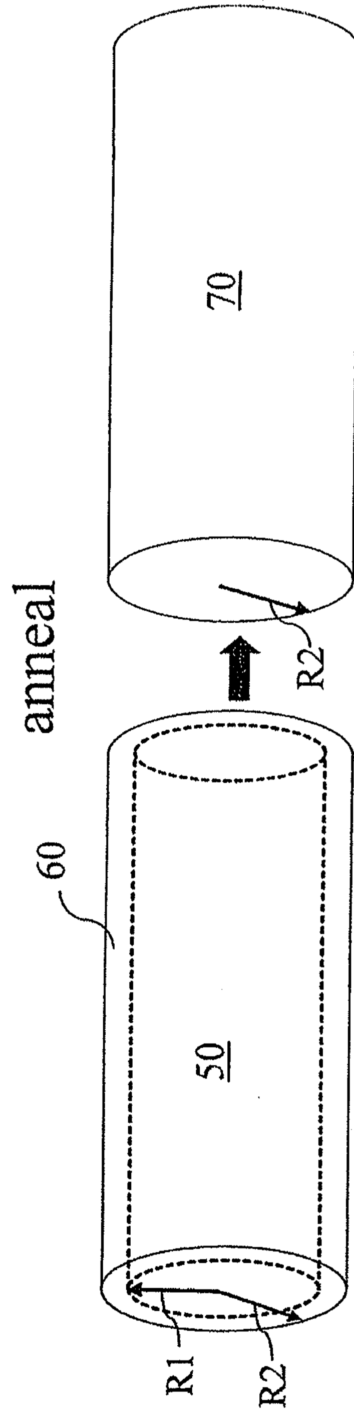


FIG. 6

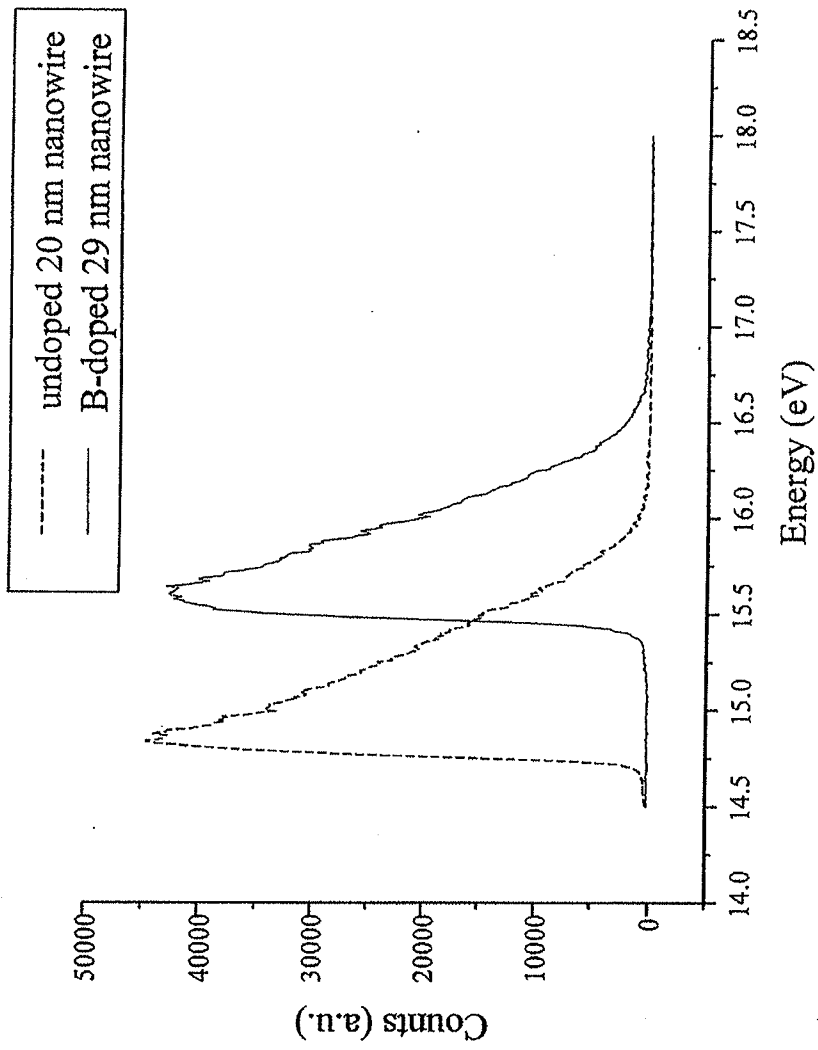


FIG. 7

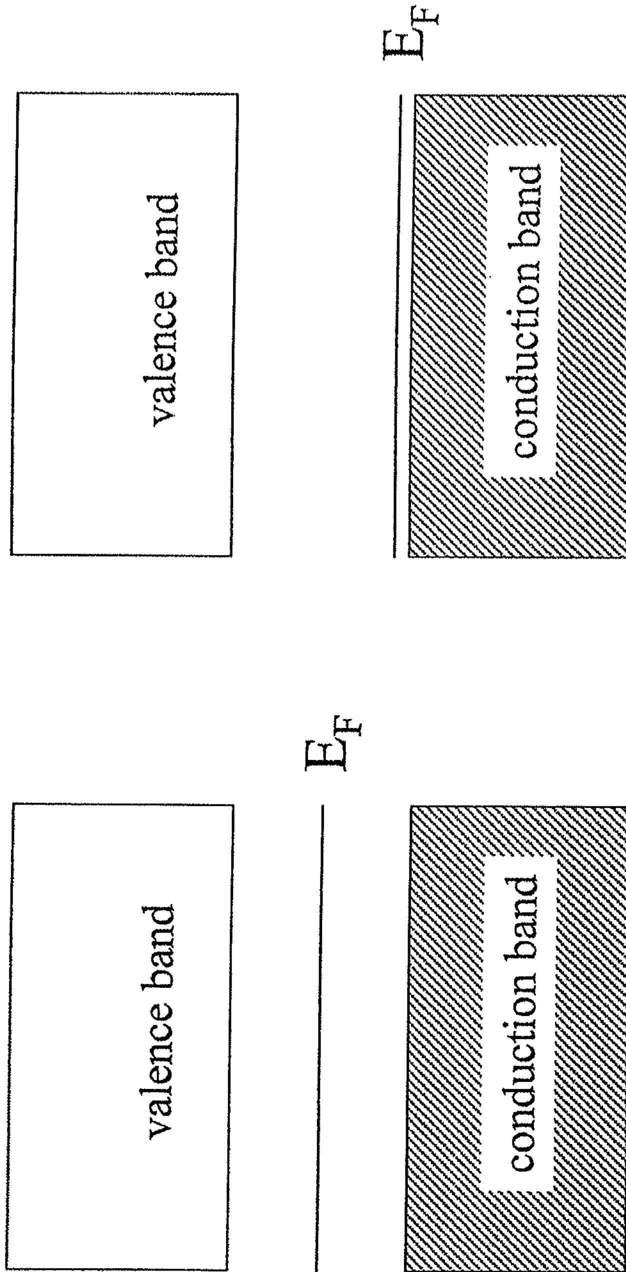


FIG. 8B

FIG. 8A

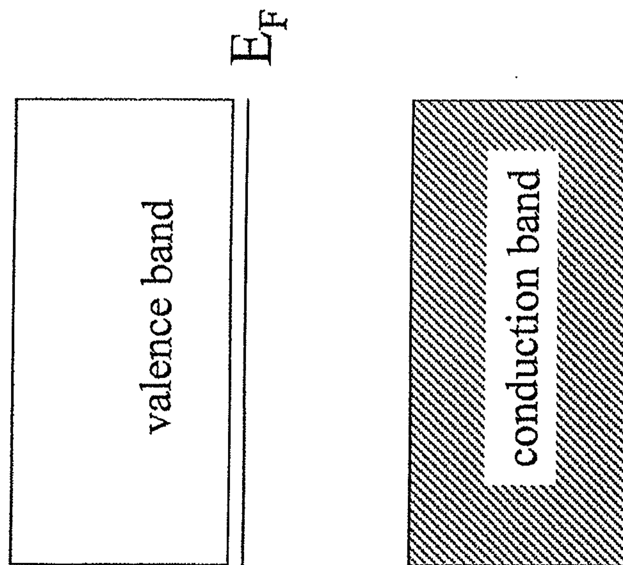
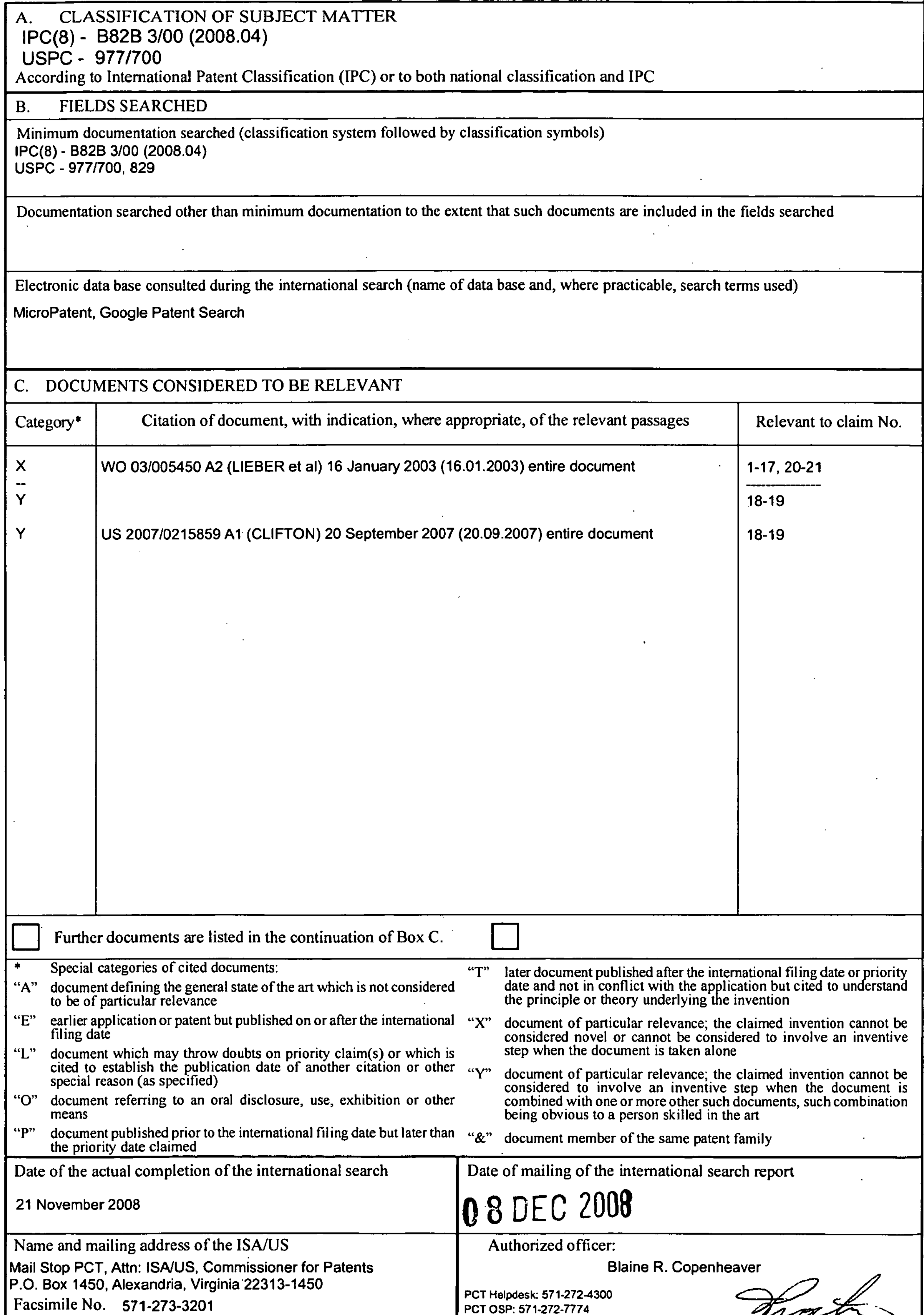


FIG. 8C



INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2008/077419

A. CLASSIFICATION OF SUBJECT MATTER
IPC(8) - B82B 3/00 (2008.04)
USPC - 977/700
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC(8) - B82B 3/00 (2008.04)
USPC - 977/700, 829

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
MicroPatent, Google Patent Search

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X -- Y	WO 03/005450 A2 (LIEBER et al) 16 January 2003 (16.01.2003) entire document	1-17, 20-21 --- 18-19
Y	US 2007/0215859 A1 (CLIFTON) 20 September 2007 (20.09.2007) entire document	18-19

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"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
21 November 2008	08 DEC 2008

Name and mailing address of the ISA/US	Authorized officer:
Mail Stop PCT, Attn: ISA/US, Commissioner for Patents P.O. Box 1450, Alexandria, Virginia 22313-1450 Facsimile No. 571-273-3201	Blaine R. Copenheaver PCT Helpdesk: 571-272-4300 PCT OSP: 571-272-7774